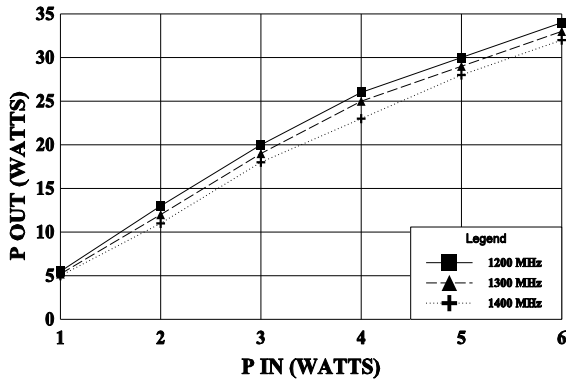




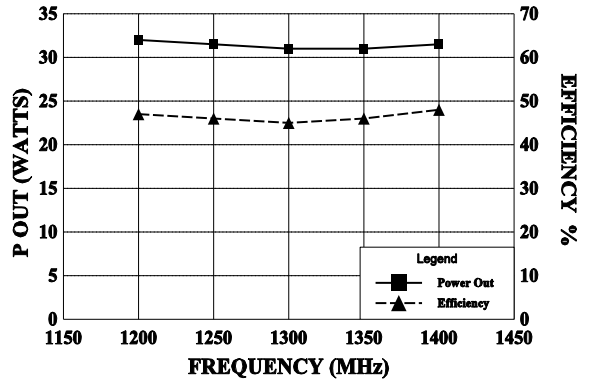
**POWER OUTPUT vs POWER INPUT**

Vcc = 28 V, PW = 2 ms, Duty = 20%



**POWER OUPUT AND EFF. vs FREQUENCY**

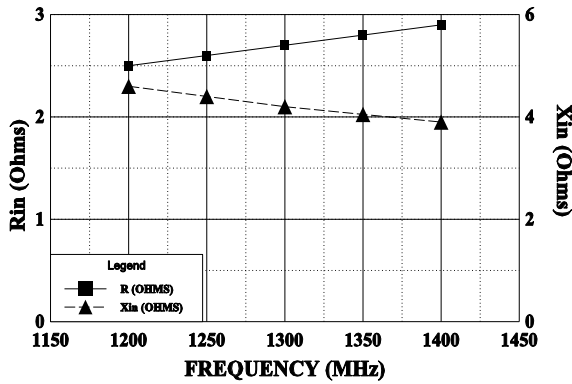
Vcc = 28 V, Pin = 6 W, 2 ms, 20%



**Typical Impedances**

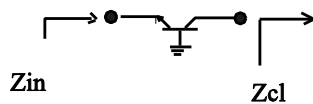
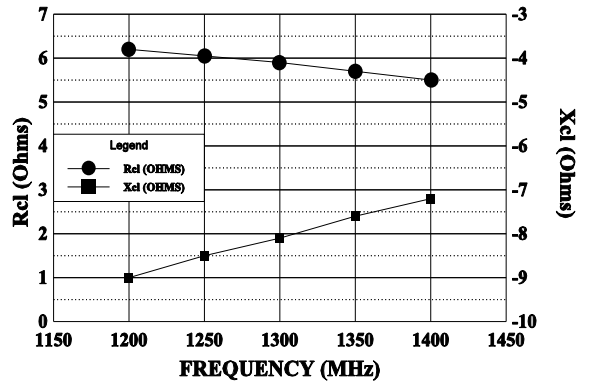
**INPUT IMPEDANCE vs FREQUENCY**

Zin = R + jX (Vcc = 28 V, Pin = 6 W)



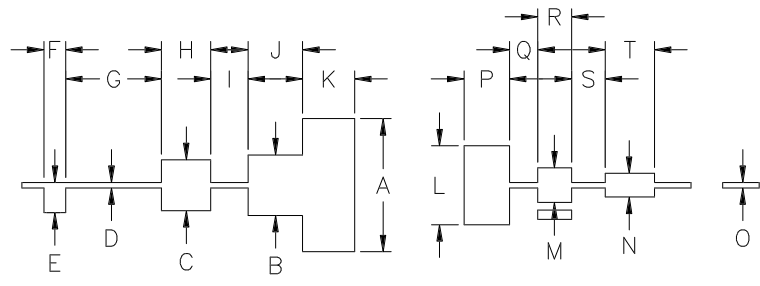
**LOAD IMPEDANCE vs FREQUENCY**

Zcl = Rcl - jXcl (Vcc = 28 V, Pin = 6 W)



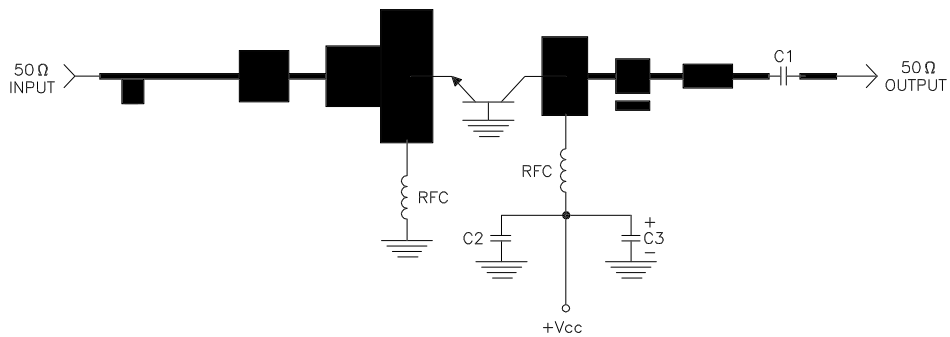
REVISIONS

ZONE	REV	DESCRIPTION	DATE	APPROVED
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DIM	INCHES
A	.730
B	.332
C	.280
D	.030
E	.165
F	.120
G	.525
H	.270
I	.205
J	.300
K	.285
L	.433
M	.190
N	.130
O	.030
P	.250
Q	.155
R	.185
S	.185
T	.270

1214-30 TEST CIRCUIT



DIELECTRIC = 10 MIL THICK  
 DUROID, Er = 2.3  
 C1, C2 = 82pF CHIP ATC "A"  
 C3 = 100MFD @ 35V  
 RFC = 5 turns #22 wire 1/16" I.D.



CAGE OPJR2	DWG NO. 1214-30	REV A
SCALE 1/1	SHEET	