Femtoclock™ Crystal-to-HSTL Clock Generator

General Description

The 842023 is an Ethernet Clock Generator. For Ethernet applications, a 25MHz crystal is used to generate 250MHz. The 842023 uses IDT 3rd generation low phase noise VCO technology and can achieve <1ps rms phase jitter, easily meeting Ethernet jitter requirements. The 842023 is packaged in a small 8-pin TSSOP, making it ideal for use in systems with limited board space.

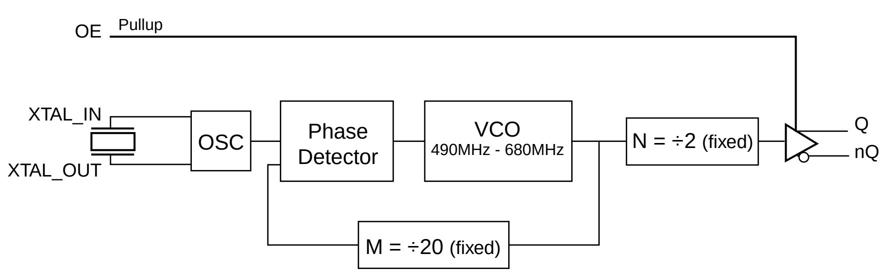
Features

- One differential HSTL output pair
- Crystal oscillator interface, 18pF parallel resonant crystal (24.5MHz – 34MHz)
- Output frequency range: 245MHz – 340MHz
- VCO range: 490MHz – 680MHz
- RMS phase jitter at: 250MHz, using a 25MHz crystal (1.875MHz – 20MHz): 0.36ps (typical)
- Full 3.3V or 2.5V output supply modes
- 0°C to 70°C ambient operating temperature
- Available in lead-free (RoHS 6) packaging

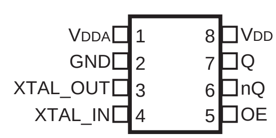
Frequency Table

Inputs				Output Frequency (MHz)
Crystal Frequency (MHz)	M	N	Multiplication Value M/N	
25	20	2	10	250

Block Diagram



Pin Assignment



842023
8 Lead TSSOP
4.40mm x 3.0mm x 0.925 package body
G Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1	V_{DDA}	Power		Analog supply pin.
2	GND	Power		Power supply ground.
3, 4	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
5	OE	Input	Pullup	Output enable pin. When HIGH, Q/nQ outputs are active. When LOW, the Q/nQ outputs are in a high impedance state. LVCMOS/LVTTL interface levels.
6, 7	nQ, Q	Output		Differential output pair. HSTL interface levels.
8	V_{DD}	Power		Core supply pin.

NOTE: *Pullup* refers to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O Continuous Current Surge Current	 50mA 100mA
Package Thermal Impedance, θ_{JA}	129.5°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 3A. Power Supply DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.11	3.3	V_{DD}	V
I_{DD}	Power Supply Current				84	mA
I_{DDA}	Analog Supply Current				11	mA

Table 3B. Power Supply DC Characteristics, V_{DD} = 2.5V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Power Supply Voltage		2.375	2.5	2.625	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.11	2.5	V_{DD}	V
I_{DD}	Power Supply Current				80	mA
I_{DDA}	Analog Supply Current				11	mA

Table 3C. LVCMOS/LVTTL DC Characteristics, V_{DD} = 3.3V ± 5% or 2.5V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{DD} = 3.3V	2		V_{DD} + 0.3	V
			V_{DD} = 2.5V	1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage		V_{DD} = 3.3V	-0.3		0.8	V
			V_{DD} = 2.5V	-0.3		0.7	V
I_{IH}	Input High Current	OE	V_{DD} = V_{IN} = 3.465V or 2.625V			5	µA
I_{IL}	Input Low Current	OE	V_{DD} = 3.465V or 2.625V, V_{IN} = 0V	-150			µA

Table 3D. HSTL DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		1.0		1.8	V
V_{OL}	Output Low Voltage; NOTE 1		0		0.6	V
V_{OX}	Output Crossover Voltage; NOTE 2		40% x (V_{OH} - V_{OL}) + V_{OL}		60% x (V_{OH} - V_{OL}) + V_{OL}	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.4		1.8	V

NOTE 1: Outputs terminated with 50Ω to GND.
NOTE 2: Defined with respect to output voltage swing at a given condition.

Table 3E. HSTL DC Characteristics, V_{DD} = 2.5V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		0.9		1.4	V
V_{OL}	Output Low Voltage; NOTE 1				0.4	V
V_{OX}	Output Crossover Voltage; NOTE 2		40% x (V_{OH} - V_{OL}) + V_{OL}		60% x (V_{OH} - V_{OL}) + V_{OL}	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.4		1.4	V

NOTE 1: Outputs terminated with 50Ω to GND.
NOTE 2: Defined with respect to output voltage swing at a given condition.

Table 4. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental		
Frequency		24.5		34	MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF

NOTE: It is not recommended to overdrive the crystal input with an external clock.

AC Electrical Characteristics

Table 5A. AC Characteristics, V_{DD} = 3.3V ± 5%, T_A = 0°C to 70°C

Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency		245		340	MHz
*t*jit(Ø)	RMS Phase Jitter, Random; NOTE 1	250MHz Integration Range: 1.875MHz – 20MHz		0.36		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	200		700	ps
odc	Output Duty Cycle		48		52	%

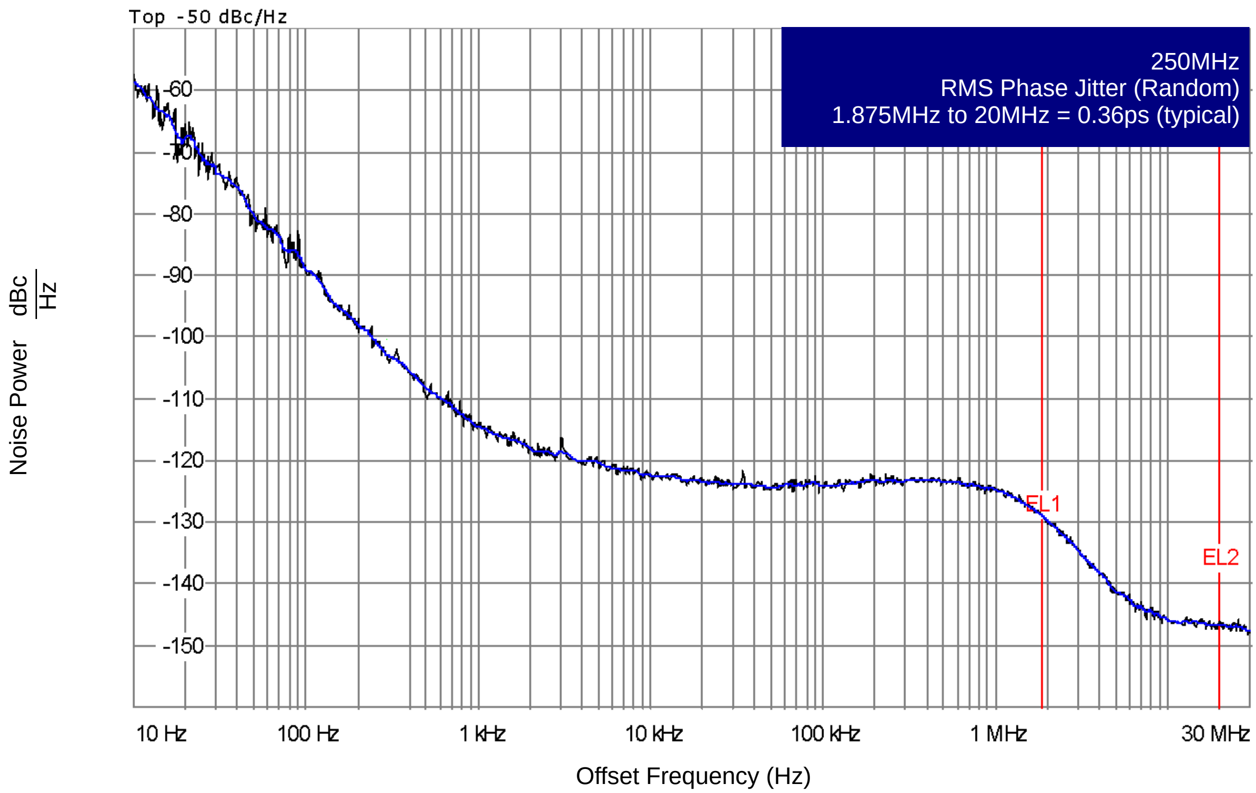
NOTE 1: Please refer to Phase Noise Plots.

Table 5B. AC Characteristics, V_{DD} = 2.5V ± 5%, T_A = 0°C to 70°C

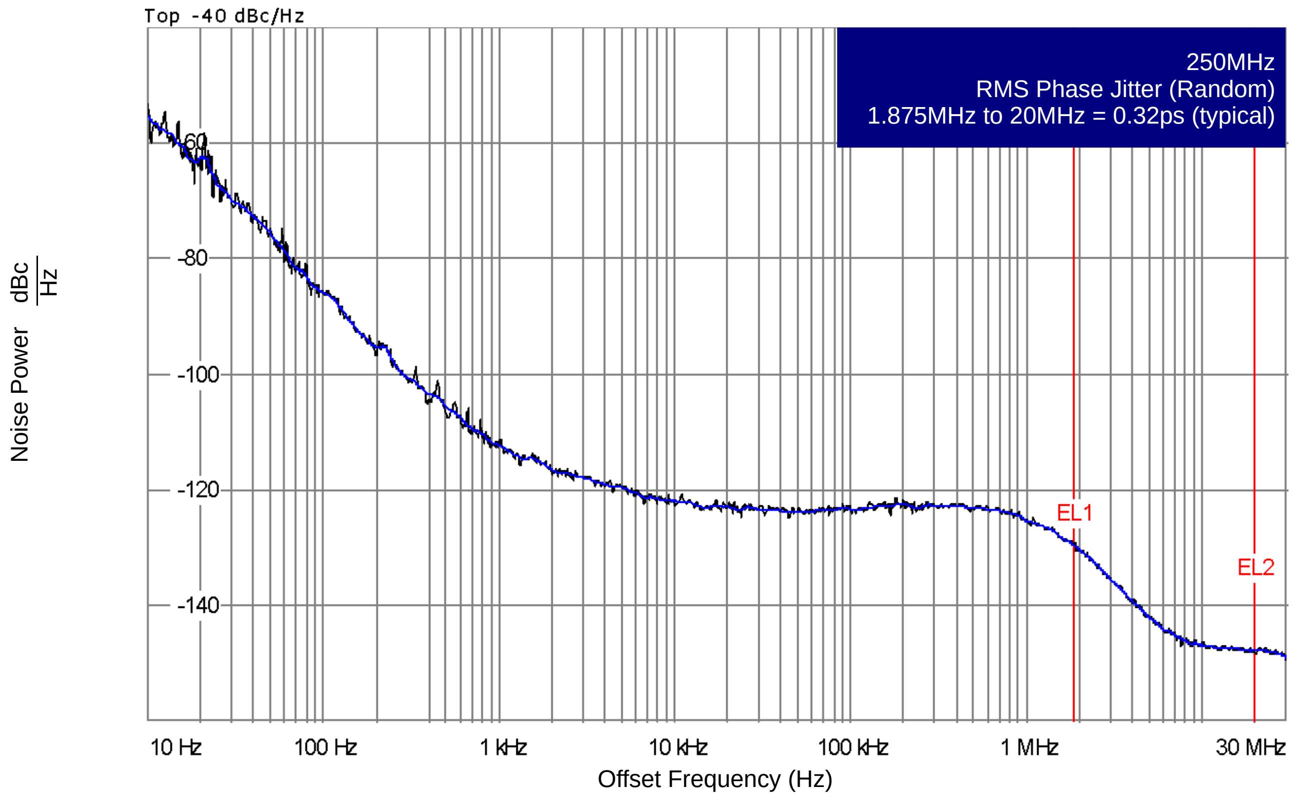
Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency		245		340	MHz
*t*jit(Ø)	RMS Phase Jitter, Random; NOTE 1	250MHz Integration Range: 1.875MHz – 20MHz		0.32		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	200		700	ps
odc	Output Duty Cycle		48		52	%

NOTE 1: Please refer to Phase Noise Plots.

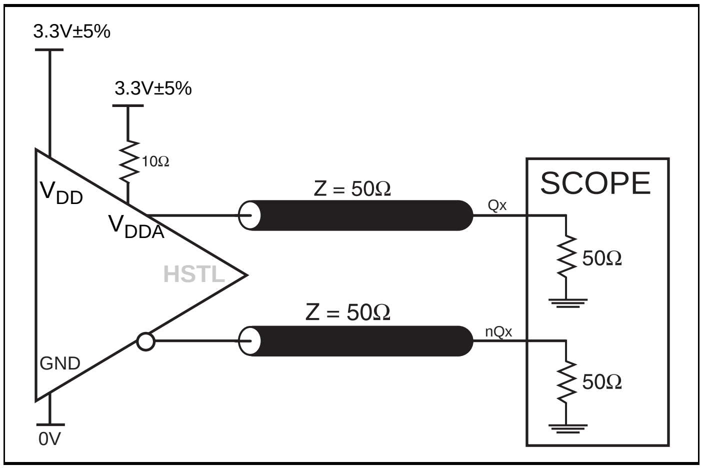
Typical Phase Noise at 250MHz (3.3V)



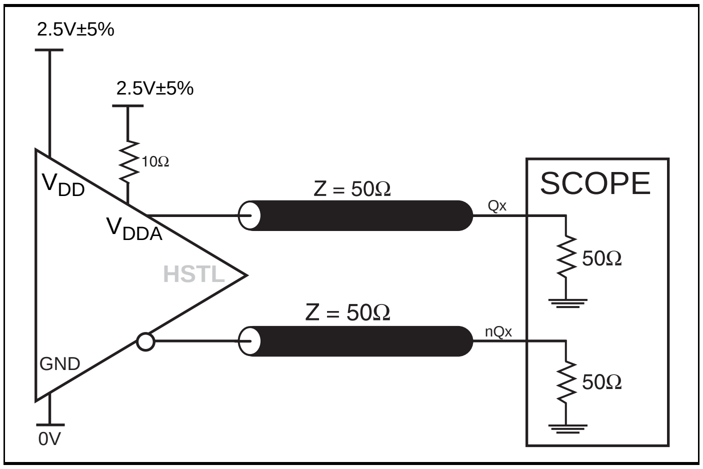
Typical Phase Noise at 250MHz (2.5V)



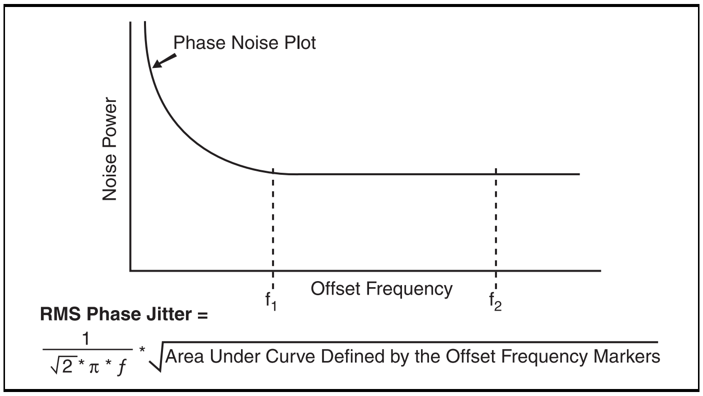
Parameter Measurement Information



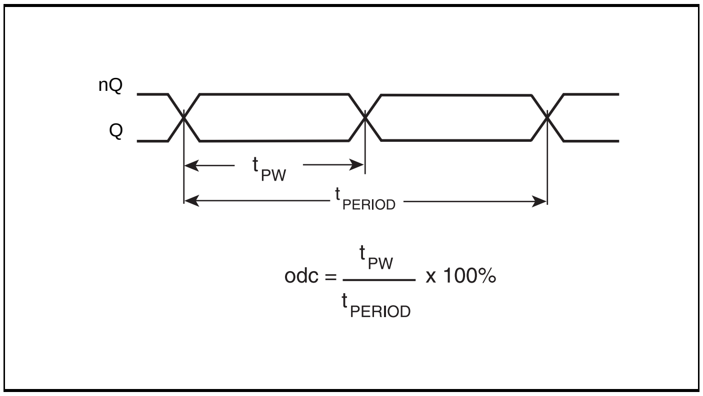
3.3V HSTL Output Load AC Test Circuit



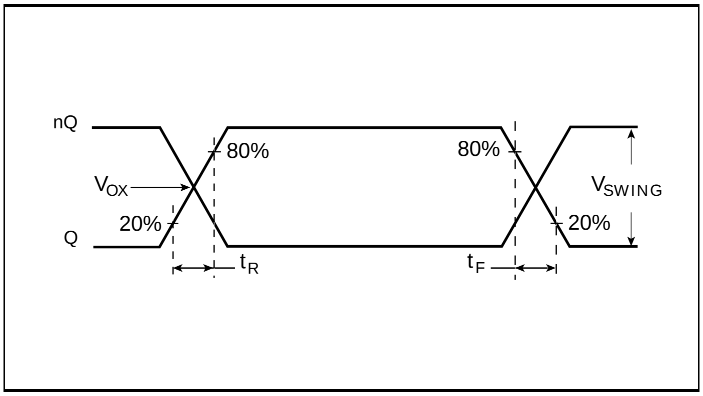
2.5V HSTL Output Load AC Test Circuit



RMS Phase Jitter



Output Duty Cycle/Pulse Width/Period



Output Rise/Fall Time

Application Information

Crystal Input Interface

The 842023 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 1* below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

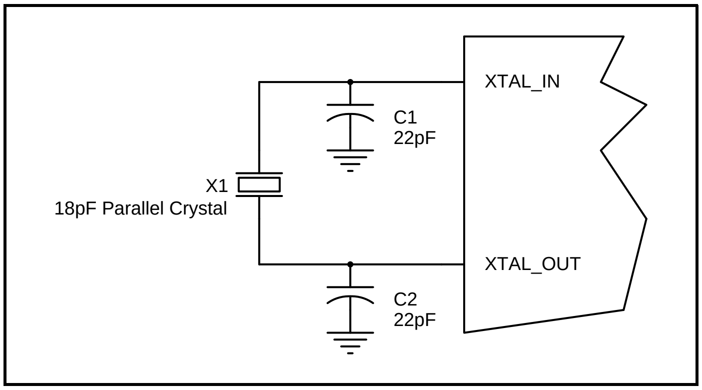


Figure 1. Crystal Input Interface

Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 842023 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD} and V_{DDA} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 3* illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{DDA} pin.

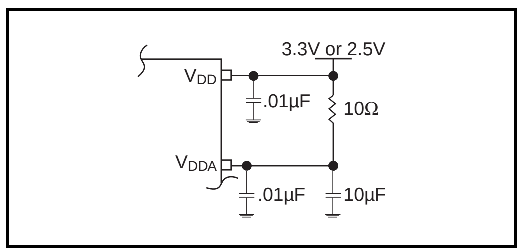


Figure 3. Power Supply Filtering

Termination for HSTL Outputs

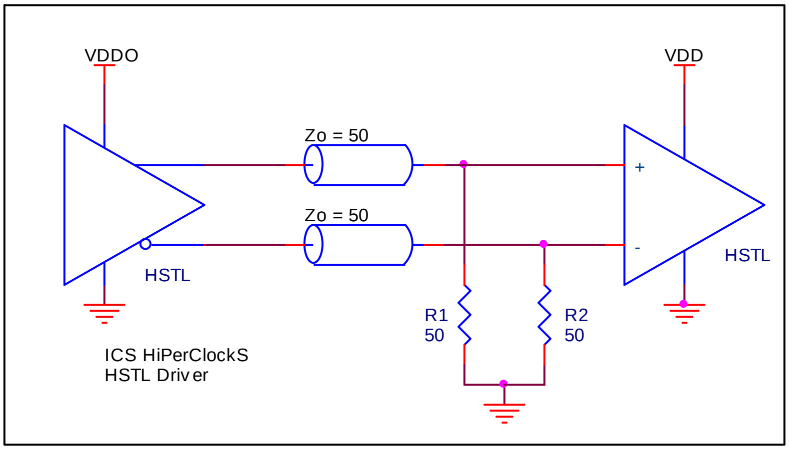


Figure 4. HSTL Output Termination

Schematic Example

Figure 5 shows an example of the 842023 application schematic. In this example, the device is operated at V_{DD} = 3.3V. The 18pF parallel resonant 25MHz crystal is used. The C1 = 22pF and C2 = 22pF are recommended for frequency accuracy. For different board layouts, the C1 and C2 may be slightly adjusted for optimizing frequency accuracy. An example of HSTL termination is shown in this schematic.

Note: Thermal pad (E-pad) must be connected to ground (GND).

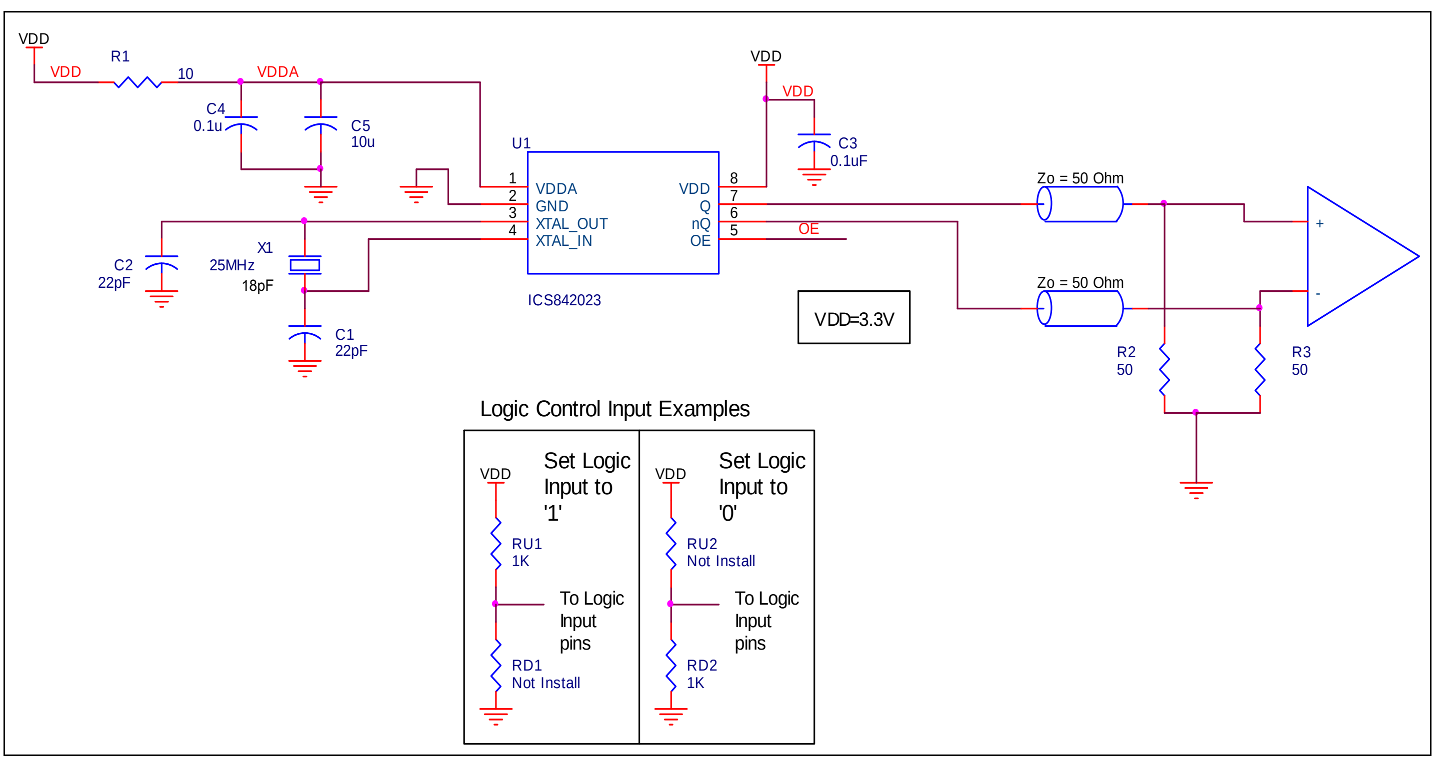


Figure 5. 842023 Schematic Example

Power Considerations

This section provides information on power dissipation and junction temperature for the 842023.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 842023 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD}= 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{DD\_MAX} * (I_{DD\_MAX} + I_{DDA\_MAX})$ = 3.465V * (84mA + 11mA) = **329.18mW**
- Power $(outputs)_{MAX}$ = **94.32mW/Loaded Output pair**

Total Power$_{\_MAX}$ (3.465V, with all outputs switching) = 329.18mW + 94.32mW = **423.49mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 129.5°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:

70°C + 0.423W * 129.5°C/W = 124.8°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 7. Thermal Resistance θ_{JA} for 8 Lead TSSOP, Forced Convection

θ_{JA} **vs. Air Flow**			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	129.5°C/W	125.5°C/W	123.5°C/W

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

HSTL output driver circuit and termination are shown in *Figure 6.*

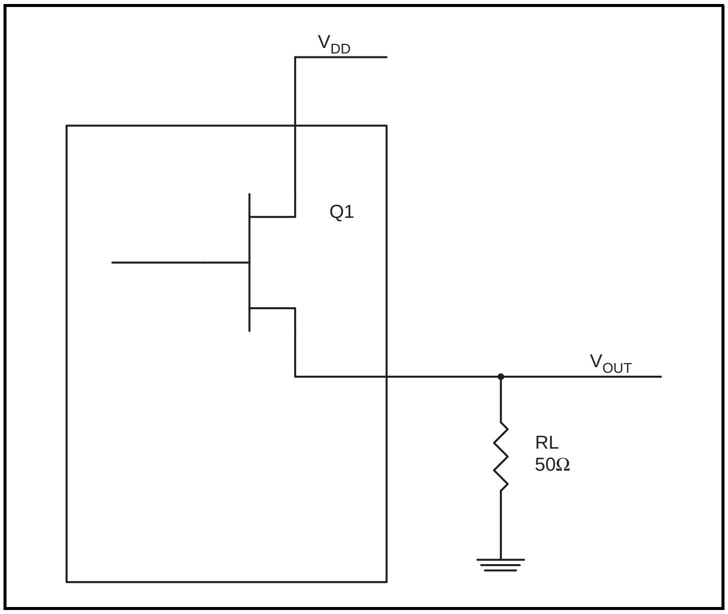


Figure 6. HSTL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load.

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = (V_{OH\_MAX}/R_L) * (V_{DD\_MAX} - V_{OH\_MAX})$

$Pd\_L = (V_{OL\_MAX}/R_L) * (V_{DD\_MAX} - V_{OL\_MAX})$

Pd_H = (1.8V/50Ω) * (3.465 - 1.8V) = 59.94mW

Pd_L = (0.6V/50Ω) * (3.465 - 0.6V) = 34.38mW

Total Power Dissipation per output pair = Pd_H + Pd_L = **94.32mW**

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for a 8 Lead TSSOP

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	129.5°C/W	125.5°C/W	123.5°C/W

Transistor Count

The transistor count for 842023 is: 2538

Package Outline and Package Dimensions

Package Outline - G Suffix for 8 Lead TSSOP

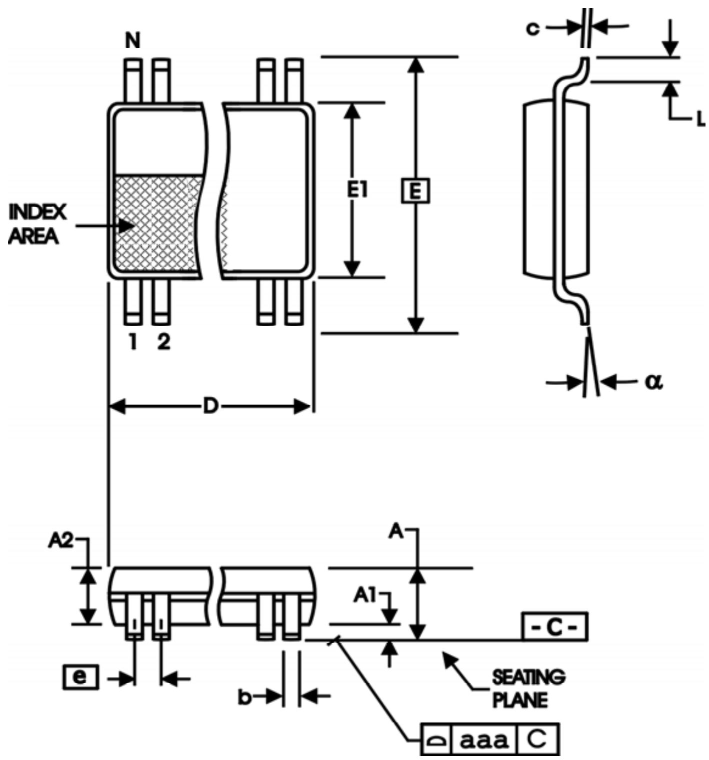


Table 9. Package Dimensions

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	8	
A		1.20
A1	0.5	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	2.90	3.10
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
842023BGLF	023BL	"Lead-Free" 8 Lead TSSOP	Tube	0°C to 70°C
842023BGLFT	023BL	"Lead-Free" 8 Lead TSSOP	Tape & Reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	 T4 10	1 4 7 8 12	Deleted HiPerClockS references throughout. Crystal Characteristics Table - added note. Deleted application note, *LVCMOS to XTAL Interface*. Added Note: Thermal pad (E-pad) must be connected to ground (GND). Deleted quantity from tape and reel.	11/2/12
A			Product Discontinuation Notice - Last time buy expires August 14, 2016. PDN CQ-15-04	8/14/15

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