CMOS
JDC π/4 DQPSK Baseband Transmit Port

AD7010

FEATURES

Single +5 V Supply
- **On-Chip π/4 DQPSK Modulator**
- **Root-Raised-Cosine Tx Filters, α = 0.5**
- **Two 10-Bit D/A Converters**
- **4th Order Reconstruction Filters**
- **Differential Analog Outputs**
- **On-Chip Ramp Up/Down Power Control**
- **On-Chip Tx Offset Calibration**
- **Very Low Power Dissipation, 30 mW typ**
- **Power Down Mode < 5 μA**

On-Chip Voltage Reference

24-Pin SSOP

APPLICATIONS

Japanese Digital Cellular Telephony

GENERAL DESCRIPTION

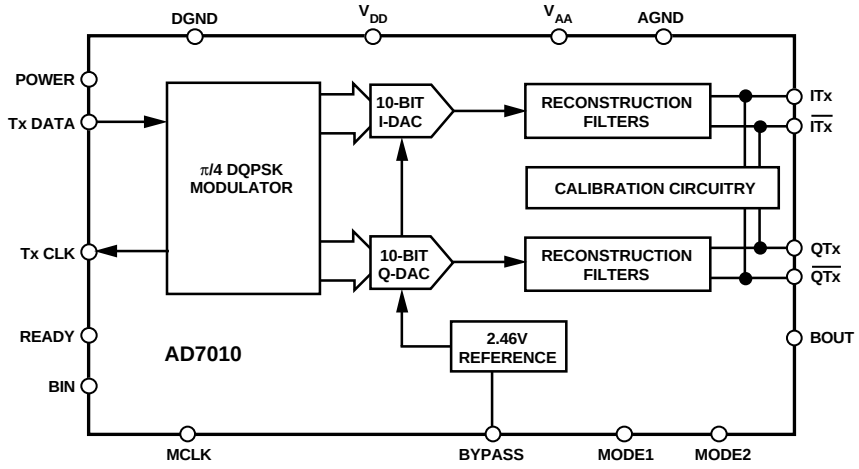
The AD7010 is a complete low power, CMOS, π/4 DQPSK modulator with single +5 V power supply. The part is designed to perform the baseband conversion of I and Q transmit waveforms in accordance with the Japanese Digital Cellular Telephone system.

The on-chip π/4 Differential Quadrature Phase Shift Keying (DQPSK) digital modulator, which includes the Root Raised Cosine filters, generates I and Q data in response to the transmit data stream. The AD7010 also contains ramp control envelope logic to shape the I and Q output waveforms when ramping up or down at the beginning or end of a transmit burst.

Besides providing all the necessary logic to perform π/4 DQPSK modulation, the part also provides reconstruction filters to smooth the DAC outputs, providing continuous time analog outputs. The AD7010 generates differential analog outputs for both the I and Q signals.

As it is a necessity for all digital mobile systems to use the lowest possible power, the device has power down options. The AD7010 is housed in a space efficient 24-pin SSOP (Shrink Small Outline Package).

FUNCTIONAL BLOCK DIAGRAM



REV. B

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AD7010–SPECIFICATIONS[1]

(V_{AA} = V_{DD} = +5 V ± 10%; Test = AGND = DGND = 0 V; f_{MCLK} = 2.688 MHz; Power = V_{DD}. All specifications are T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	AD7010ARS	Units	Test Conditions/Comments
DIGITAL MODE TRANSMIT			
No. of Channels	2		(ITx–$\overline{\text{ITx}}$) and (QTx–$\overline{\text{QTx}}$)
Output Signal Range	$V_{REF} \pm V_{REF}/4$	Volts	For Each Analog Output
Differential Output Range	$\pm V_{REF}/2$	Volts	I Channel = (ITx–$\overline{\text{ITx}}$) and Q Channel = (QTx–$\overline{\text{QTx}}$)
Signal Vector Magnitude[2]	0.875 ± 7.5%	Volts max	Measured Differentially
Error Vector Magnitude[2]	1	% rms typ	
	2.5	% rms max	
Offset Vector Magnitude[2]	0.5	% typ	
	2.5	% max	
JDC Spurious Power[2, 3]			
@ 25 kHz	–30	dB typ	
	–25	dB max	
@ 50 kHz	–60	dB typ	
	–55	dB max	
@ 75 kHz	–70	dB typ	
	–65	dB max	
@ 100 kHz, 150 kHz, 200 kHz	–70	dB typ	
	–65	dB max	
REFERENCE & CHANNEL SPECIFICATIONS			
Reference, V_{REF}	2.46	Volts	
Reference Accuracy	±5	%	
I and Q Gain Matching	±0.2	dB max	Measured @ 10 kHz
Power Down Option	Yes		Power = 0 V
LOGIC INPUTS			
V_{INH}, Input High Voltage	V_{DD}–0.9	V min	
V_{INL}, Input Low Voltage	0.9	V max	
I_{INH}, Input Current	10	µA max	
C_{IN}, Input Capacitance	10	pF max	
LOGIC OUTPUTS			
V_{OH}, Output High Voltage	V_{DD}–0.4	V min	$\lvert I_{OUT} \rvert \le 40$ µA
V_{OL}, Output Low Voltage	0.4	V max	$\lvert I_{OUT} \rvert \le 1.6$ mA
POWER SUPPLIES			
V_{DD}	4.5/5.5	V min/V max	
I_{DD}			
Transmit Section Active	8	mA max	Power = V_{DD}
	6	mA typ	
Transmit Section Powered Down[4]	35	µA max	MCLK Active
	5	µA max	MCLK Inactive

NOTES

[1]Operating temperature ranges as follows: A Version: –40°C to +85°C.

[2]See Terminology.

[3]Measured in continuous transmission and Burst transmission with the I and Q channels ramping up and down at the beginning and end of each burst.

[4]Measured while the digital inputs to the transmit interface are static and equal to 0 V or V_{DD}.

Specifications subject to change without notice.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD7010ARS	–40°C to +85°C	Shrink Small Outline Package	RS-24

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} Tx, V_{DD} Rx to AGND . . . . . –0.3 V to +7 V
AGND to DGND . . . . . –0.3 V to +0.3 V
Digital I/O Voltage to DGND . . . . . –0.3 V to V_{DD} to + 0.3 V
Analog I/O Voltage to AGND . . . . . –0.3 V to V_{DD} + 0.3 V
Operating Temperature Range
Industrial (A Version) . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature . . . . . +150°C
SSOP θ_{JA} Thermal Impedance . . . . . +122°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) . . . . . +215°C
Infrared (15 sec) . . . . . +220°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table I.

MODE 1	MODE 2	Operation
0	0	Digital JDC Mode
0	1	FTEST
1	X	Factory Test, Reserved

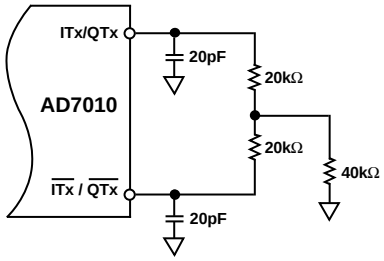


Figure 1. Analog Output Load Test Circuit

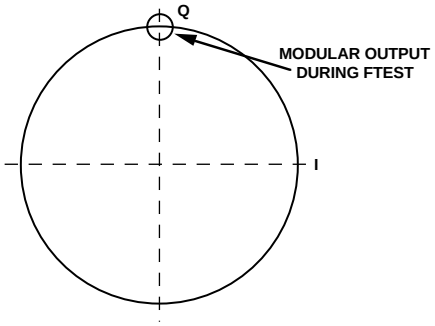


Figure 2. Modulator State During FTEST

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7010 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



MASTER CLOCK TIMING

(V_{AA} = V_{DD} = +5 V ± 10%; AGND = DGND = 0 V. All specifications are T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	Limit at T_A = –40°C to +85°C	Units	Description
t_1	300	ns min	MCLK Cycle Time
t_2	100	ns min	MCLK High Time
t_3	100	ns min	MCLK Low Time

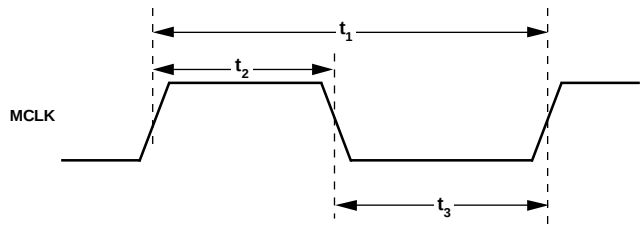


Figure 3. Master Clock (MCLK) Timing

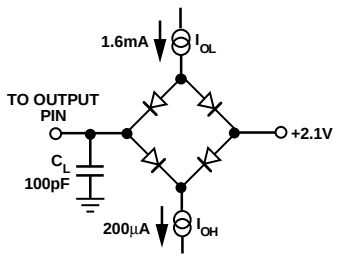


Figure 4. Load Circuit for Digital Outputs

TRANSMIT SECTION TIMING

(V_{AA} = V_{DD} = +5 V ± 10%; AGND = DGND = 0 V, f_{MCLK} = 2.688 MHz. All specifications are T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	Limit at T_A = –40°C to +85°C	Units	Description
t_4	10	ns min	POWER Setup Time.
	t_1 – 10	ns max	
t_5	$4097t_1$ + 70	ns max	MCLK rising edge, after POWER high, to READY rising edge.
t_6	10	ns min	BIN Setup Time.
	t_1 – 10	ns max	
t_7	t_1 + 70	ns max	MCLK to READY low propagation delay.
t_8	$3t_1$ + 70	ns	MCLK rising edge, after BIN high, to first TxCLK rising edge.
t_9	$64t_1$	ns	TxCLK Cycle Time.
t_{10}	$32t_1$	ns	TxCLK High Time.
t_{11}	$32t_1$	ns	TxCLK Low Time.
t_{12}	50	ns min	TxCLK falling edge to TxDATA setup time.
t_{13}	0	ns min	TxCLK falling edge to TxDATA hold time.
t_{14}	$3t_1$	ns max	BIN low setup to last transmitted symbol after ramp down.
t_{15}	$124t_1$	ns max	BIN low hold to last transmitted symbol after ramp down.
t_{16}	$7.5t_9$	ns	Ramp down cycle time after the last transmitted symbol.
t_{17}	$30t_1$	ns max	Last TxCLK falling edge to READY rising edge.
t_{18}	10	ns max	Digital Output Rise Time.
t_{19}	10	ns max	Digital Output Fall Time.

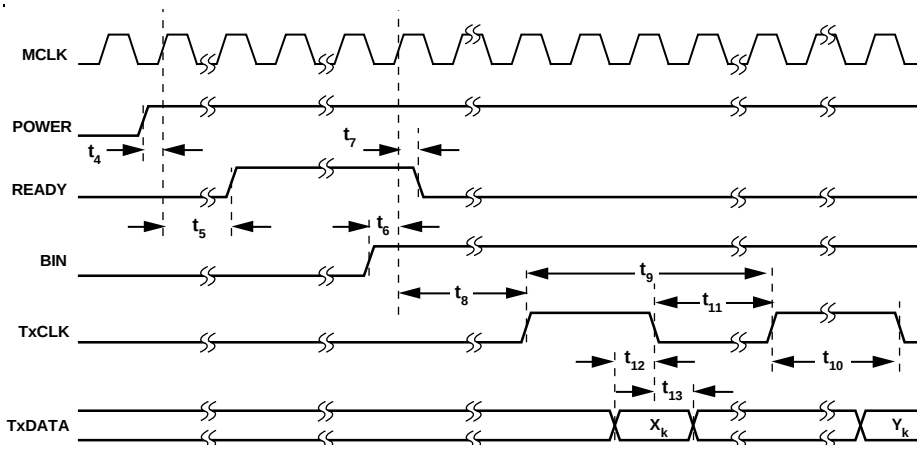


Figure 5. Transmit Timing at the Start of a Tx Burst

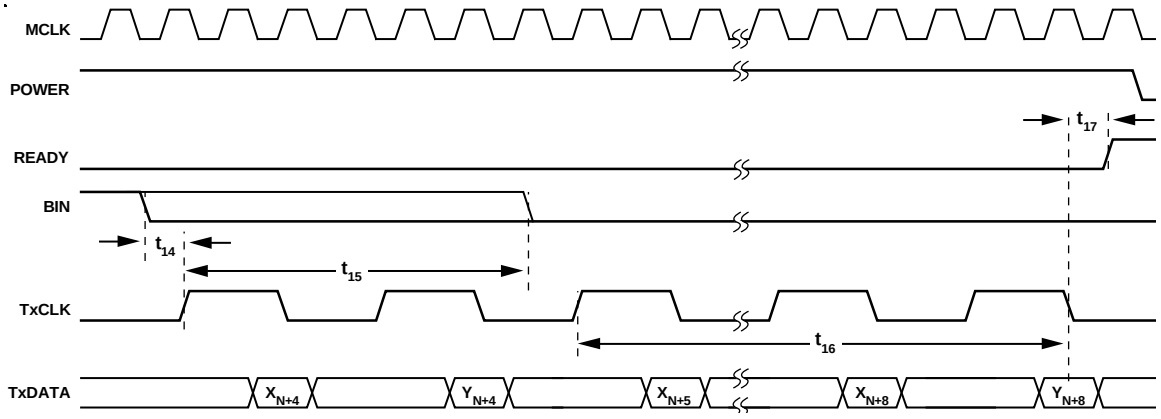
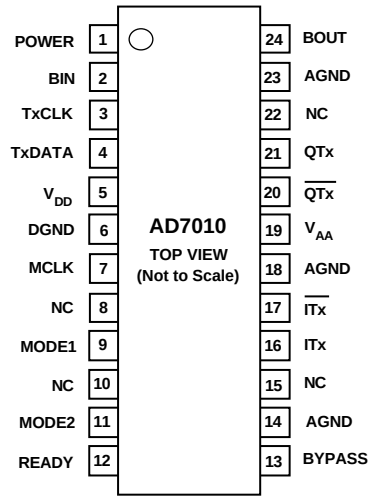


Figure 6. Transmit Timing at the End of a Tx Burst

PIN FUNCTION DESCRIPTION

SSOP Pin Number	Mnemonic	Function
POWER SUPPLY		
19	V_{AA}	Positive power supply for analog section.
5	V_{DD}	Positive power supply for digital section, both supplies should be externally tied together.
14, 18, 23	AGND	Analog ground for transmit section.
6	DGND	Digital ground for transmit section, both grounds should be externally tied together.
ANALOG SIGNAL AND REFERENCE		
13	BYPASS	Reference decoupling output. A decoupling capacitor should be connected between this pin a and AGND.
16, 17	ITx, $\overline{\text{ITx}}$	Differential analog outputs for the I channel, representing true and complementary outputs of the I waveform.
21, 20	QTx, $\overline{\text{QTx}}$	Differential analog outputs for the Q channel, representing true and complementary outputs of the Q waveform.
TRANSMIT INTERFACE AND CONTROL		
7	MCLK	Master clock, digital input. This pin should be driven by a 2.688 MHz CMOS compatible clock source in digital mode.
3	TxCLK	This is a digital output, transmit clock. This may be used to clock in transmit data at 42 kHz.
4	TxDATA	This is a digital input. This pin is used to clock in transmit data on the falling edge of TxCLK at a rate of 42 kHz.
2	BIN	This is a digital input. This input is used to initiate the ramping up (BIN high) or down (BIN low) of the I and Q waveforms.
24	BOUT	Burst out, digital output. This is the BIN input delayed by the pipeline delay, both digital and analog, of the AD7010. This can be used to turn on and off the RF amplifiers in synchronization with the I and Q waveforms.
1	POWER	Transmit sleep mode, digital input. When this goes low, the AD7010 goes into sleep mode, drawing minimal current. When this pin goes high, the AD7010 is brought out of sleep mode and initiates a self-calibration routine to eliminate the offset between ITx & $\overline{\text{ITx}}$ and the offset between QTx & $\overline{\text{QTx}}$.
12	READY	Transmit ready, digital output. This output goes high once the self-calibration routine is complete.
9, 11	MODE1, MODE2	Mode control, digital inputs. These are used to enter the AD7010 into three different operating modes, see Table I.
8, 10, 15, 22	NC	No Connects. These pins are no connects and should not be used as routes for other circuit signals.

SSOP PIN CONFIGURATION



TERMINOLOGY

Error Vector Magnitude

This is a measure of the rms error vector introduced by the AD7010 where signal error vector is defined as the rms deviation of a transmitted symbol from its ideal position, as illustrated in Figure 7, when filtered by an ideal RRC filter.

Gain Matching Between Channels

This is the Gain matching between the I and Q outputs, measured when transmitting all zeros.

Offset Vector Magnitude

This is a measure of the offset vector introduced by the AD7010 as illustrated in Figure 7. The offset vector is calculated so as to minimize the rms error vector for each of the constellation points.

Output Signal Range and Differential Output Range

The output signal range is the output voltage swing and dc bias level for each of the analog outputs. The Differential Output Range is the difference between ITx and $\overline{\text{ITx}}$ for the I channel and the difference between QTx and $\overline{\text{QTx}}$ for the Q Channel.

JDC Spurious Power

This is the rms sum of the spurious power measured at multiples of 25 kHz, in a rectangular window of ±10.5 kHz, relative to twice the rms power in a RRC window in the 0 kHz to 10.5 kHz band.

Signal Vector Magnitude

This is the radius of the IQ constellation diagram as illustrated in Figure 7.

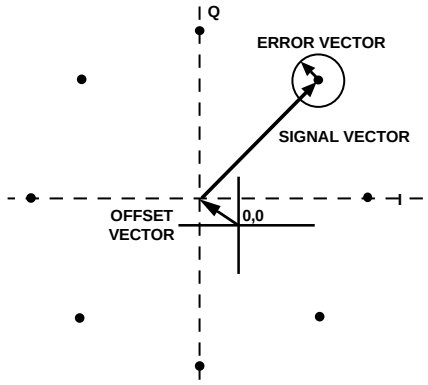


Figure 7.

CIRCUIT DESCRIPTION

TRANSMIT SECTION

The transmit section of the AD7010 generates π/4 DQPSK I and Q waveforms in accordance with JDC specification. This is accomplished by a digital π/4 DQPSK modulator, which includes the Root-Raised Cosine filters (α = 0.5), followed by two 10-bit DACs and on-chip reconstruction filters. The π/4 DQPSK (Differential Quadrature Phase Shift Keying) digital modulator generates 10-bit I and Q data in response to the transmit data stream. The 10-bit I and Q DACs are filtered by on-chip reconstruction filters, which also generate differential analog outputs for both I and Q channels.

π/4 DQPSK Modulator

The π/4 DQPSK modulator generates 10-bit I and Q data (In-phase and Quadrature) which are loaded into the I and Q 10-bit transmit DACs.

Table II.

X_k	Y_k	$\Delta\phi_k$
1	1	–3 π/4
0	1	3 π/4
0	0	π/4
1	0	–π/4

Figure 8 shows the functional block diagram of the π/4 DQPSK modulator. The transmit serial data (TxDATA) is first converted into Di-bit symbols [X_k, Y_k], using a 2-bit serial to parallel converter. The data is then differentially encoded; symbols are transmitted as changes in phase rather than absolute phases. Each symbol represents a phase change, as illustrated in Table II, and this along with the previously transmitted symbol determines the next symbol to be transmitted. The differential phase encoder generates I and Q impulses [I_k, Q_k] in response to the Di-bit symbols according to:

$$I_k = COS[\phi_{k-1} + \Delta\phi_k]$$

$$Q_k = SIN[\phi_{k-1} + \Delta\phi_k]$$

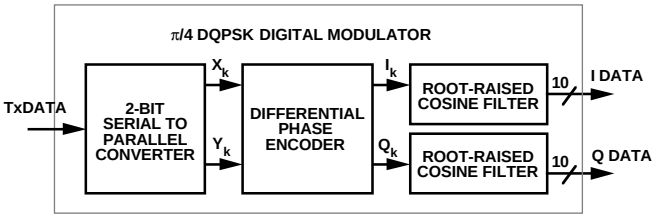


Figure 8. π/4 DQPSK Modulator Functional Block Diagram

Figure 9 illustrates the π/4 DQPSK constellation diagram as described above, showing the eight possible states for [I_k, Q_k].

The I_k and Q_k impulses are then filtered by FIR Root-Raised Cosine Filters (α = 0.5), generating 10-bit I and Q data. The FIR Root-Raised Cosine Filters have an impulse response of ±4 symbols.

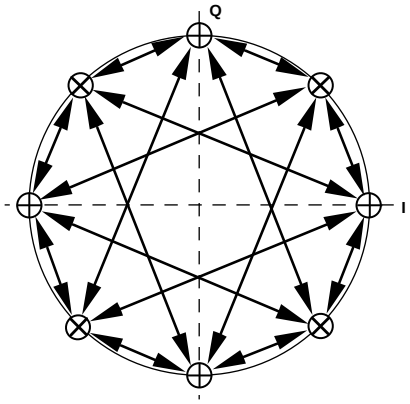


Figure 9. π/4 DQPSK Constellation Diagram

Transmit Calibration

When the transmit section is brought out of sleep mode (Power high), the transmit section initiates a self-calibration routine to remove the offset between ITx and $\overline{\text{ITx}}$ and the offset between QTx and $\overline{\text{QTx}}$. READY goes high on the completion of the self-calibration routine. Once READY goes high, BIN (Burst In) can be brought high to initiate a transmit burst.

Ramp-Up/Down Envelope Logic

The AD7010 provides on-chip envelope shaping logic, providing power shaping control for the beginning and end of a transmit burst. When BIN (Burst In) is brought high, the modulator is reset to a transmitting all zeros state (i.e., $X_k = Y_k = 0$) and continues to transmit all zeros for the first two symbols, during which the ramp-up envelope goes from zero to full scale as illustrated in Figure 10. The next symbol to be transmitted is [I_1, Q_1], which represents the first two data bits clocked in after BIN going high, i.e., [X_1, Y_1].

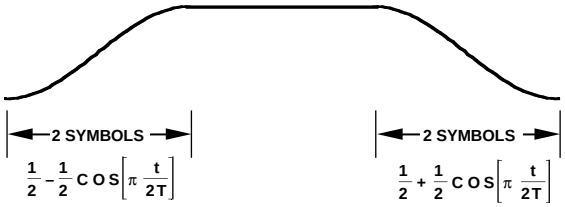


Figure 10. Ramp Envelope

When BIN is brought low, indicating the end of a transmit burst, the current Di-bit symbol [X_{N+4}, Y_{N+4}] that the AD7010 is receiving will be the last symbol to be computed for the 4 symbol ramp-down sequence. Also the N^{th} symbol is the last active symbol prior to ramping down.

However, because the impulse response is equal to ±4 symbols, four additional symbols are required to fully compute the analog outputs when transmitting the $(N+4)^{th}$ symbol. Hence there will be eight subsequent TxCLKs, latching four additional Di-bit symbols: [X_{N+5}, Y_{N+5}] to [X_{N+8}, X_{N+8}].

As Figure 11 illustrates, the ramp-down envelope reaches zero after two symbols, hence the third and fourth symbols do not actually get transmitted.

Reconstruction Filters

The reconstruction filters smooth the DAC output signals, providing continuous time I and Q waveforms at the output pins. These are 4th order Bessel low-pass filters with a –3 dB frequency of approximately 22 kHz, the frequency response is illustrated in Figure 12. The filters are designed to have a linear phase response in the passband and due to the reconstruction filters being on-chip, the phase mismatch between the I and Q transmit channels is kept to a minimum.

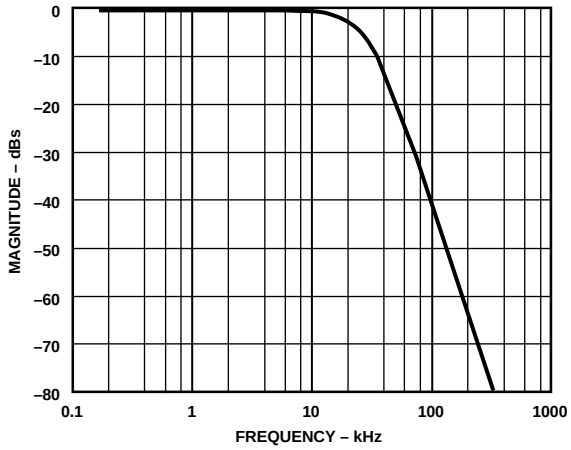


Figure 12. Reconstruction Filter Frequency Response for I and Q DACs, MCLK = 2.688 MHz

Transmit Section Digital Interface

MODE1 = MODE2 = DGND: Digital π/4 DQPSK Mode

Figures 5 and 6 show the timing diagrams for the transmit interface when operating in JDC π/4 DQPSK mode. Power is sampled on the rising edge of MCLK. When Power is brought high, the transmit section is brought out of sleep mode and initiates a self-calibration routine as described above. Once the self-calibration is complete, the READY signal goes high to indicate that a transmit burst can now begin. BIN (Burst in) is brought high to initiate a transmit burst and should only be brought high if the READY signal is already high.

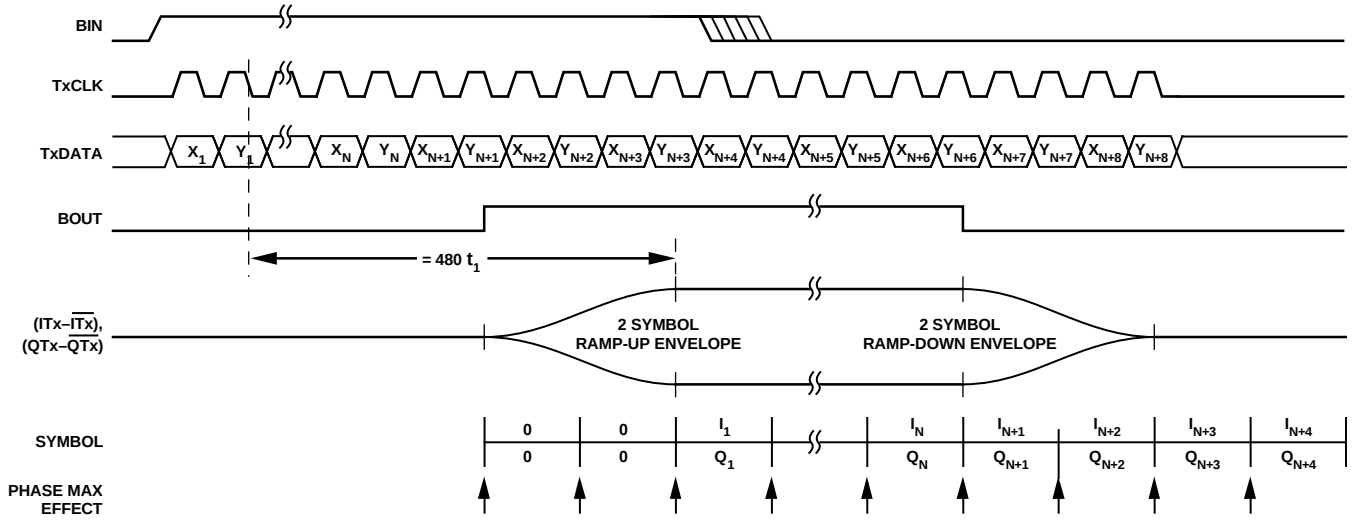


Figure 11. Transmit Burst

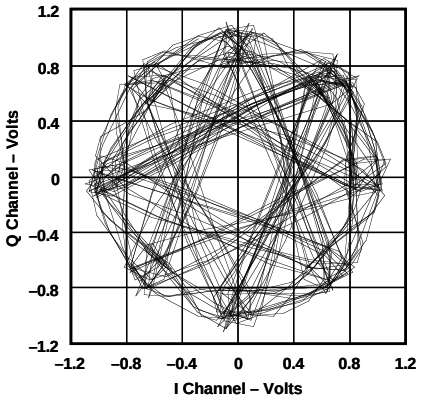


Figure 13. AD7010 I vs. Q Waveforms when Transmitting Random Data

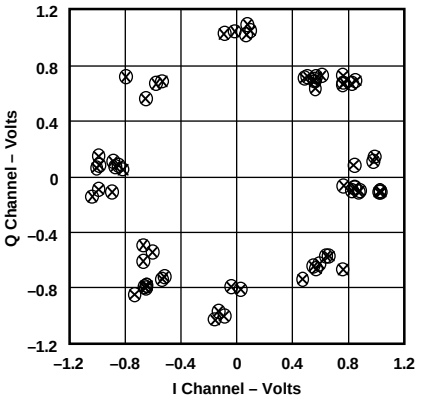


Figure 15. AD7010 Transmit Constellation Diagram

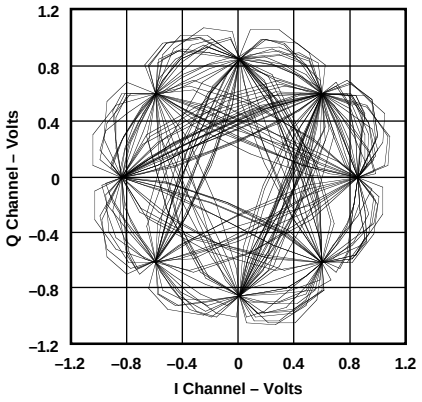


Figure 14. AD7010 I vs. Q Waveforms Filtered by an Ideal Root Raised Cosine Receive Filter

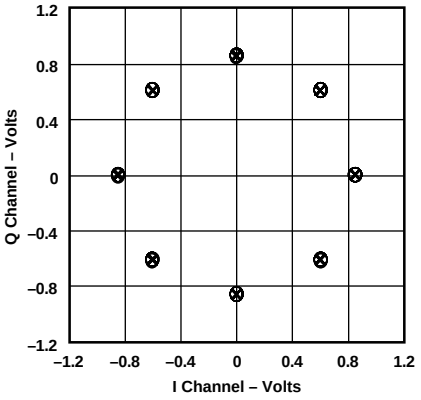


Figure 16. AD7010 Constellation Diagram when Filtered by an Ideal Root Raised Cosine Receive Filter

When BIN goes high, the READY signal goes low on the next rising edge of MCLK and TxCLK becomes active after a further two MCLK cycles. TxCLK can be used to clock out the transmit data from the ASIC or DSP on the rising edge of TxCLK and the AD7010 will latch TxDATA on the falling edge of TxCLK.

When BIN is brought low, the AD7010 will continue to clock in the current Di-bit symbol (X_{N+4}, Y_{N+4}) and will continue for a further eight TxCLK cycles (four symbols). After the final TxCLK, READY goes high waiting for BIN to be brought high to begin the next transmit burst.

When Power is brought low, this puts the transmit section into a low power sleep mode, drawing minimal current. The analog outputs go high impedance while in low power sleep mode.

MODE1 = DGND; MODE2 = V_{DD}: Frequency Test Mode

A special FTEST (Frequency TEST) mode is provided for the customer, where no phase modulation takes place and the modulator outputs remain static. ITx is set to zero and QTx is set to full scale as Figure 2 illustrates. However, the normal ramp-up/down envelope is still applied during the beginning and end of a burst.

MODE1 = V_{DD}; MODE2 = DGND: Factory Test Mode

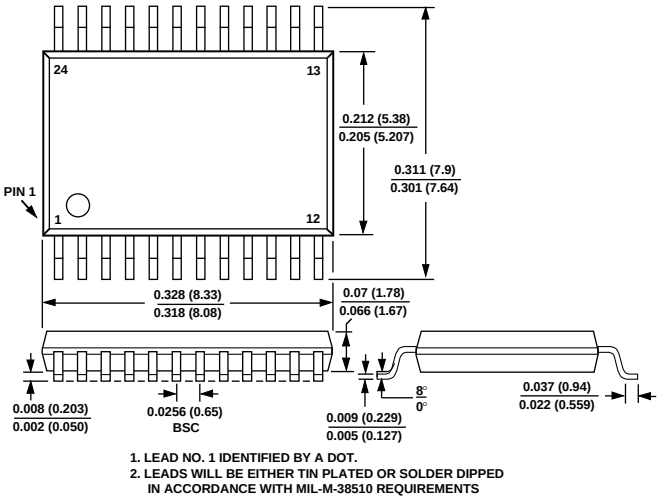
MODE1 = MODE2 = V_{DD}: Factory Test Mode

These modes are reserved for factory test only and should not be used by the customer for correct device operation.

OUTLINE DIMENSIONS

Dimensions are shown in inches and (mm).

24-Lead SSOP (RS-24)



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