Low Cost, Host-Controlled Li-Ion and Li-Polymer Battery Charger With Low Iq

FEATURES

- **NMOS-NMOS Synchronous Buck Converter with 300 kHz Frequency and >95% Efficiency**
- **30-ns Minimum Driver Dead-time and 99.5% Maximum Effective Duty Cycle**
- **High-Accuracy Voltage and Current Regulation**
  - **±0.5% Charge Voltage Accuracy**
  - **±3% Charge Current Accuracy**
  - **±3% Adapter Current Accuracy**
  - **±2% Input Current Sense Amp Accuracy**
- **Integration**
  - **Internal Loop Compensation**
  - **Internal Soft-Start**
- **Safety**
  - **Dynamic Power Management (DPM) with Status Indicator**
  - **Charger Overcurrent Protection**
  - **Battery Overvoltage Protection**
  - **Thermal Shutdown**
- **Supports Two, Three, or Four Li+ Cells**
- **8 – 24 V AC/DC-Adapter Operating Range**
- **Analog Inputs with Ratiometric Programming via Resistors or DAC/GPIO Host Control**
  - **Charge Voltage (4-4.512 V/cell)**
  - **Charge Current (up to 8 A, with 10-mΩ Sense Resistor)**
  - **Adapter Current Limit (DPM)**
- **Status and Monitoring Outputs**
  - **AC/DC Adapter Present with Programmable Voltage Threshold**
  - **DPM Loop Active ($\overline{\text{DPMDET}}$)**
  - **Current Drawn from Input Source**
- **Charge Enable**
- **24-pin, 4x4-mm QFN Package**
- **Energy Star Low Iq**
  - **< 10 μA Off-state Discharge Current**
  - **< 1.5 mA Off-state Input Quiescent Current**

APPLICATIONS

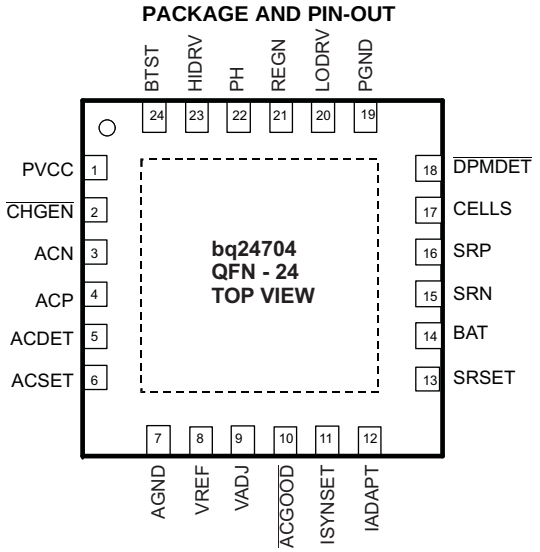
- **Notebook and Netbook Computers**
- **Portable Data-Capture Terminals**
- **Portable Printers**
- **Medical Diagnostics Equipment**
- **Battery Bay Chargers**
- **Battery Back-Up Systems**

DESCRIPTION

The bq24704 is a high-efficiency, synchronous battery charger with integrated compensation offering low component count for space-limited Li-Ion and Li-Polymer battery charging applications. Charge current and voltage programming allows high regulation accuracies, and can be either hardwired with resistors, or programmed by the system power-management microcontroller using a DAC or GPIOs.

The bq24704 charges two, three, or four series Li+ cells, supporting up to 8 A of charge current, and is available in a 24-pin, 4x4-mm thin QFN package.

PACKAGE AND PIN-OUT



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PowerPad is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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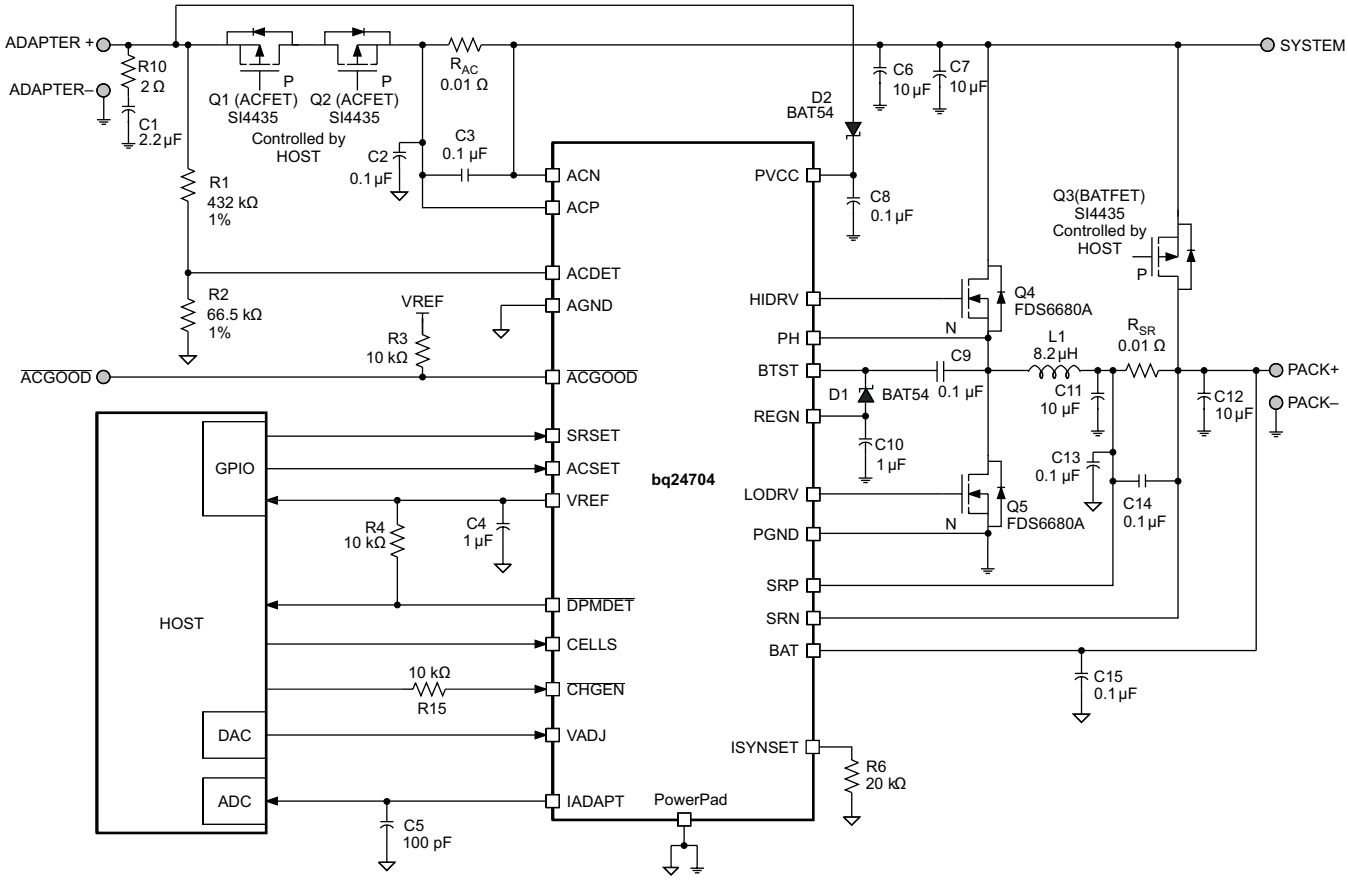
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

The bq24704 features Dynamic Power Management (DPM) and input power limiting. These features reduce battery charge current when the input power limit is reached to avoid overloading the AC adapter when supplying the load and the battery charger simultaneously. A highly-accurate current-sense amplifier enables precise measurement of input current from the AC adapter to monitor the overall system power.



(1) Pull-up rail could be either VREF or other system rail.

(2) SRSET/ACSET could come from either DAC or resistor dividers.

(3) V_{IN} = 20 V, V_{BAT} = 3-cell Li-Ion, I_{CHARGE} = 3 A, $I_{ADAPTER_LIMIT}$ = 4 A

Figure 1. Typical System Schematic, Voltage and Current Programmed by DAC

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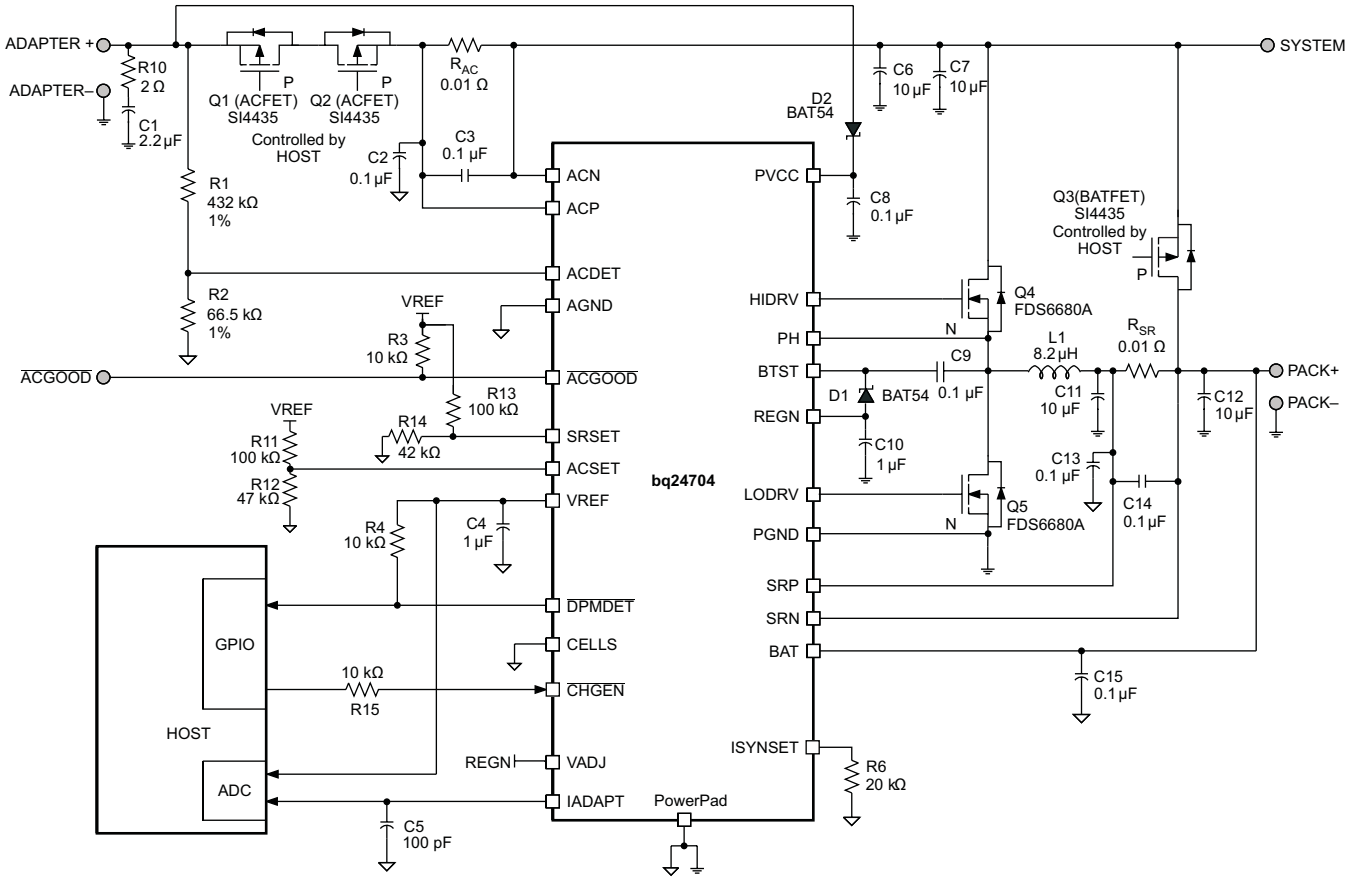

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Figure 2. Typical System Schematic, Voltage and Current Programmed by Resistor

ORDERING INFORMATION

Part Number	Package	Ordering Number (Tape and Reel)	Quantity
bq24704	24-PIN 4 x 4 mm QFN	bq24704RGER	3000
		bq24704RGET	250

PACKAGE THERMAL DATA

PACKAGE	θ_{JA}	T_A=25°C POWER RATING	DERATING FACTOR ABOVE T_A= 25°C
QFN – RGE(1)(2)	45°C/W	2.33 W	0.023 W/°C

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

(2) This data is based on using the JEDEC High-K board and the exposed die pad is connected to a Cu pad on the board. This is connected to the ground plane by a 2x3 via matrix.

Table 1. TERMINAL FUNCTIONS – 24-PIN QFN

TERMINAL		DESCRIPTION
NAME	NO.	
PVCC	1	IC power positive supply. Place a 0.1-µF ceramic capacitor from PVCC to PGND pin close to the IC.
$\overline{\text{CHGEN}}$	2	Charge enable active-low logic input. LO enables charge. HI disables charge. Connect a 10-kΩ pull-up resistor from $\overline{\text{CHGEN}}$ to a pull-up supply rail.
ACN	3	Adapter current sense resistor, negative input. A 0.1-µF ceramic capacitor is placed from ACN to ACP to provide ACN 2 differential-mode filtering. An optional 0.1-µF ceramic capacitor is placed from ACN pin to AGND for common-mode filtering.
ACP	4	Adapter current sense resistor, positive input. A 0.1-µF ceramic capacitor is placed from ACN to ACP to provide differential-mode filtering. A 0.1-µF ceramic capacitor is placed from ACP pin to AGND for common-mode filtering.
ACDET	5	Adapter detected voltage set input. Program the adapter detect threshold by connecting a resistor divider from adapter input to ACDET pin to AGND pin. Adapter voltage is detected if ACDET-pin voltage is greater than 2.4 V. The I_{ADAPT} current sense amplifier is active when the ACDET pin voltage is greater than 0.6 V.
ACSET	6	Adapter current set input. The voltage ratio of ACSET voltage versus VREF voltage programs the input current regulation set-point during Dynamic Power Management (DPM). Program by connecting a resistor divider from VREF to ACSET to AGND; or by connecting the output of an external DAC to the ACSET pin.
AGND	7	Analog ground. Ground connection for low-current sensitive analog and digital signals. On PCB layout, connect to the analog ground plane, and only connect to PGND through the PowerPad underneath the IC.
VREF	8	3.3-V regulated voltage output. Place a 1-µF ceramic capacitor from VREF to AGND pin close to the IC. This voltage could be used for ratiometric programming of voltage and current regulation.
VADJ	9	Charge voltage set input. The voltage ratio of VADJ voltage versus VREF voltage programs the battery voltage regulation set-point. Program by connecting a resistor divider from VREF to VADJ, to AGND; or, by connecting the output of an external DAC to VADJ. VADJ connected to REGN programs the default of 4.2 V per cell.
$\overline{\text{ACGOOD}}$	10	Valid adapter active-low detect logic open-drain output. Pulled low when input voltage is above ACDET programmed threshold. Connect a 10-kΩ pullup resistor from $\overline{\text{ACGOOD}}$ pin to pullup supply rail.
ISYNSET	11	Synchronous mode current set input. Place a resistor from ISYNSET to AGND to program the charge undercurrent threshold to force non-synchronous converter operation at low output current, and to prevent negative inductor current. Threshold should be set at greater than half of the maximum inductor ripple current (50% duty cycle).
IADAPT	12	Adapter current sense amplifier output. IADAPT voltage is 16 times the differential voltage across ACP-ACN. Place a 100-pF or less ceramic decoupling capacitor from IADAPT to AGND.
SRSET	13	Charge current set input. The voltage ratio of SRSET voltage versus VREF voltage programs the charge current regulation set-point. Program by connecting a resistor divider from VREF to SRSET to AGND; or by connecting the output of an external DAC to SRSET pin.
BAT	14	Battery voltage remote sense. Directly connect a kelvin sense trace from the battery pack positive terminal to the BAT pin to accurately sense the battery pack voltage. Place a 0.1-µF capacitor from BAT to AGND close to the IC to filter high-frequency noise.
SRN	15	Charge current sense resistor, negative input. A 0.1-µF ceramic capacitor is placed from SRN to SRP to provide differential-mode filtering. An optional 0.1-µF ceramic capacitor is placed from SRN pin to AGND for common-mode filtering.
SRP	16	Charge current sense resistor, positive input. A 0.1-µF ceramic capacitor is placed from SRN to SRP to provide differential-mode filtering. A 0.1-µF ceramic capacitor is placed from SRP pin to AGND for common-mode filtering.
CELLS	17	2, 3 or 4 cells selection logic input. Logic low programs 3 cell. Logic high programs 4 cell. Floating programs 2 cell.
$\overline{\text{DPMDET}}$	18	Dynamic power management (DPM) input current loop active, open-drain output status. Logic low indicates input current is being limited by reducing the charge current. Connect 10-kΩ pullup resistor from $\overline{\text{DPMDET}}$ to VREF or a different pullup-supply rail.
PGND	19	Power ground. Ground connection for high-current power converter node. On PCB layout, connect directly to source of low-side power MOSFET, to ground connection of in put and output capacitors of the charger. Only connect to AGND through the PowerPad underneath the IC.
LODRV	20	PWM low side driver output. Connect to the gate of the low-side power MOSFET with a short trace.
REGN	21	PWM low side driver positive 6-V supply output. Connect a 1-µF ceramic capacitor from REGN to PGND, close to the IC. Use for high-side driver bootstrap voltage by connecting a small-signal Schottky diode from REGN to BTST.
PH	22	PWM high side driver negative supply. Connect to the phase switching node (junction of the low-side power MOSFET drain, high-side power MOSFET source, and output inductor). Connect the 0.1-µF bootstrap capacitor from from PH to BTST.
HIDRV	23	PWM high side driver output. Connect to the gate of the high-side power MOSFET with a short trace.
BTST	24	PWM high side driver positive supply. Connect a 0.1-µF bootstrap ceramic capacitor from BTST to PH. Connect a small bootstrap Schottky diode from REGN to BTST.

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Table 1. TERMINAL FUNCTIONS – 24-PIN QFN (continued)

TERMINAL NAME	TERMINAL NO.	DESCRIPTION
PowerPad™		Exposed pad beneath the IC. AGND and PGND star-connected only at the PowerPad plane. Always solder PowerPad to the board, and have vias on the PowerPad plane connecting to AGND and PGND planes . It also serves as a thermal pad to dissipate the heat.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1) (2)

		VALUE	UNIT
Voltage range	PVCC, ACP, ACN, SRP, SRN, BAT	–0.3 to 30	V
	PH	–1 to 30	
	REGN, LODRV, VADJ, ACSET, SRSET, ACDET, ISYNSET, $\overline{\text{CHGEN}}$, CELLS, $\overline{\text{ACGOOD}}$, $\overline{\text{DPMDET}}$, IADAPT	–0.3 to 7	
	VREF	–0.3 to 3.6	
	BTST, HIDRV with respect to AGND and PGND	–0.3 to 36	
Maximum difference voltage	ACP–ACN, SRP–SRN, AGND–PGND	–0.5 to 0.5	V
Junction temperature range		–40 to 155	°C
Storage temperature range		–55 to 155	

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND if not specified. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the data book for thermal limitations and considerations of packages.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Voltage range	PH	–1		24	V
	PVCC, ACP, ACN, SRP, SRN, BAT	0		24	
	REGN, LODRV, VADJ	0		6.5	
	VREF	0		3.3	
	ACSET, SRSET, ACDET, ISYNSET, $\overline{\text{CHGEN}}$, CELLS, $\overline{\text{ACGOOD}}$, $\overline{\text{DPMDET}}$, IADAPT	0		5.5	
	BTST, HIDRV with respect to AGND and PGND	0		30	
	AGND, PGND	–0.3		0.3	
Maximum difference voltage: ACP–ACN, SRP–SRN		–0.3		0.3	V
Junction temperature range		–40		125	°C
Storage temperature range		–55		150	

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ELECTRICAL CHARACTERISTICS

7 V ≤ V_{PVCC} ≤ 24 V, 0°C < T_J < +125°C, typical values are at T_A = 25°C, with respect to AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPERATING CONDITIONS						
V_{PVCC_OP}	PVCC Input voltage operating range		5		24	V
CHARGE VOLTAGE REGULATION						
$V_{BAT_REG_RNG}$	BAT voltage regulation range	4V-4.512V per cell, times 2,3,4 cell	8		18	V
V_{ADJ_OP}	VADJ voltage range		0		REGN	V
	Charge voltage regulation accuracy	8 V, 8.4 V, 9.024 V	–0.5%		0.5%	
		12 V, 12.6 V, 13.536 V	–0.5%		0.5%	
		16 V, 16.8 V, 18.048 V	–0.5%		0.5%	
	Charge voltage regulation set to default to 4.2 V per cell	VADJ connected to REGN, 8.4 V, 12.6 V, 16.8 V	–0.5%		0.5%	
CHARGE CURRENT REGULATION						
V_{IREG_CHG}	Charge current regulation differential voltage range	V_{IREG_CHG} = V_{SRP} – V_{SRN}	0		100	mV
V_{SRSET_OP}	SRSET voltage range		0		VREF	V
	Charge current regulation accuracy	V_{IREG_CHG} = 40–100 mV	–3%		3%	
		V_{IREG_CHG} = 20 mV	–5%		5%	
		V_{IREG_CHG} = 5 mV	–25%		25%	
		V_{IREG_CHG} = 1.5 mV (V_{BAT} ≥ 4V)	–33%		33%	
INPUT CURRENT REGULATION						
V_{IREG_DPM}	Adapter current regulation differential voltage range	V_{IREG_DPM} = V_{ACP} – V_{ACN}	0		125	mV
V_{ACSET_OP}	ACSET voltage range		0		VREF	V
	Input current regulation accuracy	V_{IREG_DPM} = 40–125 mV	–3%		3%	
		V_{IREG_DPM} = 20 mV	–5%		5%	
		V_{IREG_DPM} = 5 mV	–25%		25%	
		V_{IREG_DPM} = 1.5 mV	–33%		33%	
VREF REGULATOR						
V_{VREF_REG}	VREF regulator voltage	V_{ACDET} > 0.6 V, 0-30 mA	3.267	3.3	3.333	V
I_{VREF_LIM}	VREF current limit	V_{VREF} = 0 V, V_{ACDET} > 0.6 V	35		75	mA
REGN REGULATOR						
V_{REGN_REG}	REGN regulator voltage	V_{ACDET} > 0.6 V, 0-75 mA, PVCC > 10 V	5.6	5.9	6.2	V
I_{REGN_LIM}	REGN current limit	V_{REGN} = 0 V, V_{ACDET} > 0.6 V	90		135	mA
ADAPTER CURRENT SENSE AMPLIFIER						
V_{ACP/N_OP}	Input common mode range	Voltage on ACP/ACN	0		24	V
V_{IADAPT}	IADAPT output voltage range		0		2	V
I_{IADAPT}	IADAPT output current		0		1	mA
A_{IADAPT}	Current sense amplifier voltage gain	A_{IADAPT} = V_{IADAPT} / $V_{ACP-ACN}$		16		V/V
	Adapter current sense accuracy at the condition $V_{ACP-ACN}$<1.5V x $I_{ADAPTER}$ x R_{AC} (1)	$V_{ACP-ACN}$ = 40–125 mV	–2%		2%	
		$V_{ACP-ACN}$ = 20 mV	–3%		3%	
		$V_{ACP-ACN}$ = 5 mV	–25%		25%	
		$V_{ACP-ACN}$ = 1.5 mV	–30%		30%	
I_{IADAPT_LIM}	Output current limit	V_{IADAPT} = 0 V	1			mA
C_{IADAPT_MAX}	Maximum output load capacitance	For stability with 0 mA to 1 mA load			100	pF

(1) $I_{ADAPTER}$ is the input adapter current regulation setting (refer to Equation 3).

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ELECTRICAL CHARACTERISTICS (continued)

7 V ≤ V_{PVCC} ≤ 24 V, 0°C < T_J < +125°C, typical values are at T_A = 25°C, with respect to AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ACDET COMPARATOR						
$V_{PVCC-BAT_OP}$	Differential Voltage from PVCC to BAT		–20		24	V
V_{ACDET_CHG}	ACDET adapter-detect rising threshold	Min voltage to enable charging, V_{ACDET} rising	2.376	2.40	2.424	V
$V_{ACDET_CHG_HYS}$	ACDET falling hysteresis	V_{ACDET} falling		40		mV
	ACDET rising deglitch(2)	V_{ACDET} rising	0.9	1.2	1.5	s
	ACDET falling deglitch	V_{ACDET} falling		10		µs
V_{ACDET_BIAS}	ACDET enable-bias rising threshold	Min voltage to enable all bias, V_{ACDET} rising	0.56	0.62	0.68	V
$V_{ACDET_BIAS_HYS}$	Adapter present falling hysteresis	V_{ACDET} falling		20		mV
	ACDET_BIAS rising deglitch (2)	V_{ACDET} rising		10		µs
	ACDET_BIAS falling deglitch	V_{ACDET} falling		10		
OPEN-DRAIN LOGIC OUTPUT PIN CHARACTERISTICS ($\overline{ACGOOD}$)						
$V_{O(LO)}$	Output low saturation voltage	Sink Current = 4 mA			0.5	V
	$\overline{ACGOOD}$ falling delay	V_{ACDET} rising	0.9	1.2	1.5	s
	$\overline{ACGOOD}$ rising delay	V_{ACDET} falling		10		µs
PVCC / BAT COMPARATOR						
$V_{PVCC-BAT_FALL}$	PVCC to BAT falling threshold	V_{PVCC} – V_{BAT} falling to disable Charger	140	185	240	mV
$V_{PVCC-BAT__HYS}$	PVCC to BAT hysteresis			50		mV
	PVCC to BAT Rising Deglitch	V_{PVCC} – V_{BAT} > $V_{PVCC-BAT_RISE}$	7	9	11	ms
	PVCC to BAT Falling Deglitch	V_{PVCC} – V_{BAT} < $V_{PVCC-BAT_FALL}$		6		µs
INPUT UNDERVOLTAGE LOCK-OUT COMPARATOR (UVLO)						
UVLO	AC Undervoltage rising threshold	Measure on PVCC	3.5	4	4.5	V
	AC Undervoltage hysteresis, falling			260		mV
BAT OVERVOLTAGE COMPARATOR						
V_O	Overvoltage rising threshold (2)	As percentage of V_{BAT_REG}		104%		
	Overvoltage falling threshold (2)			102%		
CHARGE OVERCURRENT COMPARATOR						
V_{OC}	Charge overcurrent rising threshold	As percentage of I_{REG_CHG}		145%		
	Minimum Current Limit (SRP-SRN)			50		mV
THERMAL SHUTDOWN COMPARATOR						
T_{SHUT}	Thermal shutdown rising temperature	Temperature Increasing		155		°C
T_{SHUT_HYS}	Thermal shutdown hysteresis, falling			20		
PWM HIGH SIDE DRIVER (HIDRV)						
$R_{DS(on)}$	High side driver turn-on resistance	V_{BTST} – V_{PH} = 5.5 V, tested at 100 mA		3	6	Ω
	High side driver turn-off resistance	V_{BTST} – V_{PH} = 5.5 V, tested at 100 mA		0.7	1.4	
$V_{BTST_REFRESH}$	Bootstrap refresh comparator threshold voltage	V_{BTST} – V_{PH} when low side refresh pulse is requested	4			V

(2) Specified by design.

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ELECTRICAL CHARACTERISTICS (continued)

7 V ≤ V_{PVCC} ≤ 24 V, 0°C < T_J < +125°C, typical values are at T_A = 25°C, with respect to AGND (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PWM LOW SIDE DRIVER (LODRV)						
$R_{DS(on)}$	Low side driver turn-on resistance	REGN = 6 V, tested at 100 mA		3	6	Ω
	Low side driver turn-off resistance	REGN = 6 V, tested at 100 mA		0.6	1.2	
PWM DRIVERS TIMING						
	Driver Dead Time — Dead time when switching between LODRV and HIDRV. No load at LODRV and HIDRV		30			ns
PWM OSCILLATOR						
F_{SW}	PWM switching frequency		240	300	360	kHz
V_{RAMP_HEIGHT}	PWM ramp height	As percentage of PVCC		6.6		%PVCC
QUIESCENT CURRENT						
I_{OFF_STATE}	Total off-state battery current from SRP, SRN, BAT, VCC, BTST, PH, etc.	V_{BAT} = 16.8 V, V_{ACDET} < 0.6 V, V_{PVCC} > 5 V, T_J = 85°C		7	10	µA
		V_{BAT} = 16.8 V, V_{ACDET} < 0.6 V, V_{PVCC} > 5 V, T_J = 125°C		7	11	
I_{AC}	Adapter quiescent current	V_{PVCC} = 20 V, charge disabled		1	1.5	mA
INTERNAL SOFT START (8 steps to regulation current)						
	Soft start steps			8		step
	Soft start step time			1.7		ms
CHARGER SECTION POWER-UP SEQUENCING						
	Charge-enable delay after power-up	Delay from when adapter is detected to when the charger is allowed to turn on	0.9	1.2	1.5	s
ISYNSET AMPLIFIER AND COMPARATOR (SYNCHRONOUS TO NON-SYNCHRONOUS TRANSITION)						
	I_{SYN} Accuracy	$V_{(SRP-SRN)}$ = 5 mV	–20%		20%	
$V_{ISYNSET}$	ISYNSET pin voltage			1		V
	ISYNSET rising deglitch			20		µs
	ISYNSET falling deglitch			640		µs
LOGIC IO PIN CHARACTERISTICS ($\overline{CHGEN}$)						
$V_{IN(LO)}$	Input low threshold voltage				0.8	V
$V_{IN(HI)}$	Input high threshold voltage		2.1			
I_{BIAS}	Input bias current	$V_{\overline{CHGEN}}$ = 0 to V_{REGN}			1	µA
LOGIC INPUT PIN CHARACTERISTICS (CELLS)						
$V_{IN(LO)}$	Input low threshold voltage, 3 cells	CELLS voltage falling edge			0.5	V
$V_{IN(MID)}$	Input mid threshold voltage, 2 cells	CELLS voltage rising for MIN, CELLS voltage falling for MAX	0.8		1.8	
$V_{IN(HI)}$	Input high threshold voltage, 4 cells	CELLS voltage rising	2.5			
I_{BIAS_FLOAT}	Input bias float current for 2-cell selection	V = 0 to V_{REGN}	–1		1	µA
OPEN-DRAIN LOGIC OUTPUT PIN CHARACTERISTICS ($\overline{DPMDET}$)						
$V_{O(LO)}$	Output low saturation voltage	Sink Current = 5 mA			0.5	V
	Delay, rising/falling		7	9	11	ms

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TYPICAL CHARACTERISTICS

Table of Graphs(1)

Y	X	Figure
VREF Load and Line Regulation	vs Load Current	Figure 3
REGN Load and Line Regulation	vs Load Current	Figure 4
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(1) Test results based on Figure 2 application schematic. V_{IN} = 20 V, V_{BAT} = 3-cell Li-Ion, I_{CHG} = 3 A, $I_{ADAPTER_LIMIT}$ = 4 A, T_A = 25°C, unless otherwise specified.

VREF LOAD AND LINE REGULATION vs Load Current

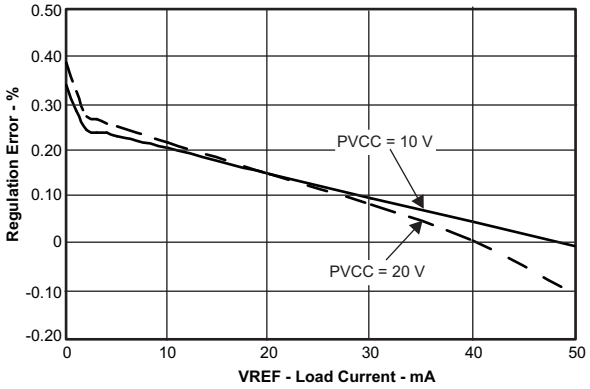

Figure 3.

REGN LOAD AND LINE REGULATION vs LOAD CURRENT

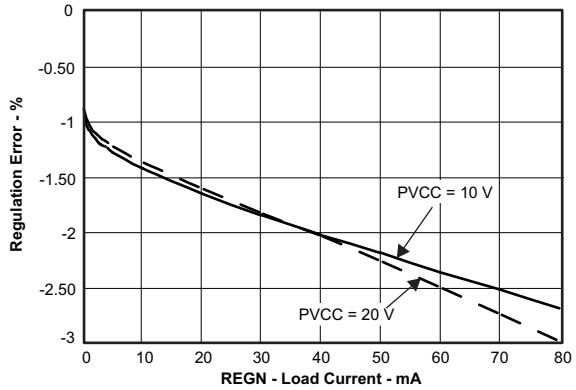

Figure 4.

BAT VOLTAGE vs VADJ/VREF RATIO

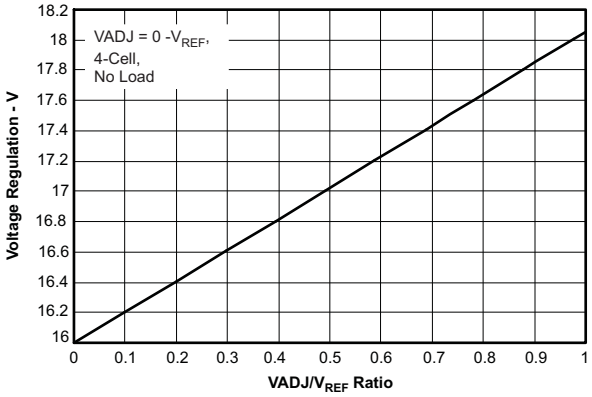

Figure 5.

CHARGE CURRENT vs SRSET/VREF RATIO

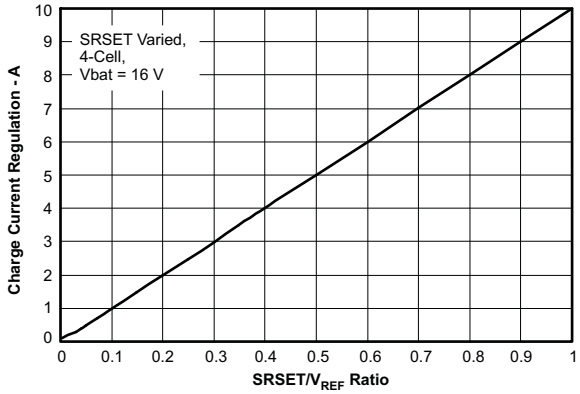

Figure 6.

INPUT CURRENT vs ACSET/VREF RATIO

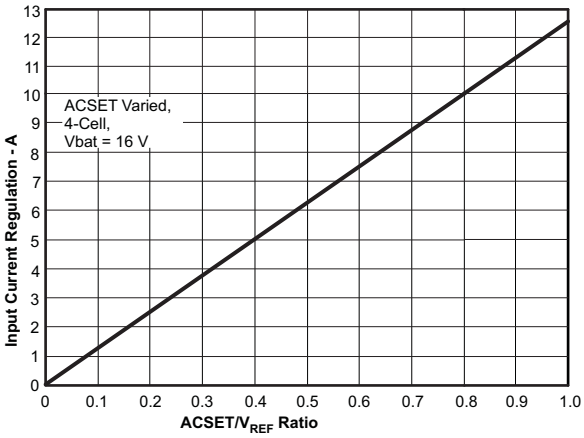

Figure 7.

BAT VOLTAGE REGULATION ACCURACY vs CHARGE CURRENT

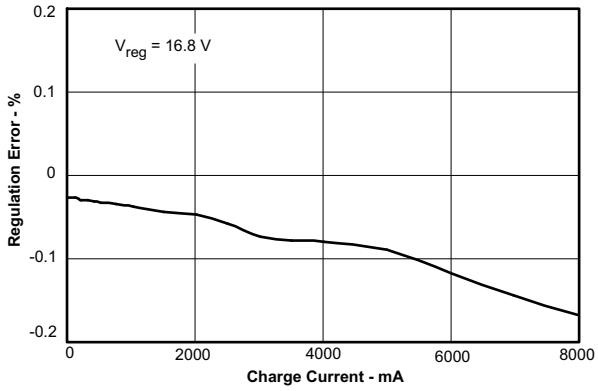

Figure 8.

BAT VOLTAGE REGULATION ACCURACY

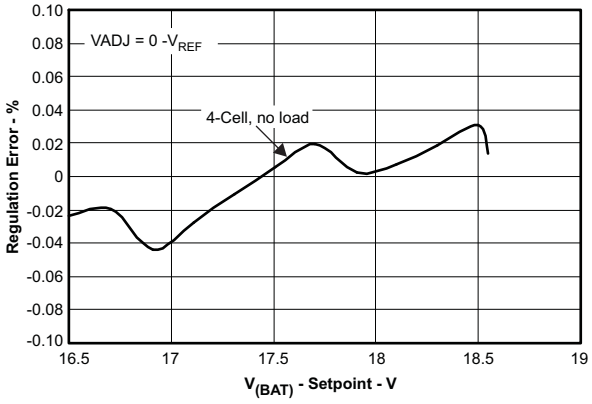

Figure 9.

CHARGE CURRENT REGULATION ACCURACY

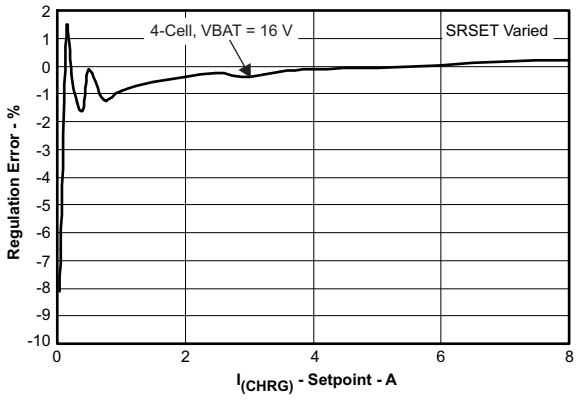

Figure 10.

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INPUT CURRENT REGULATION (DPM) ACCURACY

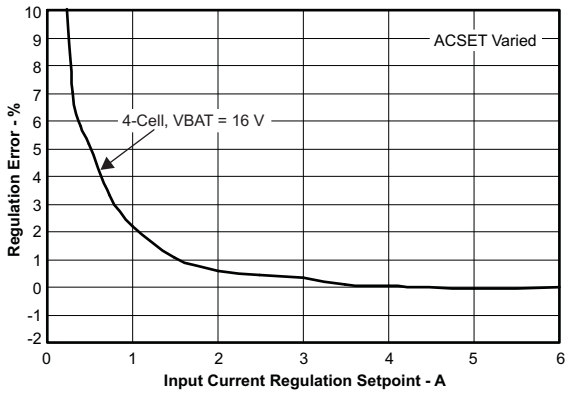

Figure 11.

V_{IADAPT} INPUT CURRENT SENSE AMPLIFIER ACCURACY

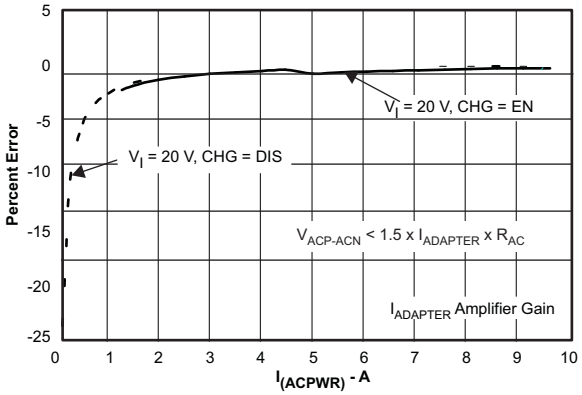

Figure 12.

INPUT REGULATION CURRENT (DPM), AND CHARGE CURRENT vs SYSTEM CURRENT

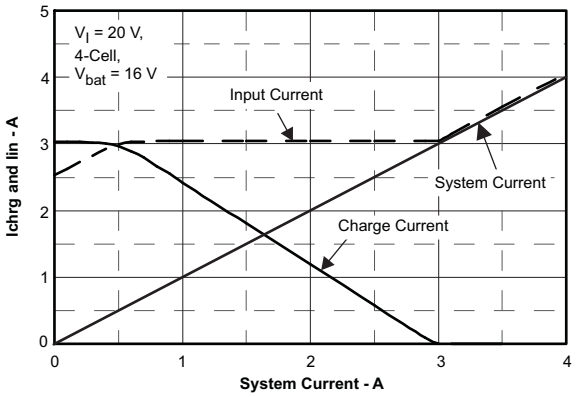

Figure 13.

TRANSIENT SYSTEM LOAD (DPM) RESPONSE

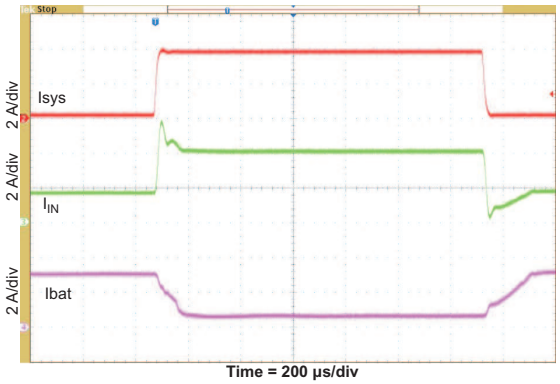

Figure 14.

CHARGE CURRENT REGULATION vs BAT VOLTAGE

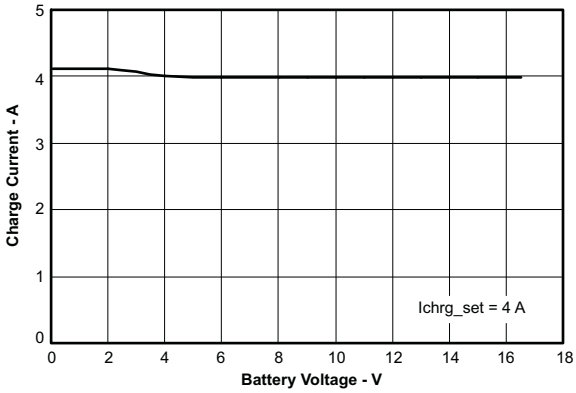

Figure 15.

EFFICIENCY vs BATTERY CHARGE CURRENT

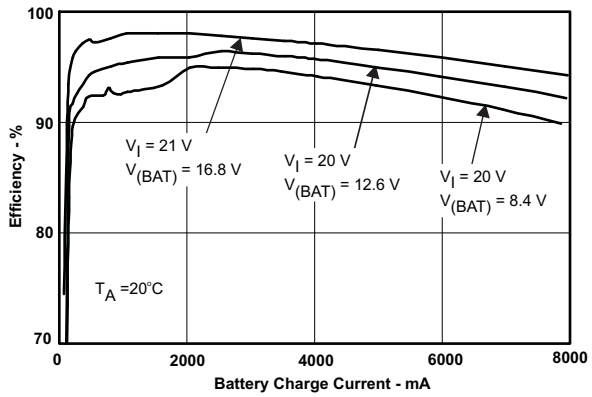

Figure 16.

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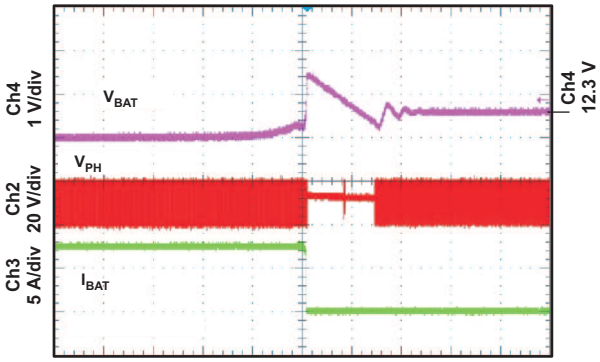
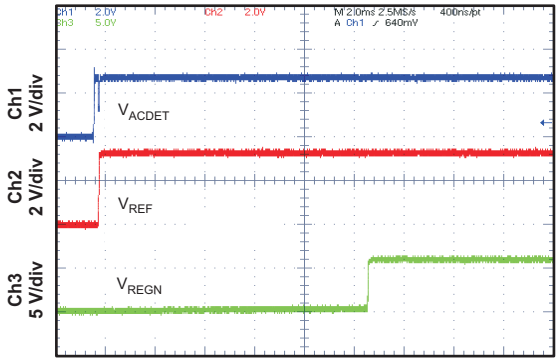
BATTERY REMOVAL



t − Time = 5 ms/div

Figure 17.

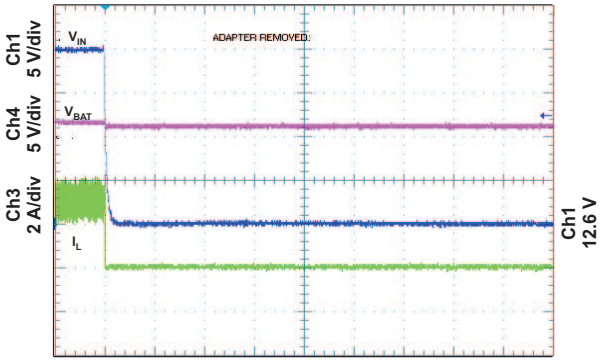
REF AND REGN STARTUP



t − Time = 2 ms/div

Figure 18.

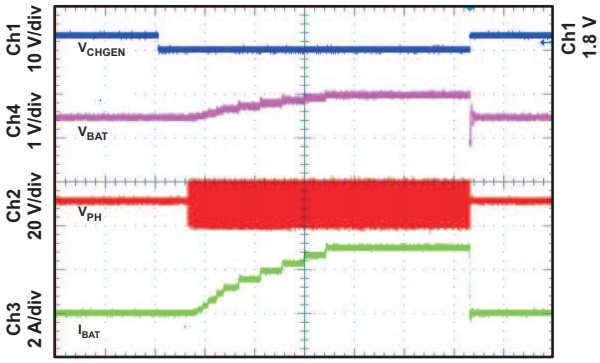
CHARGER ON ADAPTER REMOVAL



t − Time = 200 μs/div

Figure 19.

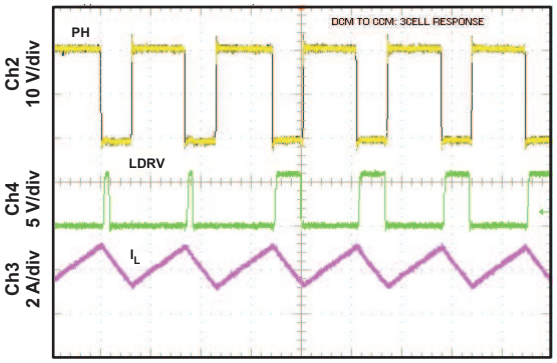
CHARGE ENABLE / DISABLE AND CURRENT SOFT-START



t − Time = 4 ms/div

Figure 20.

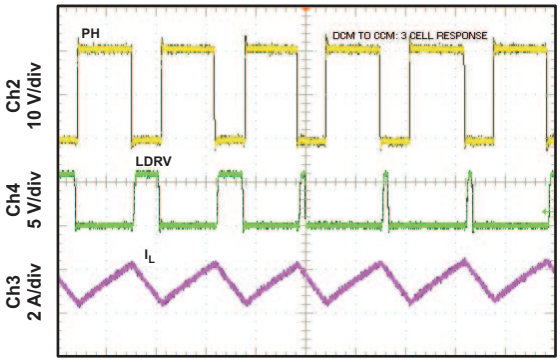
NONSYNCHRONOUS TO SYNCHRONOUS TRANSITION



t − Time = 1 μs/div

Figure 21.

SYNCHRONOUS TO NONSYNCHRONOUS TRANSITION



t − Time = 1 μs/div

Figure 22.

NEAR 100% DUTY CYCLE BOOTSTRAP RECHARGE PULSE

Figure 23.

BATTERY SHORTED CHARGER RESPONSE, OVERCURRENT PROTECTION (OCP) AND CHARGE CURRENT REGULATION

Figure 24.

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CONTINUOUS CONDUCTION MODE (CCM) SWITCHING WAVEFORMS

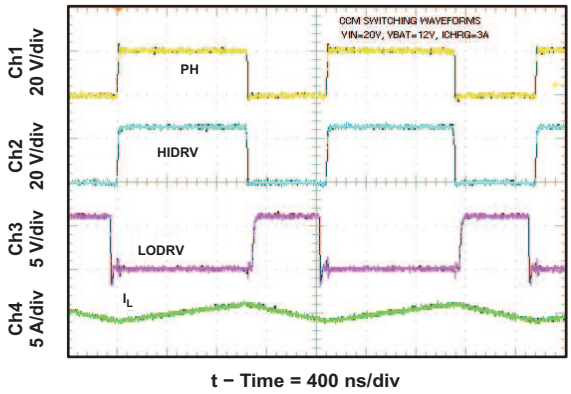


Figure 25.

DISCONTINUOUS CONDUCTION MODE (DCM) SWITCHING WAVEFORMS

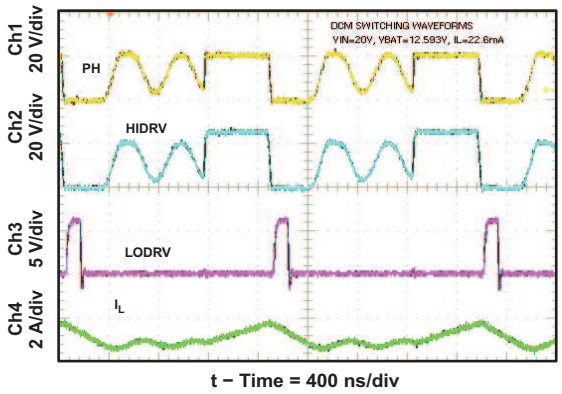


Figure 26.

$\overline{\text{DPMDET}}$ RESPONSE WITH TRANSIENT SYSTEM LOAD

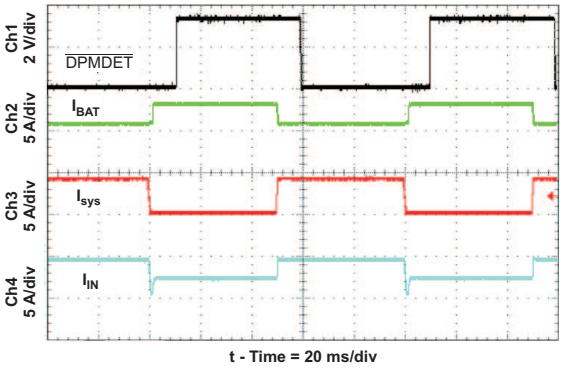
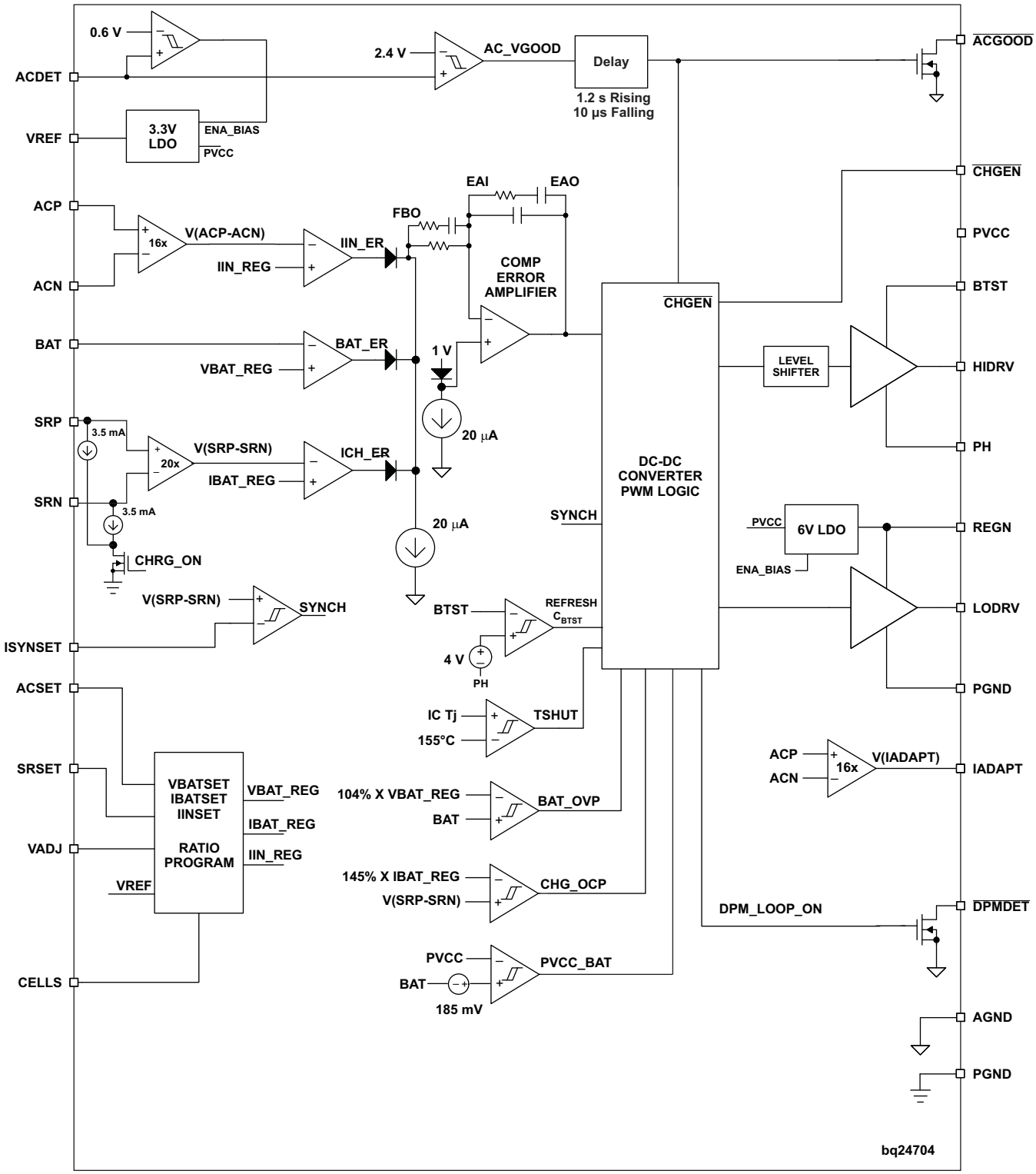


Figure 27.

FUNCTIONAL BLOCK DIAGRAM



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DETAILED DESCRIPTION

BATTERY VOLTAGE REGULATION

The bq24704 uses a high-accuracy voltage regulator for charging voltage. The internal default battery voltage setting V_{BATT}= 4.2 V × cell count. The regulation voltage is ratio-metric with respect to VREF. The ratio of VADJ and VREF provides extra 12.5% adjust range on V_{BATT} regulation voltage. By limiting the adjust range to 12.5% of the regulation voltage, the external resistor mismatch error is reduced from ±1% to ±0.1%. Therefore, an overall voltage accuracy as good as 0.5% is maintained, while using 1% mis-match resistors. Ratio-metric conversion also allows compatibility with D/As or microcontrollers (µC). The battery voltage is programmed through VADJ and VREF using Equation 1.

$$V_{BAT} = \text{cell count} \times \left[4V + \left(0.512 \times \frac{V_{VADJ}}{V_{REF}}\right)\right] \quad (1)$$

VADJ is set between 0 and VREF. V_{BATT} defaults to 4.2 V × cell count when VADJ is connected to REGN.

CELLS pin is the logic input for selecting cell count. Connect CELLS to charge 2,3, or 4 Li+ cells. When charging other cell chemistries, use CELLS to select an output voltage range for the charger.

CELLS	CELL COUNT
Float	2
AGND	3
VREF	4

The per-cell battery termination voltage is function of the battery chemistry. Consult the battery manufacturer to determine this voltage.

The BAT pin is used to sense the battery voltage for voltage regulation and should be connected as close to the battery as possible, or directly on the output capacitor. A 0.1-µF ceramic capacitor from BAT to AGND is recommended to be as close to the BAT pin as possible to decouple high frequency noise.

BATTERY CURRENT REGULATION

The SRSET input sets the maximum charging current. Battery current is sensed by resistor R_{SR} connected between SRP and SRN. The full-scale differential voltage between SRP and SRN is 100 mV. Thus, for a 0.010 Ω sense resistor, the maximum charging current is 10 A. SRSET is ratio-metric with respect to VREF using Equation 2:

$$I_{CHARGE} = \frac{V_{SRSET}}{V_{REF}} \times \frac{0.10}{R_{SR}} \quad (2)$$

The input voltage range of SRSET is between 0 and VREF, up to 3.3 V.

The SRP and SRN pins are used to sense across R_{SR} with default value of 10 mΩ. However, resistors of other values can also be used. A larger the sense resistor, gives a larger sense voltage, and a higher regulation accuracy, but at the expense of higher conduction loss.

INPUT ADAPTER CURRENT REGULATION

The total input from an AC adapter or other DC sources is a function of the system supply current and the battery charging current. System current normally fluctuates as portions of the systems are powered up or down. Without Dynamic Power Management (DPM), the source must be able to supply the maximum system current and the maximum charger input current simultaneously. By using DPM, the input current regulator reduces the charging current when the input current exceeds the input current limit set by ACSET. The current capability of the AC adapter can be lowered, which may reduce the system cost.

Similar to setting battery regulation current, adapter current is sensed by resistor R_{AC} connected between ACP and ACN. The maximum value is set by ACSET, which is a ratio-metric with respect to VREF, using Equation 3.

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$$I_{ADAPTER} = \frac{V_{ACSET}}{V_{REF}} \times \frac{0.125}{R_{AC}} \quad (3)$$

The input voltage range of ACSET is between 0 and VREF, up to 3.3 V.

The ACP and ACN pins are used to sense R_{AC} with default value of 10mΩ. However, resistors of other values can also be used. A larger the sense resistor, gives a larger sense voltage, and a higher regulation accuracy; but, at the expense of higher conduction loss.

ADAPTER DETECT AND POWER UP

An external resistor voltage divider attenuates the adapter voltage before it goes to ACDET. The adapter detect threshold should typically be programmed to a value greater than the maximum battery voltage, and lower than the minimum allowed adapter voltage. The ACDET divider should be placed before the ACFET in order to sense the true adapter input voltage whether the ACFET is on or off.

If PVCC is below 4 V, the device is disabled.

If ACDET is below 0.6 V but PVCC is above 4 V, part of the bias is enabled, including a crude bandgap reference. IADAPT is disabled and pulled down to GND. The total quiescent current is less than 10 μA.

Once ACDET rises above 0.6 V and PVCC is above 4 V, all the bias circuits are enabled. VREF goes to 3.3 V and REGN output goes to 6 V. IADAPT becomes valid to proportionally reflect the adapter current.

When ACDET rises and passes 2.4 V, a valid AC adapter is present. Then the following occurs:

- $\overline{\text{ACGOOD}}$ becomes high through external pull-up resistor to the host digital voltage rail;
- Charger turns on if all the conditions are satisfied (see *Enable and Disable Charging*).

ENABLE AND DISABLE CHARGING

The following conditions must be valid before a charge is enabled:

- $\overline{\text{CHGEN}}$ is LOW;
- PVCC > UVLO;
- Adapter is detected;
- Adapter is higher than PVCC-BAT threshold;
- Adapter is not over voltage;
- 1.2 s delay is complete after adapter detected;
- REGNGOOD and VREFGOOD are valid;
- Thermal Shut (TSHUT) is not valid;

One of the following conditions will stop on-going charging:

- $\overline{\text{CHGEN}}$ is HIGH;
- PVCC < UVLO;
- Adapter is removed;
- Adapter is less than PVCC-BAT threshold;
- Adapter is over voltage;
- Adapter is over current;
- TSHUT IC temperature threshold is reached (155°C on rising-edge with 20°C hysteresis).

AUTOMATIC INTERNAL SOFT-START CHARGER CURRENT

The charger automatically soft-starts the charger regulation current every time the charger is enabled to ensure there is no overshoot or stress on the output capacitors or the power converter. The soft-start consists of stepping-up the charge regulation current into 8 evenly divided steps up to the programmed charge current. Each step lasts around 1.7ms, for a typical rise time of 13.6ms. No external components are needed for this function.

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CONVERTER OPERATION

The synchronous buck PWM converter uses a fixed frequency (300 kHz) voltage mode with feed-forward control scheme. A type III compensation network allows using ceramic capacitors at the output of the converter. The compensation input stage is connected internally between the feedback output (FBO) and the error amplifier input (EAI). The feedback compensation stage is connected between the error amplifier input (EAI) and error amplifier output (EAO). The LC output filter is selected to give a resonant frequency of 8–12.5 kHz nominal.

Where resonant frequency, f_o, is given by: $f_O = \frac{1}{2\pi\sqrt{L_O C_O}}$ where (from Figure 1 schematic)

- C_O = C11 + C12
- L_O = L1

An internal saw-tooth ramp is compared to the internal EAO error control signal to vary the duty-cycle of the converter. The ramp height is one-fifteenth of the input adapter voltage making it always directly proportional to the input adapter voltage. This cancels out any loop gain variation due to a change in input voltage, and simplifies the loop compensation. The ramp is offset by 200 mV in order to allow zero percent duty-cycle, when the EAO signal is below the ramp. The EAO signal is also allowed to exceed the saw-tooth ramp signal in order to get a 100% duty-cycle PWM request. Internal gate drive logic allows achieving 99.98% duty-cycle while ensuring the N-channel upper device always has enough voltage to stay fully on. If the BTST pin to PH pin voltage falls below 4 V for more than 3 cycles, then the high-side n-channel power MOSFET is turned off and the low-side n-channel power MOSFET is turned on to pull the PH node down and recharge the BTST capacitor. Then the high-side driver returns to 100% duty-cycle operation until the (BTST-PH) voltage is detected to fall low again due to leakage current discharging the BTST capacitor below the 4 V, and the reset pulse is reissued.

The 300 kHz fixed frequency oscillator keeps tight control of the switching frequency under all conditions of input voltage, battery voltage, charge current, and temperature, simplifying output filter design and keeping it out of the audible noise region. The charge current sense resistor R_{SR} should be placed with at least half or more of the total output capacitance placed before the sense resistor contacting both sense resistor and the output inductor; and the other half or remaining capacitance placed after the sense resistor. The output capacitance should be divided and placed onto both sides of the charge current sense resistor. A ratio of 50:50 percent gives the best performance; but the node in which the output inductor and sense resistor connect should have a minimum of 50% of the total capacitance. This capacitance provides sufficient filtering to remove the switching noise and give better current sense accuracy. The type III compensation provides phase boost near the cross-over frequency, giving sufficient phase margin.

SYNCHRONOUS AND NON-SYNCHRONOUS OPERATION

The charger operates in non-synchronous mode when the sensed charge current is below the ISYNSET value. Otherwise, the charger operates in synchronous mode.

During synchronous mode, the low-side n-channel power MOSFET is on, when the high-side n-channel power MOSFET is off. The internal gate drive logic ensures there is break-before-make switching to prevent shoot-through currents. During the 30ns dead time where both FETs are off, the back-diode of the low-side power MOSFET conducts the inductor current. Having the low-side FET turn-on keeps the power dissipation low, and allows safely charging at high currents. During synchronous mode the inductor current is always flowing and operates in Continuous Conduction Mode (CCM), creating a fixed two-pole system.

During non-synchronous operation, after the high-side n-channel power MOSFET turns off, and after the break-before-make dead-time, the low-side n-channel power MOSFET will turn-on for around 80ns, then the low-side power MOSFET will turn-off and stay off until the beginning of the next cycle, where the high-side power MOSFET is turned on again. The 80ns low-side MOSFET on-time is required to ensure the bootstrap capacitor is always recharged and able to keep the high-side power MOSFET on during the next cycle. This is important for battery chargers, where unlike regular dc-dc converters, there is a battery load that maintains a voltage and can both source and sink current. The 80-ns low-side pulse pulls the PH node (connection between high and low-side MOSFET) down, allowing the bootstrap capacitor to recharge up to the REGN LDO value. After the 80 ns, the low-side MOSFET is kept off to prevent negative inductor current from occurring. The inductor current is blocked by the off low-side MOSFET, and the inductor current will become discontinuous. This mode is called Discontinuous Conduction Mode (DCM).

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During the DCM mode the loop response automatically changes and has a single pole system at which the pole is proportional to the load current, because the converter does not sink current, and only the load provides a current sink. This means at low currents the loop response is slower, as there is less sinking current available to discharge the output voltage. At low currents during non-synchronous operation, there may be a small amount of negative inductor current during the 80 ns recharge pulse. The charge should be low enough to be absorbed by the input capacitance.

When BTST – PH < 4 V, the 80-ns recharge pulse occurs on LODRV, the high-side MOSFET does not turn on. The low-side MOSFET does not turn on (only 80-ns recharge pulse).

ISYNSET CONTROL (SYN AND NON-SYN MODE SETTING)

The ISYNSET pin is used to program the charge current threshold at which the charger changes from synchronous operation into non-synchronous operation. The low side driver turns on for only 80 ns to charge the boost capacitor. This is important to prevent negative inductor current, which may cause a boost effect in which the input voltage increases as power is transferred from the battery to the input capacitors. This boost effect can lead to an overvoltage on the PVCC node, and potentially cause some damage to the system. This programmable value allows setting the current threshold for any inductor current ripple, and avoiding negative inductor current. The minimum synchronous threshold should be set from 1/2 of the inductor current ripple to the full ripple current, where the inductor current ripple is given by:

$$\frac{I_{RIPPLE_MAX}}{2} \leq I_{SYN} \leq I_{RIPPLE_MAX}$$

and

$$I_{RIPPLE} = \frac{(V_{IN} - V_{BAT}) \times \frac{V_{BAT}}{V_{IN}} \times \frac{1}{f_S}}{L} = \frac{V_{IN} \times (1 - D) \times D \times \frac{1}{f_S}}{L} \quad (4)$$

where:

V_{IN} = adapter voltage
V_{BAT} = BAT voltage
f_S = switching frequency
L = output inductor
D = duty-cycle

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I_{RIPPLE_MAX} happens when the duty-cycle, D is mostly near to 0.5 at given V_{in}, f_s,and L.

The ISYNSET comparator, or charge undercurrent comparator, compares the voltage between SRP-SRN, and the threshold set by an external resistor $R_{ISYNSET}$, which can be calculated by:

$$R_{ISYNSET} = \frac{250\ V}{I_{SYN} \times R_{SENSE}}\ \Omega \tag{5}$$

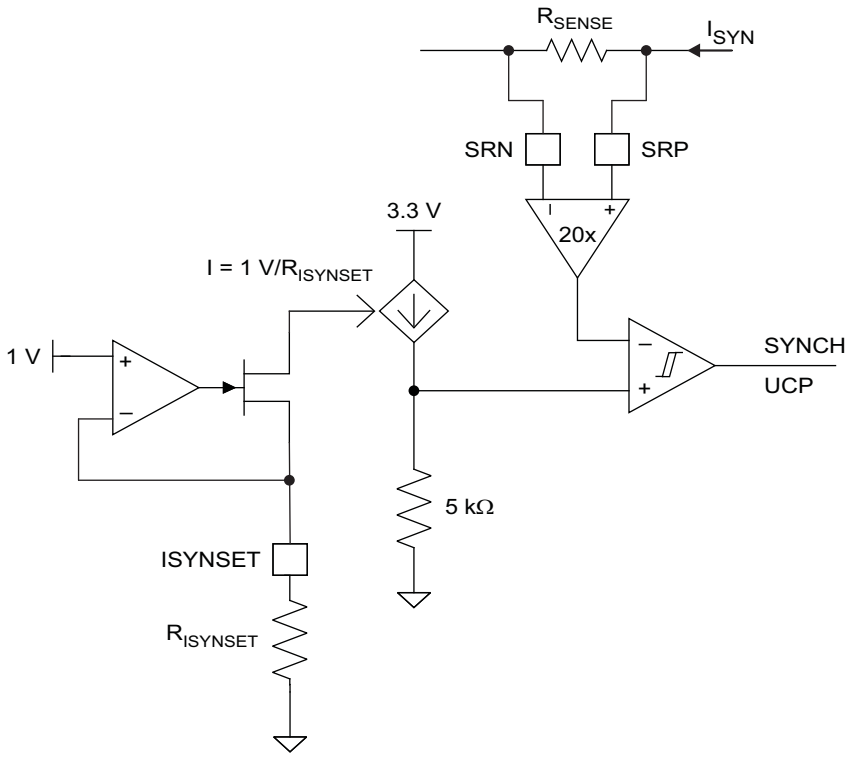

Figure 28. ISYNSET Comparator Block

HIGH ACCURACY IADAPT USING CURRENT SENSE AMPLIFIER (CSA)

An industry standard, high accuracy current sense amplifier (CSA) is used to monitor the input current by the host or some discrete logic through the analog voltage output of the IADAPT pin. The CSA amplifies the input sensed voltage of ACP – ACN by 16x through the IADAPT pin. The IADAPT output is a voltage source 16 times the input differential voltage. Once PVCC is above 5 V and ACDET is above 0.6V, IADAPT no longer stays at ground, but becomes active. If the user wants to lower the voltage, they could use a resistor divider from IOUT to AGND, and still achieve accuracy over temperature as the resistors can be matched their thermal coefficients.

A 100-pF capacitor connected on the output is recommended for decoupling high-frequency noise. An additional RC filter is optional, after the 100-pF capacitor, if additional filtering is desired. Note that adding filtering also adds additional response delay.

INPUT UNDERVOLTAGE LOCK OUT (UVLO)

The system must have a minimum 4 V PVCC voltage to allow proper operation. This PVCC voltage could come from either input adapter or battery, using a diode-OR input. When the PVCC voltage is below 4 V the bias circuits REGN and VREF stay inactive, even with ACDET above 0.6 V.

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BATTERY OVERVOLTAGE PROTECTION

The converter stops switching when BAT voltage goes above 104% of the regulation voltage. The converter will not allow the high-side FET to turn on until the BAT voltage goes below 102% of the regulation voltage. This allows one-cycle response to an overvoltage condition, such as when the load is removed or the battery is disconnected. A 10-mA current sink from BAT to PGND is on only during charge, and allows discharging the stored output-inductor energy into the output capacitors.

CHARGE OVERCURRENT PROTECTION

The charger has a secondary overcurrent protection. It monitors the charge current, and prevents the current from exceeding 145% of regulated charge current. The high-side gate drive turns off when the overcurrent is detected, and automatically resumes when the current falls below the overcurrent threshold.

THERMAL SHUTDOWN PROTECTION

The QFN package has low thermal impedance, which provides good thermal conduction from the silicon to the ambient, to keep junctions temperatures low. As added level of protection, the charger converter turns off and self-protects whenever the junction temperature exceeds the TSHUT threshold of 155°C. The charger stays off until the junction temperature falls below 135°C.

Status Outputs ($\overline{\text{ACGOOD}}$, $\overline{\text{DPMDET}}$)

Two status outputs are available, and they require external pull up resistors to pull the pins to system digital rail for a high level.

$\overline{\text{ACGOOD}}$ open-drain output goes low if ACDET is above 2.4 V.

$\overline{\text{DPMDET}}$ open-drain output goes low when the DPM loop is active to reduce the battery charge current (after a 10-ms delay).

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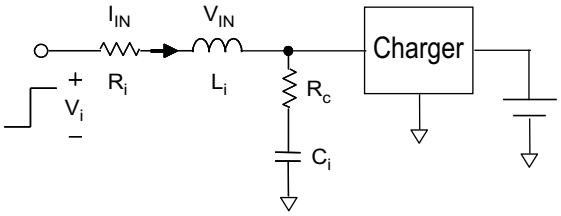
Table 2. Component List for Typical System Circuit of Figure 1

PART DESIGNATOR	QTY	DESCRIPTION
Q1, Q2, Q3	3	P-channel MOSFET, –30V,-6A, SO-8, Vishay-Siliconix, Si4435
Q4, Q5	2	N-channel MOSFET, 30V, 12.5A, SO-8, Fairchild, FDS6680A
D1, D2	2	Diode, Dual Schottky, 30V, 200mA, SOT23, Fairchild, BAT54C
R_{AC}, R_{SR}	2	Sense Resistor, 10 mΩ, 1%, 1W, 2010, Vishay-Dale, WSL2010R0100F
L1	1	Inductor, 8.2µH, Vishay-Dale, IHLP5050CE-01
C6, C7, C11, C12	4	Capacitor, Ceramic, 10µF, 25V, 20%, X5R, 1206, Panasonic, ECJ-3YB1E106M
C4, C10	2	Capacitor, Ceramic, 1µF, 25V, 10%, X7R, 2012, TDK, C2012X7R1E105K
C2, C3, C8, C9, C13, C14, C15	7	Capacitor, Ceramic, 0.1µF, 50V, 10%, X7R, 0805, Kemet, C0805C104K5RACTU
C5	1	Capacitor, Ceramic, 100pF, 25V, 10%, X7R, 0805, Kemet, C0805C101K5RACTU
C1	1	Capacitor, Ceramic, 2.2µF, 25V, 10%, X7R, 2012, TDK, C2012X7R1E225K
R3, R4, R15	3	Resistor, Chip, 10 kΩ, 1/16W, 5%, 0402
R1	1	Resistor, Chip, 432 kΩ, 1/16W, 1%, 0402
R2	1	Resistor, Chip, 66.5 kΩ, 1/16W, 1%, 0402
R10	1	Resistor, Chip, 2 Ω, 1W, 1%, 1210
R6	1	Resistor, Chip, 20 kΩ, 1/16W, 1%, 0402

APPLICATION INFORMATION

Input Capacitance Calculation

During the adapter hot plug-in, the ACFET has not been turned on. The AC switch is off and the simplified equivalent circuit of the input is shown in Figure 29.



A. R_i: Equivalent resistance of cable
B. L_i: Equivalent inductance of cable
C. R_C ESR of C_i
D. C_i: Decoupling capacitor

Figure 29. Simplified Equivalent Circuit During Adapter Insertion

The voltage on the input capacitor(s) is given by:

$$V_{IN}(t) = I_{IN}(t) \times R_C + V_{Ci}(t) = V_i - V_I e^{\frac{R_t}{2L_i}t}\left[\frac{R_i - R_C}{\omega L_i}\sin\omega t + \cos\omega t\right]$$

$$V_{Ci}(t) = V_i - V_I e^{\frac{R_t}{2L_i}t}\left[\frac{R_t}{2\omega L_i}\sin\omega t + \cos\omega t\right]$$

$$R_t = R_i + R_C \quad \omega = \sqrt{\frac{I}{L_i C_i} - \left(\frac{R_t}{2L_i}\right)^2} \qquad I_{In}(t) = \frac{V_i}{\omega L_i} e^{\frac{R_t}{2L_i}t}\sin\omega t \tag{6}$$

Damping Conditions:

$$R_t = R_i + R_C > 2\sqrt{\frac{L_i}{C_i}} \tag{7}$$

Figure 30(a) demonstrates a highr C_i which helps dampen the voltage spike. Figure 30(b) demonstrates the effect of the input stray inductance (L_i) on the input voltage spike. The dashed curve in Figure 30(b) represents the worst case for C_i = 40 µF. Figure 30(c) shows how the resistance helps to suppress the input voltage spike.

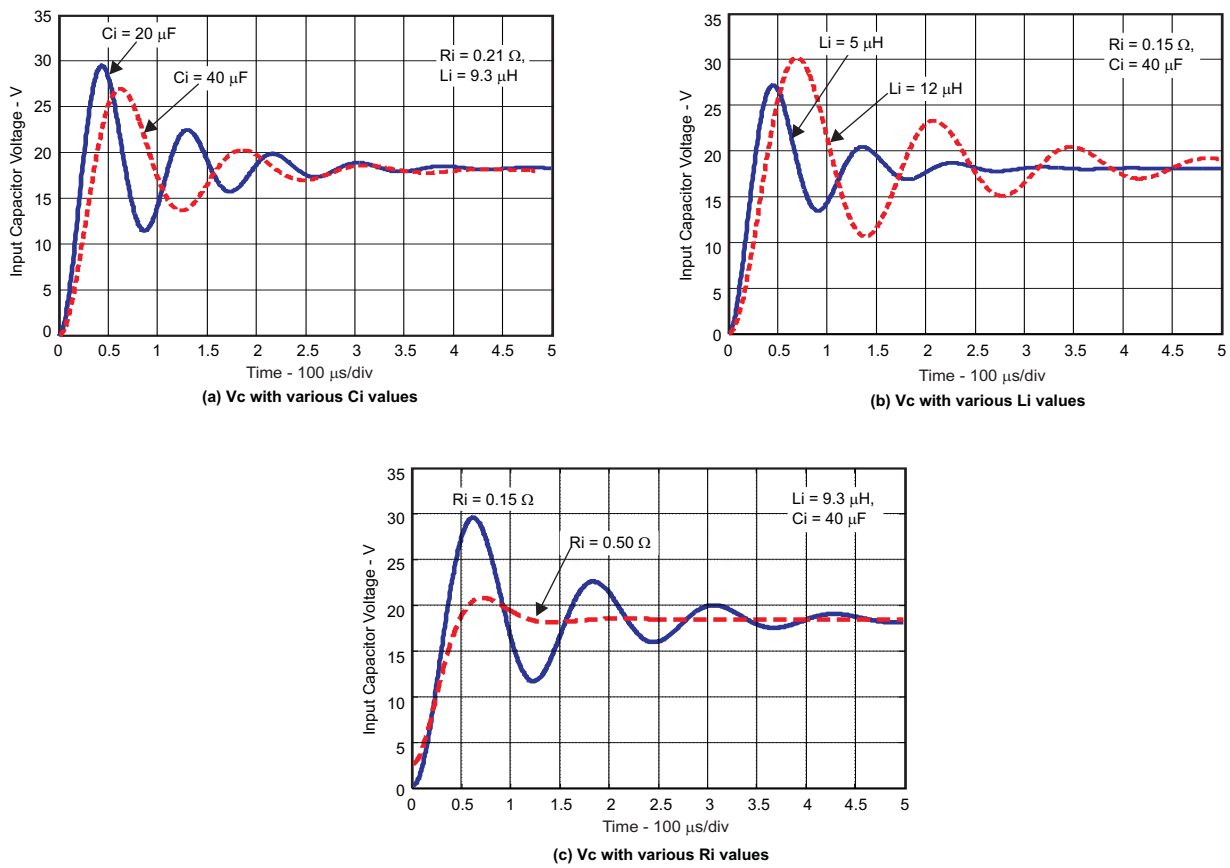


Figure 30. Parametric Study Of The Input Voltage

As shown in Figure 30, minimizing the input stray inductance, increasing the input capacitance, and adding resistance (including using higher ESR capacitors) helps supress the input voltage spike. However, a user often cannot control input srtay inductance, and increasing capacitance can increase costs. therefore, the most efficient and cost-effective approach is to add an external resistor.

Figure 31 depicts the recommended input filter design. The measured input voltage and current waveforms are shown in Figure 32. The input voltage spike has been well damped by adding a 2 Ω resistor, while keeping the capacitance low.

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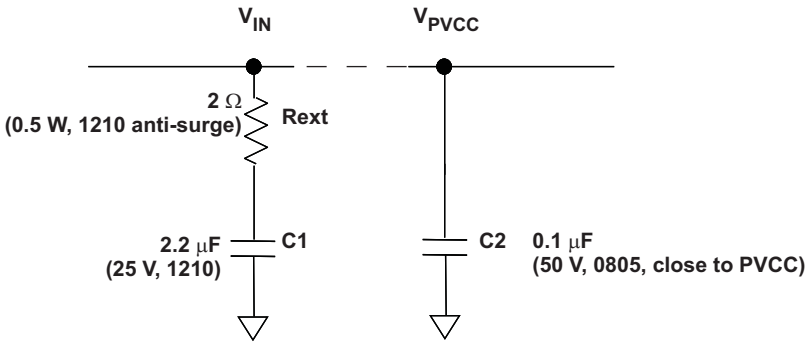


Figure 31. Recommended Input Filter Design

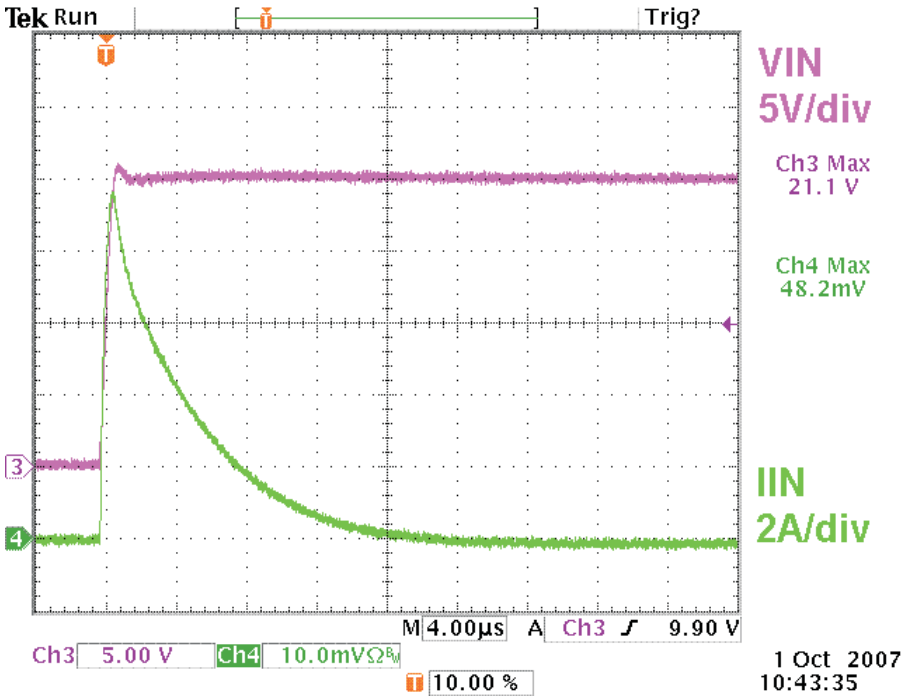
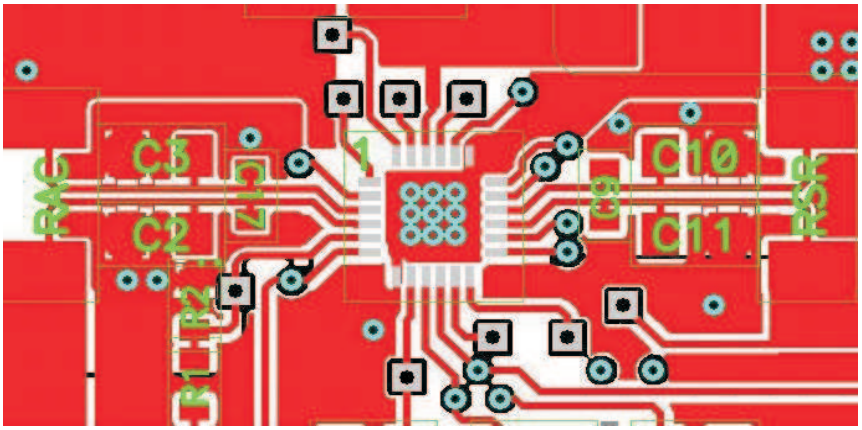


Figure 32. Adapter DC Side Hot Plug-In Test Waveforms

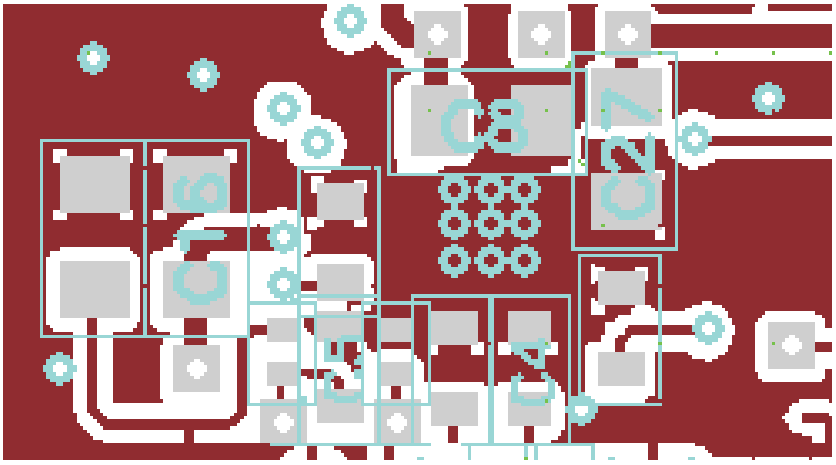
PCB Layout Design Guideline

1. It is critical that the exposed power pad on the backside of the IC package be soldered to the PCB ground. Ensure that there are sufficient thermal vias directly under the IC, connecting to the ground plane on the other layers.
2. The control stage and the power stage should be routed separately. At each layer, the signal ground and the power ground are connected only at the power pad.
3. The AC current-sense resistor must be connected to ACP (pin 4) and ACN (pin 3) with a Kelvin contact. The area of this loop must be minimized. An additional 0.1 µF decoupling capacitor for ACN is required to further reduce the noise. The decoupling capacitors for these pins should be placed as close to the IC as possible.
4. The charge-current sense resistor must be connected to SRP (pin 16), SRN (pin 15) with a Kelvin contact. The area of this loop must be minimized. An additional 0.1µF decoupling capacitor for SRN is required to further reduce the noise. The decoupling capacitors for these pins should be placed as close to the IC as possible.
5. Decoupling capacitors for PVCC (pin 1), VREF (pin 8), REGN (pin 21) should be placed underneath the IC (on the bottom layer) with the interconnections to the IC as short as possible.
6. Decoupling capacitors for BAT (pin 14), IADAPT (pin 12) must be placed close to the corresponding IC pins with the interconnections to the IC as short as possible.
7. Decoupling capacitor CX for the charger input must be placed close to the Q4 drain and Q5 source.

Figure 33 shows the recommended component placement with trace and via locations. For the QFN information, see the SCBA017 and SLUA271 documents.



(a) Top Layer



(b) Bottom Layer

Figure 33. Layout Example

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PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
BQ24704RGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24704RGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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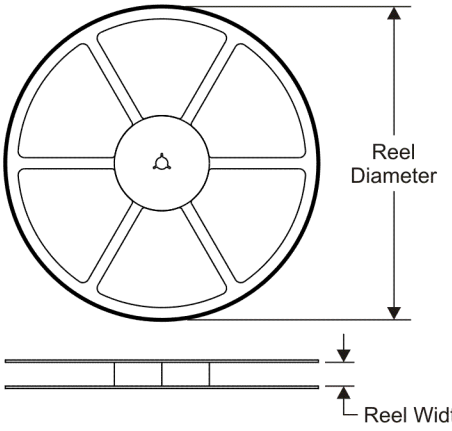
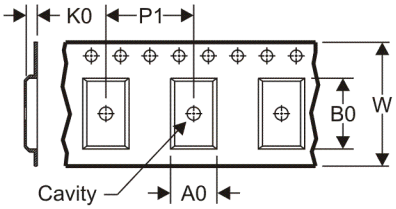
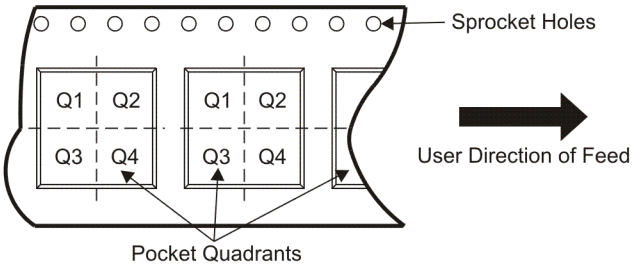


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

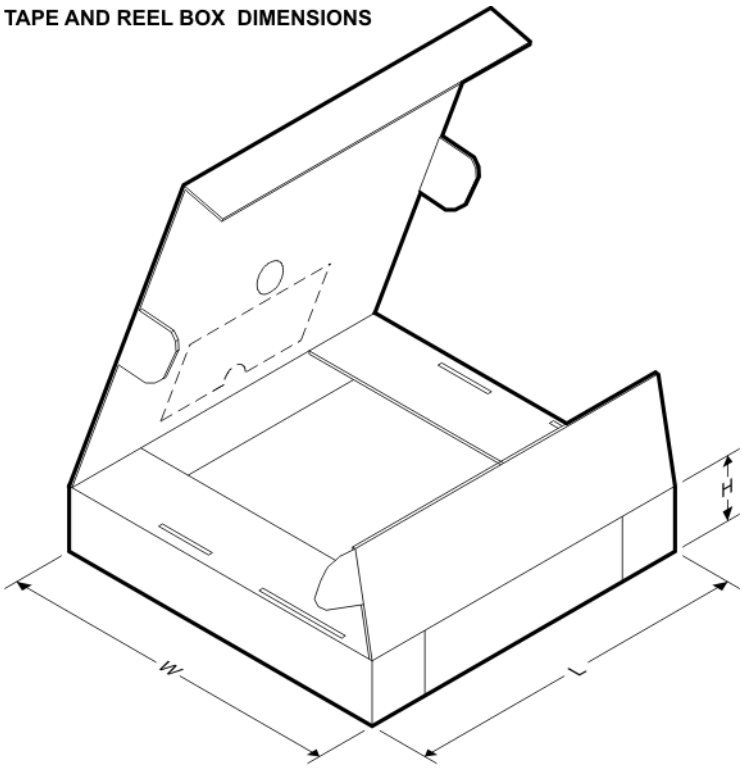
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24704RGER	VQFN	RGE	24	3000	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2

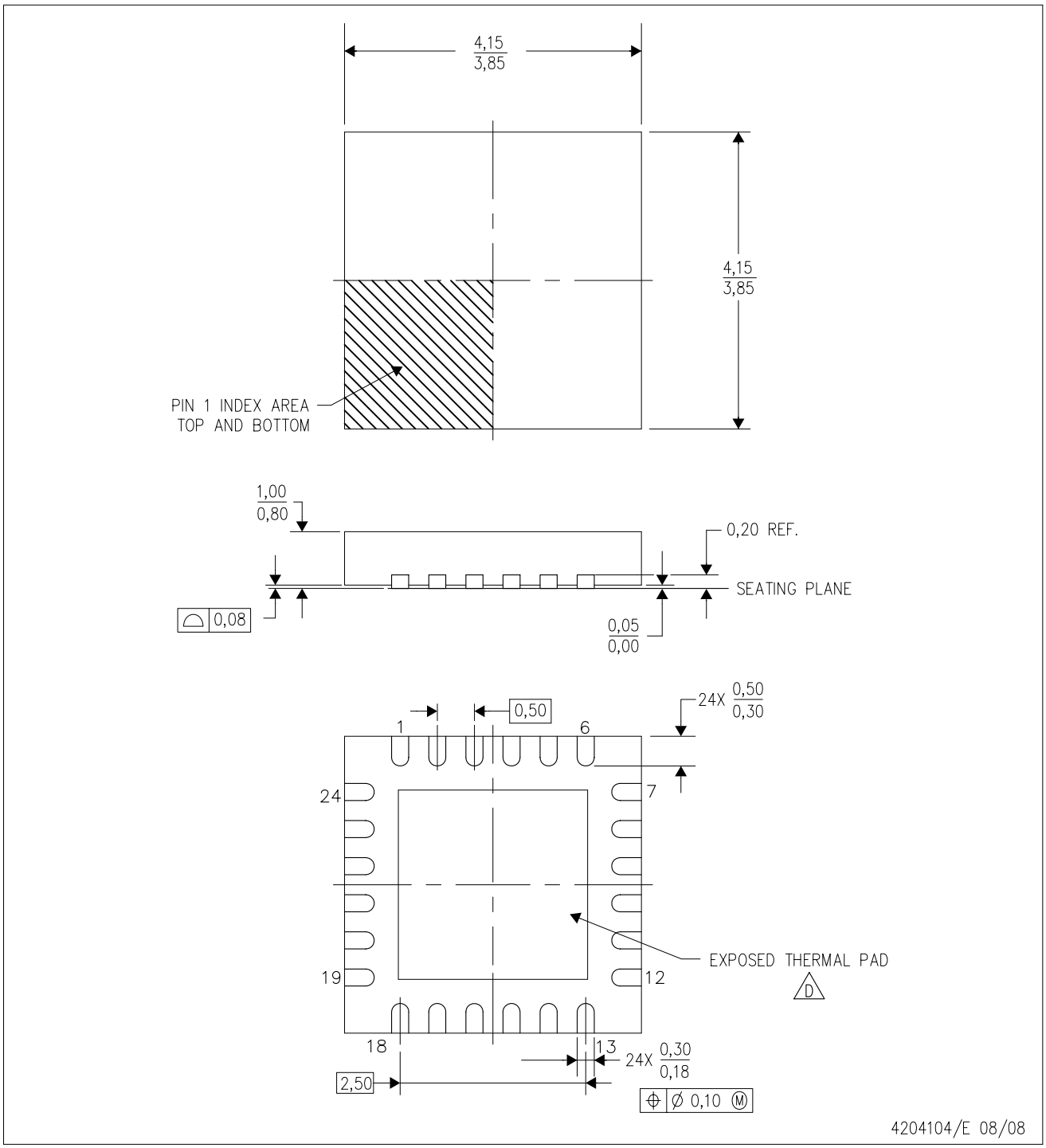
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24704RGER	VQFN	RGE	24	3000	346.0	346.0	29.0

RGE (S-PVQFN-N24) PLASTIC QUAD FLATPACK NO-LEAD



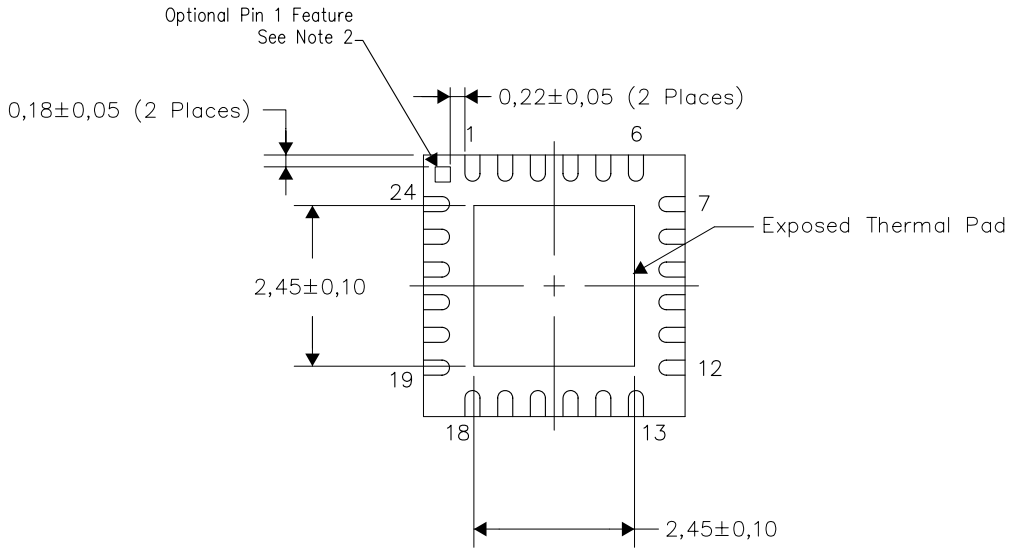
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No-Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO-220.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



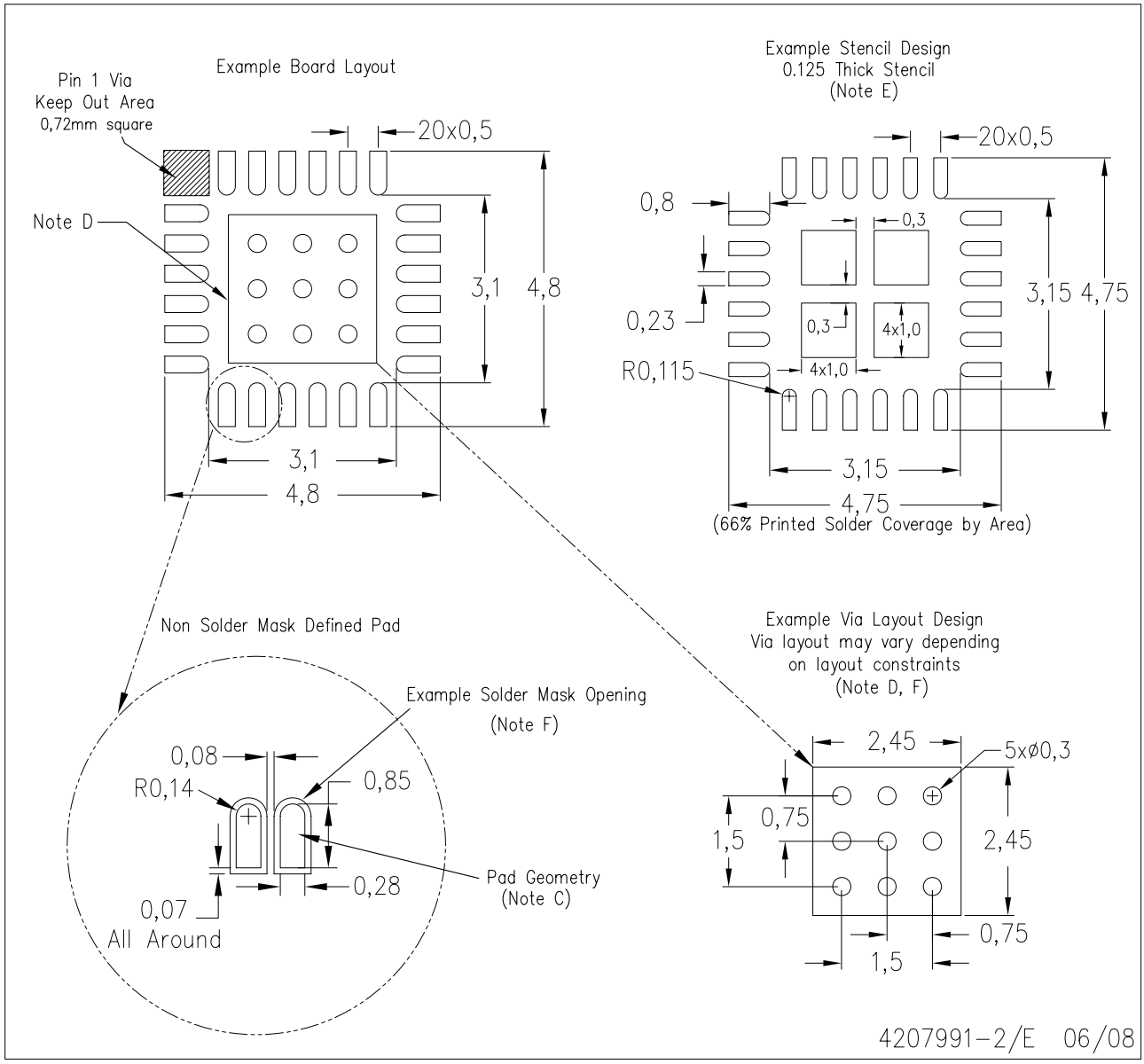
Bottom View

Exposed Thermal Pad Dimensions

NOTES:

1) All linear dimensions are in millimeters
2) The Pin 1 Identification mark is an optional feature that may be present on some devices In addition, this Pin 1 feature if present is electrically connected to the center thermal pad and therefore should be considered when routing the board layout.

RGE (S–PVQFN–N24)



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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