

Features

- Fast Access Time: 30/35/40/45ns
- Fast EDO Page Cycle Time: 13.3/15/16/18ns
- EDO Page Mode Operation
- Single +5V \pm 10% Power Supply
- Low Power Dissipation
- Individual Byte Control via Dual CAS Inputs
- Three Refresh Modes
- 512-Cycle Refresh in 8ms(9 rows and 9 columns)
- TTL Compatible
- 40-Pin, 400-mil Plastic SOJ Package, or 40/44-Pin, 400-mil Plastic TSOP-II Package.

Ordering Information

Part Number	Speed	Package
Em614163A-30	30ns	SOJ
EM614163TS-30	30ns	TSOP-II
Em614163A-35	35ns	SOJ
EM614163TS-35	35ns	TSOP-II
Em614163A-40	40ns	SOJ
EM614163TS-40	40ns	TSOP-II
Em614163A-45	45ns	SOJ
EM614163TS-45	45ns	TSOP-II

Key Specifications

Speed	t _{rac}	t _{cac}	t _{aa}	t _{oEA}	t _{rc}	t _{pc}
-30	30ns	9ns	16ns	9ns	53ns	13.3ns
-35	35ns	10ns	18ns	9ns	60ns	15ns
-40	40ns	11ns	20ns	10ns	66ns	16ns
-45	45ns	12ns	22ns	10ns	75ns	18ns

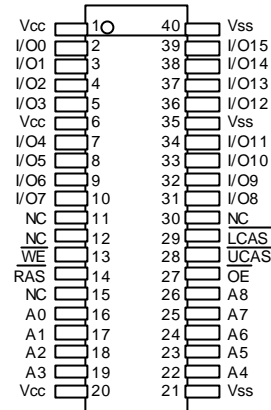
Overview

The Em614163A-30/35/40/45 is a high speed EDO(Extended Data Output) DRAM organized in 262,144 words by 16 bits. It supports EDO Page Mode and 16-bit data width for high data bandwidth applications. The EDO Page Mode is an accelerated access that provides a shorter page cycle and a faster data access time than the traditional Fast Page Mode.

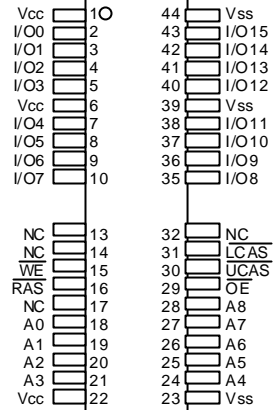
Compared with Fast Page Mode DRAM, the EDO DRAM data output will be held valid after $\overline{\text{CAS}}$ goes HIGH, as long as RAS and $\overline{\text{OE}}$ are held LOW and $\overline{\text{WE}}$ is held HIGH. This feature allows $\overline{\text{CAS}}$

Pin Assignment (Top View)

40-Pin SOJ



40/44-Pin TSOP-II



Pin Names

A0 - A8	Address Inputs
RAS	Row Address Strobe
UCAS	Column Address Strobe (Upper Byte Control)
LCAS	Column Address Strobe (Lower Byte Control)
WE	Write Enable
OE	Output Enable
I/O0 - I/O15	Data Input/Output
Vcc	+5V Power Supply
Vss	Ground
NC	No Connection

precharge time to occur without the output data going invalid. Therefore, the EDO CAS timing can be condensed to carry more data out in a given period.

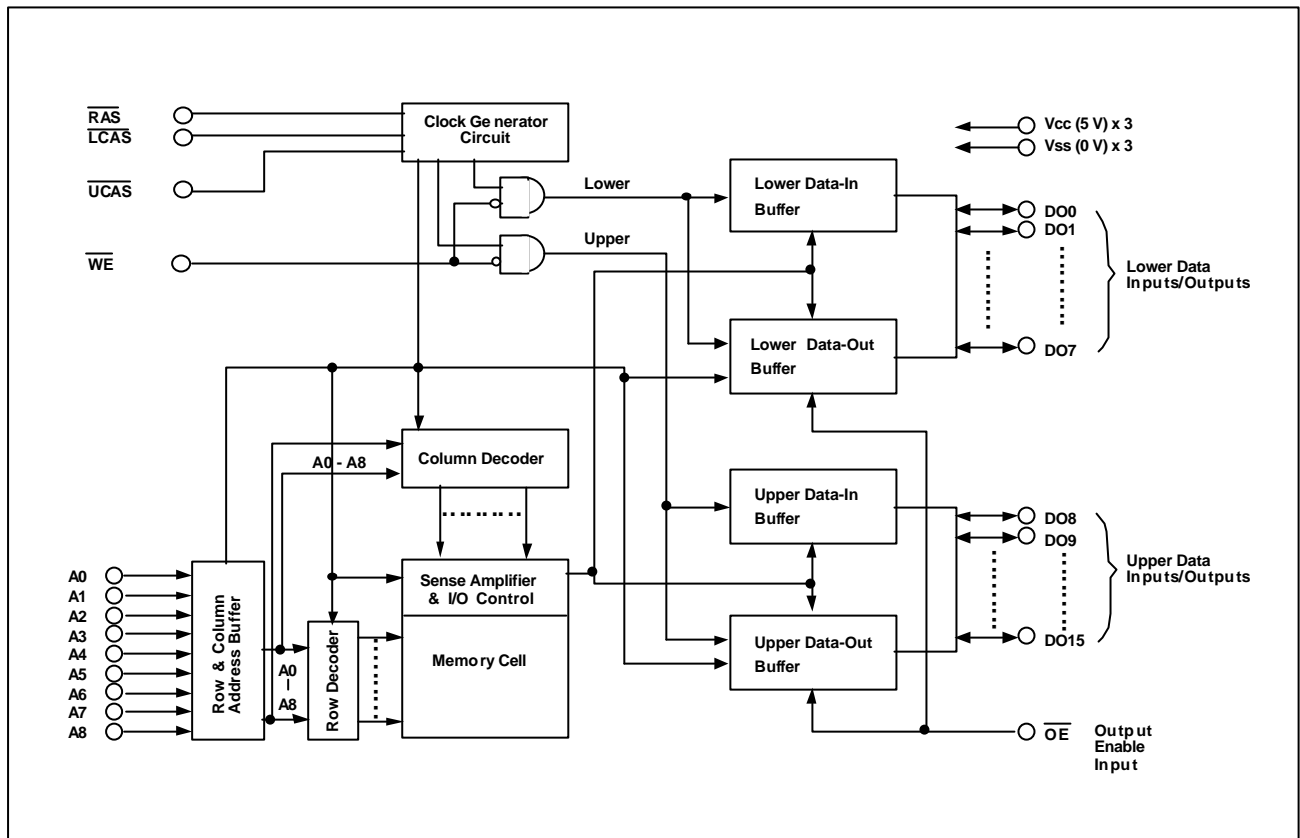
The Em614163A-30/35/40/45 fully utilizes the EDO Page Mode advantages. It allows 512 random access within a page with a fast cycle time as short as 13.3/15/16/18 ns.

The Em614163A-30/35/40/45 is ideally suitable for high performance graphics frame buffers, CD-ROMs, disk drivers, set top boxes, and DSP applications.

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Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V _{SS}	V _T	- 0.5 to +7.0	V
Supply voltage relative to V _{SS}	V _{CC}	- 0.5 to +7.0	V
Short circuit output current	I _{OUT}	50	mA
Power dissipation	P _T	1.0	W
Operating temperature	T _{OPT}	0 to +70	°C
Storage temperature	T _{STG}	- 55 to +125	°C

Capacitance

(T_a = 25°C; V_{CC} = 5V ; ϕ 10%; f = 1MHz)

Parameter	Symbol	Typ.	Max.	Unit	Note
Input capacitance (A0 - A8)	C _{I1}	5	5	pF	1
Input capacitance (RAS, UCAS, LCAS, WE, OE)	C _{I2}	5	5	pF	1
Output capacitance(I/O0 - I/O15)	C _{I/O}	7	7	pF	1

Notes:

1. Capacitance is sampled and not 100% tested.

Truth Table

Function		RAS	LCAS	UCAS	WE	OE	Addresses		DQs	Notes
							tr	tc		
Standby		H	H→X	H→X	X	X	X	X	High-Z	
Read: Word		L	L	L	H	L	ROW	COL	Data-out	
Read: Lower Byte		1	1	1	1	1	ROW	COL	Lower byte, data-out Upper byte, high-Z	
Read: Upper Byte		1	1	1	1	1	ROW	COL	Lower byte, high-Z Upper byte, data-out	
Write: Word (Early Write)		1	1	1	1	1	ROW	COL	Data-in	
Write: Lower Byte (Early)		1	1	1	1	1	ROW	COL	Lower byte, data-in Upper byte, high-Z	
Write: Upper Byte (Early)		1	1	1	1	1	ROW	COL	Lower byte, high-Z Upper byte, data-in	
Read Write		L	L	L	H→L	L→H	ROW	COL	Data-out, Data-in	1, 2
EDO-Page- Mode Read	1st Cycle	L	H→L	H→L	H	L	ROW	COL	Data-out	2
	2nd Cycle	L	H→L	H→L	H	L	n/a	COL	Data-out	2
EDO-Page- Mode Write	1st Cycle	L	H→L	H→L	L	X	ROW	COL	Data-in	1
	2nd Cycle	L	H→L	H→L	L	X	n/a	COL	Data-in	1
EDO- Page-Mode Read-Write	1st Cycle	L	H→L	H→L	H→L	L→H	ROW	COL	Data-out, Data-in	1, 2
	2nd Cycle	1	1	1	1	1	n/a	COL	Data-out, Data-in	1, 2
Hidden	Read	L→H→L	L	L	H	L	ROW	COL	Data-out	2
Refresh	Write	L→H→L	L	L	L	X	ROW	COL	Data-in	1, 3
RAS# only refresh		L	H	H	X	X	ROW	n/a	High-Z	
CBR Refresh		H→L	L	L	X	X	X	X	High-Z	4

Notes:

1. These WRITE cycles may also be BYTE WRITE cycles (either $\overline{\text{LCAS}}$ or $\overline{\text{UCAS}}$ active).
2. These READ cycles may also be BYTE READ cycles (either $\overline{\text{LCAS}}$ or $\overline{\text{UCAS}}$ active).
3. EARLY WRITE only.

4. At least one of the two $\overline{\text{CAS}}$ signals must be active (LCAS or UCAS).

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply voltage	V _{SS}	0	0	0	V	2
	V _{CC}	4.5	5.0	5.5	V	1, 2
Input high voltage	V _{IH}	2.4	i ⌀	V _{CC} + 0.3	V	1
Input low voltage	V _{IL}	- 0.5	i ⌀	0.8	V	1, 3

Notes:

1. All voltage referenced to V_{SS}.
2. The supply voltage with all V_{CC} pins must be the same level.
The supply voltage with all V_{SS} pins must be the same level.
3. V_{IL}(min.) = - 1.2V for pulse width i ⌀30ns.

DC Characteristics

T_A = 0 to +70°C; V_{CC} = +5V ± 10%, V_{SS} = 0V

Parameter	Symbol	Test Conditions	Em614163A		Unit	Notes
			-30/35/40/45			
			Min	Max		
Operating current	I _{CC1}	RAS cycling LCAS, UCAS cycling trc = min.	i ⌀	280/250/225/200	mA	1, 2
Standby current	I _{CC2}	RAS, LCAS, UCAS = V _{IH} Dout = High-Z	i ⌀	2	mA	
		RAS, LCAS, UCAS, OE = V _{CC} - 0.2V Dout = High-Z	i ⌀	1	mA	
RAS-only refresh current	I _{CC3}	RAS cycling, CAS = V _{IH} trc = min.	i ⌀	280/250/225/200	mA	2
Standby current	I _{CC5}	RAS = V _{IH} LCAS, UCAS = V _{IL} Dout = enable	i ⌀	5	mA	1
CAS-before-RAS refresh current	I _{CC6}	trc = min. RAS, CAS cycling	i ⌀	280/250/225/200	mA	
Fast page mode current	I _{CC7}	tpc = min.	i ⌀	280/250/225/200	mA	1, 2
Input leakage current	I _{LI}	0V _i \bar{O} V _{in} \bar{O} V _{CC}	-10	10	μA	
Output leakage current	I _{LO}	0V _i \bar{O} V _{out} \bar{O} V _{CC} Dout = Disable	-10	10	μA	
Output high voltage	V _{OH}	I _{OH} = - 2.5 mA	2.4		V	
Output low voltage	V _{OL}	I _{OL} = + 2.1 mA		0.4	V	

Notes:

1. I_{CC} depends on output load condition when the device is selected. I_{CC}-max is specified at the output open condition.
2. Address can be changed once or less while $\bar{RAS} = V_{IL}$.
3. Address can be changed once or less while LCAS and UCAS = V_{IL}.
4. All the V_{CC} pins shall be supplied with the same voltage. And all the V_{SS} pins shall be supplied with the same voltage.

AC Characteristics (2, 3, 4, 5)

($T_a = 0$ to $+70^\circ\text{C}$; $V_{cc} = 5\text{V}$; $\pm 10\%$, $V_{ss} = 0\text{V}$)

Test Conditions

- Input rise and fall times: 2ns
- AC test condition, input pulse levels 0V to 3V
- Output load: 1 TTL loads and 50pF
- Output timing reference levels: $V_{OH} = 2.0\text{V}$
 $V_{OL} = 0.8\text{V}$

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Parameter	Symbol	Em614163A		Unit	Notes
		-30/35/40/45			
		Min	Max		
Random read or write cycle time	t _{RC}	53/60/66/75	i Ⓣ	ns	1
RAS precharge time	t _{RP}	19/21/22/26	i Ⓣ	ns	
RAS pulse width	t _{RAS}	30/35/40/45	100,000	ns	6
$\overline{\text{U/LCAS}}$ pulse width	t _{CAS}	5/6/7/8	100,000	ns	7
Row address setup time	t _{ASR}	0	i Ⓣ	ns	
Row address hold time	t _{RAH}	6/6/6/7	i Ⓣ	ns	
Column address setup time	t _{ASC}	0	i Ⓣ	ns	8
Column address hold time	t _{CAH}	5/6/6/7	i Ⓣ	ns	8
RAS to $\overline{\text{U/LCAS}}$ delay time	t _{RC$\overline{\text{D}}$}	10/11/12/13	21/25/29/33	ns	9
RAS to column address delay time	t _{RAD}	8/9/10/11	15/17/18/20	ns	10
Column address to RAS lead time	t _{RAL}	16/18/20/22	i Ⓣ	ns	
RAS hold time	t _{RS$\overline{\text{H}}$}	6/7/7/8	i Ⓣ	ns	
$\overline{\text{U/LCAS}}$ hold time	t _{CS$\overline{\text{H}}$}	30/35/40/45	i Ⓣ	ns	
Column address hold time from RAS	t _{AR}	22/25/30/35	i Ⓣ	ns	
Write command time from RAS	t _{WCR}	22/25/30/35	i Ⓣ	ns	
Data-in hold time from RAS	t _{DHR}	22/25/30/35	i Ⓣ	ns	
$\overline{\text{U/LCAS}}$ to RAS precharge time	t _{CRP}	5/5/5/5	i Ⓣ	ns	11
$\overline{\text{OE}}$ to data-in delay time	t _{OE$\overline{\text{D}}$}	7/7/8/8	i Ⓣ	ns	
Transition time (rise and fall)	t _T	1	50	ns	12
Refresh period	t _{REF}	i Ⓣ	8	ms	
$\overline{\text{CAS}}$ to output in Low-Z	t _{CLZ}	0		ns	

Read Cycle

Parameter	Symbol	Em614163A		Unit	Notes
		-30/35/40/45			
		Min	Max		
Access time from RAS	t _{RAC}	i Ⓣ	30/35/40/45	ns	13
Access time from $\overline{\text{U/LCAS}}$	t _{CAC}	i Ⓣ	9/10/11/12	ns	14, 15, 16
Access time from column address	t _{AA}	i Ⓣ	16/18/20/22	ns	15, 17
Access time from $\overline{\text{OE}}$	t _{OE A}	i Ⓣ	9/9/10/10	ns	
Read command setup time	t _{RCS}	0	i Ⓣ	ns	8
Read command hold time to $\overline{\text{U/LCAS}}$	t _{RCH}	0	i Ⓣ	ns	11, 18
Read command hold time to RAS	t _{RRH}	0	i Ⓣ	ns	18
Output buffer turn-off time	t _{OFF}	0	6/7/8/8	ns	19
Output buffer turn-off $\overline{\text{OE}}$	t _{OE Z}	0	6/7/8/8	ns	19

Write Cycle

Write command setup time	t _{WCS}	0	i Ⓣ	ns	8, 20
Write command hold time	t _{WCH}	5/6/6/6	i Ⓣ	ns	8
Write command pulse width	t _{WP}	5/6/6/6	i Ⓣ	ns	
Write command to RAS lead time	t _{RWL}	10	i Ⓣ	ns	
Write command to $\overline{\text{U/LCAS}}$ lead time	t _{CWL}	5/5/6/6	i Ⓣ	ns	21
Data-in setup time	t _{DS}	0	i Ⓣ	ns	22
Data-in hold time	t _{DH}	5/6/6/7	i Ⓣ	ns	22
$\overline{\text{OE}}$ hold time from $\overline{\text{WE}}$	t _{OE H}	5/6/6/6	i Ⓣ	ns	

Read-Modify-Write Cycle

Parameter	Symbol	Em614163A		Unit	Notes
		-30/35/40/45			
		Min	Max		
Read-modify-write cycle time	t _{RWC}	73/83/90/100	i Ⓣ	ns	1
RAS to $\overline{\text{WE}}$ delay time	t _{RWD}	41/49/54/60	i Ⓣ	ns	20
$\overline{\text{U/LCAS}}$ to $\overline{\text{WE}}$ delay time	t _{CWD}	20/24/25/27	i Ⓣ	ns	20
Column address to $\overline{\text{WE}}$ delay time	t _{AWD}	33/40/44/49	i Ⓣ	ns	20

Refresh Cycle

$\overline{\text{U/LCAS}}$ setup time ($\overline{\text{CAS}}$ -before-RAS refresh cycle)	t _{CSR}	6/7/8/9	i Ⓣ	ns	8
$\overline{\text{U/LCAS}}$ hold time ($\overline{\text{CAS}}$ -before-RAS refresh cycle)	t _{CHR}	7/8/9/10	i Ⓣ	ns	11
RAS precharge to $\overline{\text{U/LCAS}}$ hold time	t _{RPC}	5	i Ⓣ	ns	8
$\overline{\text{U/LCAS}}$ precharge time in normal mode	t _{CPN}	5/5/5/6	i Ⓣ	ns	23

EDO Page Mode Cycle

Parameter	Symbol	Em614163A		Unit	Notes
		-30/35/40/45			
		Min	Max		
EDO page mode cycle time	tPC	13.3/15/16/18	i Ⓣ	ns	25
EDO page mode $\overline{U/LCAS}$ precharge time	tCP	5/5/5/6	i Ⓣ	ns	23
EDO page mode \overline{RAS} pulse width	tRASP	30/35/40/45	100,000	ns	24
Access time from $\overline{U/LCAS}$ precharge	tCPA	i Ⓣ	18/21/23/25	ns	11, 15
\overline{RAS} hold time from $\overline{U/LCAS}$ precharge	tCPRH	13/14/15/16	i Ⓣ	ns	
EDO page mode read-modify-write cycle $\overline{U/LCAS}$ precharge to \overline{WE} delay time	tCPW	27/31/36/41	i Ⓣ	ns	11
EDO page mode read-modify-write cycle time	tPRWC	35/40/45/50	i Ⓣ	ns	
\overline{OE} low to \overline{CAS} high setup time	tOES	5	i Ⓣ	ns	
\overline{OE} high hold time from \overline{CAS} high	tOEHC	6	i Ⓣ	ns	
\overline{OE} high pulse width	tOEP	6	i Ⓣ	ns	
\overline{OE} setup prior to \overline{RAS} during hidden refresh cycle	tORD	0	i Ⓣ	ns	
Data output hold after \overline{CAS} low	tCOH	3/3/3/5	i Ⓣ	ns	
Output disable delay from \overline{WE}	tWHZ	0	13	ns	
\overline{WE} pulse width for output disable when \overline{CAS} high	tWPZ	6	i Ⓣ	ns	

Counter Test Cycle

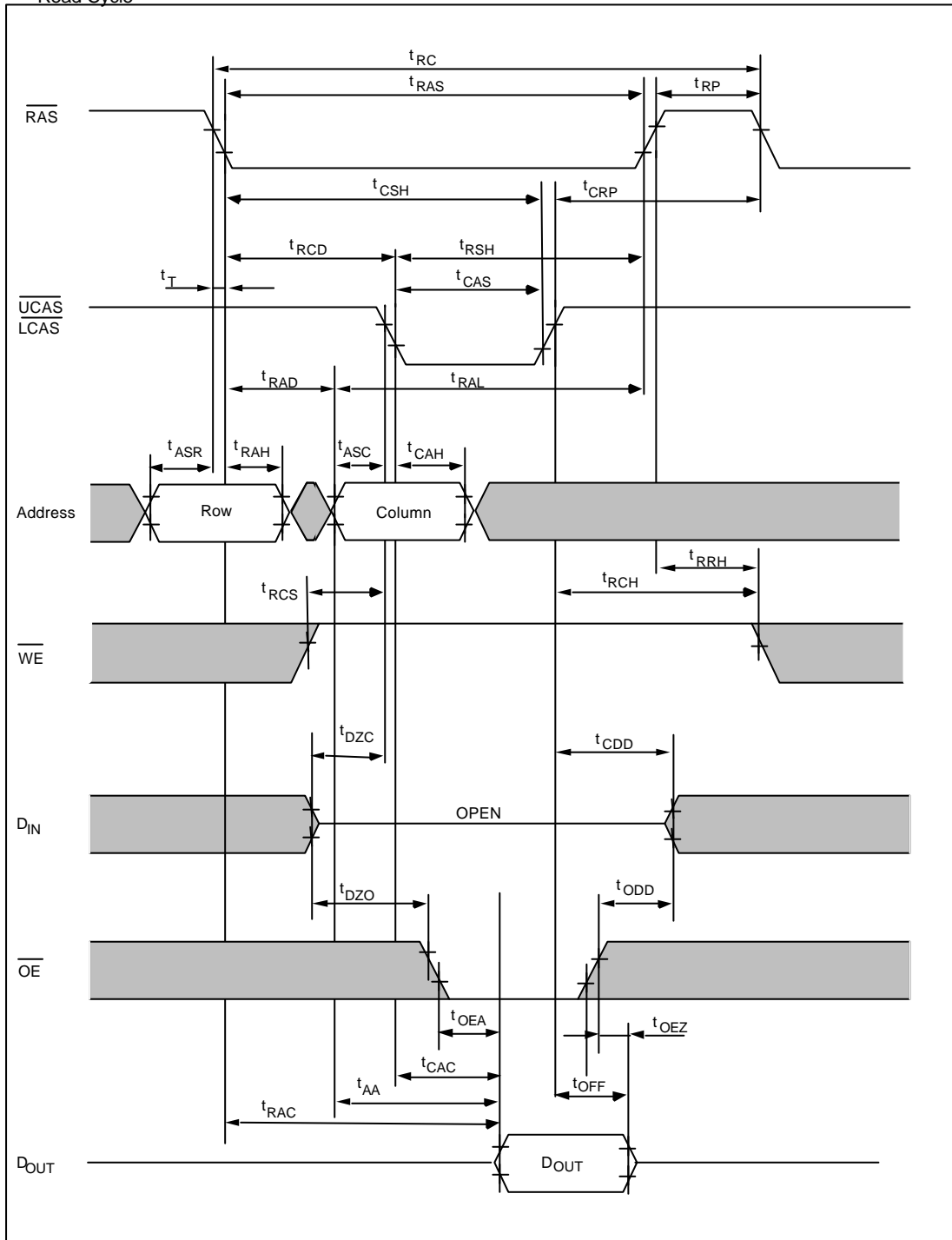
$\overline{U/LCAS}$ precharge time in counter test cycle	tcPT	30	i Ⓣ	ns	23
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Notes:

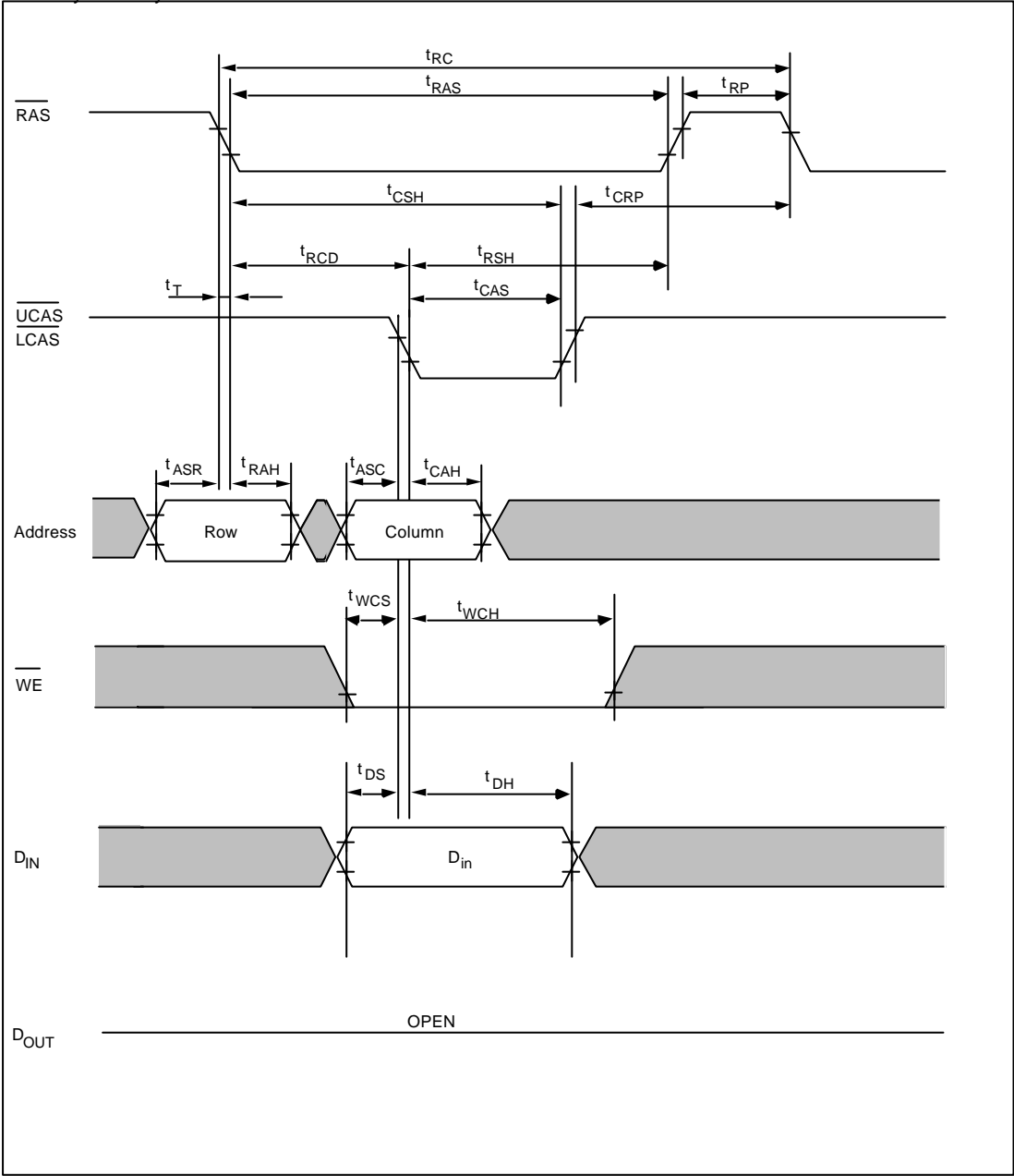
1. Assume $t_T = 2\text{ns}$.
2. An initial pause of 100 μs is required after power up followed by a minimum of eight initialization cycles ($\overline{\text{RAS}}$ -only refresh cycle or $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycle). If the internal refresh counter is used, a minimum of eight $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycles are required.
3. In delayed write or read-modify-write cycles, $\overline{\text{OE}}$ must disable output buffer prior to applying data to the device.
4. When both $\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ go low at the same time, all 16-bits data are written into the device. $\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ cannot be straggled within the same write/read cycles.
5. All the V_{CC} and all the V_{SS} pins shall be supplied with the same voltages.
6. $t_{\text{RAS}}(\text{min}) = t_{\text{RWD}}(\text{min}) + t_{\text{RWL}}(\text{min}) + t_T$ in read-modify-write cycle.
7. $t_{\text{CAS}}(\text{min}) = t_{\text{CWD}}(\text{min}) + t_{\text{CWL}}(\text{min}) + t_T$ in read-modify-write cycle.
8. t_{ASC} , t_{CAH} , t_{RCS} , t_{CSR} , t_{WCS} , t_{WCH} , and t_{RPC} are determined by the earlier falling edge of $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$.
9. Operation with the $t_{\text{RCD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met. $t_{\text{RCD}}(\text{max})$ is specified as a reference point only: If t_{RCD} is greater than the specified $t_{\text{RCD}}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
10. Operation with the $t_{\text{RAD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met. $t_{\text{RAD}}(\text{max})$ is specified as a reference point only: If t_{RAD} is greater than the specified $t_{\text{RAD}}(\text{max})$ limit, then access time is controlled exclusively by t_{AA} .
11. t_{CRP} , t_{CHR} , t_{RCH} , t_{CPA} and t_{CPW} are determined by the later rising edge of $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$.
12. $V_{\text{IH}}(\text{min})$ and $V_{\text{IL}}(\text{max})$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
13. Assumes that $t_{\text{RCD}}; \emptyset t_{\text{RCD}}(\text{max})$ and $t_{\text{RAD}}; \emptyset t_{\text{RAD}}(\text{max})$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
14. Assumes that $t_{\text{RCD}}; \emptyset t_{\text{RCD}}(\text{max})$ and $t_{\text{RAD}}; \emptyset t_{\text{RAD}}(\text{max})$.
15. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{CPA} .
16. t_{CAC} is guaranteed for one TTL and 50pF load.
17. Assumes that $t_{\text{RCD}}; \emptyset t_{\text{RCD}}(\text{max})$ and $t_{\text{RAD}}; \emptyset t_{\text{RAD}}(\text{max})$.
18. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
19. $t_{\text{OFF}}(\text{max})$ and $t_{\text{OEZ}}(\text{max})$ define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels. The t_{OFF} is determined by the later rising edge of $\overline{\text{RAS}}$ or $\overline{\text{CAS}}$.
20. t_{WCS} , t_{RWD} , t_{CWD} , and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{\text{WCS}}; \dot{U} t_{\text{WCS}}(\text{min})$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{\text{RWD}}; \dot{U} t_{\text{RWD}}(\text{min})$, $t_{\text{CWD}}; \dot{U} t_{\text{CWD}}(\text{min})$, $t_{\text{AWD}}; \dot{U} t_{\text{AWD}}(\text{min})$ and $t_{\text{CPW}}; \dot{U} t_{\text{CPW}}(\text{min})$, the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
21. t_{CWL} shall be satisfied by both $\overline{\text{UCAS}}$, $\overline{\text{LCAS}}$.
22. These parameters are referenced to $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$ leading edge in an early write cycle and to $\overline{\text{WE}}$ edge in a delayed write or a read-modify-write cycle.
23. t_{CPN} , t_{CP} , and t_{CPT} are determined by the time that both $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$ are high.
24. t_{RASP} defines $\overline{\text{RAS}}$ pulse width in fast page mode cycles.
25. Assume $t_T = 2\text{ns}$.

Timing Waveforms

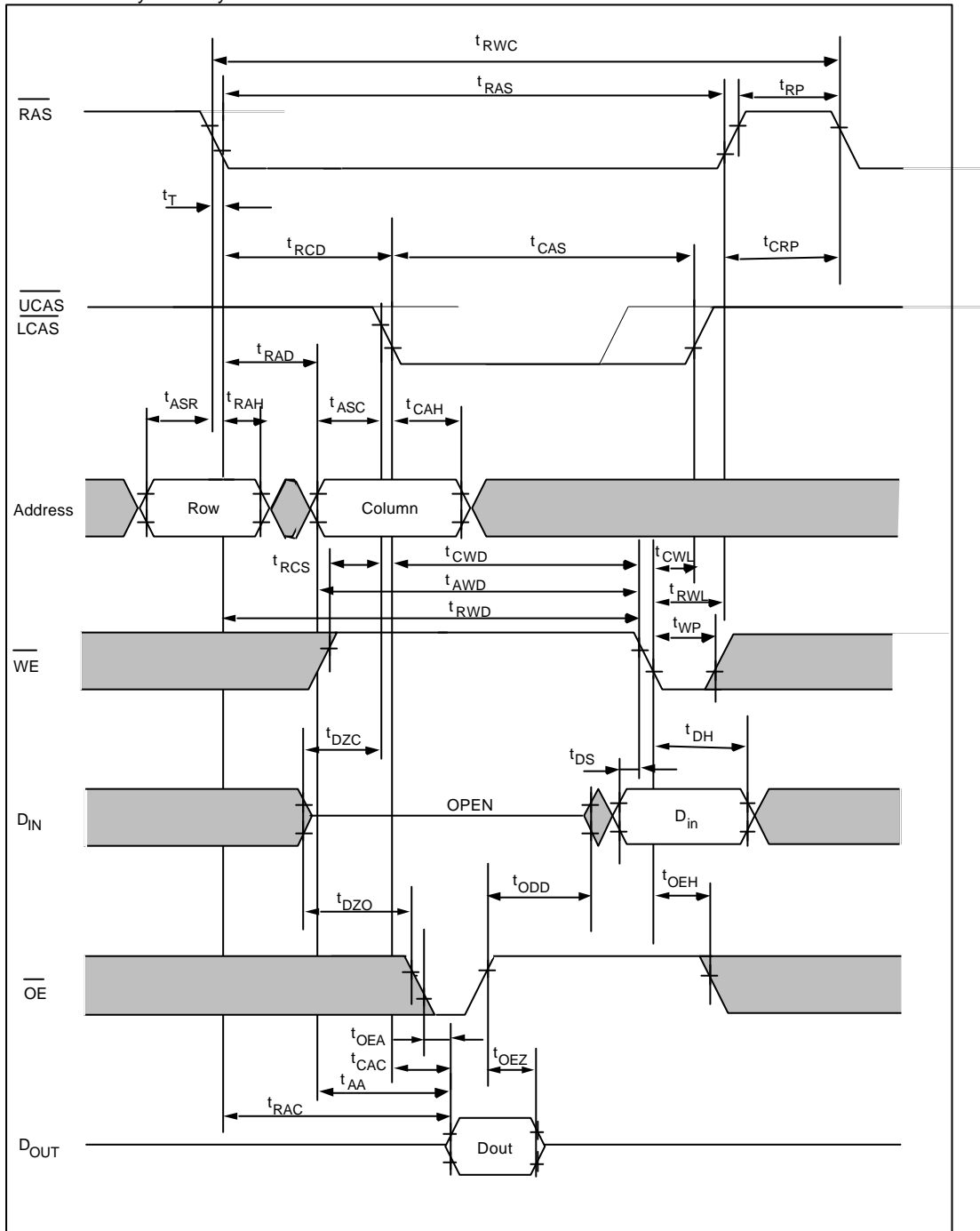
- Read Cycle



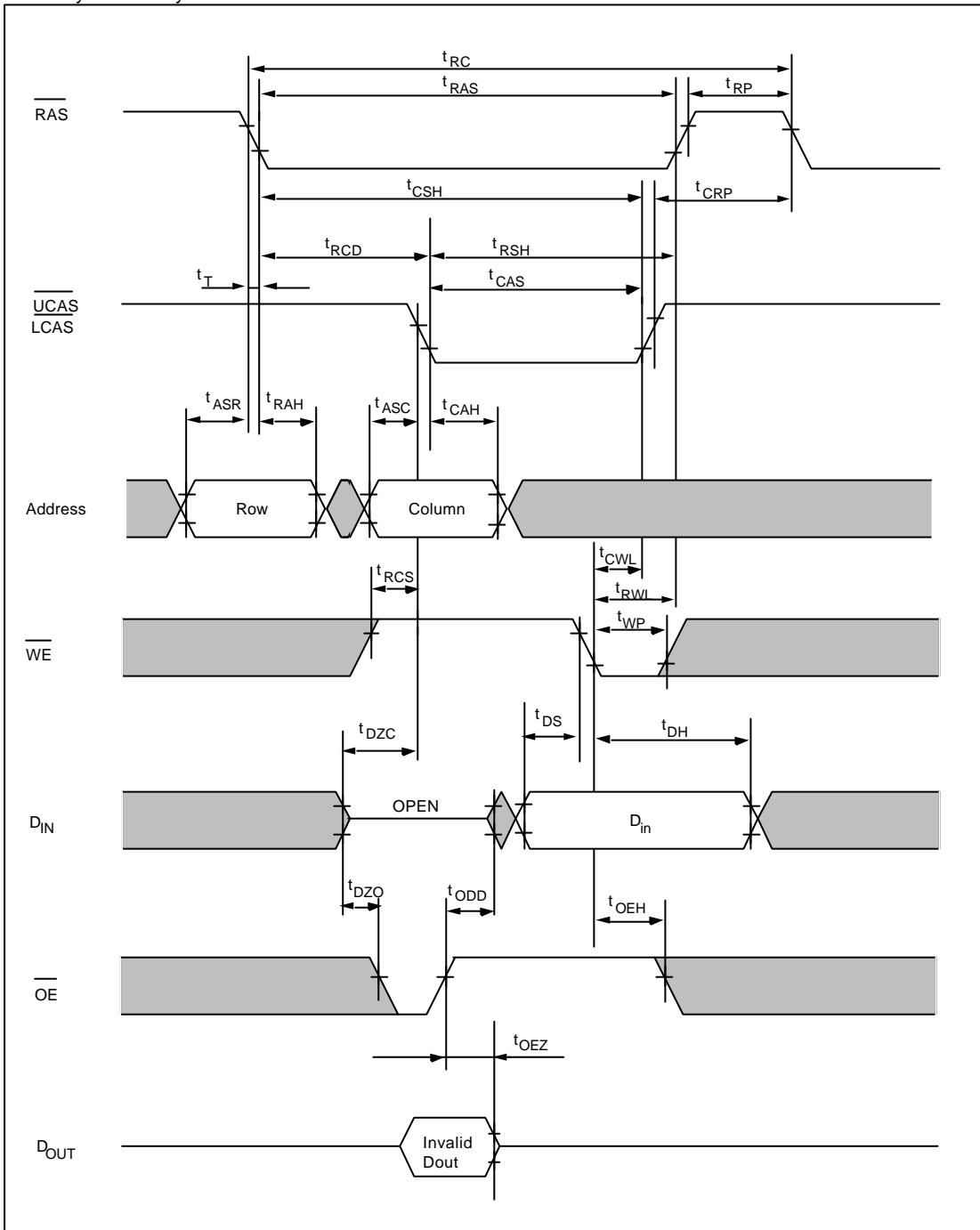
• Early Write Cycle



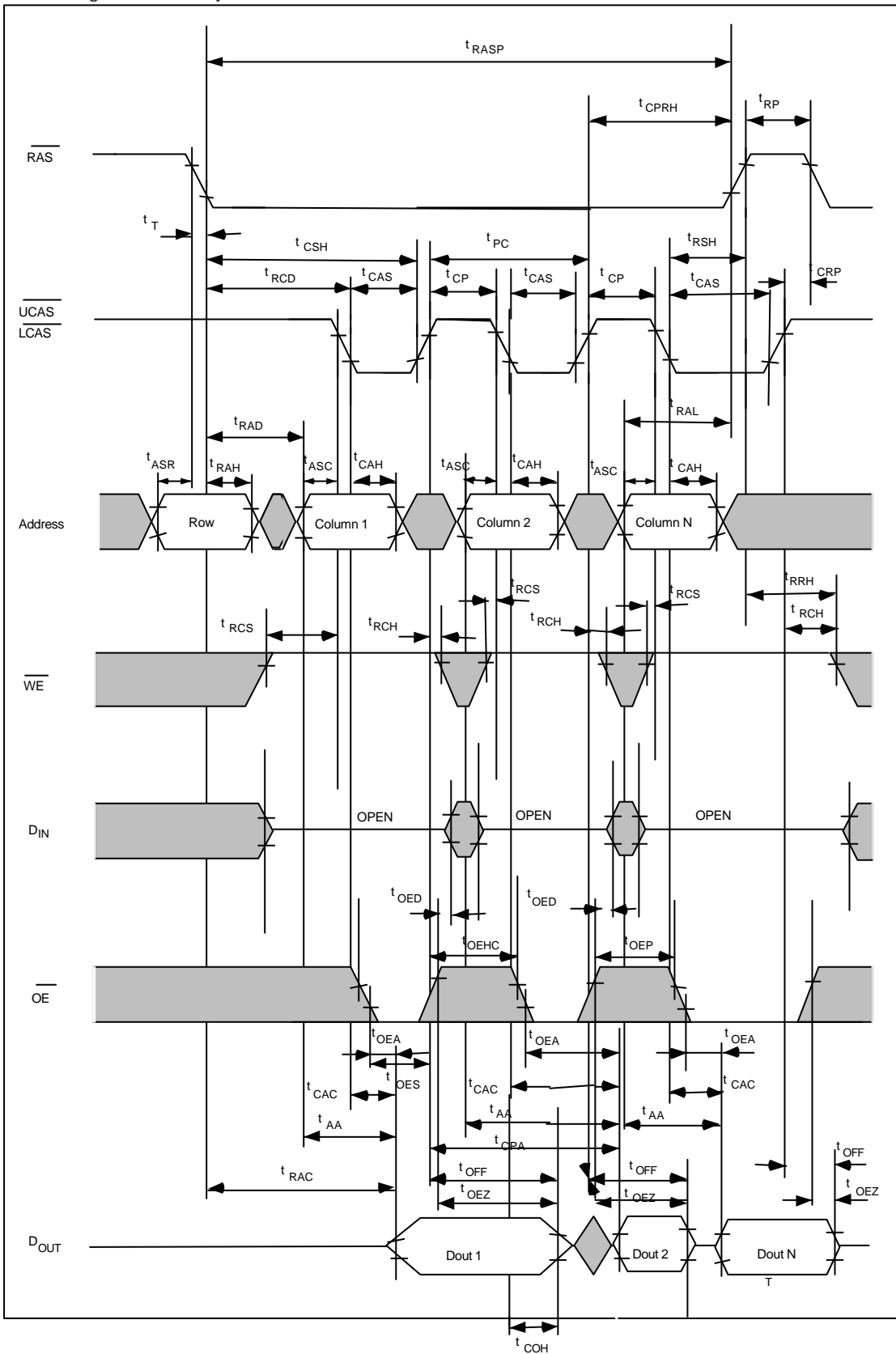
• Read-Modify-Write Cycle



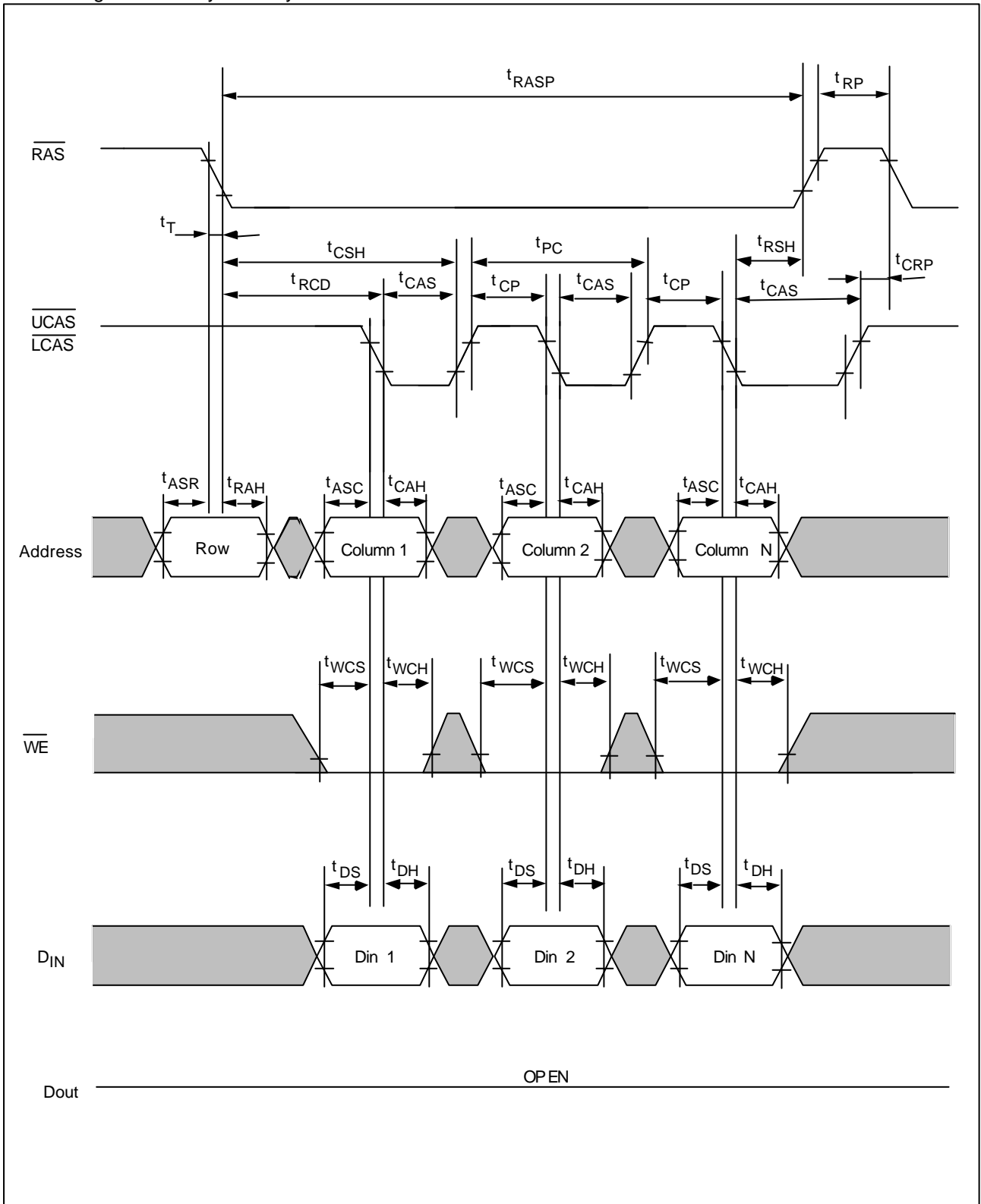
• Delayed Write Cycle



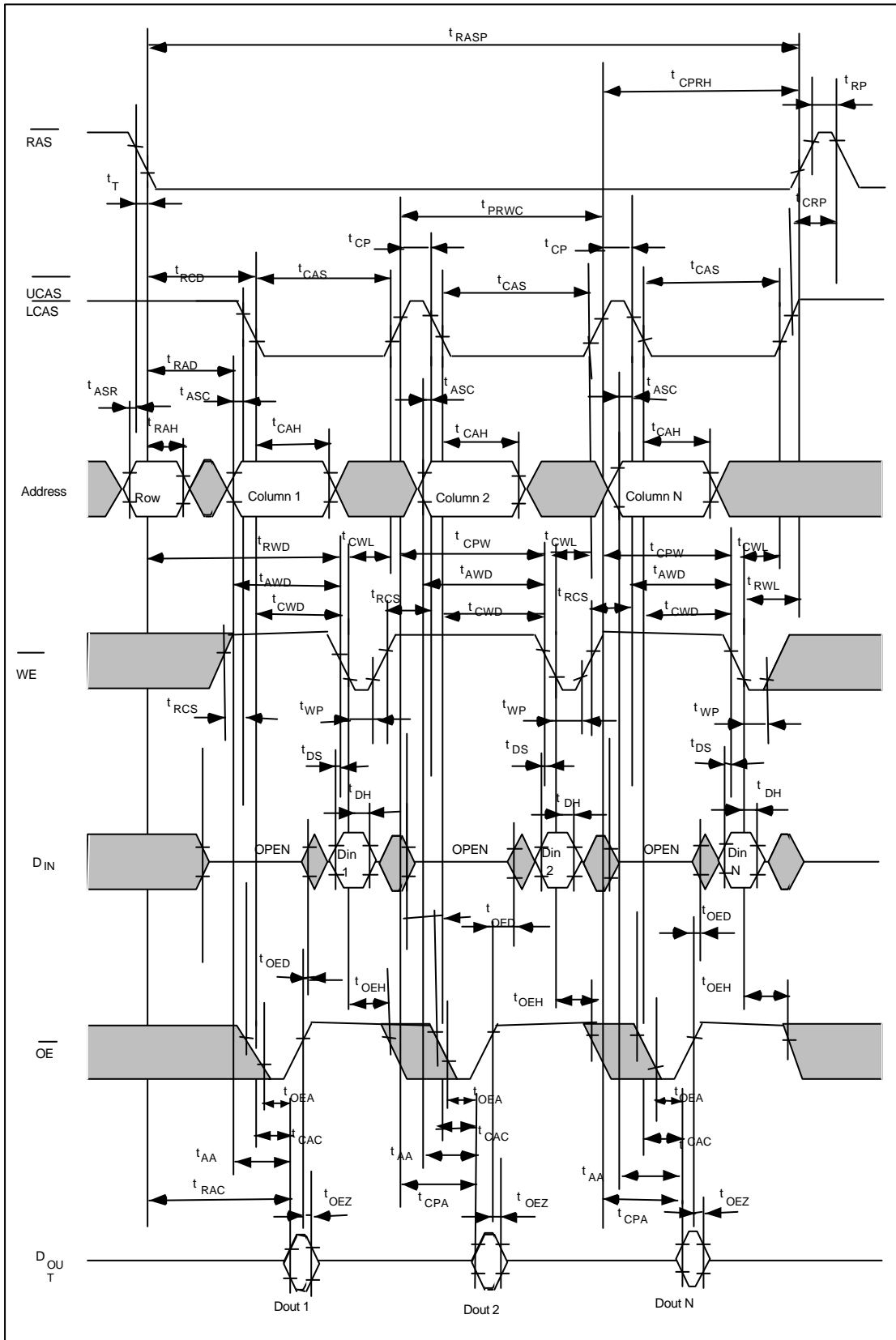
• EDO Page Mode Read Cycle



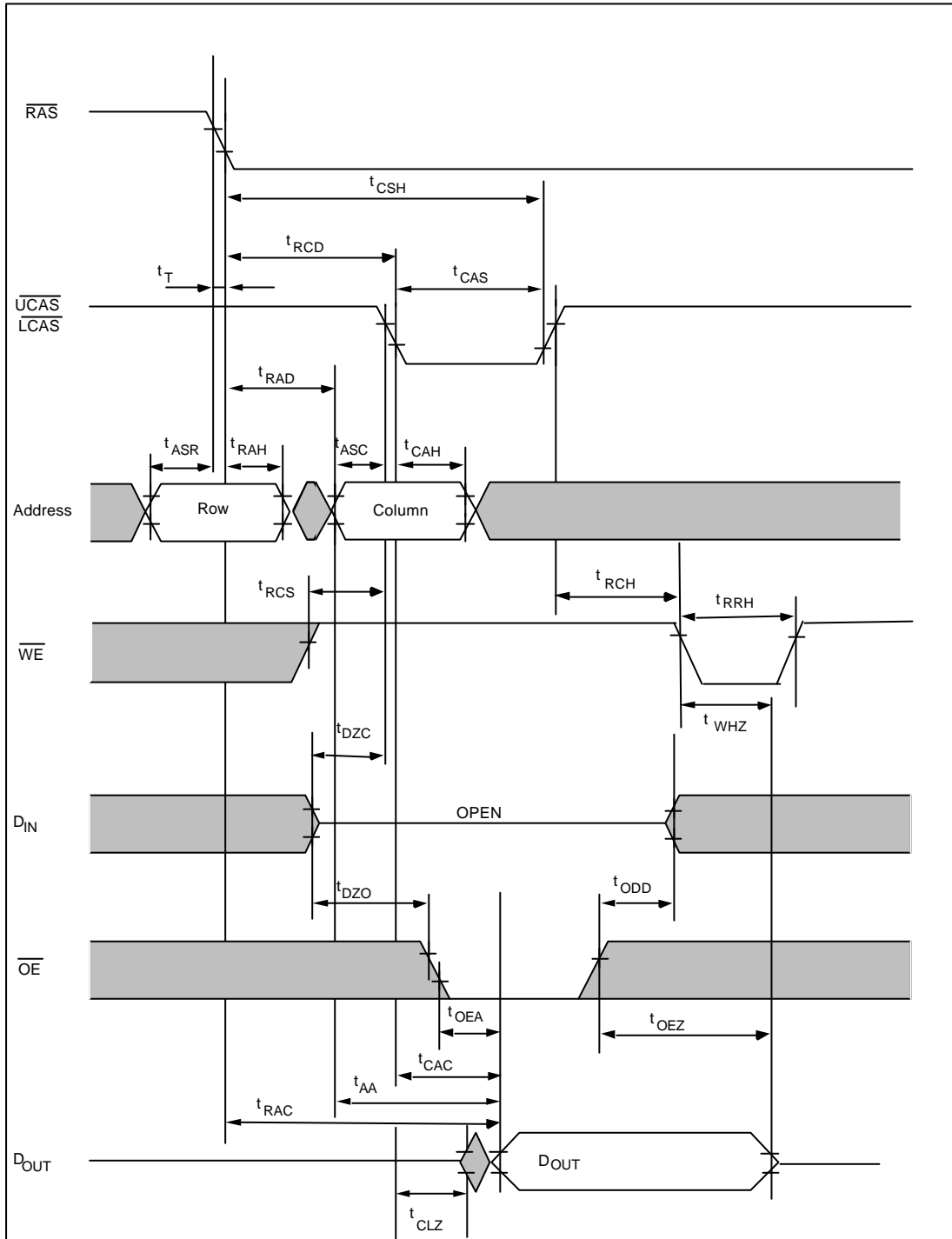
• EDO Page Mode Early Write Cycle



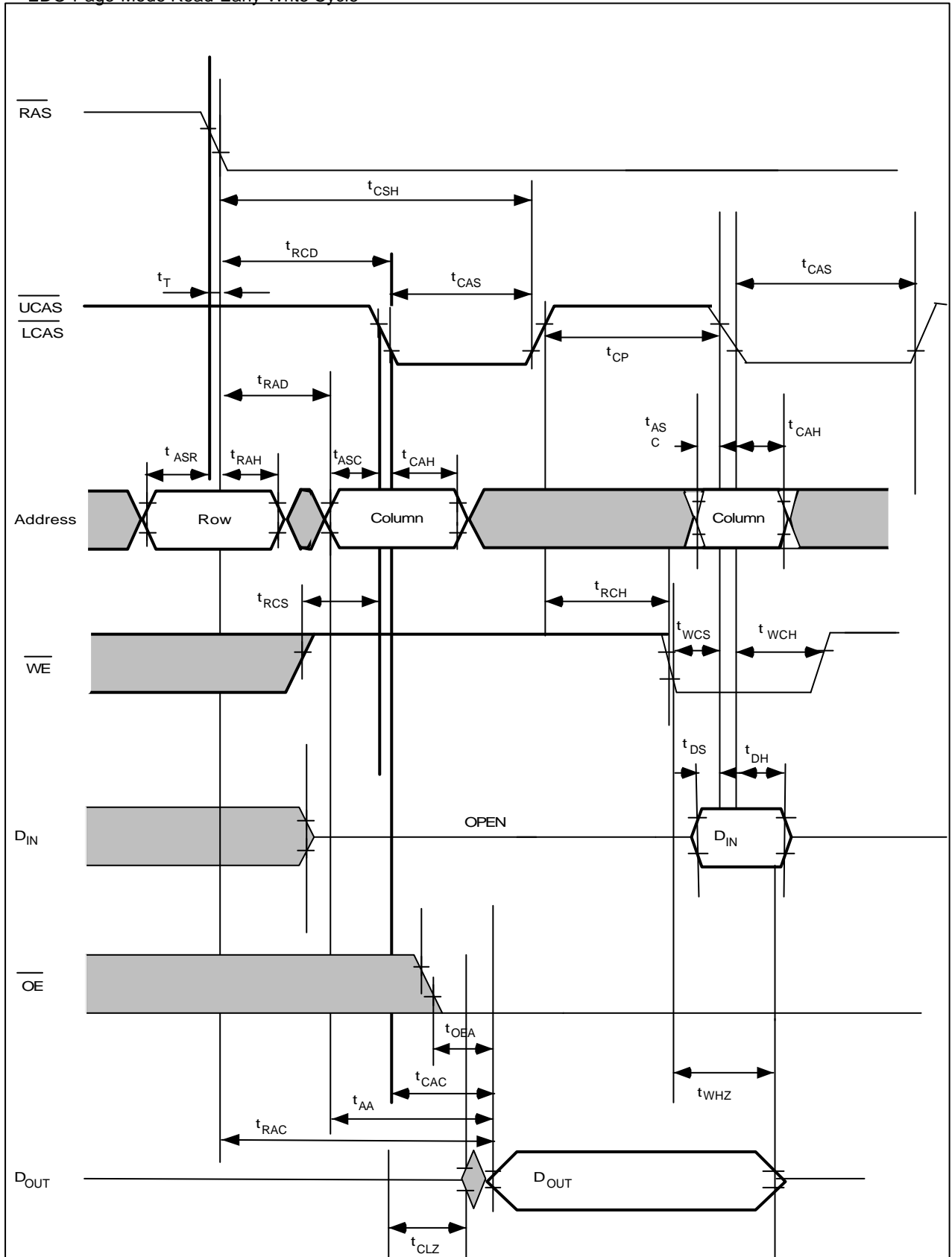
• EDO Page Mode Read/Modify-Write Cycle



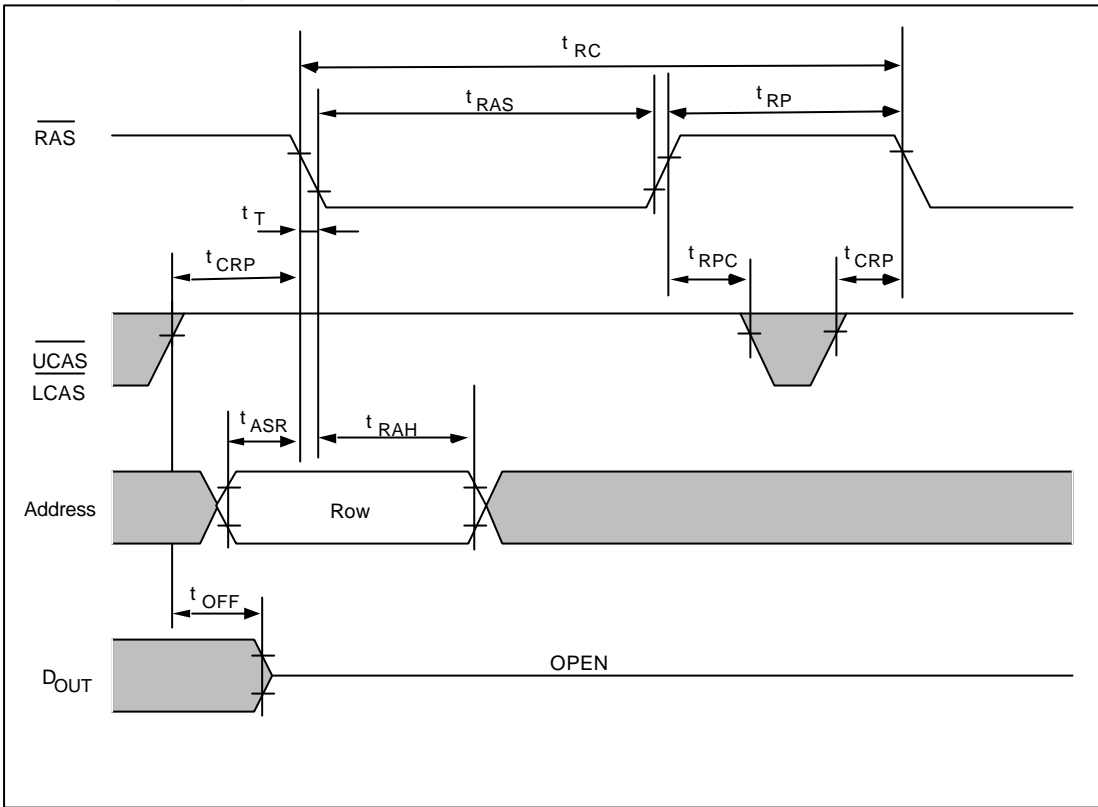
Read Cycle with \overline{WE} Controlled Disable



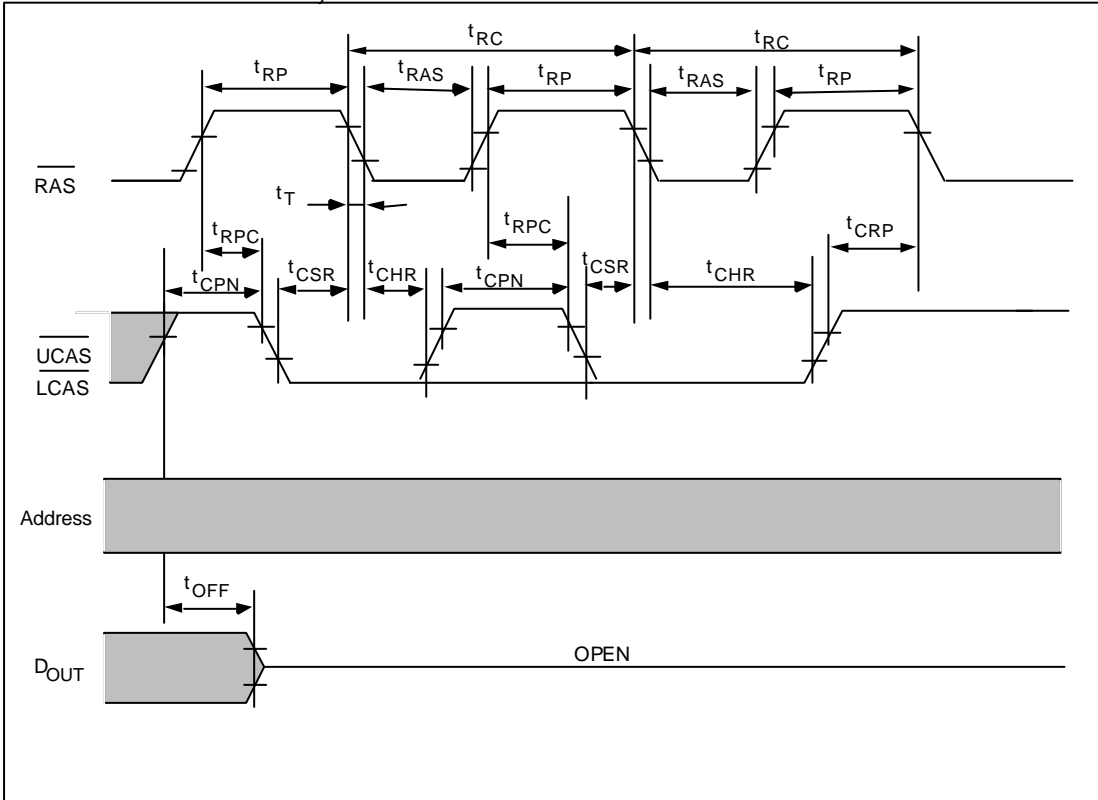
• EDO-Page-Mode Read-Early-Write Cycle



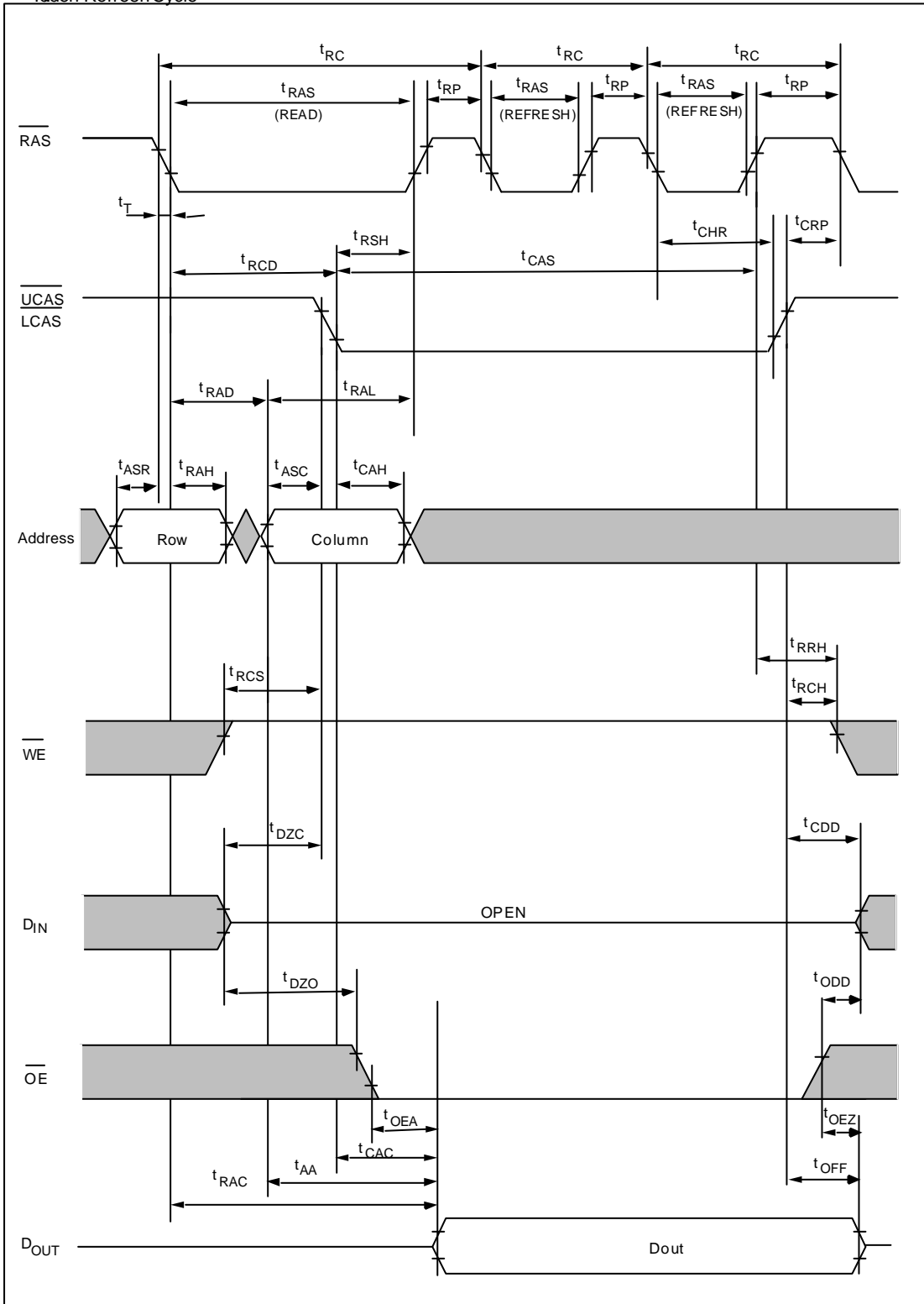
• RAS-Only Refresh Cycle



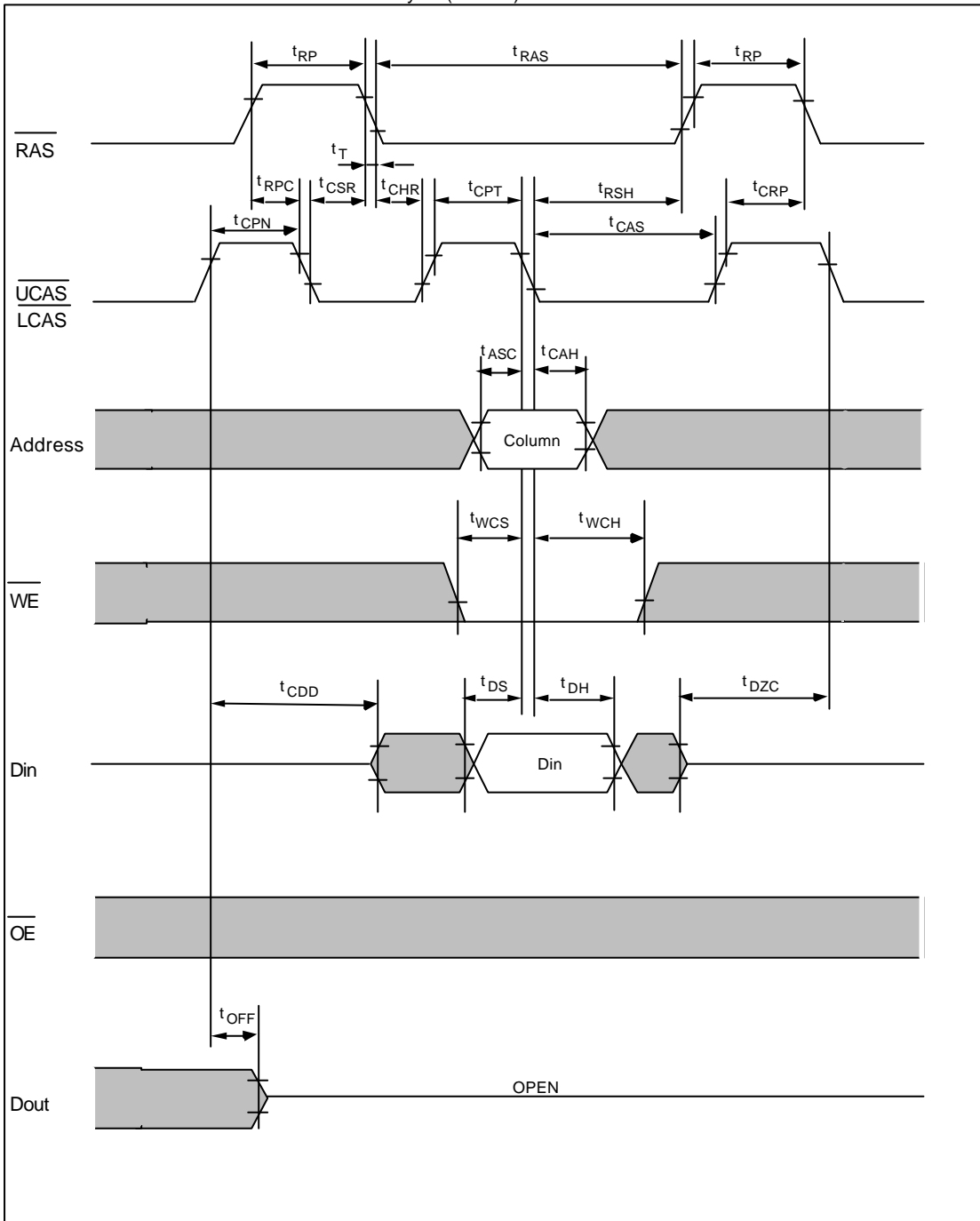
• CAS-Before-RAS Refresh Cycle



• Hidden Refresh Cycle

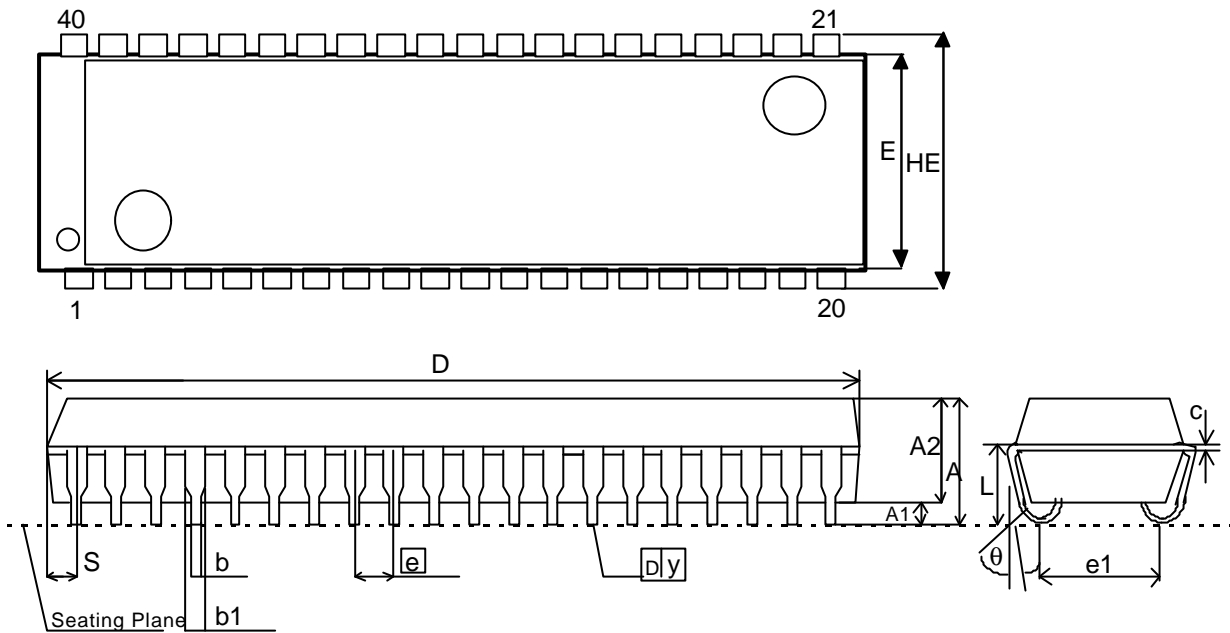


- CAS Before RAS Refresh Counter Check Cycle (WRITE)



Outline Drawing

40-Pin SOJ

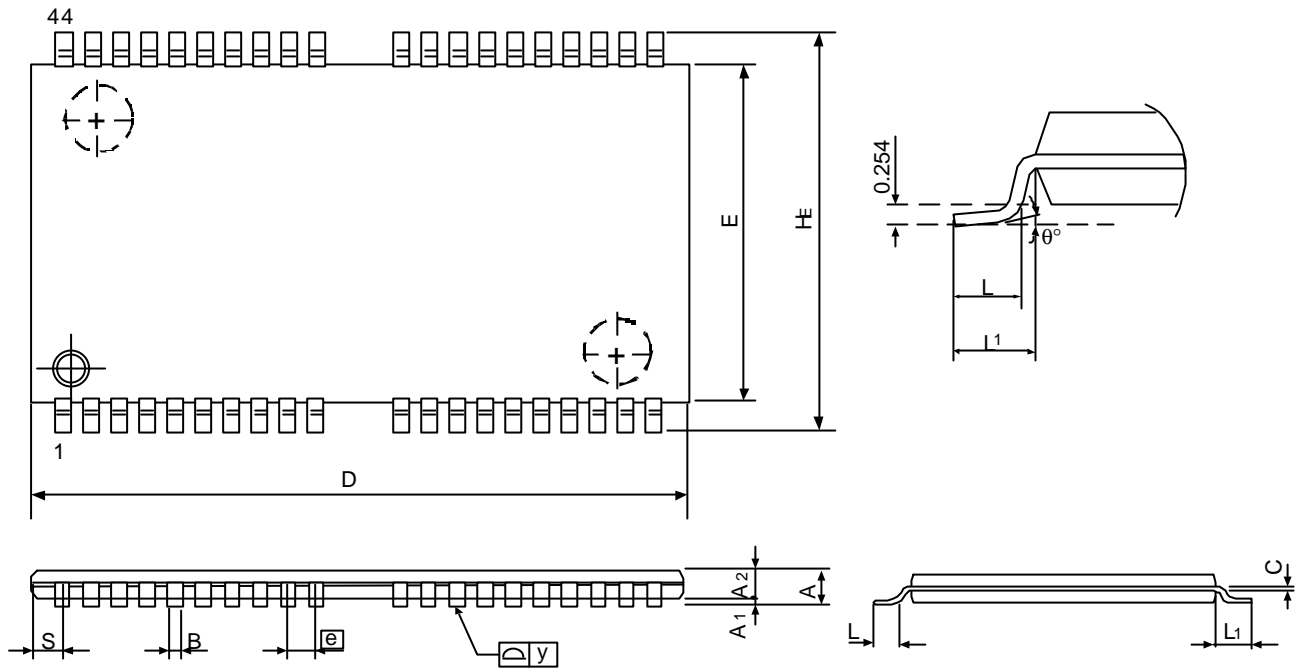


Symbol	Dimension in inch			Dimension in mm		
	Min	Num	Max	Min	Num	Max
A	$i \text{ } \overline{\text{D}}$	$i \text{ } \overline{\text{D}}$	0.144	$i \text{ } \overline{\text{D}}$	$i \text{ } \overline{\text{D}}$	3.66
A1	0.025	$i \text{ } \overline{\text{D}}$	$i \text{ } \overline{\text{D}}$	0.64	$i \text{ } \overline{\text{D}}$	$i \text{ } \overline{\text{D}}$
A2	0.105	0.110	0.115	2.67	2.79	2.92
b1	0.026	0.028	0.032	0.66	0.71	0.81
b	0.016	0.018	0.022	0.41	0.46	0.56
c	0.008	0.010	0.014	0.20	0.25	0.36
D	$i \text{ } \overline{\text{D}}$	1.025	1.035	$i \text{ } \overline{\text{D}}$	26.04	26.29
E	0.395	0.400	0.405	10.03	10.16	10.29
e	0.044	0.050	0.056	1.12	1.2	1.42
e1	0.348	0.368	0.388	8.84	9.35	9.86
HE	0.430	0.440	0.450	10.92	11.18	11.43
L	0.088	0.098	0.108	2.24	2.49	2.74
S	$i \text{ } \overline{\text{D}}$	$i \text{ } \overline{\text{D}}$	0.050	$i \text{ } \overline{\text{D}}$	$i \text{ } \overline{\text{D}}$	1.27
Y	$i \text{ } \overline{\text{D}}$	$i \text{ } \overline{\text{D}}$	0.004	$i \text{ } \overline{\text{D}}$	$i \text{ } \overline{\text{D}}$	0.10
q	0 $\text{ } \overline{\text{C}}$ X	$i \text{ } \overline{\text{D}}$	10 $\text{ } \overline{\text{C}}$ X	0 $\text{ } \overline{\text{C}}$ X	$i \text{ } \overline{\text{D}}$	10 $\text{ } \overline{\text{C}}$ X

Notes:

1. Dimension D Max & S include mold flash or tie bar burrs.
2. Dimension b1 does not include dambar protrusion/intrusion.
3. Dimension D & E include mold mismatch and are determined at the mold parting line.
4. Controlling dimension : inch
5. General appearance spec. should be based on final visual inspection spec.

40/44-Pin TSOP-II



Symbol	Dimension in inch			Dimension in mm		
	Min	Num	Max	Min	Num	Max
A	$i \text{ } \bar{\text{D}}$	$i \text{ } \bar{\text{D}}$	0.047	$i \text{ } \bar{\text{D}}$	$i \text{ } \bar{\text{D}}$	1.20
A1	0.002	$i \text{ } \bar{\text{D}}$	$i \text{ } \bar{\text{D}}$	0.05	$i \text{ } \bar{\text{D}}$	$i \text{ } \bar{\text{D}}$
A2	0.037	0.039	0.041	0.95	1.00	1.05
B	0.010	0.014	0.018	0.25	0.35	0.45
c	$i \text{ } \bar{\text{D}}$	0.006	$i \text{ } \bar{\text{D}}$	$i \text{ } \bar{\text{D}}$	0.15	$i \text{ } \bar{\text{D}}$
D	0.721	0.725	0.729	18.31	18.41	18.51
E	0.396	0.400	0.404	10.06	10.16	10.26
e	$i \text{ } \bar{\text{D}}$	0.031	$i \text{ } \bar{\text{D}}$	$i \text{ } \bar{\text{D}}$	0.80	$i \text{ } \bar{\text{D}}$
HE	0.455	0.463	0.471	11.56	11.76	11.96
L	0.016	0.020	0.024	0.40	0.50	0.60
L1	$i \text{ } \bar{\text{D}}$	0.031	$i \text{ } \bar{\text{D}}$	$i \text{ } \bar{\text{D}}$	0.80	$i \text{ } \bar{\text{D}}$
S	$i \text{ } \bar{\text{D}}$	$i \text{ } \bar{\text{D}}$	0.036	$i \text{ } \bar{\text{D}}$	$i \text{ } \bar{\text{D}}$	0.93
y	$i \text{ } \bar{\text{D}}$	$i \text{ } \bar{\text{D}}$	0.004	$i \text{ } \bar{\text{D}}$	$i \text{ } \bar{\text{D}}$	0.10
q	0c X	$i \text{ } \bar{\text{D}}$	5c X	0c X	$i \text{ } \bar{\text{D}}$	5c X

Notes :

1. Dimension D&E do not include interlead flash.
2. Dimension B does not include dambar protrusion/intrusion.
3. Dimension S includes end flash.
4. Controlling dimension : MM