

AUTOSWITCHING POWER MUX

Check for Samples: [TPS2110A](#), [TPS2111A](#)

FEATURES

- Two-Input, One-Output Power Multiplexer with Low $r_{DS(on)}$ Switches:
 - 84 mΩ Typ (TPS2111A)
 - 120 mΩ Typ (TPS2110A)
- Reverse and Cross-Conduction Blocking
- Wide Operating Voltage Range: 2.8 V to 5.5 V
- Low Standby Current: 0.5 μ A Typ
- Low Operating Current: 55 μ A Typ
- Adjustable Current Limit
- Controlled Output Voltage Transition Time: Limits Inrush Current
Minimizes Output Voltage Hold-Up Capacitance
- CMOS- and TTL-Compatible Control Inputs
- Manual and Auto-Switching Operating Modes
- Thermal Shutdown
- Available in a TSSOP-8 Package

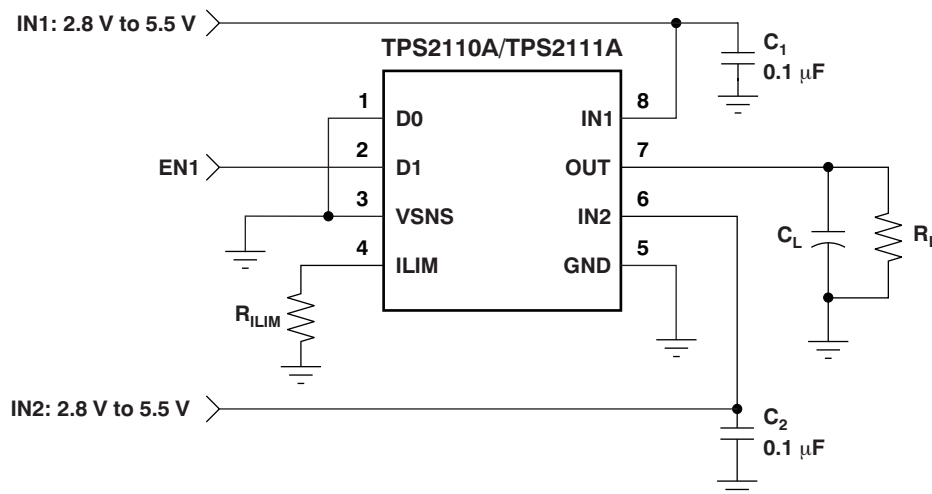
APPLICATIONS

- PCs
- PDAs
- Digital Cameras
- Modems
- Cell Phones
- Digital Radios
- MP3 Players

DESCRIPTION

The TPS211xA family of power multiplexers enables seamless transition between two power supplies, such as a battery and a wall adapter, each operating at 2.8 V to 5.5 V and delivering up to 1 A. The TPS211xA family includes extensive protection circuitry, including user-programmable current limiting, thermal protection, inrush current control, seamless supply transition, cross-conduction blocking, and reverse-conduction blocking. These features greatly simplify designing power multiplexer applications.

TYPICAL APPLICATION



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

AVAILABLE OPTIONS

FEATURE		TPS2110A	TPS2111A	TPS2112A	TPS2113A	TPS2114A	TPS2115A
Current Limit Adjustment Range		0.31 A to 0.75 A	0.63 A to 1.25 A	0.31 A to 0.75 A	0.63 A to 1.25 A	0.31 A to 0.75 A	0.63 A to 1.25 A
Switching Modes	Manual	Yes	Yes	No	No	Yes	Yes
	Automatic	Yes	Yes	Yes	Yes	Yes	Yes
Switch Status Output		No	No	Yes	Yes	Yes	Yes

ORDERING INFORMATION⁽¹⁾

T _A	PACKAGE	ORDERING NUMBER	PACKAGE MARKING
-40°C to 85°C	TSSOP-8 (PW)	TPS2110APW	2110A
		TPS2111APW	2111A

- (1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Over recommended operating junction temperature range, unless otherwise noted.

		TPS2110A, TPS2111A	UNIT
Input voltage range at pins IN1, IN2, D0, D1, VSNS, ILIM ⁽²⁾		−0.3 to 6	V
Output voltage range, V _{O(OUT)} ⁽²⁾		−0.3 to 6	V
Continuous output current, I _O	TPS2110A	0.9	A
	TPS2111A	1.5	
Continuous total power dissipation		See Dissipation Ratings table	
Operating virtual junction temperature range, T _J		Internally Limited	
ESD	Human body model (HBM)	2	kV
	Charged device model (CDM)	500	V

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to GND.

DISSIPATION RATINGS

PACKAGE	DERATING FACTOR ABOVE T _A = 25°C	T _A ≤ 25°C POWER RATING	T _A = 70°C POWER RATING	T _A = 85°C POWER RATING
TSSOP-8 (PW)	3.9 mW/°C	387 mW	213 mW	155 mW

RECOMMENDED OPERATING CONDITIONS

		TPS2110A, TPS2111A			UNIT
		MIN	NOM	MAX	
Input voltage at IN1, $V_{I(IN1)}$	$V_{I(IN2)} \geq 2.8 \text{ V}$	1.5		5.5	V
	$V_{I(IN2)} < 2.8 \text{ V}$	2.8		5.5	
Input voltage at IN2, $V_{I(IN2)}$	$V_{I(IN1)} \geq 2.8 \text{ V}$	1.5		5.5	V
	$V_{I(IN1)} < 2.8 \text{ V}$	2.8		5.5	
Input voltage: $V_{I(D0)}$, $V_{I(D1)}$, $V_{I(VSNS)}$		0		5.5	V
Current limit adjustment range, $I_{O(OUT)}$	TPS2110A	0.31		0.75	A
	TPS2111A	0.63		1.25	
Operating virtual junction temperature, T_J		–40		125	°C

ELECTRICAL CHARACTERISTICS: Power Switch

Over recommended operating junction temperature, $V_{I(IN1)} = V_{I(IN2)} = 5.5 \text{ V}$, and $R_{ILIM} = 400 \Omega$, unless otherwise noted.

PARAMETER		TEST CONDITIONS		TPS2110A			TPS2111A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Drain-source on-state resistance (INx–OUT)	$r_{DS(on)}^{(1)}$	$T_J = 25^\circ\text{C}$, $I_L = 500 \text{ mA}$	$V_{I(IN1)} = V_{I(IN2)} = 5.0 \text{ V}$		120	140		84	110	mΩ
			$V_{I(IN1)} = V_{I(IN2)} = 3.3 \text{ V}$		120	140		84	110	
			$V_{I(IN1)} = V_{I(IN2)} = 2.8 \text{ V}$		120	140		84	110	
		$T_J = 125^\circ\text{C}$, $I_L = 500 \text{ mA}$	$V_{I(IN1)} = V_{I(IN2)} = 5.0 \text{ V}$			220			150	mΩ
			$V_{I(IN1)} = V_{I(IN2)} = 3.3 \text{ V}$			220			150	
			$V_{I(IN1)} = V_{I(IN2)} = 2.8 \text{ V}$			220			150	

(1) The TPS211xA can switch a voltage as low as 1.5 V as long as there is a minimum of 2.8 V at one of the input power pins. In this specific case, the lower supply voltage has no effect on the IN1 and IN2 switch on-resistances.

ELECTRICAL CHARACTERISTICS

Over recommended operating junction temperature, $V_{I(IN1)} = V_{I(IN2)} = 5.5 \text{ V}$, $I_{O(OUT)} = 0 \text{ A}$, and $R_{ILIM} = 400 \Omega$, unless otherwise noted.

PARAMETER		TEST CONDITIONS	TPS2110A, TPS2111A			UNIT	
			MIN	TYP	MAX		
LOGIC INPUTS (D0 AND D1)							
High-level input voltage	V _{IH}		2			V	
Low-level input voltage	V _{IL}		0.7			V	
Input current at D0 or D1		D0 or D1 = High, sink current	1			μA	
		D0 or D1 = Low, source current	0.5	1.4	5		
SUPPLY AND LEAKAGE CURRENTS							
Supply current from IN1 (operating)		D1 = High, D0 = Low (IN1 active), V _{I(IN2)} = 3.3 V	55			90	μA
		D1 = High, D0 = Low (IN1 active), V _{I(IN1)} = 3.3 V	1			12	
		D0 = D1 = Low (IN2 active), V _{I(IN2)} = 3.3 V				75	
		D0 = D1 = Low (IN2 active), V _{I(IN1)} = 3.3 V				1	
Supply current from IN2 (operating)		D1 = High, D0 = Low (IN1 active), V _{I(IN2)} = 3.3 V				1	μA
		D1 = High, D0 = Low (IN1 active), V _{I(IN1)} = 3.3 V				75	
		D0 = D1 = Low (IN2 active), V _{I(IN2)} = 3.3 V	1			12	
		D0 = D1 = Low (IN2 active), V _{I(IN1)} = 3.3 V	55			90	

ELECTRICAL CHARACTERISTICS (continued)

Over recommended operating junction temperature, $V_{I(IN1)} = V_{I(IN2)} = 5.5\text{ V}$, $I_{O(OUT)} = 0\text{ A}$, and $R_{ILIM} = 400\ \Omega$, unless otherwise noted.

PARAMETER		TEST CONDITIONS	TPS2110A, TPS2111A			UNIT
			MIN	TYP	MAX	
SUPPLY AND LEAKAGE CURRENTS, continued						
Quiescent current from IN1 (standby)		D0 = D1 = High (inactive), $V_{I(IN2)} = 3.3\text{ V}$	0.5		2	μA
		D0 = D1 = High (inactive), $V_{I(IN1)} = 3.3\text{ V}$			1	
Quiescent current from IN2 (standby)		D0 = D1 = High (inactive), $V_{I(IN2)} = 3.3\text{ V}$			1	μA
		D0 = D1 = High (inactive), $V_{I(IN1)} = 3.3\text{ V}$	0.5		2	
Forward leakage current from IN1 (measured from OUT to GND)		D0 = D1 = High (inactive), IN2 open, $V_{O(OUT)} = 0\text{ V}$ (shorted), $T_J = 25^\circ\text{C}$	0.1		5	μA
Forward leakage current from IN2 (measured from OUT to GND)		D0 = D1 = High (inactive), IN1 open, $V_{O(OUT)} = 0\text{ V}$ (shorted), $T_J = 25^\circ\text{C}$	0.1		5	μA
Reverse leakage current to INx (measured from INx to GND)		D0 = D1 = High (inactive), $V_{I(INx)} = 0\text{ V}$, $V_{O(OUT)} = 5.5\text{ V}$, $T_J = 25^\circ\text{C}$	0.3		5	μA
CURRENT LIMIT CIRCUIT						
Current limit accuracy	TPS2110A	$R_{ILIM} = 400\ \Omega$	0.51	0.63	0.80	A
		$R_{ILIM} = 700\ \Omega$	0.30	0.36	0.50	
	TPS2111A	$R_{ILIM} = 400\ \Omega$	0.95	1.25	1.56	A
		$R_{ILIM} = 700\ \Omega$	0.47	0.71	0.99	
Current limit settling time	t_d	Time for short-circuit output current to settle within 10% of its steady state value.	1			ms
Input current at ILIM		$V_{I(ILIM)} = 0\text{ V}$, $I_{O(OUT)} = 0\text{ A}$	−15		0	μA
VSNS COMPARATOR						
VSNS threshold voltage		$V_{I(VSNS)} \uparrow$	0.78	0.80	0.82	V
		$V_{I(VSNS)} \downarrow$	0.735	0.755	0.775	
VSNS comparator hysteresis			30		60	mV
Deglitch of VSNS comparator (both $\uparrow \downarrow$)			90	150	220	μs
Input current		$0\text{ V} \leq V_{I(VSNS)} \leq 5.5\text{ V}$	−1		1	μA
UVLO						
IN1 and IN2 UVLO		Falling edge	1.15	1.25		V
		Rising edge		1.30	1.35	
IN1 and IN2 UVLO hysteresis			30	57	65	mV
Internal V_{DD} UVLO (the higher of IN1 and IN2)		Falling edge	2.4	2.53		V
		Rising edge		2.58	2.8	
Internal V_{DD} UVLO hysteresis			30	50	75	mV
UVLO deglitch for IN1, IN2		Falling edge		110		μs
REVERSE CONDUCTION BLOCKING						
Minimum output-to-input voltage difference to block switching	$\Delta V_{O(I_block)}$	D0 = D1 = high, $V_{I(INx)} = 3.3\text{ V}$. Connect OUT to a 5-V supply through a series 1-k Ω resistor. Let D0 = low. Slowly decrease the supply voltage until OUT connects to IN1.	80	100	120	mV
THERMAL SHUTDOWN						
Thermal shutdown threshold		TPS211xA is in current limit.	135			$^\circ\text{C}$
Recovery from thermal shutdown		TPS211xA is in current limit.	125			$^\circ\text{C}$
Hysteresis			10			$^\circ\text{C}$
IN2-IN1 COMPARATORS						
Hysteresis of IN2-IN1 comparator			0.1		0.2	V
Deglitch of IN2-IN1 comparator (both $\uparrow \downarrow$)			10	20	50	μs

SWITCHING CHARACTERISTICS

Over recommended operating junction temperature, $V_{I(IN1)} = V_{I(IN2)} = 5.5 \text{ V}$, and $R_{LIM} = 400 \Omega$, unless otherwise noted.

PARAMETER		TEST CONDITIONS		TPS2110A			TPS2111A			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t _R	Output rise time from an enable	V _{I(IN1)} = V _{I(IN2)} = 5 V	T _J = 25°C, C _L = 1 μF, I _L = 500 mA; see Figure 1(a).	0.5	1.0	1.5	1	1.8	3	ms
t _F	Output fall time from a disable	V _{I(IN1)} = V _{I(IN2)} = 5 V	T _J = 25°C, C _L = 1 μF, I _L = 500 mA; see Figure 1(a).	0.35	0.5	0.7	0.5	1	2	ms
t _T	Transition time	IN1 to IN2 transition, V _{I(IN1)} = 3.3 V, V _{I(IN2)} = 5 V	T _J = 125°C, C _L = 10 μF, I _L = 500 mA; measure transition time as 10% to 90% rise time or from 3.4 V to 4.8 V on V _{O(OUT)} . See Figure 1(b).	40	60		40	60	μs	
		IN2 to IN1 transition, V _{I(IN1)} = 5 V, V _{I(IN2)} = 3.3 V		40	60		40	60		
t _{PLH1}	Turn-on propagation delay from an enable	V _{I(IN1)} = V _{I(IN2)} = 5 V Measured from enable to 10% of V _{O(OUT)}	T _J = 25°C, C _L = 10 μF, I _L = 500 mA; see Figure 1(a).	0.5			1			ms
t _{PHL1}	Turn-off propagation delay from a disable	V _{I(IN1)} = V _{I(IN2)} = 5 V Measured from disable to 90% of V _{O(OUT)}	T _J = 25°C, C _L = 10 μF, I _L = 500 mA; see Figure 1(a).	3			5			ms
t _{PLH2}	Switch-over rising propagation delay	Logic 1 to Logic 0 transition on D1, V _{I(IN1)} = 1.5 V, V _{I(IN2)} = 5 V, V _{I(D0)} = 0 V, Measured from D1 to 10% of V _{O(OUT)}	T _J = 25°C, C _L = 10 μF, I _L = 500 mA; see Figure 1(c).	40	100		40	100	μs	
t _{PHL2}	Switch-over falling propagation delay	Logic 0 to Logic 1 transition on D1, V _{I(IN1)} = 1.5 V, V _{I(IN2)} = 5 V, V _{I(D0)} = 0 V, Measured from D1 to 90% of V _{O(OUT)}	T _J = 25°C, C _L = 10 μF, I _L = 500 mA; see Figure 1(c).	2	3	10	2	5	10	ms

PARAMETER MEASUREMENT INFORMATION

TIMING WAVEFORMS

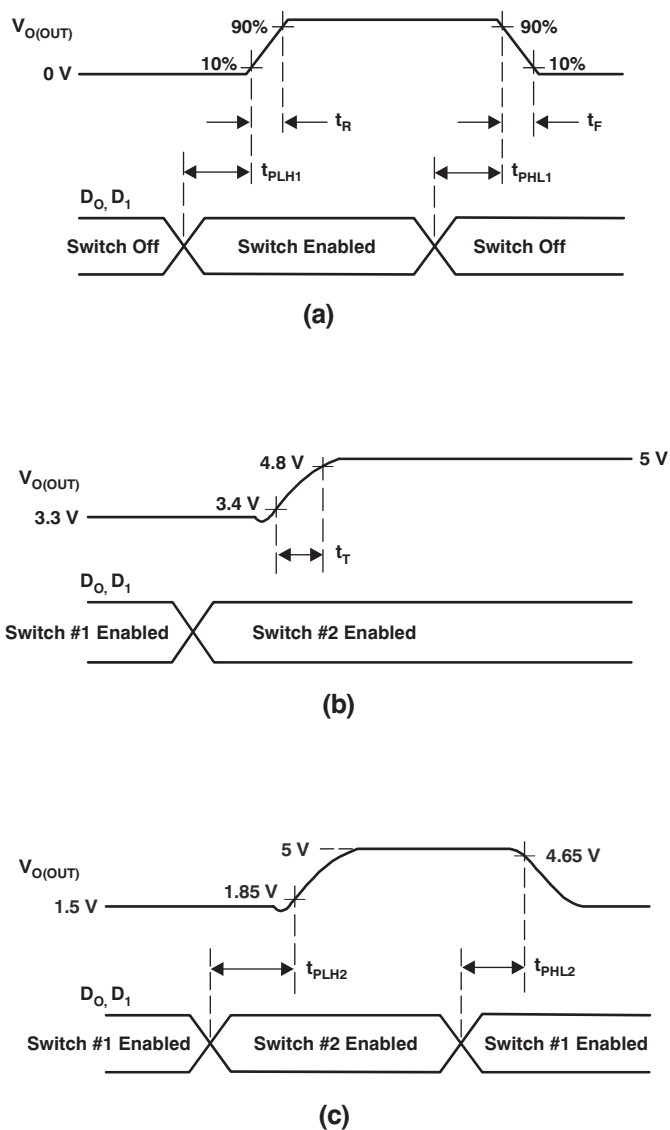


Figure 1. Propagation Delays and Transition Timing Waveforms

DEVICE INFORMATION

TRUTH TABLE

D1	D0	$V_{I(VSNS)} > 0.8 \text{ V}^{(1)}$	$V_{I(IN2)} > V_{I(IN1)}$	OUT ⁽²⁾
0	0	X	X	IN2
0	1	Yes	X	IN1
0	1	No	No	IN1
0	1	No	Yes	IN2
1	0	X	X	IN1
1	1	X	X	Hi-Z

- (1) X = Don't care.
(2) The undervoltage lockout circuit causes the output to go Hi-Z if the selected power supply does not exceed the IN1/IN2 UVLO, or if neither of the supplies exceeds the internal V_{DD} UVLO.

PIN CONFIGURATIONS

PW PACKAGE
TSSOP-8
(TOP VIEW)

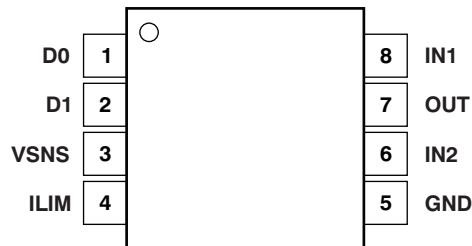
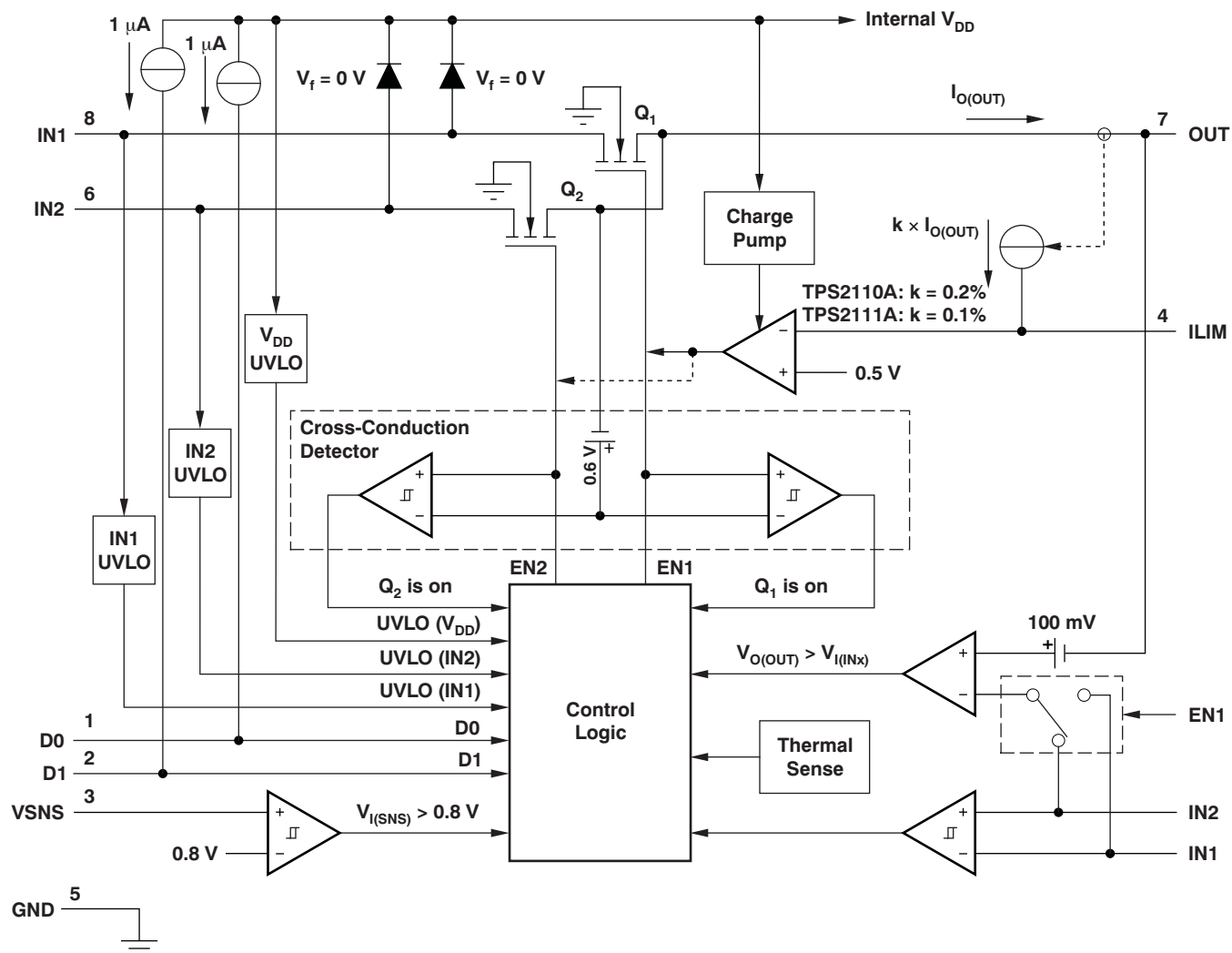


Table 1. TERMINAL FUNCTIONS

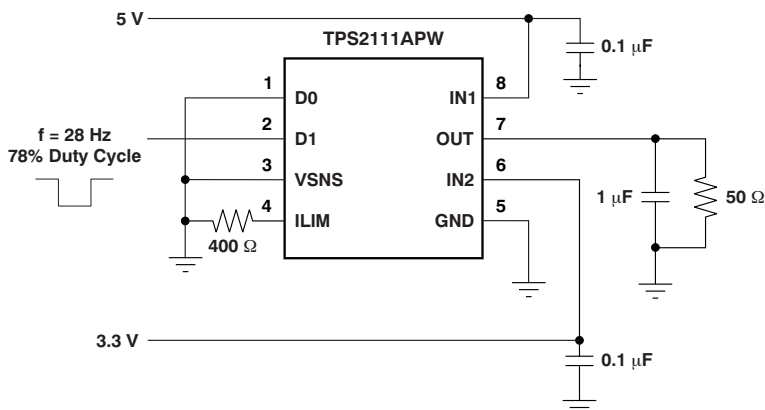
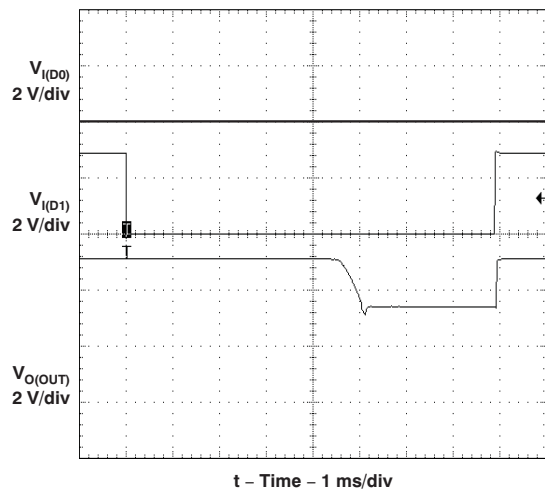
TERMINAL		I/O	DESCRIPTION
NAME	NO.		
D0	1	I	TTL- and CMOS-compatible input pins. Each pin has a 1- μ A pull-up. The Truth Table illustrates the functionality of D0 and D1.
D1	2	I	
GND	5	Power	Ground
IN1	8	I	Primary power switch input. The IN1 switch can be enabled only if the IN1 supply is above the UVLO threshold and at least one supply exceeds the internal V_{DD} UVLO.
IN2	6	I	Secondary power switch input. The IN2 switch can be enabled only if the IN2 supply is above the UVLO threshold and at least one supply exceeds the internal V_{DD} UVLO.
ILIM	4	I	A resistor (R_{ILIM}) from ILIM to GND sets the current limit I_L to $250/R_{ILIM}$ and $500/R_{ILIM}$ for the TPS2110A and TPS2111A, respectively.
OUT	7	O	Power switch output
VSNS	3	I	In the auto-switching mode ($D0 = 1$, $D1 = 0$), an internal power FET connects OUT to IN1 if the VSNS voltage is greater than 0.8 V. Otherwise, the FET connects OUT to the higher of IN1 and IN2. The Truth Table illustrates the functionality of VSNS.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

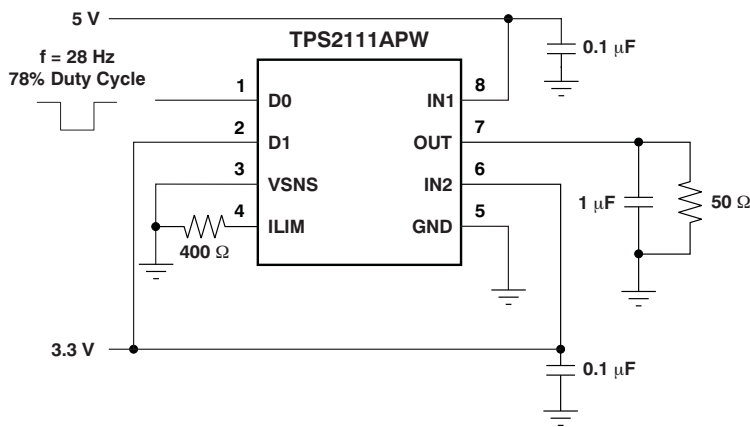
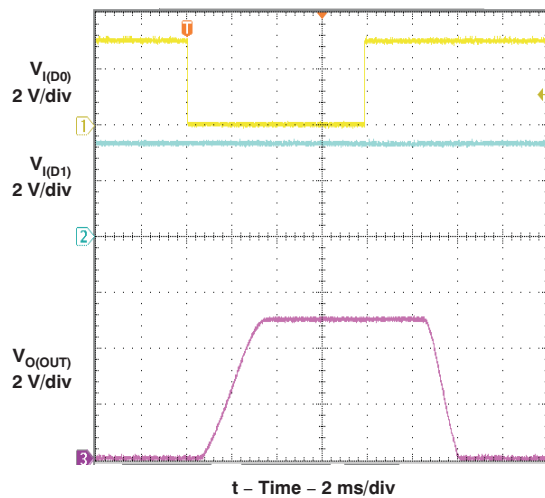
OUTPUT SWITCHOVER RESPONSE



Output Switchover Response Test Circuit

Figure 2.

OUTPUT TURN-ON RESPONSE

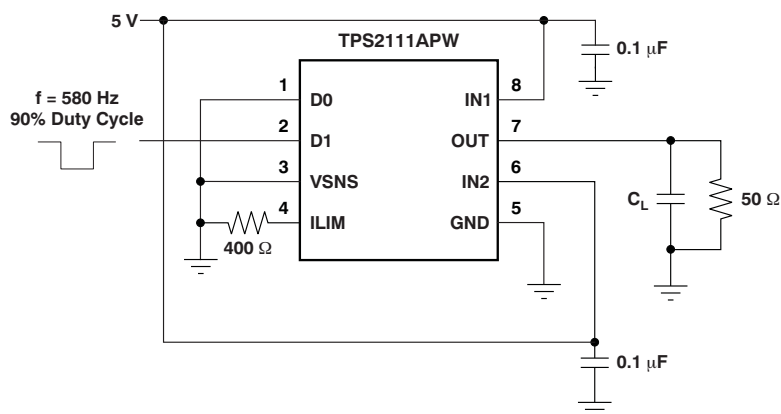
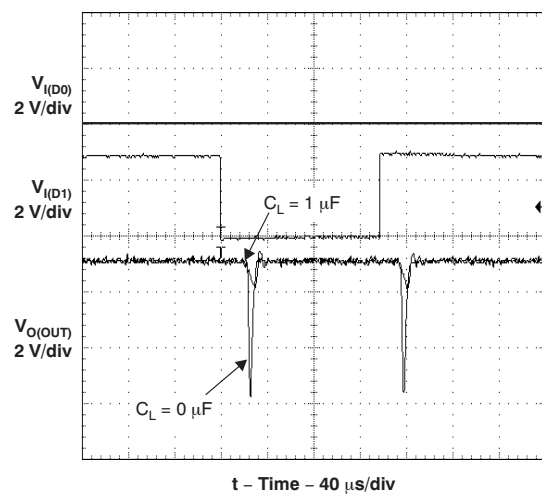


Output Turn-On Response Test Circuit

Figure 3.

TYPICAL CHARACTERISTICS (continued)

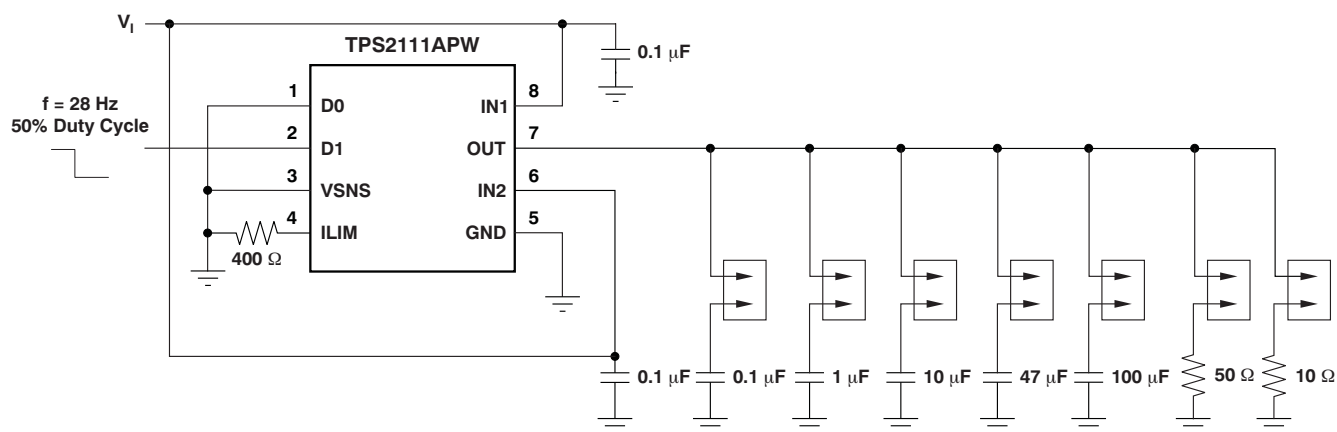
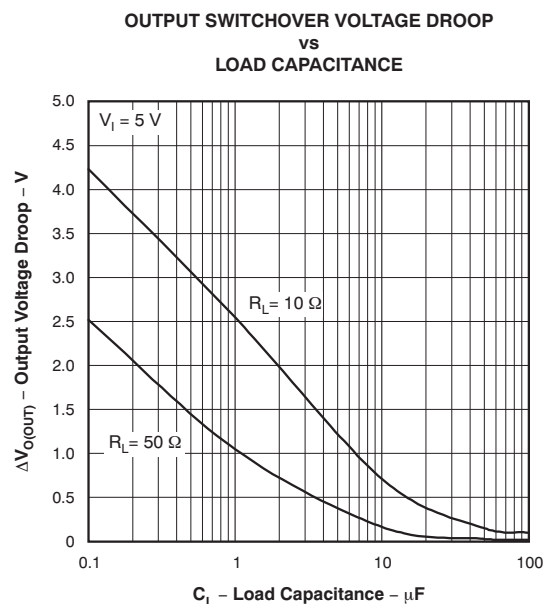
OUTPUT SWITCHOVER VOLTAGE DROOP



Output Switchover Voltage Droop Test Circuit

Figure 4.

TYPICAL CHARACTERISTICS (continued)

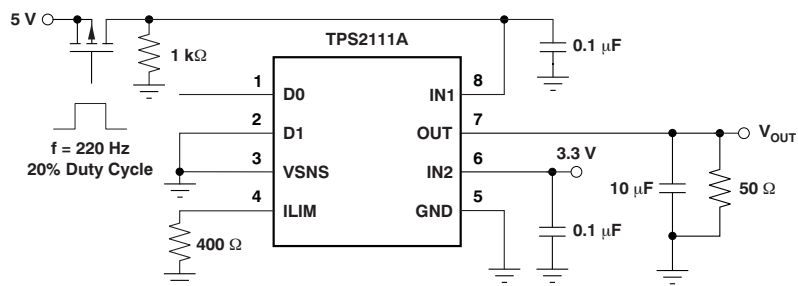
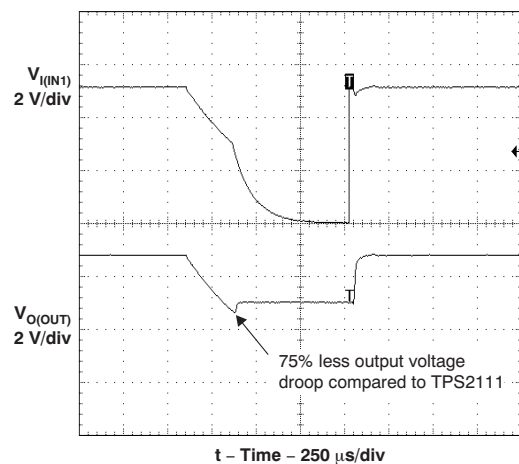


Output Swicthover Voltage Droop Test Circuit

Figure 5.

TYPICAL CHARACTERISTICS (continued)

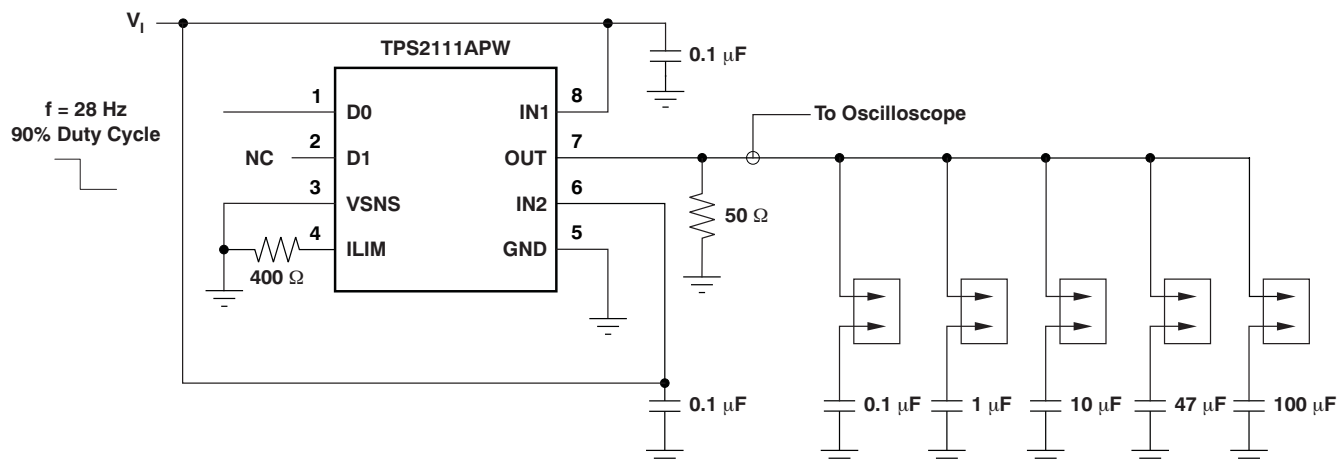
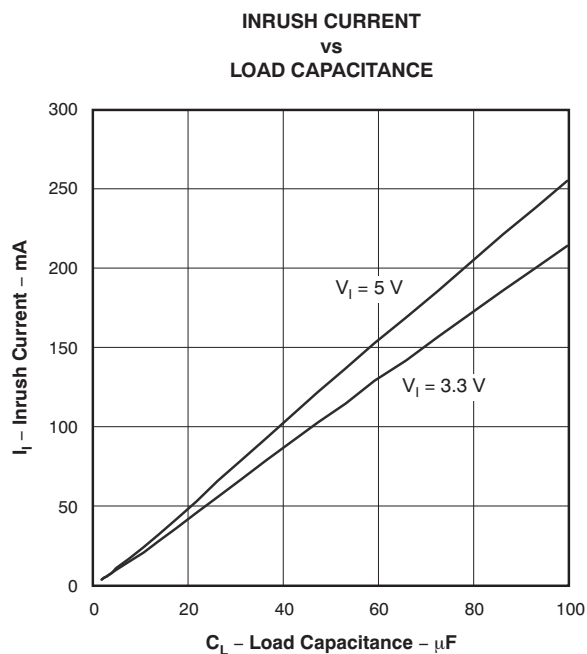
AUTO SWITCHOVER VOLTAGE DROOP



Auto Switchover Voltage Droop Test Circuit

Figure 6.

TYPICAL CHARACTERISTICS (continued)



Output Capacitor Inrush Current Test Circuit

Figure 7.

TYPICAL CHARACTERISTICS (continued)

SWITCH ON-RESISTANCE
vs
JUNCTION TEMPERATURE

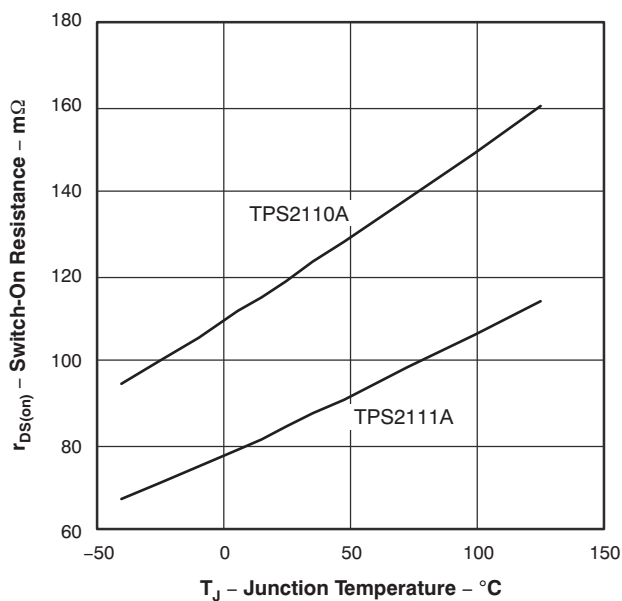


Figure 8.

SWITCH ON-RESISTANCE
vs
SUPPLY VOLTAGE

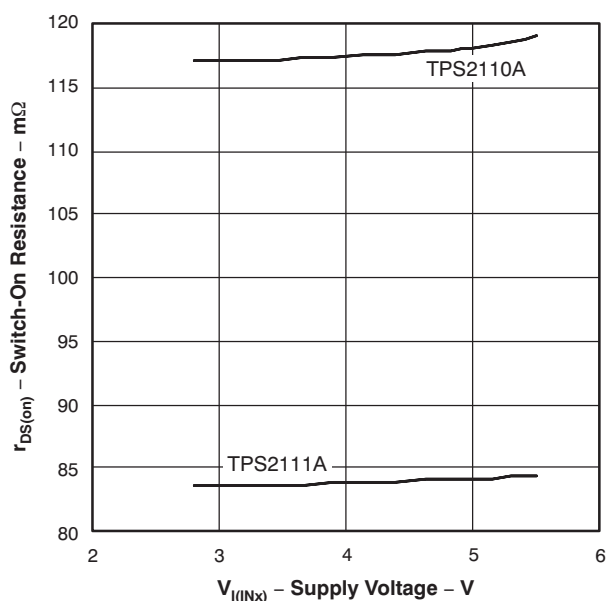


Figure 9.

IN1 SUPPLY CURRENT
vs
SUPPLY VOLTAGE

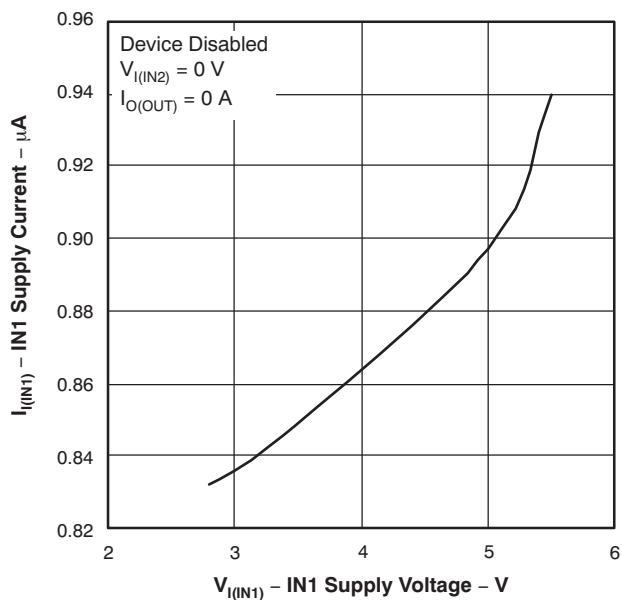


Figure 10.

IN1 SUPPLY CURRENT
vs
SUPPLY VOLTAGE

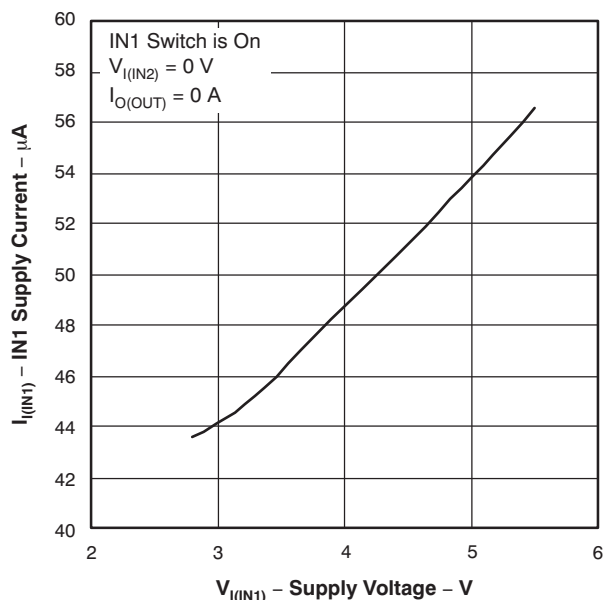


Figure 11.

TYPICAL CHARACTERISTICS (continued)

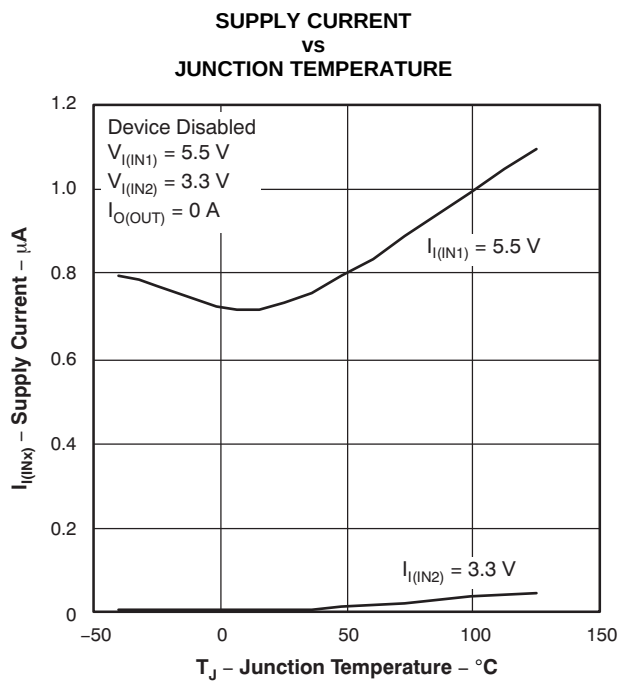


Figure 12.

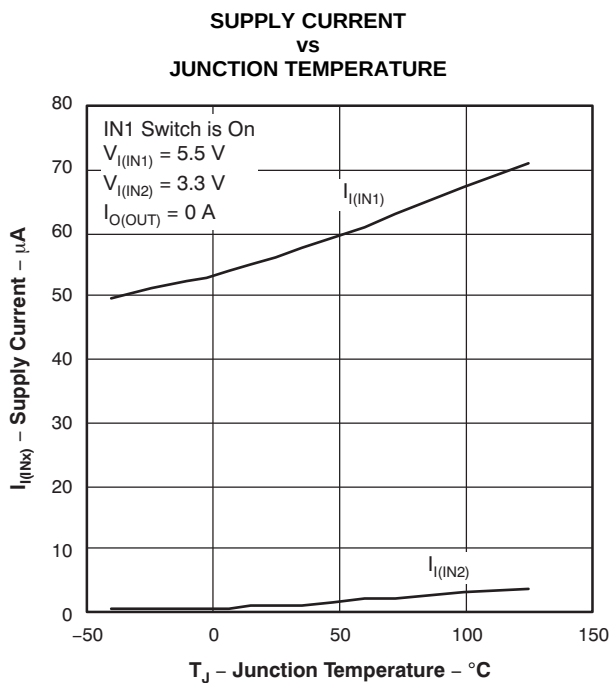


Figure 13.

APPLICATION INFORMATION

Some applications have two energy sources, one of which should be used in preference to another. [Figure 14](#) shows a circuit that will connect IN1 to OUT until the voltage at IN1 falls below a user-specified value. Once the voltage on IN1 falls below this value, the TPS211xA will select the higher of the two supplies. This usually means that the TPS211xA will swap to IN2.

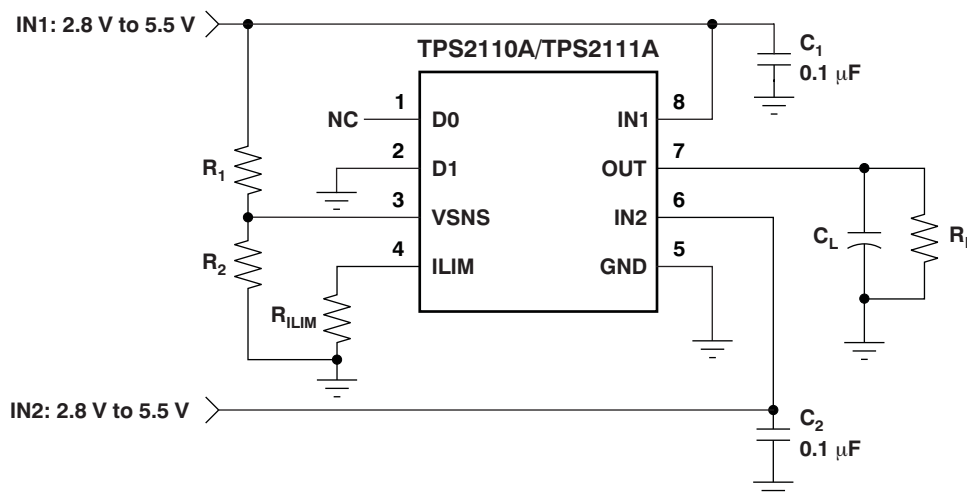


Figure 14. Auto-Selecting for a Dual Power-Supply Application

In [Figure 15](#), the multiplexer selects between two power supplies based upon the EN1 logic signal. OUT connects to IN1 if EN1 is logic '1'; otherwise, OUT connects to IN2. The logic thresholds for the D1 terminal are compatible with both TTL and CMOS logic.

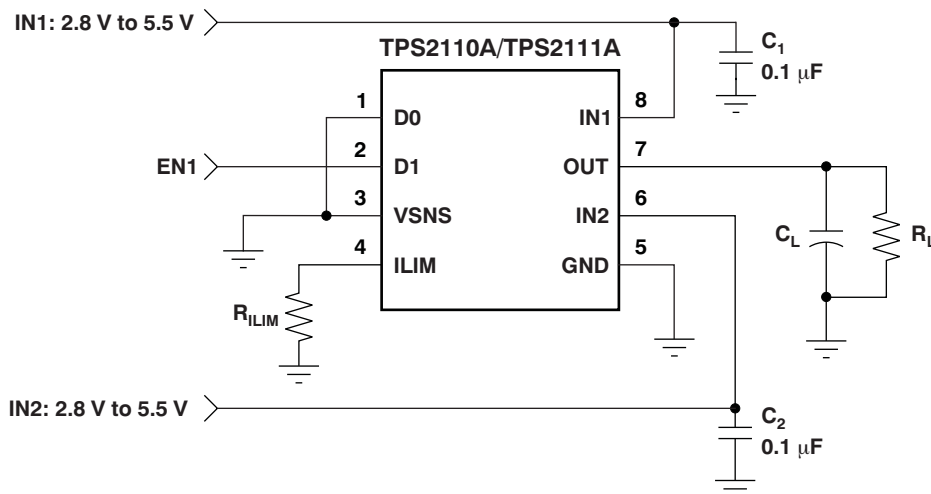


Figure 15. Manually Switching Power Sources

DETAILED DESCRIPTION

AUTO-SWITCHING MODE

D0 equal to logic '1' and D1 equal to logic '0' selects the auto-switching mode. In this mode, OUT connects to IN1 if $V_{I(VSNS)}$ is greater than 0.8 V; otherwise, OUT connects to the higher of IN1 and IN2.

The VSNS terminal includes hysteresis equal to 3.75% to 7.5% of the threshold selected for transition from the primary supply to the higher of the two supplies. This hysteresis helps avoid repeated switching from one supply to the other due to resistive drops.

MANUAL SWITCHING MODE

D0 equal to logic '0' selects the manual-switching mode. In this mode, OUT connects to IN1 if D1 is equal to logic '1'; otherwise, OUT connects to IN2.

N-CHANNEL MOSFETs

Two internal high-side power MOSFETs implement a single-pole double-throw (SPDT) switch. Digital logic selects the IN1 switch, IN2 switch, or no switch (Hi-Z state). The MOSFETs have no parallel diodes so output-to-input current cannot flow when the FET is off. An integrated comparator prevents turn-on of a FET switch if the output voltage is greater than the input voltage.

CROSS-CONDUCTION BLOCKING

The switching circuitry ensures that both power switches will never conduct at the same time. A comparator monitors the gate-to-source voltage of each power FET and allows a FET to turn on only if the gate-to-source voltage of the other FET is below the turn-on threshold voltage.

REVERSE-CONDUCTION BLOCKING

When the TPS211xA switches from a higher-voltage supply to a lower-voltage supply, current can potentially flow back from the load capacitor into the lower-voltage supply. To minimize such reverse conduction, the TPS211xA will not connect a supply to the output until the output voltage has fallen to within 100 mV of the supply voltage. Once a supply has been connected to the output, it will remain connected regardless of output voltage.

CHARGE PUMP

The higher of supplies IN1 and IN2 powers the internal charge pump. The charge pump provides power to the current limit amplifier and allows the output FET gate voltage to be higher than the IN1 and IN2 supply voltages. A gate voltage that is higher than the source voltage is necessary to turn on the N-channel FET.

CURRENT LIMITING

A resistor R_{ILIM} from ILIM to GND sets the current limit to $250/R_{ILIM}$ and $500/R_{ILIM}$ for the TPS2110A and TPS2111A, respectively. Setting resistor R_{ILIM} equal to zero is not recommended as that disables current limiting.

OUTPUT VOLTAGE SLEW-RATE CONTROL

The TPS211xA slews the output voltage at a slow rate when OUT switches to IN1 or IN2 from the Hi-Z state (see the [Truth Table](#)). A slow slew rate limits the inrush current into the load capacitor. High inrush currents can glitch the voltage bus and cause a system to hang up or reset. It can also cause reliability issues—like pit the connector power contacts, when hot-plugging a load such as a PCI card. The TPS211xA slews the output voltage at a much faster rate when OUT switches between IN1 and IN2. The fast rate minimizes the output voltage droop and reduces the output voltage hold-up capacitance requirement.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (March, 2004) to Revision A	Page
• Updated document to current format	1
• Deleted package information from <i>Available Options</i> table	2
• Revised <i>Ordering Information</i> table	2
• Deleted <i>lead temperature</i> and <i>storage temperature</i> specifications from, added <i>electrostatic discharge</i> specifications to Absolute Maximum Ratings table; changed <i>operating virtual junction temperature</i> specification; deleted <i>ESD Protection</i> table	2
• Updated conditions for <i>Electrical Characteristics</i>	3
• Deleted footnote 1 for <i>Electrical Characteristics</i> table	3
• Deleted footnote 1 for <i>Switching Characteristics</i> table	5

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS2110APW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2110A	Samples
TPS2110APWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2110A	Samples
TPS2110APWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2110A	Samples
TPS2111APW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2111A	Samples
TPS2111APWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2111A	Samples
TPS2111APWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2111A	Samples
TPS2111APWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	2111A	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

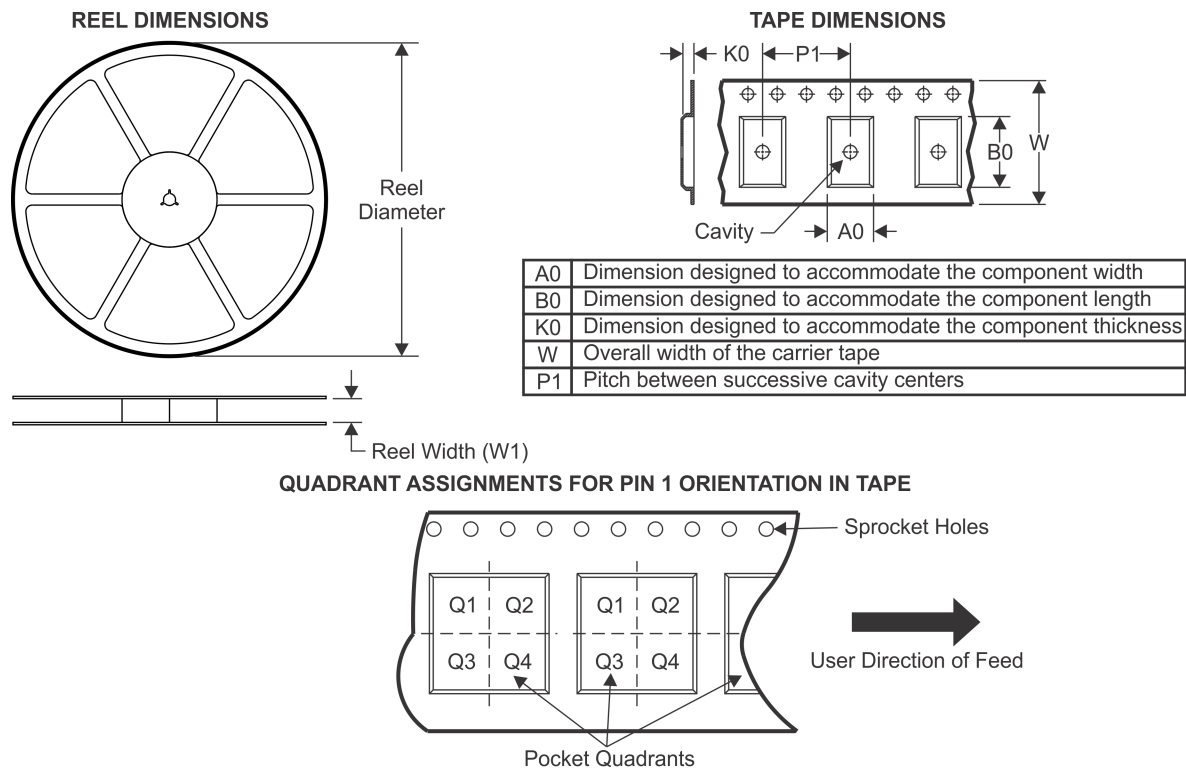
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

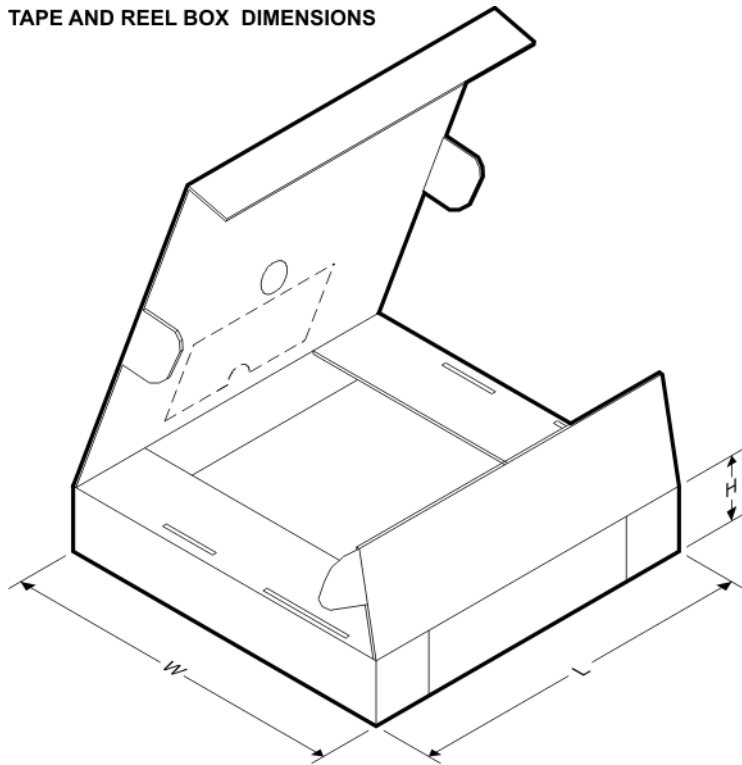
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2110APWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TPS2111APWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2110APWR	TSSOP	PW	8	2000	367.0	367.0	45.0
TPS2111APWR	TSSOP	PW	8	2000	367.0	367.0	35.0

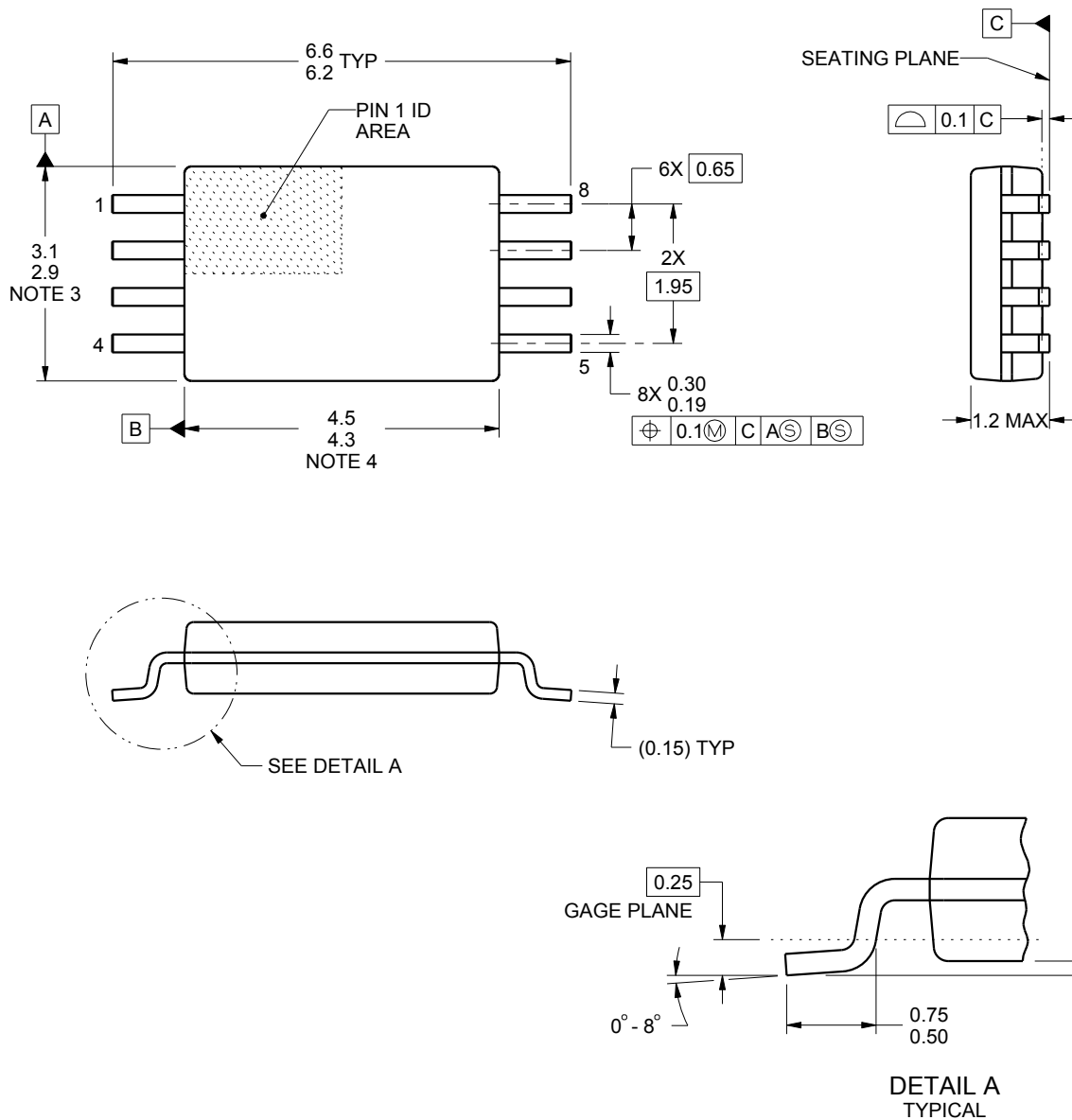
PW0008A



PACKAGE OUTLINE

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4221848/A 02/2015

NOTES:

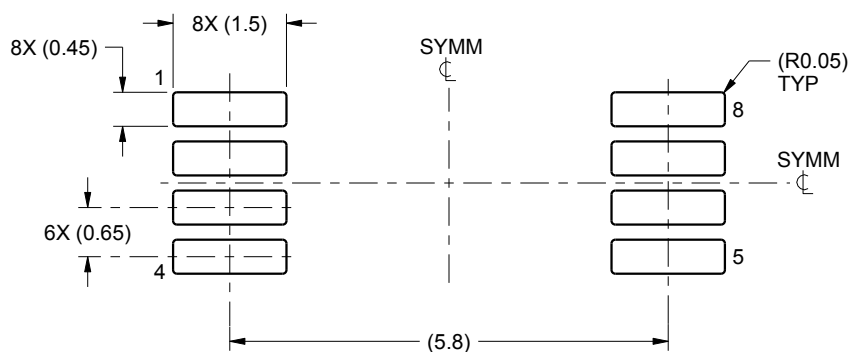
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

EXAMPLE BOARD LAYOUT

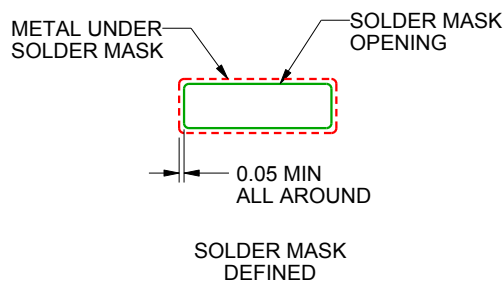
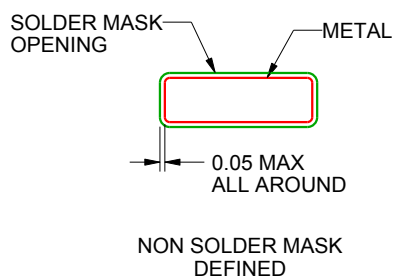
PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

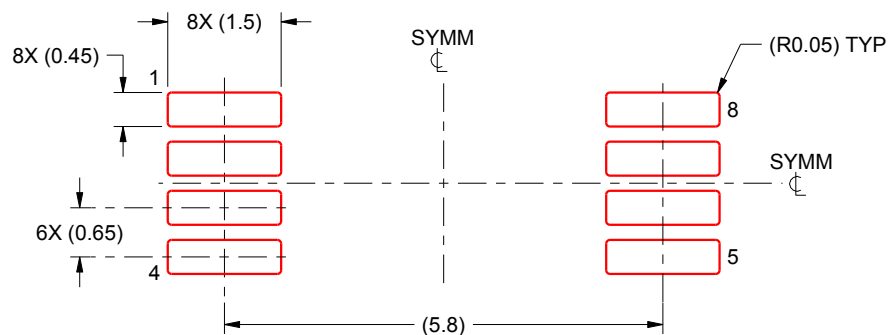
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0008A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com