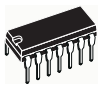
TS924

Rail-to-rail High Output Current Quad Operational Amplifier

- Rail-to-rail input and output
- Low noise: 9nV/√Hz
- Low distortion
- High output current: 80mA (able to drive 32Ω loads)
- High-speed: 4MHz, 1.3V/µs
- Operating from 2.7V to 12V
- Low input offset voltage: 900µV max (TS924A)
- ESD Internal protection: 3kV
- Latch-up immunity
- Macromodel included in this specification



N
DIP14
(Plastic Package)

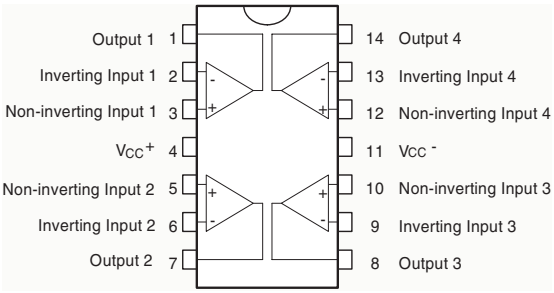


D
SO-14
(Plastic Micropackage)



P
TSSOP14
(Thin Shrink Small Outline Package)

Pin connection (top view)



Description

The TS924 is a rail-to-rail quad BiCMOS operational amplifier optimized and fully specified for 3V and 5V operation.

High output current allows low load impedances to be driven.

The TS924 exhibits a very low noise, low distortion, low offset and high output current capability making this device an excellent choice for high quality, low voltage or battery operated audio systems.

The device is stable for capacitive loads up to 500pF.

Applications

- Headphone amplifier
- Piezoelectric speaker driver
- Sound cards
- MPEG boards, multimedia systems,...
- Line driver, buffer
- Cordless telephones and portable communication equipment
- Instrumentation with low noise as key factor

Order Codes

Part Number	Temperature Range	Package	Packaging	Marking
TS924IN	-40°C, +125°C	DIP14	Tube	TS924IN
TS924AIN				TS924AIN
TS924ID/IDT		SO-14	Tube or Tape & Reel	924I
TS924AID/AIDT				924AI
TS924IPT		TSSOP14 (Thin Shrink Outline Package)	Tape & Reel	924I
TS924AIPT				924AI
TS924IYD/IYDT		SO-14 (automotive grade level)	Tube or Tape & Reel	924IY
TS924AIYD/AIYDT				924AIY
TS924IYPT		TSSOP14 (automotive grade level)	Tape & Reel	924IY
TS924IAIYPT				924AIY

1 Absolute Maximum Ratings

Table 1. Key parameters and their absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage (1)	14	V
Vid	Differential Input Voltage (2)	±1	V
V_i	Input Voltage (3)	V_{DD} -0.3 to V_{CC}+0.3	V
T_{stg}	Storage Temperature	-65 to +150	°C
T_j	Maximum Junction Temperature	150	°C
R_{thja}	Thermal Resistance Junction to Ambient DIP14	103	°C/W
	SO14	66	
	TSSOP14	100	
ESD	HBM: Human Body Model(4)	3	kV
	MM: Machine Model(5)	100	V
	CDM: Charged Device Model	1	kV
	Output Short Circuit Duration	see note(6)	
	Latch-up Immunity	200	mA
	Soldering Temperature (10sec), leaded version	250	°C
	Soldering Temperature (10sec), unleaded version	260	°C

1. All voltages values, except differential voltage are with respect to network ground terminal.
2. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal. If Vid > ±1V, the maximum input current must not exceed ±1mA. In this case (Vid > ±1V) an input serie resistor must be added to limit input current.
3. Do not exceed 14V.
4. Human body model, 100pF discharged through a 1.5kΩ resistor into pin of device.
5. Machine model ESD, a 200pF cap is charged to the specified voltage, then discharged directly into the IC with no external series resistor (internal resistor < 5Ω), into pin to pin of device.
6. There is no short-circuit protection inside the device: short-circuits from the output to V_{cc} can cause excessive heating. The maximum output current is approximately 80mA, independent of the magnitude of V_{cc}. Destructive dissipation can result from simultaneous short-circuits on all amplifiers.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	2.7 to 12	V
V_{icm}	Common Mode Input Voltage Range	V_{DD} -0.2 to V_{CC} +0.2	V
T_{oper}	Operating Free Air Temperature Range	-40 to +125	°C

2 Electrical Characteristics

Table 3. V_{CC} = +3V, V_{DD} = 0V, V_{icm} = V_{CC}/2, T_{amb} = 25°C, R_L connected to V_{CC}/2 (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input Offset Voltage - TS924 TS924A $T_{min.} \le T_{amb} \le T_{max.}$ - TS924 TS924A			3 0.9 5 1.8	mV
DV_{io}	Input Offset Voltage Drift		2		µV/°C
I_{io}	Input Offset Current Vout = Vcc/2		1	30	nA
I_{ib}	Input Bias Current Vout = Vcc/2		15	100	nA
V_{OH}	High Level Output Voltage R_L= 100k R_L = 600Ω R_L = 32Ω	2.90 2.87	 2.63		V
V_{OL}	Low Level Output Voltage R_L= 10k R_L = 600Ω R_L = 32Ω		 180	50 100	mV
A_{vd}	Large Signal Voltage Gain (V_{out} = 2Vpk-pk) R_L= 10k R_L = 600Ω R_L = 32Ω		200 35 16		V/mV
I_{cc}	Total Supply Current no load, V_{out} = $V_{cc/2}$		4.5	7	mA
GBP	Gain Bandwidth Product R_L = 600Ω		4		MHz
CMR	Common Mode Rejection Ratio	60	80		dB
SVR	Supply Voltage Rejection Ratio - V_{cc} = 2.7 to 3.3V	60	85		dB
I_o	Output Short Circuit Current	50	80		mA
SR	Slew Rate	0.7	1.3		V/µs
ϕm	Phase Margin at Unit Gain - R_L = 600Ω, C_L =100pF		68		Degrees
G_m	Gain Margin - R_L = 600Ω, C_L =100pF		12		dB
e_n	Equivalent Input Noise Voltage - f = 1kHz		9		$\frac{nV}{\sqrt{Hz}}$
THD	Total Harmonic Distortion V_{out} = 2Vpk-pk, F = 1kHz, A_v = 1, R_L =600Ω		0.005		%
C_s	Channel Separation		120		dB

Table 4. V_{CC} = +5V, V_{DD} = 0V, V_{icm} = V_{CC}/2, T_{amb} = 25°C, R_L connected to V_{CC}/2 (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{io}	Input Offset Voltage - TS924 TS924A $T_{min.} \le T_{amb} \le T_{max.}$ - TS924 TS924A			3 0.9 5 1.8	mV
DV_{io}	Input Offset Voltage Drift		2		µV/°C
I_{io}	Input Offset Current Vout = Vcc/2		1	30	nA
I_{ib}	Input Bias Current Vout = Vcc/2		15	100	nA
V_{OH}	High Level Output Voltage R_L= 100k R_L = 600Ω R_L = 32Ω	4.90 4.85	 4.4		V
V_{OL}	Low Level Output Voltage R_L= 10k R_L = 600Ω R_L = 32Ω		 300	50 120	mV
A_{vd}	Large Signal Voltage Gain (V_{out} = 2Vpk-pk) R_L= 10k R_L = 600Ω R_L = 32Ω		200 40 17		V/mV
I_{cc}	Total Supply Current no load, V_{out} = $V_{cc/2}$		4.5	7	mA
GBP	Gain Bandwidth Product R_L = 600Ω		4		MHz
CMR	Common Mode Rejection Ratio	60	80		dB
SVR	Supply Voltage Rejection Ratio V_{cc} = 3V to 5V	60	85		dB
I_o	Output Short Circuit Current	50	80		mA
SR	Slew Rate	0.7	1.3		V/µs
ϕm	Phase Margin at Unit Gain R_L = 600Ω, C_L =100pF		68		Degrees
G_m	Gain Margin R_L = 600Ω, C_L =100pF		12		dB
e_n	Equivalent Input Noise Voltage f = 1kHz		9		$\frac{nV}{\sqrt{Hz}}$
THD	Total Harmonic Distortion V_{out} = 2Vpk-pk, F = 1kHz, A_v = 1, R_L =600Ω		0.005		%
C_s	Channel Separation		120		dB

Figure 1. Output short circuit current vs. output voltage

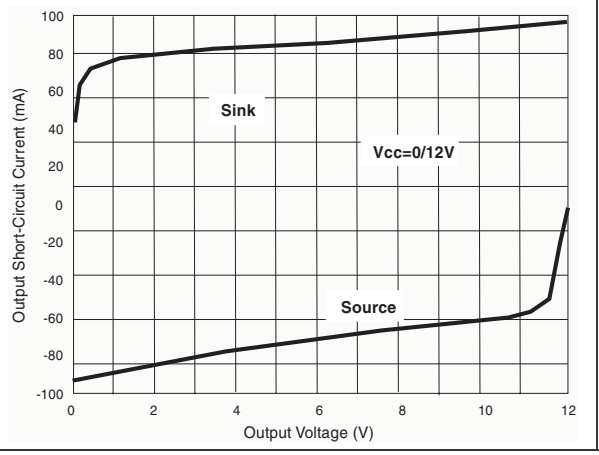


Figure 2. Output short circuit current vs. output voltage

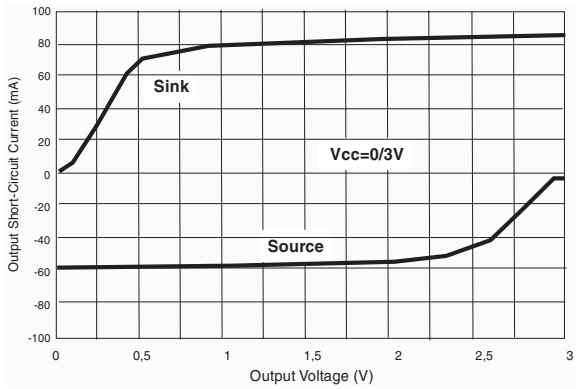


Figure 3. Voltage gain and phase vs. frequency

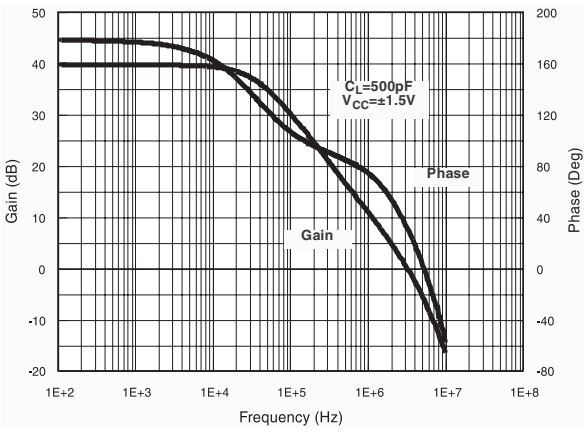


Figure 4. Output short circuit current vs. output voltage

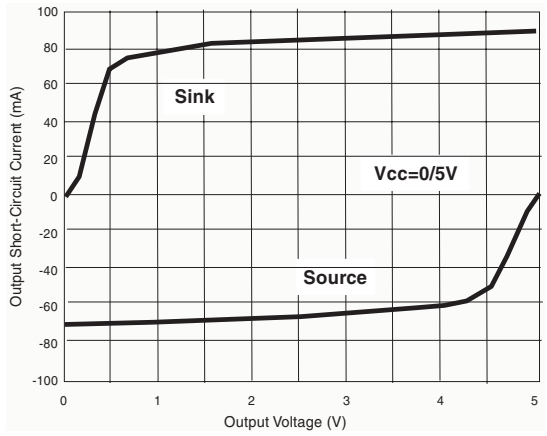


Figure 5. Voltage gain & phase vs. frequency

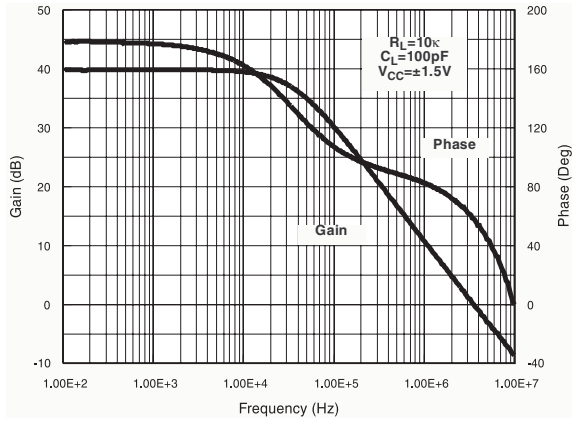


Figure 6. THD + noise vs. frequency

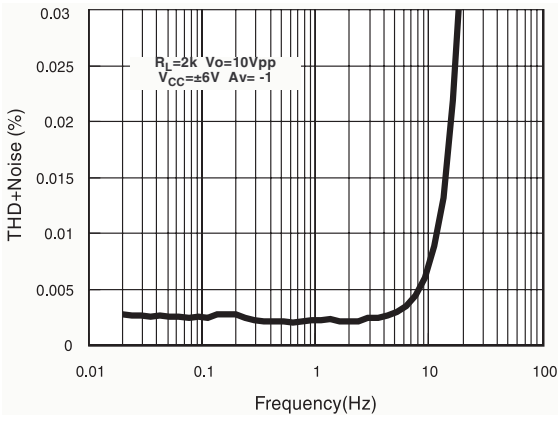


Figure 7. THD + noise vs. frequency

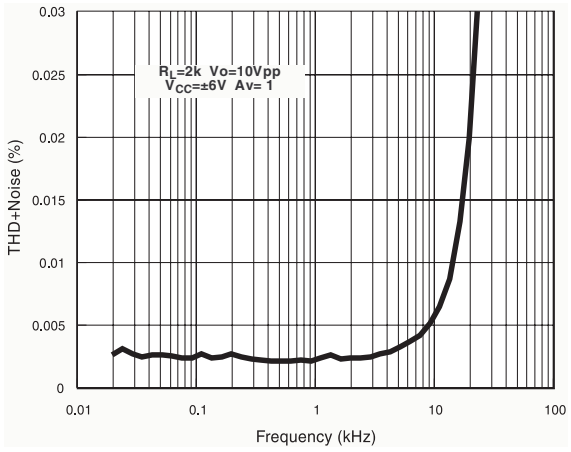


Figure 8. THD + noise vs. frequency

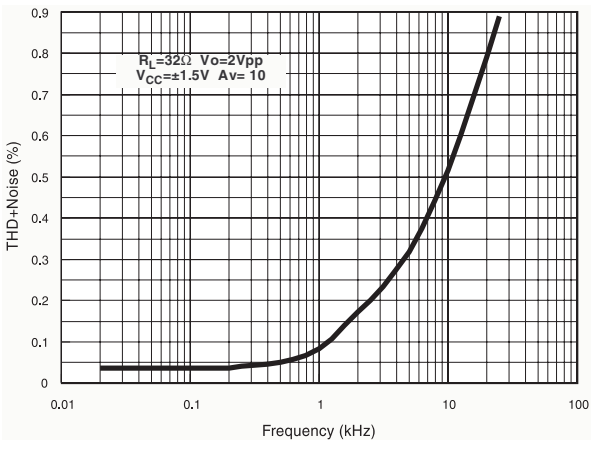


Figure 9. THD + noise vs. Vout

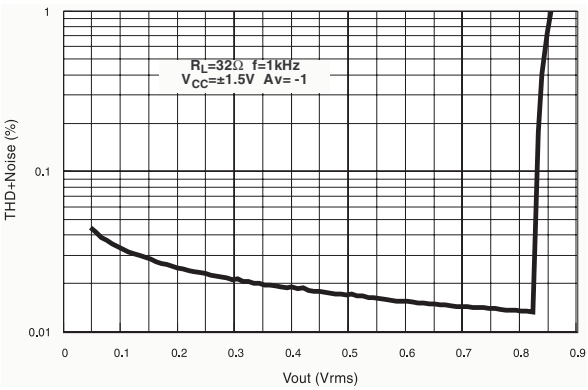


Figure 10. THD + noise vs. frequency

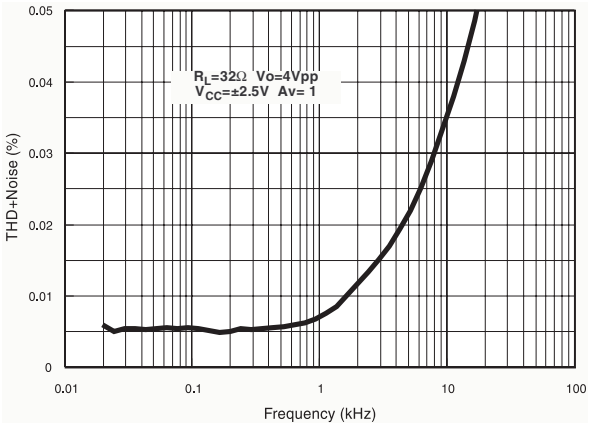


Figure 11. THD + noise vs. Vout

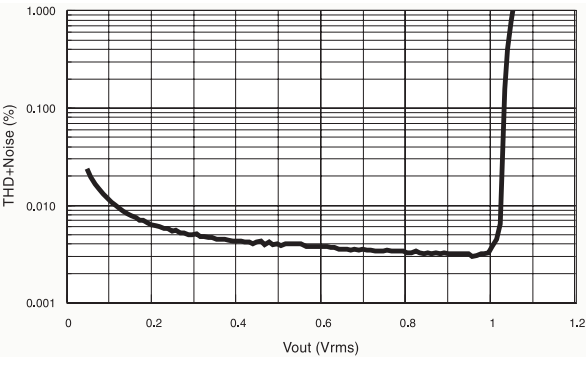
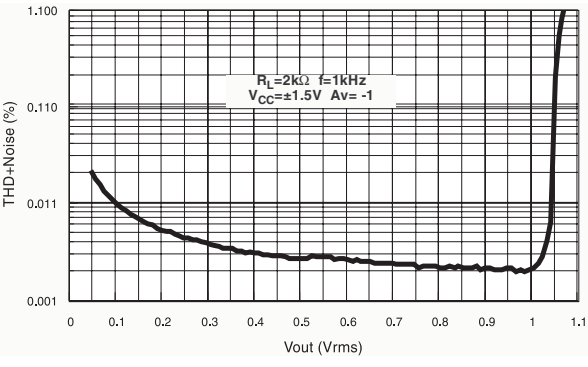


Figure 12. THD + noise vs. Vout



3 Macromodel

3.1 Important note concerning this macromodel

Please consider following remarks before using this macromodel.

- All models are a trade-off between accuracy and complexity (i.e. simulation time).
- Macromodels are not a substitute to breadboarding; rather, they confirm the validity of a design approach and help to select surrounding component values.
- A macromodel emulates the NOMINAL performance of a TYPICAL device within SPECIFIED OPERATING CONDITIONS (i.e. temperature, supply voltage, etc.). Thus the macromodel is often not as exhaustive as the datasheet, its goal is to illustrate the main parameters of the product.
- Data issued from macromodels used outside of its specified conditions (Vcc, Temperature, etc.) or even worse: outside of the device operating conditions (Vcc, Vicm, etc.) are not reliable in any way.

In *Section 3.3*, the electrical characteristics resulting from the use of these macromodels are presented.

3.2 Electrical characteristics from macromodelization

Table 5. Electrical characteristics resulting from macromodel simulation at V_{CC} = 3V, V_{DD} = 0V, R_L, C_L connected to $V_{CC/2}$, T_{amb} = 25°C (unless otherwise specified)

Symbol	Conditions	Value	Unit
V_{io}		0	mV
A_{vd}	R_L = 10kΩ	200	V/mV
I_{CC}	No load, per operator	1.2	mA
V_{icm}		-0.2 to 3.2	V
V_{OH}	R_L = 10kΩ	2.95	V
V_{OL}	R_L = 10kΩ	25	mV
I_{sink}	V_O = 3V	80	mA
I_{source}	V_O = 0V	80	mA
GBP	R_L = 600kΩ	4	MHz
SR	R_L = 10kΩ, C_L = 100pF	1	V/µs
ϕm	R_L = 600kΩ	68	Degrees

3.3 Macromodel code

```
** Standard Linear Ics Macromodels, 1996.
** CONNECTIONS:
* 1 INVERTING INPUT
* 2 NON-INVERTING INPUT
* 3 OUTPUT
* 4 POSITIVE POWER SUPPLY
* 5 NEGATIVE POWER SUPPLY

.SUBCKT TS92X 1 2 3 4 5
*
.MODEL MDTH D IS=1E-8 KF=2.664234E-16 CJO=10F
*
* INPUT STAGE
CIP 2 5 1.000000E-12
CIN 1 5 1.000000E-12
EIP 10 5 2 5 1
EIN 16 5 1 5 1
RIP 10 11 8.125000E+00
RIN 15 16 8.125000E+00
RIS 11 15 2.238465E+02
DIP 11 12 MDTH 400E-12
DIN 15 14 MDTH 400E-12
VOFP 12 13 DC 153.5u
VOFN 13 14 DC 0
IPOL 13 5 3.200000E-05
CPS 11 15 1e-9
DINN 17 13 MDTH 400E-12
VIN 17 5 -0.100000e+00
DINR 15 18 MDTH 400E-12
VIP 4 18 0.400000E+00
FCP 4 5 VOFP 1.865000E+02
FCN 5 4 VOFN 1.865000E+02
FIBP 2 5 VOFP 6.250000E-03
FIBN 5 1 VOFN 6.250000E-03
* GM1 STAGE ***************
FGM1P 119 5 VOFP 1.1
FGM1N 119 5 VOFN 1.1
RAP 119 4 2.6E+06
RAN 119 5 2.6E+06
* GM2 STAGE ***************
G2P 19 5 119 5 1.92E-02
G2N 19 5 119 4 1.92E-02
R2P 19 4 1E+07
R2N 19 5 1E+07
*************************
VINT1 500 0 5
GCONVP 500 501 119 4 19.38
VP 501 0 0
GCONVN 500 502 119 5 19.38
VN 502 0 0
```

```
********* orientation isink isource *******
VINT2 503 0 5
FCOPY 503 504 VOUT 1
DCOPYP 504 505 MDTH 400E-9
VCOPYP 505 0 0
DCOPYN 506 504 MDTH 400E-9
VCOPYN 0 506 0
**************************
F2PP 19 5 poly(2) VCOPYP VP 0 0 0 0 0.5
F2PN 19 5 poly(2) VCOPYP VN 0 0 0 0 0.5
F2NP 19 5 poly(2) VCOPYN VP 0 0 0 0 1.75
F2NN 19 5 poly(2) VCOPYN VN 0 0 0 0 1.75
* COMPENSATION ************
CC 19 119 25p
* OUTPUT ***********
DOPM 19 22 MDTH 400E-12
DONM 21 19 MDTH 400E-12
HOPM 22 28 VOUT 6.250000E+02
VIPM 28 4 5.000000E+01
HONM 21 27 VOUT 6.250000E+02
VINM 5 27 5.000000E+01
VOUT 3 23 0
ROUT 23 19 6
COUT 3 5 1.300000E-10
DOP 19 25 MDTH 400E-12
VOP 4 25 1.052
DON 24 19 MDTH 400E-12
VON 24 5 1.052
.ENDS ;TS92X
```

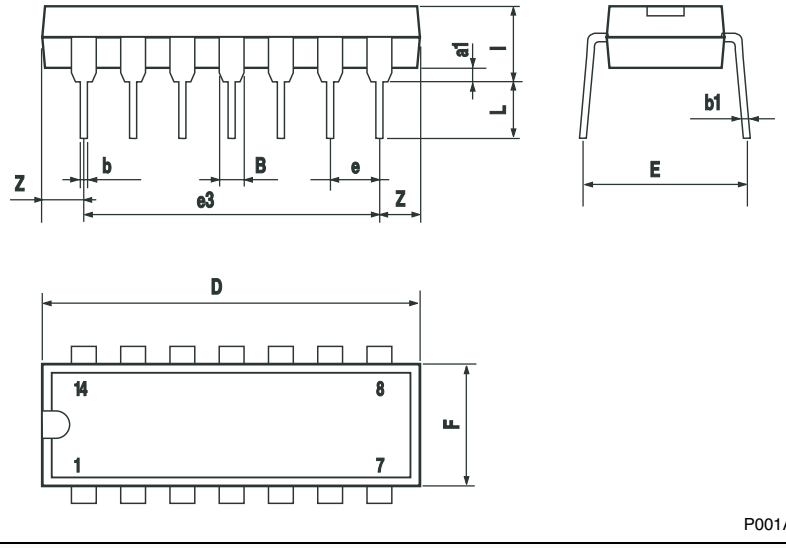
4 Package Mechanical Data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

4.1 DIP14 Package

Plastic DIP-14 MECHANICAL DATA

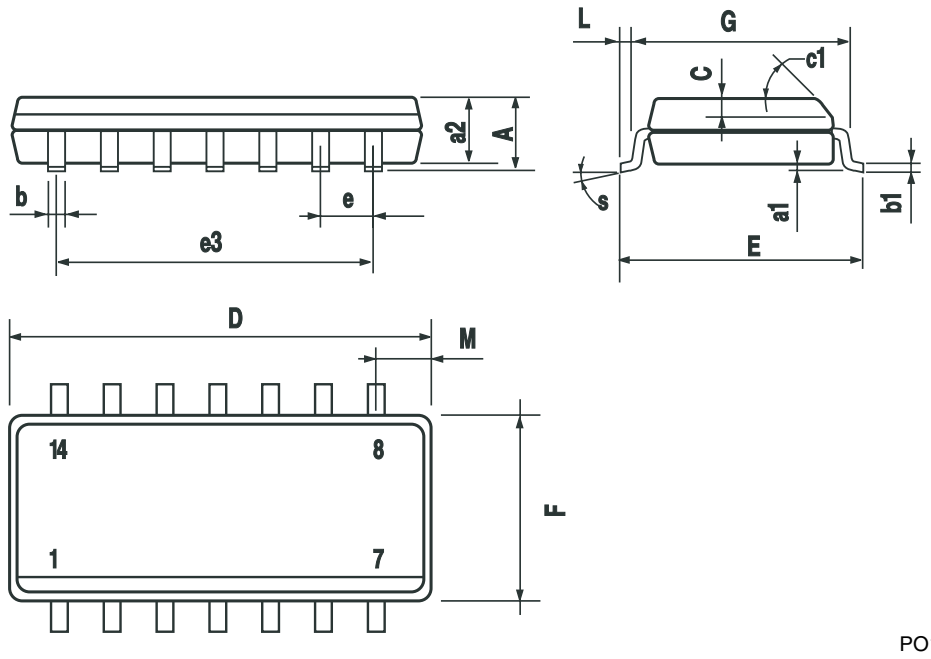
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	1.39		1.65	0.055		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		15.24			0.600	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z	1.27		2.54	0.050		0.100



4.2 SO-14 package

SO-14 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.68			0.026
S	8° (max.)					

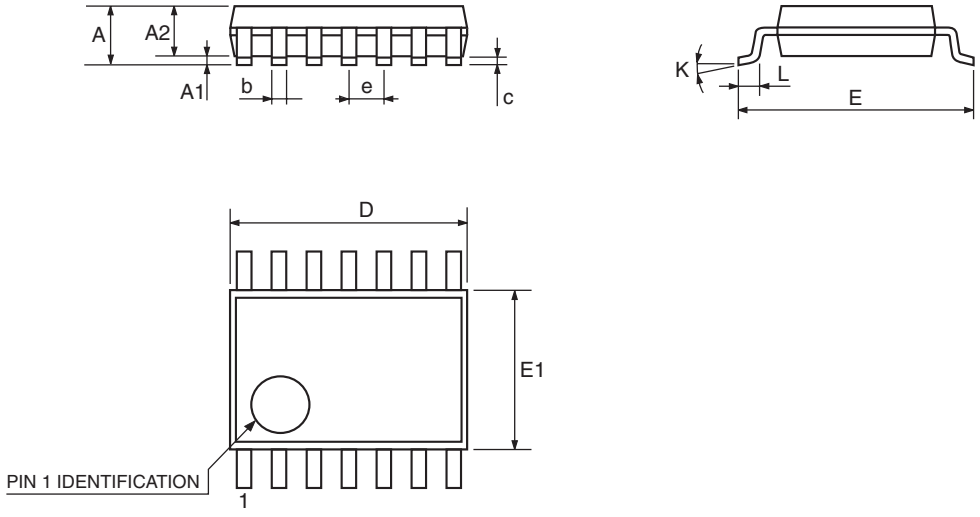


PO13G

4.3 TSSOP14 package

TSSOP14 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030



5 Revision History

Date	Revision	Changes
May 2001	1	First Release
May 2005	2	Modifications on AMR *Table 1 on page 3* (explanation of Vid and Vi limits, ESD MM and CDM values added, Rthja added)
July 2005	3	PPAP references inserted in the datasheet see *Table on page 2*.
Nov. 2005	4	– Package mechanical data modified – TS924IYPT/TS924AYIPT PPAP reference inserted in *Table on page 2*. – Macromodel modified

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