MP2224

High-Efficiency, 4A, 18V, 500kHz Synchronous Step-Down Converter

The Future of Analog IC Technology

DESCRIPTION

The MP2224 is a high-efficiency, synchronous, rectified, step-down, switch-mode converter with built-in power MOSFETs. It offers a very compact solution to achieve a 4A output current with excellent load and line regulation over a wide input supply range. The MP2224 has synchronous mode operation for higher efficiency over the output current load range.

Current-mode operation provides fast transient response and eases loop stabilization.

Full protection features include over-current protection and thermal shutdown.

The MP2224 requires a minimal number of readily available, standard, external components and is available in a space-saving 8-pin TSOT23 package.

FEATURES

- Wide 4.5V to 18V Operating Input Range
- Adjustable Output Voltage as low as 0.6V
- Low 70mΩ/25mΩ $R_{DS(ON)}$ of Internal Power MOSFETs
- High Efficiency up to 97%
- Fixed 500kHz Switching Frequency
- Synchronizes from a 200kHz to 2MHz External Clock
- 2.4ms Internal Soft-Start Time
- 1% Reference Accuracy at Room Temperature
- Internal Power-Save Mode
- OCP with Hiccup Mode
- Available in 8-pin TSOT23

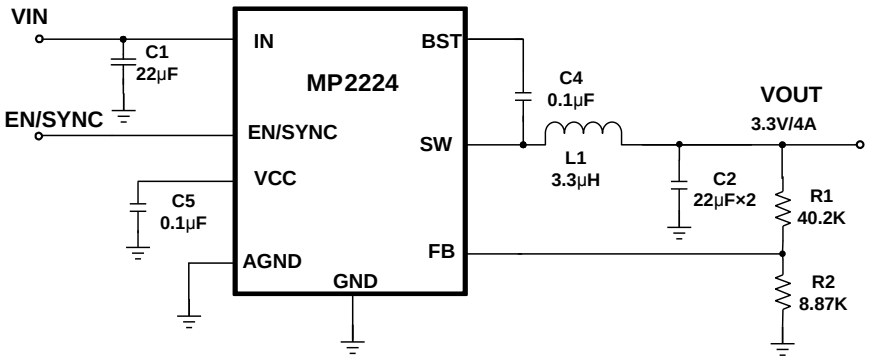
APPLICATIONS

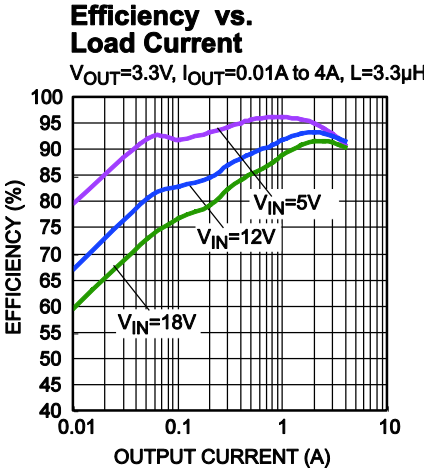
- Flat-Panel Television and Monitors
- Notebook Systems and I/O Power
- Digital Set-Top Boxes
- Distributed Power Systems

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance.

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TYPICAL APPLICATION





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ORDERING INFORMATION

Part Number*	Package	Top Marking
MP2224GJ	TSOT23-8	*See Below*

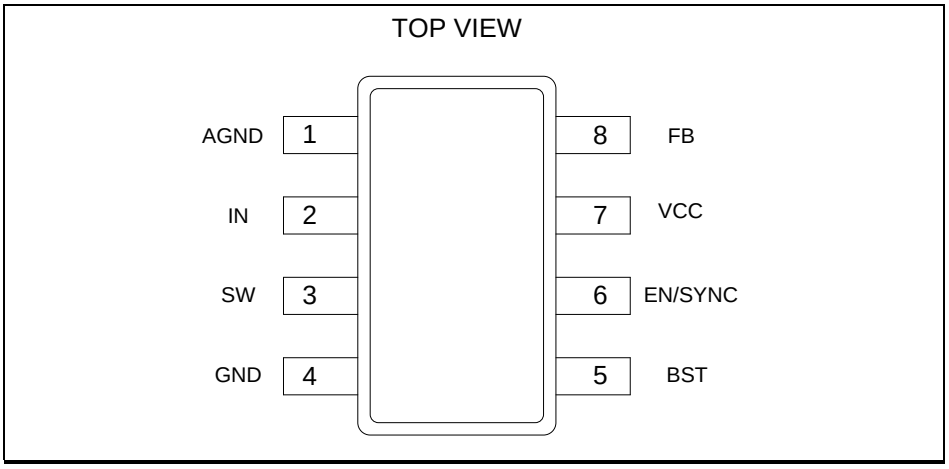
For Tape & Reel, add suffix –Z (e.g. MP2224GJ–Z)

TOP MARKING

|AULY

AUL: Product code of MP2224GJ
Y: Year code

PACKAGE REFERENCE



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ABSOLUTE MAXIMUM RATINGS (1)

V_{IN} …….. -0.3V to 20V
V_{SW}……..
-0.3V (-5V for <10ns) to V_{IN}+0.3V (23V for <10ns)
V_{BST} …….. V_{SW}+5.5V
All other pins……..-0.3V to 5.5V (2)
Continuous power dissipation (T_A = +25°C) (3)
TSOT23-8…….. .....1.25W
Junction temperature……..…150°C
Lead temperature……260°C
Storage temperature……-65°C to 150°C

Recommended Operating Conditions (4)

Supply voltage (V_{IN})…… 4.5V to 18V
Output voltage (V_{OUT})……...0.6V to min. of V_{IN} -1V and V_{IN} x Dmax
Operating junction temp. (T_J). .. -40°C to +125°C

Thermal Resistance (5) θ_{JA} θ_{JC}

TSOT23-8…….. ……..……..	100	55... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) For additional details on EN's ABS MAX rating, please refer to Page 11, the "Enable/SYNC Control" section.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_J = -40°C to +125°C(6), Typical value is tested at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (shutdown)	I_{IN}	V_{EN} = 0V,T_J = 25°C			1	μA
Supply current (shutdown)	I_{IN}	V_{EN} = 0V			3	μA
Supply current (quiescent)	I_Q	V_{EN} = 2V, V_{FB} = 0.7V		320	400	μA
HS switch-on resistance	HS_{RDS-ON}	V_{BST-SW} = 5V		70		mΩ
LS switch-on resistance	LS_{RDS-ON}	V_{CC} = 5V		25		mΩ
Switch leakage	SW_{LKG}	V_{EN} = 0V, V_{SW} = 12V, T_J = 25°C			1	μA
Current limit (7)	I_{LIMIT}	Under 40% duty cycle	5.5			A
Oscillator frequency	F_{SW}	V_{FB} = 0.48V	380	500	580	kHz
Foldback frequency	F_{FB}	V_{FB} < 300mV		0.56		F_{SW}
Maximum duty cycle	D_{MAX}	V_{FB} = 500mV	90	95		%
Minimum on time(8)	T_{ON_MIN}			50		ns
Sync frequency range	F_{SYNC}		0.2		2	MHz
Feedback voltage	V_{FB}	T_J = 25°C	594	600	606	mV
Feedback voltage	V_{FB}		591	600	609	mV
Feedback current	I_{FB}	V_{FB} = 620mV		10	50	nA
EN rising threshold	V_{EN_RISING}		1.15	1.4	1.65	V
EN hysteresis	$V_{EN\ HYS}$			160		mV
EN input current	I_{EN}	V_{EN} = 2V		1.85		μA
		V_{EN} = 0		0		μA
EN turn-off delay	EN_{td-off}		5	10		μs
VIN under-voltage lockout threshold-rising	$INUV_{Vth}$		3.85	4.1	4.35	V
VIN under-voltage lockout threshold-hysteresis	$INUV_{HYS}$			735		mV
Soft-start time	T_{SS}	10% to 90% output voltage		2.4		ms
Thermal shutdown (8)	T_{SD}			150		°C
Thermal hysteresis (8)	$T_{SD\ HYS}$			20		°C

Notes:

6) Not tested in production. Guaranteed by over-temperature correlation.
7) Guaranteed by engineering sample characterization.
8) Guaranteed by design.

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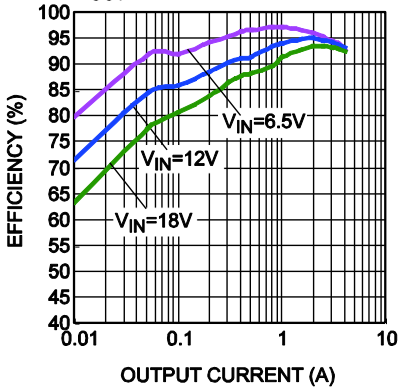
TYPICAL PERFORMANCE CHARACTERISTICS

Performance waveforms are tested on the evaluation board described in the Design Example section.

V_{IN} = 12V, V_{OUT} = 3.3V, T_A = 25°C, unless otherwise noted.

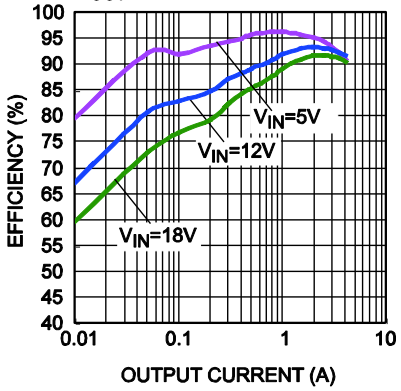
Efficiency vs. Load Current

V_{OUT}=5V, L=4.7µH



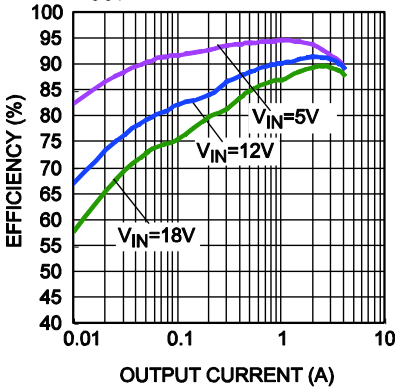
Efficiency vs. Load Current

V_{OUT}=3.3V, L=3.3µH



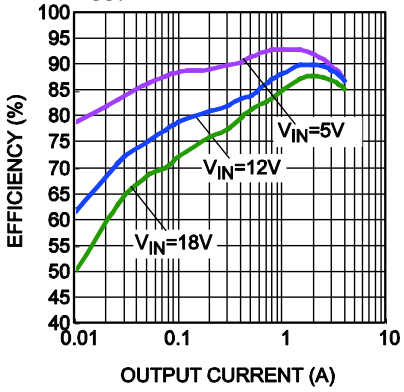
Efficiency vs. Load Current

V_{OUT}=2.5V, L=2.2µH



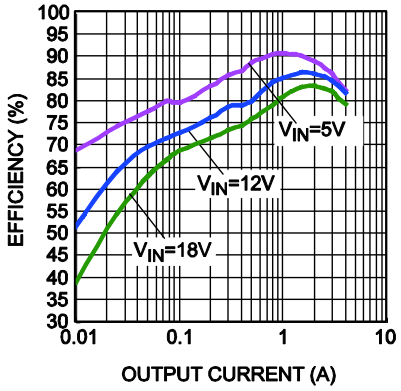
Efficiency vs. Load Current

V_{OUT}=1.8V, L=2.2µH

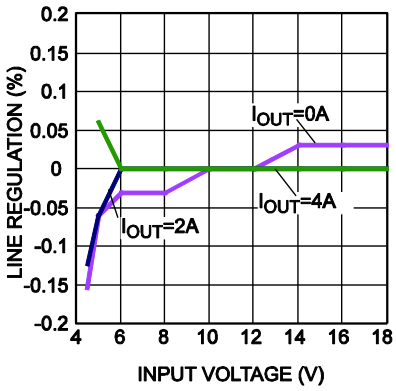


Efficiency vs. Load Current

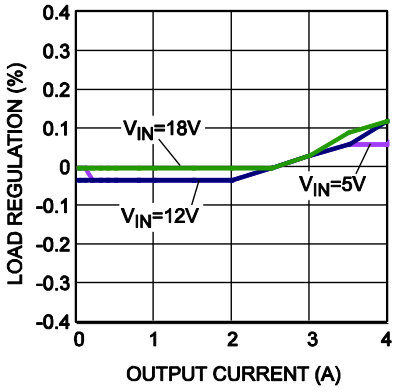
V_{OUT}=1V, L=1µH



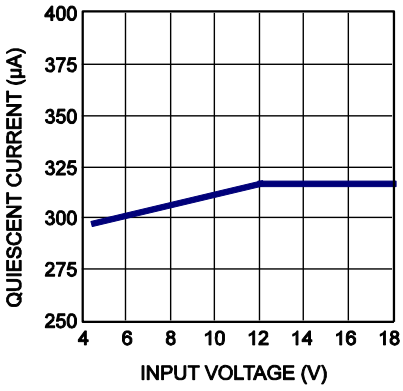
Line Regulation



Load Regulation

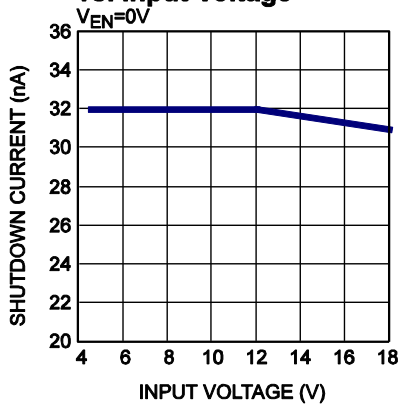


Quiescent Current vs. Input Voltage



Shutdown Current vs. Input Voltage

V_{EN}=0V



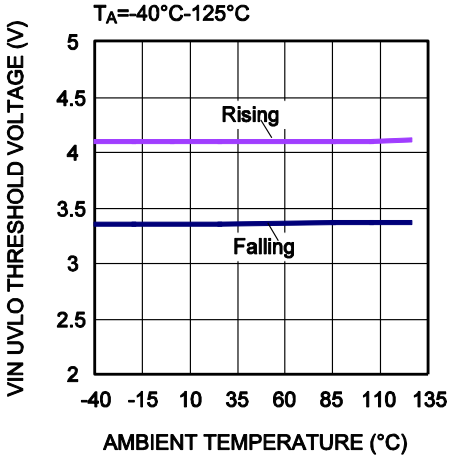
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

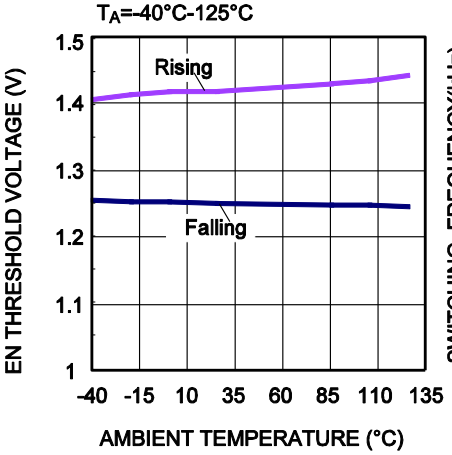
Performance waveforms are tested on the evaluation board described in the Design Example section.

V_{IN} = 12V, V_{OUT} = 3.3V, T_A = 25°C, unless otherwise noted.

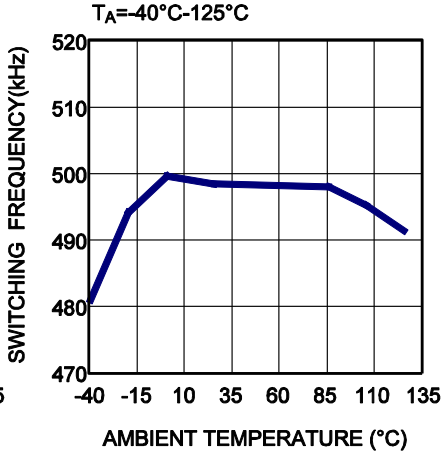
V_{IN} UVLO vs. Temperature



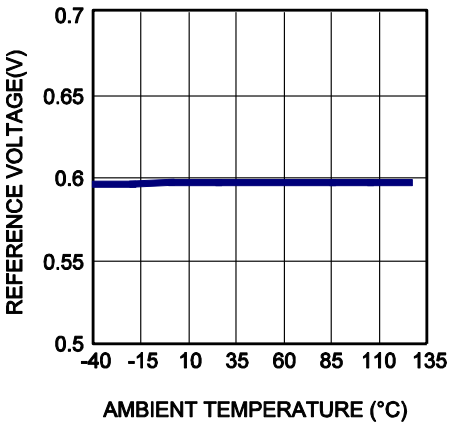
EN Threshold vs. Temperature



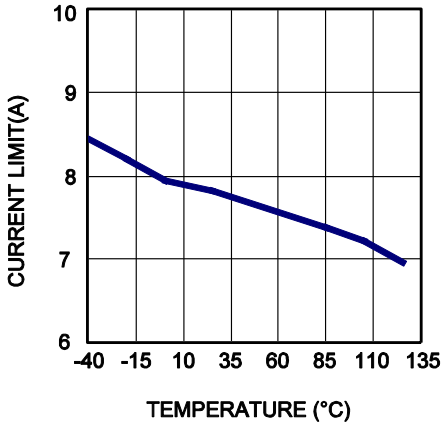
Switching Frequency vs. Ambient Temperature



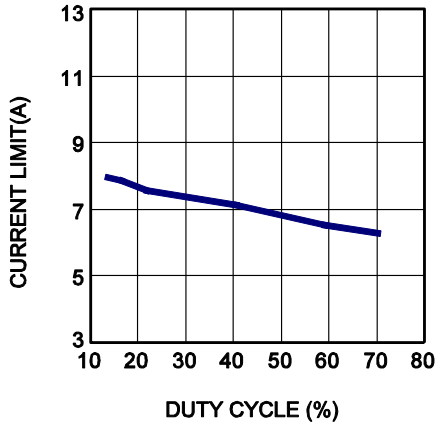
Reference Voltage vs. Temperature



Current Limit vs. Temperature



Current Limit vs. Duty Cycle



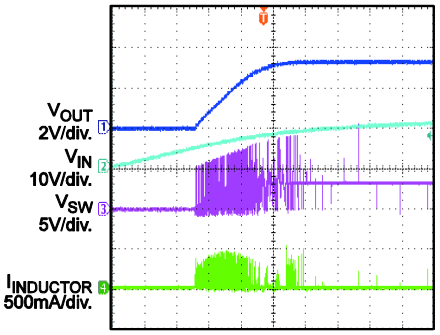
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

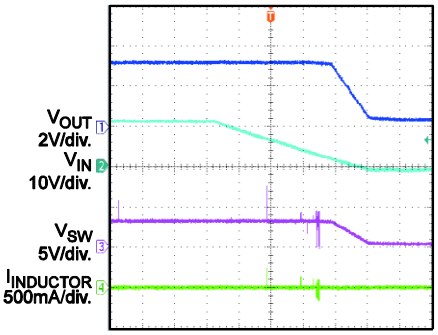
Performance waveforms are tested on the evaluation board described in the Design Example section.

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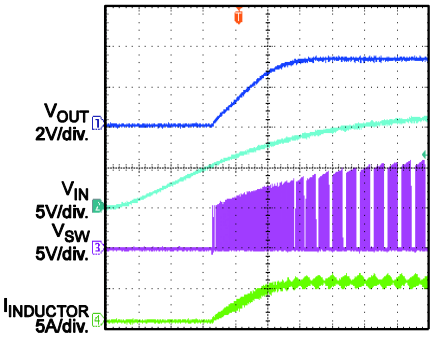
Start-Up through Input Voltage
I_{OUT}=0A



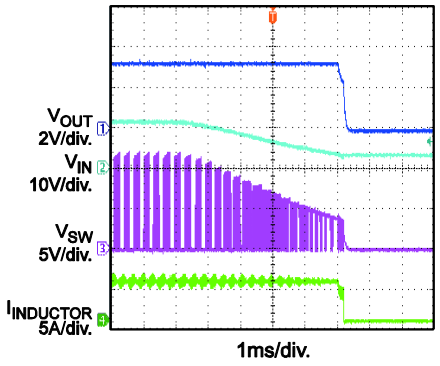
Shutdown through Input Voltage
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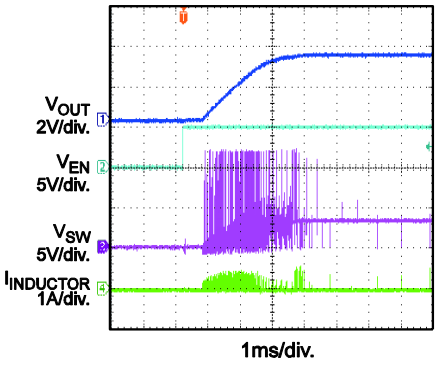
Start-Up through Input Voltage
I_{OUT}=4A



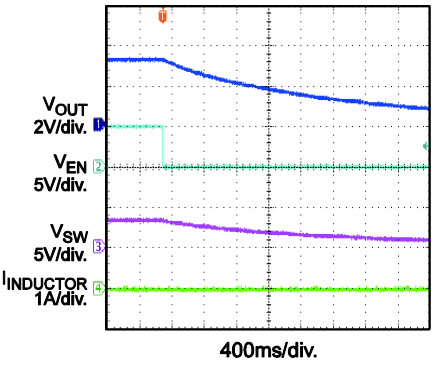
Shutdown through Input Voltage
I_{OUT}=4A



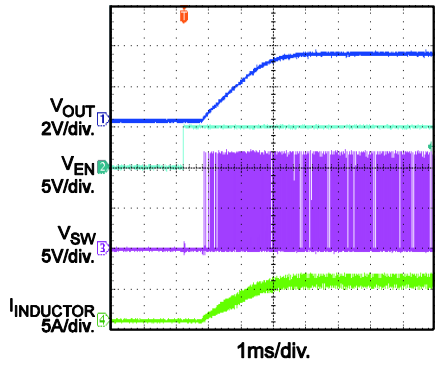
Start-Up through Enable
I_{OUT}=0A



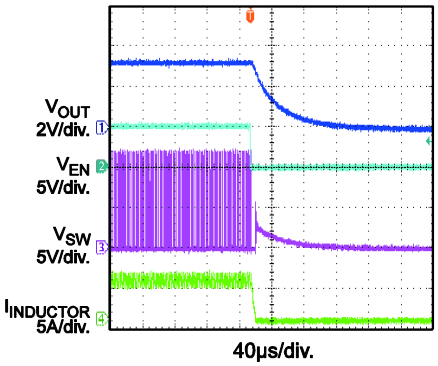
Shutdown through Enable
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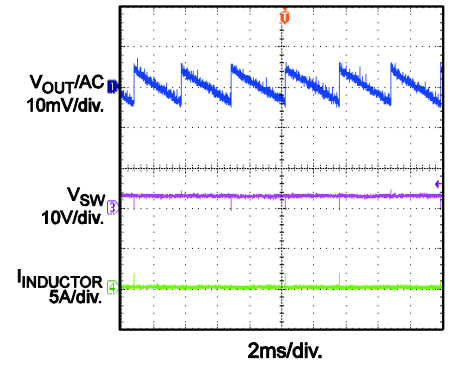
Start-Up through Enable
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Shutdown through Enable
I_{OUT}=4A



Output Ripple
I_{OUT}=0A



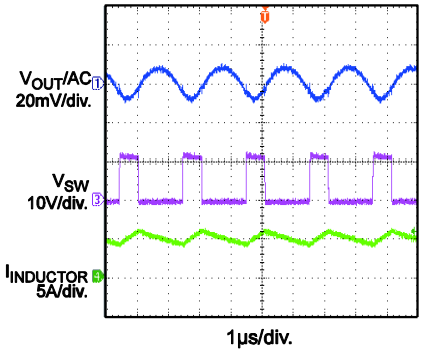
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

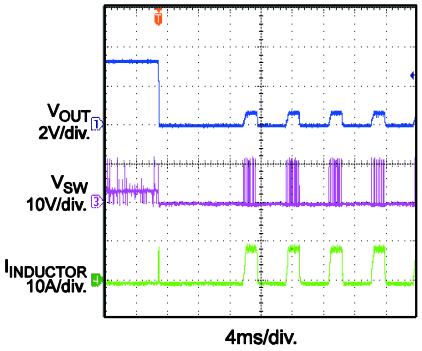
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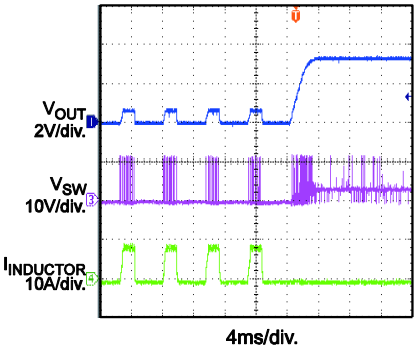
Output Ripple
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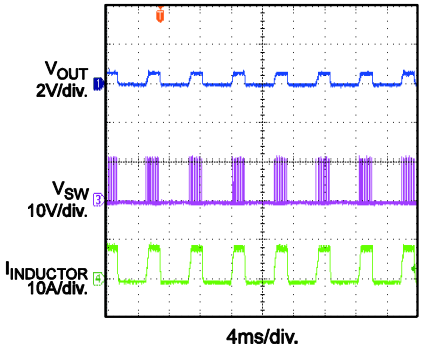
Short-Circuit Entry
I_{OUT}=0A



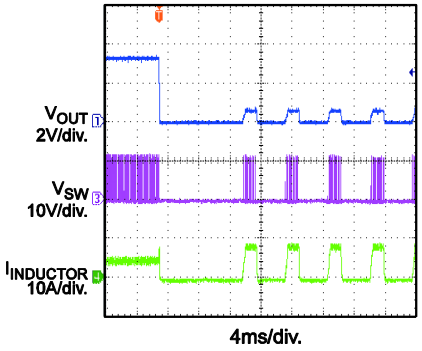
Short-Circuit Recovery
I_{OUT}=0A



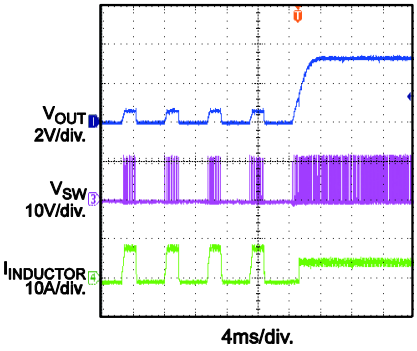
Short-Circuit Steady State



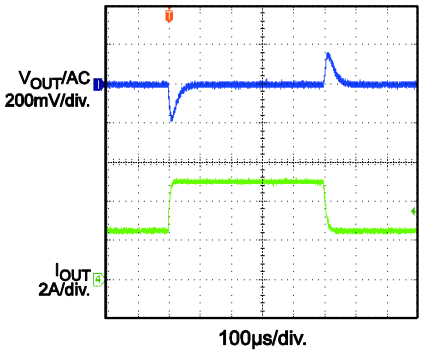
Short-Circuit Entry
I_{OUT}=4A



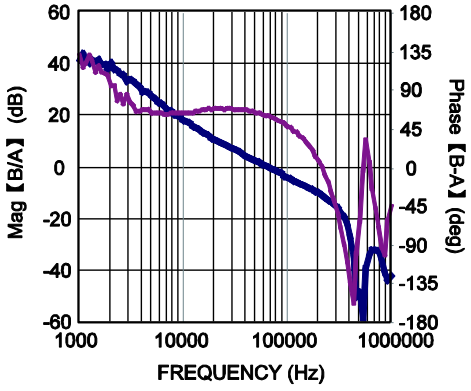
Short-Circuit Recovery
I_{OUT}=4A



Transient Response
I_{OUT}=2A-4A, 2.5A/µs



Bode Plot
I_{OUT}=2A



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PIN FUNCTIONS

Pin #	Name	Description
1	AGND	**Analog Ground**. Connect AGND to GND.
2	IN	**Supply Voltage**. The MP2224 operates from a 4.5V to 18V input rail. IN requires C1 to decouple the input rail. Connect using a wide PCB trace.
3	SW	**Switch Output.** Connect using a wide PCB trace.
4	GND	**Power Ground.** GND requires special consideration during PCB layout. Connect to GND with copper traces and vias.
5	BST	**Bootstrap**. BST requires a capacitor between the SW and BST pins to form a floating supply across the high-side switch driver.
6	EN/SYNC	**EN high to enable the MP2224.** An external clock can be applied to EN to change the switching frequency.
7	VCC	**Bias Supply.** Decouple with a 0.1μF to 0.22μF capacitor.
8	FB	**Feedback.** Connect FB to the tap of an external resistor divider from the output to GND to set the output voltage. The frequency foldback comparator lowers the oscillator frequency when the FB voltage is below 480mV to prevent current-limit runaway during a short-circuit fault condition.

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FUNCTIONAL BLOCK DIAGRAM

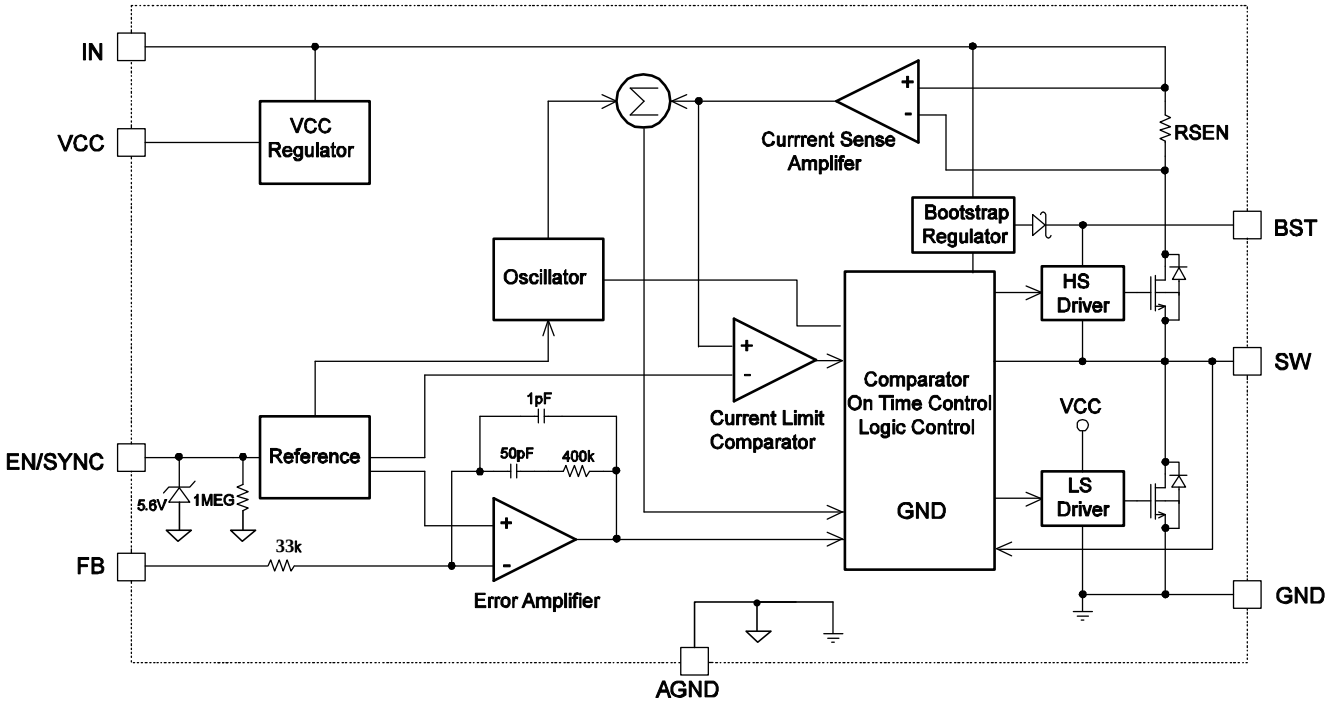


Figure 1: Functional Block Diagram

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OPERATION

The MP2224 is a high-efficiency, synchronous, rectified, step-down, switch-mode converter with built-in power MOSFETs. It offers a very compact solution to achieve a 4A output current with excellent load and line regulation over a wide input supply range.

The MP2224 operates in a fixed-frequency, peak-current-control mode to regulate the output voltage. An internal clock initiates a PWM cycle. The integrated high-side power MOSFET turns on and remains on until the current reaches the value set by the COMP voltage. When the power switch is off, it remains off until the next clock cycle starts. If the current in the power MOSFET does not reach the value set by the COMP value (within 95% of one PWM period), the power MOSFET is forced to turn off.

VCC Regulator

A 5V internal regulator powers most of the internal circuitries. This regulator takes the V_{IN} input and operates in the full V_{IN} range. When V_{IN} is greater than 5.0V, the output of the regulator is in full regulation. When V_{IN} is lower than 5.0V, the output decreases, and the part requires a 0.1µF ceramic capacitor to decouple noise.

AAM Operation

The MP2224 has advanced asynchronous modulation (AAM), which is the internal power-save mode for light-load operation. AAM voltage (V_{AAM}) is fixed internally. In a heavy-load condition, the V_{COMP} is higher than V_{AAM}. When the clock pulses high, the high-side power MOSFET turns on and remains on until $V_{ILsense}$ reaches the value set by the COMP voltage. The internal clock resets every time V_{COMP} is higher than V_{AAM}.

In a light-load condition, the value of V_{COMP} becomes lower. When V_{COMP} is less than V_{AAM} and V_{FB} is less than V_{REF}, V_{COMP} ramps up until it exceeds V_{AAM}. During this time, the internal clock is blocked, causing the MP2224 to skip pulses for pulse frequency modulation (PFM) mode, which achieves the light-load power save.

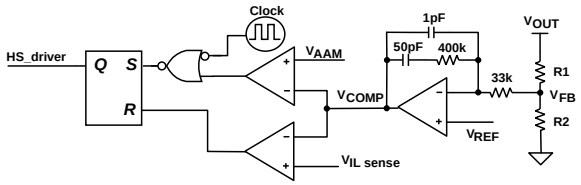


Figure 2: Simplified AAM Control Logic

In a light-load condition, the inductor peak current is set internally to about 800mA (see Figure 2).

Error Amplifier

The error amplifier compares the FB voltage against the internal 0.6V reference (REF) and generates COMP voltage as the output — COMP controls the power MOSFET current. The optimized internal compensation network minimizes the external component count and simplifies the control loop design.

Enable/SYNC Control

EN/SYNC is a digital control pin that turns the converter on and off. Drive EN/SYNC high to turn on the converter; drive it low to turn it off. An internal 1MΩ resistor from EN/SYNC to GND allows EN/SYNC to be floated to shut down the chip.

EN/SYNC is clamped internally using a 5.6V series-Zener-diode (see Figure 3). Connecting the EN/SYNC input pin through a pull-up resist or to the voltage on the V_{IN} pin limits the EN/SYNC input current to less than 100µA.

For example, with 12V connected to Vin, $R_{PULLUP} \geq (12V – 5.6V) \div 100\mu A = 64k\Omega$.

Connecting EN/SYNC directly to a voltage source without a pull-up resistor requires limiting the amplitude of the voltage source to ≤5V to prevent damage to the Zener diode.

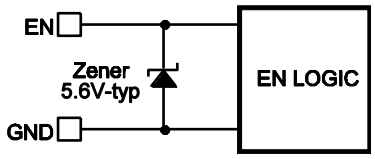


Figure 3: 5.6V Zener Diode Connection

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To use external clock synchronization, connect a clock with a frequency range between 200kHz and 2MHz. The internal clock rising edge will synchronize with the external clock rising edge. Meanwhile the width of the high level should be longer than 250ns, and the width of low level should be longer than 100ns.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The MP2224 UVLO comparator monitors the output voltage of the internal regulator (VCC). The UVLO rising threshold is about 4.1V while its falling threshold is 3.4V.

Soft Start

The soft start prevents the converter output voltage from overshooting during start-up. When the chip starts up, the internal circuitry generates a soft-start voltage (SS) that ramps up from 0V to VCC. When SS is lower than REF, the error amplifier uses SS as the reference. When SS is higher than REF, the error amplifier uses REF as the reference.

The SS time is set to 2.4ms internally.

Over-Current Protection and Hiccup

The MP2224 has a cycle-by-cycle over-current limit, which limits the inductor current in case of an output over load or short circuit (SC). If the over load or SC events last long, the FB voltage can drop below the under-voltage (UV) threshold—typically 30% of the reference. Once UV is triggered, the MP2224 enters hiccup mode to restart the part periodically. This protection mode is especially useful when the output is dead shorted to ground. The average short-circuit current is greatly reduced to alleviate thermal issues and protect the regulator. The MP2224 exits hiccup mode once the over-current condition is removed.

Thermal Shutdown

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the temperature of the silicon reaches 150°C, the whole chip shuts down. When the temperature drops below its lower threshold, (typically 130°C), the chip is enabled again.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection. This UVLO's rising threshold is 2.6V with a hysteresis of 350mV. The bootstrap capacitor voltage is regulated internally by V_{IN} through D1, M1, C4, L1, and C2 (see Figure 4). If (V_{BST}-V_{SW}) exceeds 5V, U1 will regulate M1 to maintain a 5V BST voltage across C4.

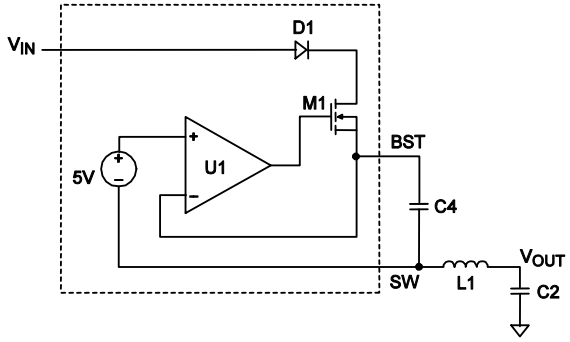


Figure 4: Internal Bootstrap Charging Circuit

Start-Up and Shutdown

If both V_{IN} and EN exceed their respective thresholds, the chip starts up. The reference block starts up first, generating stable reference voltage, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

Three events can shut down the chip: EN low, V_{IN} low, and thermal shutdown. During the shutdown procedure, the signaling path is blocked first to avoid any fault triggering. The COMP voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

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APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider sets the output voltage (see Typical Application on page 1). Also, the feedback resistor R1 sets the feedback loop bandwidth with the internal compensation capacitor. First, choose a value for R1, R2 is then given with Equation (1):

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.6V} - 1} \quad (1)$$

The feedback network—as shown in Figure 5—is highly recommended.

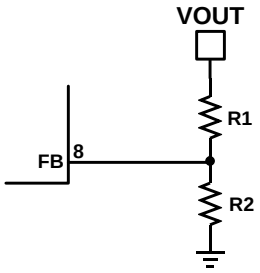


Figure 5: Feedback Network

Table 1 lists the recommended resistors values for common output voltages.

Table 1: Component Selection for Common Output Voltages (9)

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
1.0	120	180
1.2	120	120
1.35	100	80.6
1.5	80.6	53.6
1.8	80.6	40.2
2.5	80.6	25.5
3.3	40.2	8.87
5	40.2	5.49

9) The recommended parameters are based on a 500kHz switching frequency. Different output inductors and capacitors affect the recommended values of R1 and R2. For the other components' parameters, please refer to the TYPICAL APPLICATION CIRCUITS on pages 16-18.

Selecting the Inductor

Use a 1µH to 10µH inductor with a DC current rating at least 25% higher than the maximum load current for most applications.

For highest efficiency, use an inductor with a DC resistance less than 15mΩ. For most designs, the inductance value can be derived from Equation (2).

$$L_1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}} \quad (2)$$

Where ΔI_L is the inductor ripple current.

Choose the inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (3)$$

Use a larger inductor for improved efficiency under light-load conditions—below 100mA.

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous, therefore it requires a capacitor to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Use ceramic capacitors with X5R or X7R dielectrics for best results because of their low ESR and small temperature coefficients. For most applications, use a 22µF capacitor.

Since C1 absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (4):

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (4)$$

The worse case condition occurs at $V_{IN} = 2V_{OUT}$, see Equation (5):

$$I_{C1} = \frac{I_{LOAD}}{2} \quad (5)$$

For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (e.g. 0.1µF) placed as close to the IC

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as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at the input. The input voltage ripple caused by capacitance can be estimated with Equation (6):

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (6)$$

Selecting the Output Capacitor

The output capacitor (C2) maintains the DC output voltage. Use ceramic, tantalum, or low ESR electrolytic capacitors. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with Equation (7):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right) \quad (7)$$

Where L_1 is the inductor value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For ceramic capacitors, the capacitance dominates the impedance at the switching frequency, and the capacitance causes the majority of the output voltage ripple. For simplification, the output voltage ripple can be estimated with Equation (8):

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^2 \times L_1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (8)$$

For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated with Equation (9):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L_1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (9)$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MP2224 can be optimized for a wide range of capacitance and ESR values.

External Bootstrap Diode

BST voltage may become insufficient in particular conditions. In these cases an external bootstrap diode can enhance the efficiency of the regulator and help avoid an output ripple caused by BST voltage insufficiency during PFM operation at light load.

For better efficiency, the diode is needed if the conditions below occur at the same time:

- V_{IN} < 5V
- The duty cycle is large: Duty= $\frac{V_{OUT}}{V_{IN}}$ >65%

To avoid the ripple caused by a BST refresh, the diode is needed if the condition below occurs:

- V_{IN} -V_{OUT}<2.6V

In these cases, it is recommended to add an external BST diode from VCC to BST (see Figure 6).

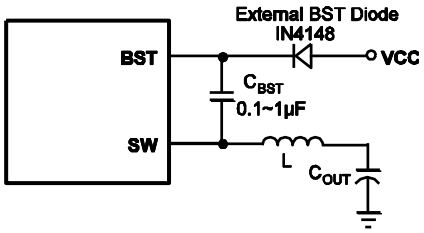


Figure 6: Optional External Bootstrap Diode

The recommended external BST diode is IN4148, and the BST capacitor value is 0.1µF to 1µF.

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PC Board Layout [9]

Efficient PCB layout is critical for stable operation. Refer to Figure 7 and follow the guidelines below for best results.

1) Connect the input ground to GND using the shortest and widest possible trace.

2) Connect the input capacitor to IN using the shortest and widest possible trace.

3) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.

4) Route SW away from sensitive analog areas such as FB.

5) Connect AGND to GND plane with a single trace.

Notes:

10) The recommended layout is based on the Typical Application circuits on page 16 (Figures 8-15).

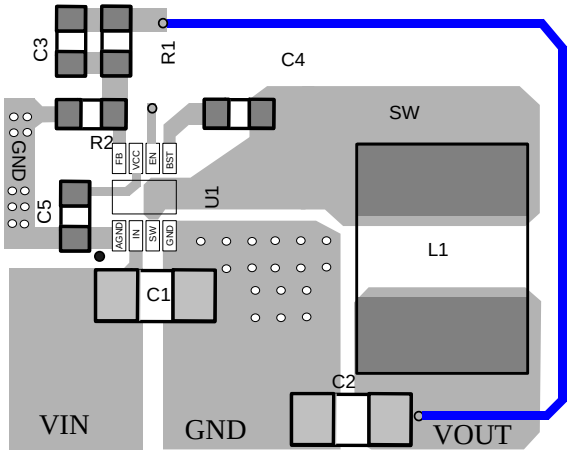


Figure 7: Recommend PCB Layout

Design Example

Table 2 is a design example following the application guidelines for the specifications below:

Table 2: Design Example

V_{IN}	12V
V_{OUT}	3.3V
I_{OUT}	4A

The detailed application schematic is shown in Figure 14. The typical performance and circuit waveforms have been shown in the Typical Performance Characteristics section. For more device applications, please refer to the related evaluation board datasheets.

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TYPICAL APPLICATION CIRCUITS

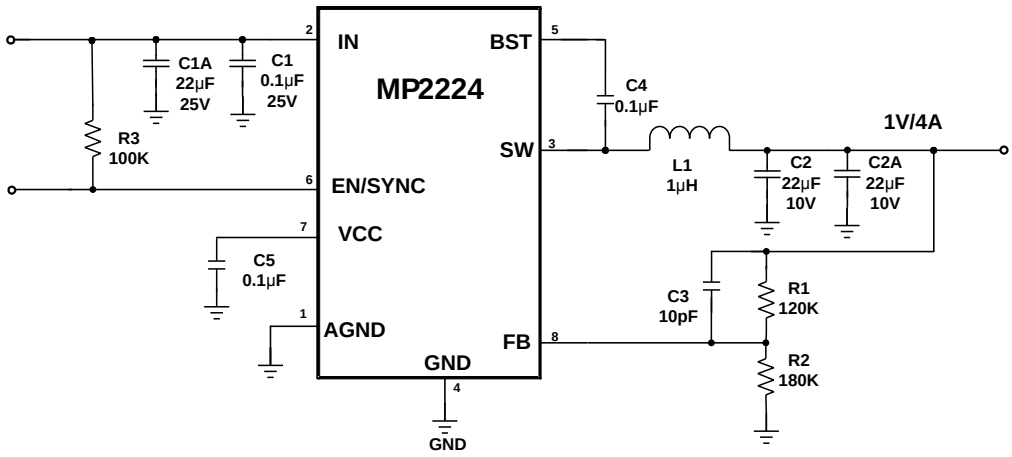


Figure 8: $12V_{IN}$, 1V/4A

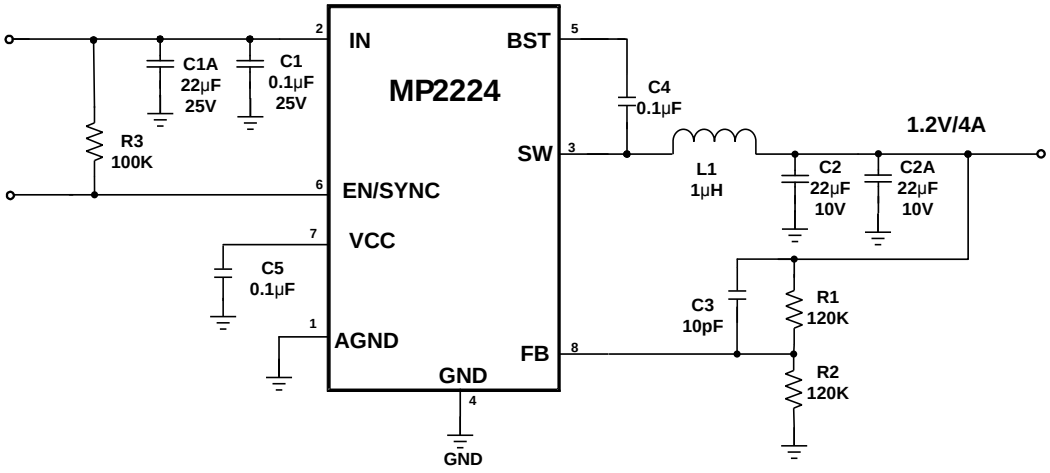


Figure 9: $12V_{IN}$, 1.2V/4A

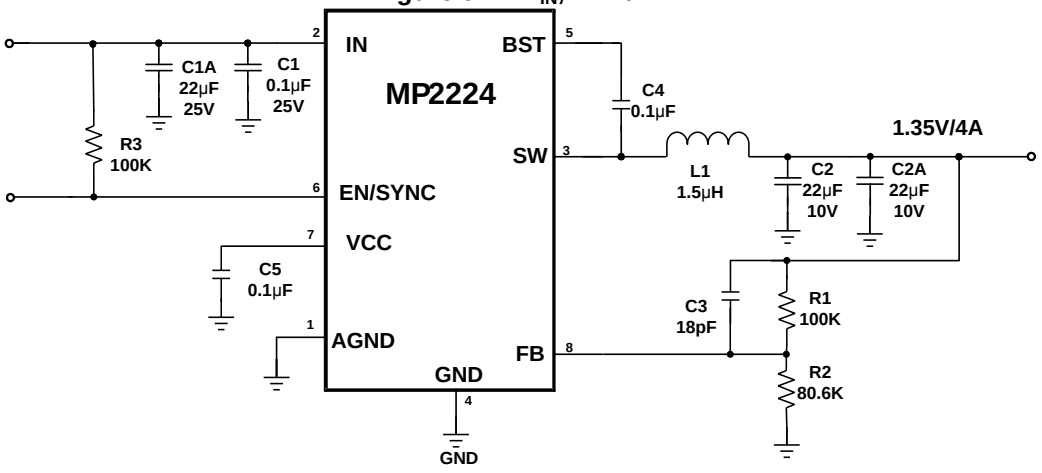


Figure 10: $12V_{IN}$, 1.35V/4A

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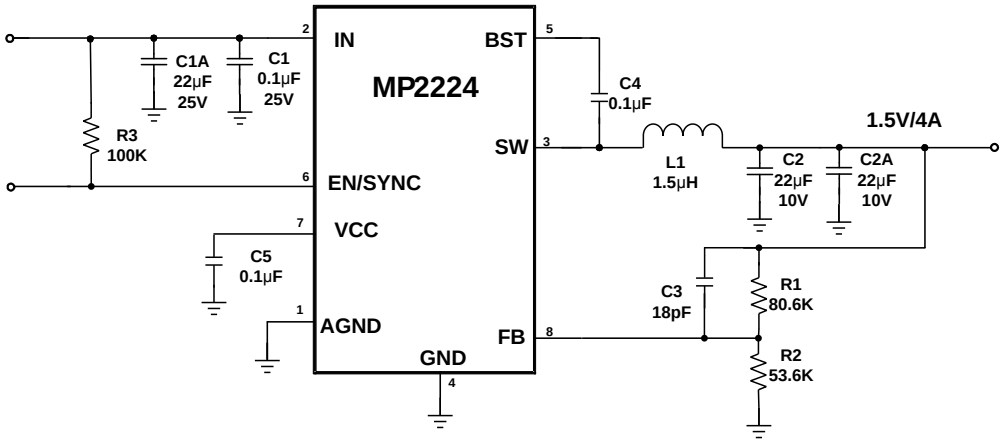


Figure 11: $12V_{IN}$, 1.5V/4A

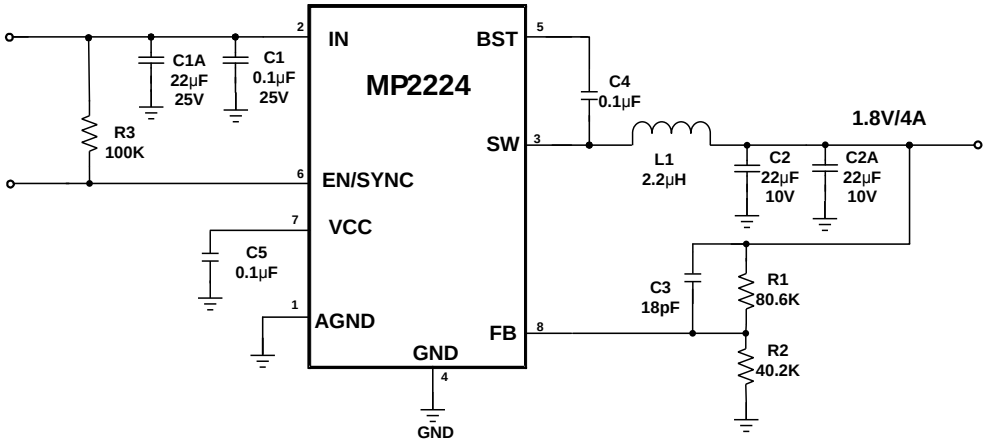


Figure 12: $12V_{IN}$, 1.8V/4A

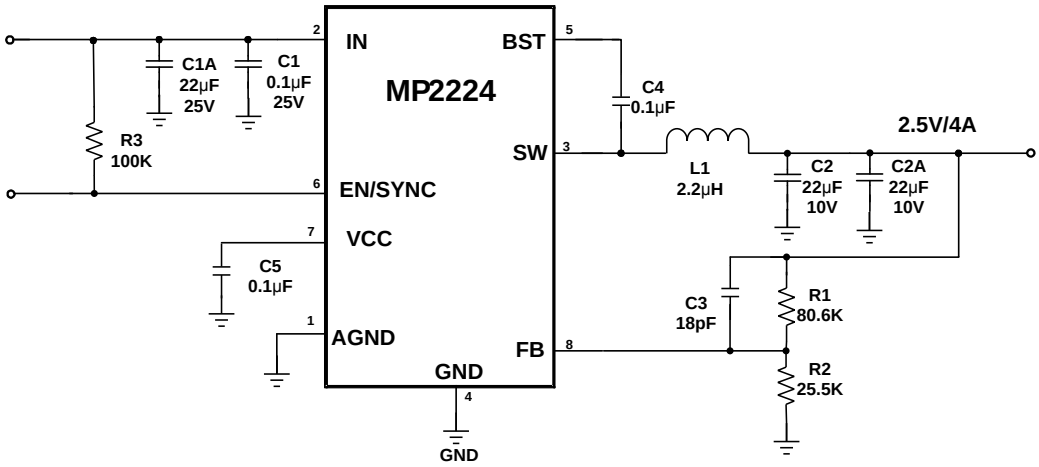


Figure 13: $12V_{IN}$, 2.5V/4A

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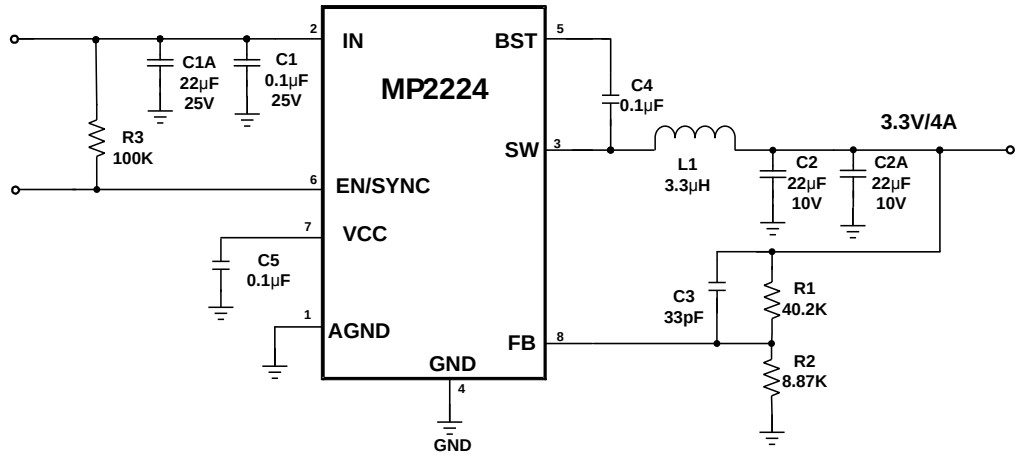


Figure 14: $12V_{IN}$, 3.3V/4A

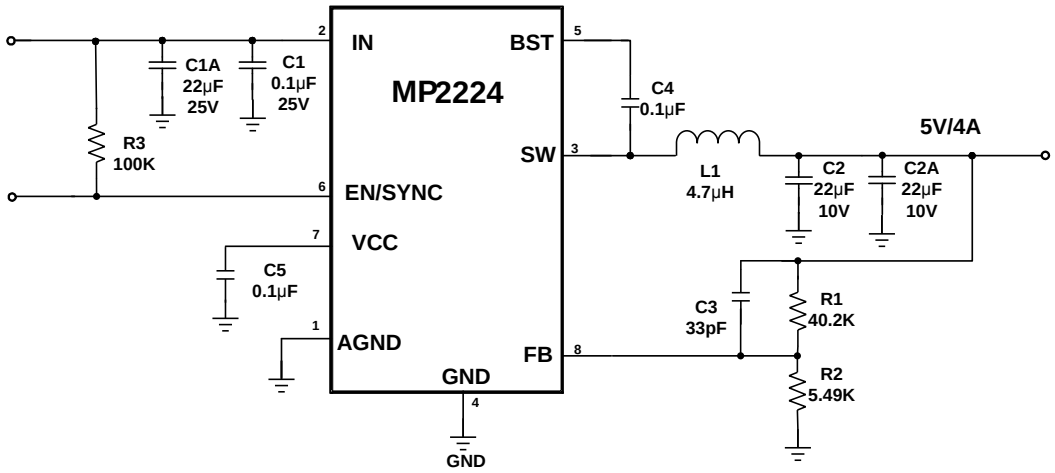
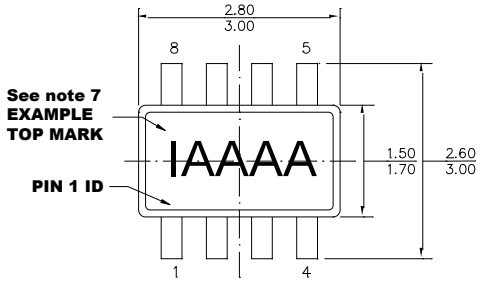


Figure 15: $12V_{IN}$, 5V/4A

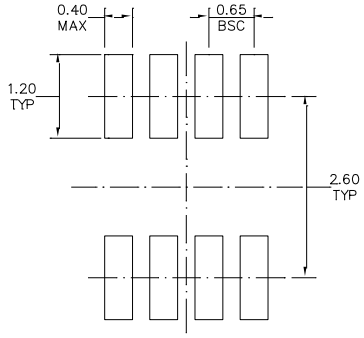
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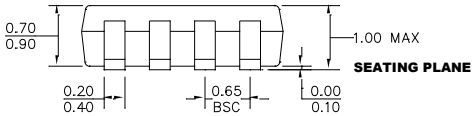
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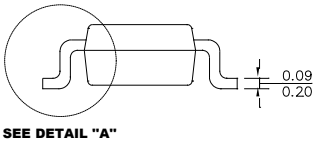
TOP VIEW



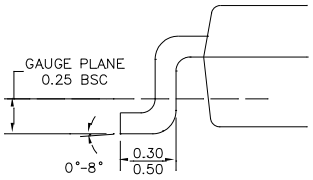
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW



DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) JEDEC REFERENCE IS MO-193, VARIATION BA.
6) DRAWING IS NOT TO SCALE.
7) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)

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