CYV270M0104EQ

Adaptive Video Cable Equalizer

Features

- Adaptive cable equalization
- SMPTE 259M Compliant
- Supports DVB-ASI at 270 Mbps
- Multi standard operation from 143 Mbps to 360 Mbps
- Maximum cable length adjustment
- Carrier detect and mute functionality
- Equalizer bypass mode
- Seamless connection with HOTLink II™ Family and HOTLink® Receiver
- Equalizes up to 350m of Belden 1694A and Canare L-5CFB coaxial cable at 270 Mbps
- Low power: 160 mW at 3.3V
- Single 3.3V supply
- 16-pin Quad Flat Pb-free (QFN) package
- 0.18 μm CMOS technology
- Pb-free and RoHS compliant
- Pin compatible to existing QFN equalizer devices
- Uses Cypress CLEANLink™ technology

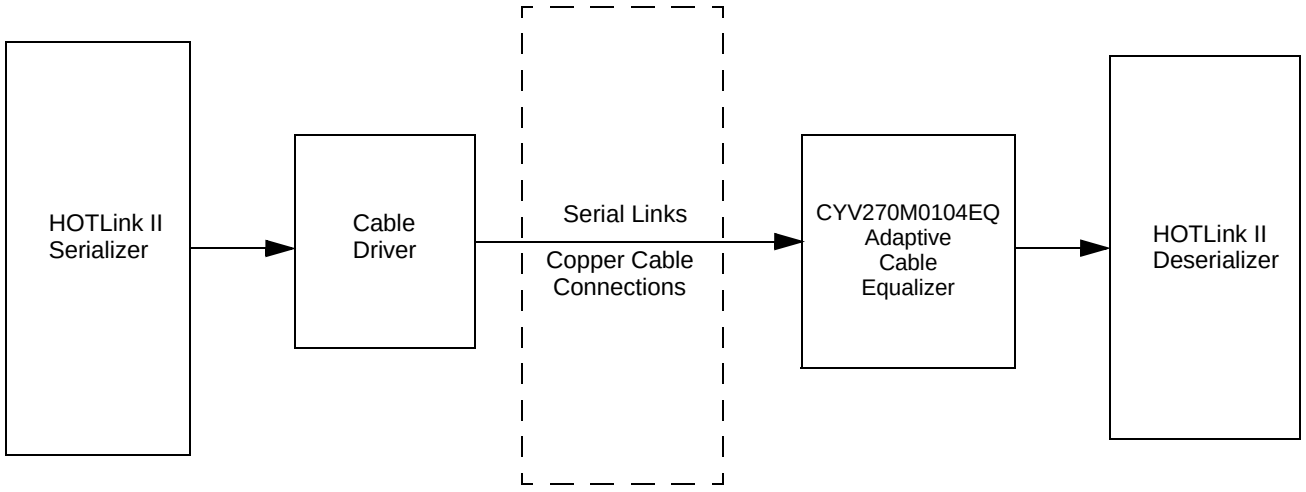
Functional Description

The CYV270M0104EQ is an adaptive video cable equalizer designed to equalize and restore signals received over 75Ω coaxial cable. The equalizer is designed to meet SMPTE 259M data rates and is optimized for performance at 270 Mbps. The CYV270M0104EQ is optimized to equalize up to 350m of Belden 1694A and Canare L-5CFB coaxial cable at 270 Mbps. The CYV270M0104EQ connects seamlessly to the HOTLink II family of transceiver devices and HOTLink receiver devices.

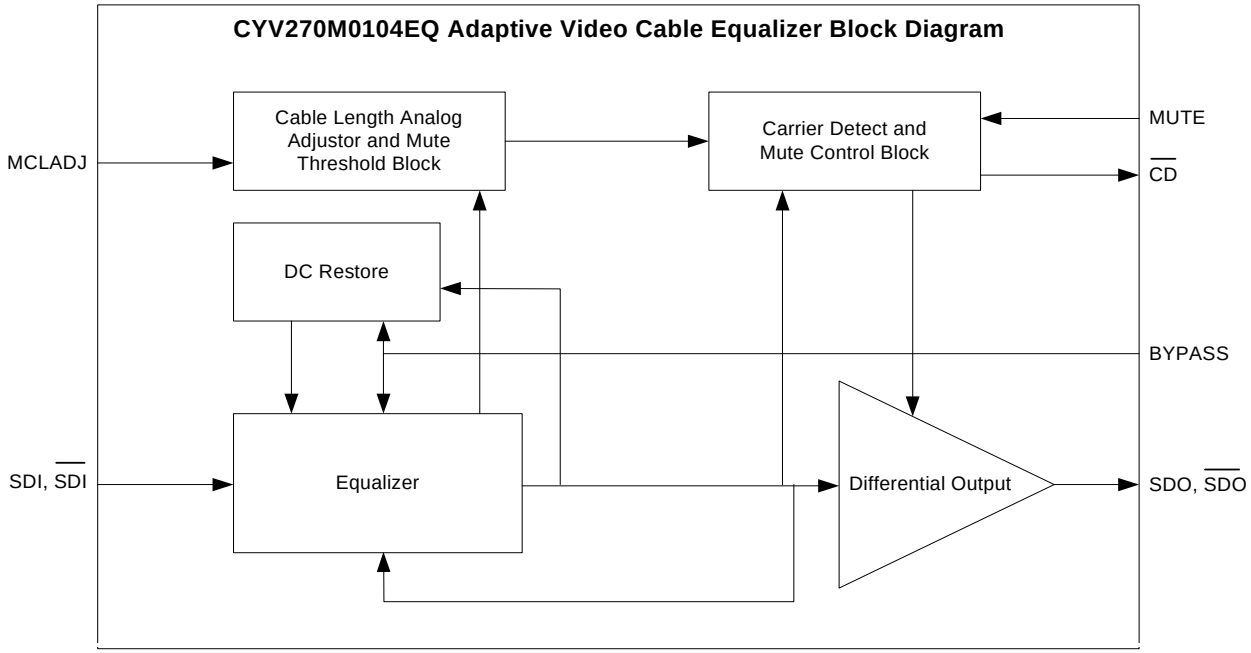
The CYV270M0104EQ has DC restoration to compensate for the DC content of the SMPTE pathological patterns. The maximum cable length adjust (MCLADJ) sets the approximate maximum cable length to equalize. The CYV270M0104EQ's differential serial outputs (SDO, $\overline{SDO}$) mute, when the approximate cable length set by MCLADJ is reached and carrier detect ($\overline{CD}$) is tied to MUTE. The MUTE pin controls muting of the equalizer outputs.

Power consumption is typically 160 mW at 3.3V.

Equalizer System Connection Diagram

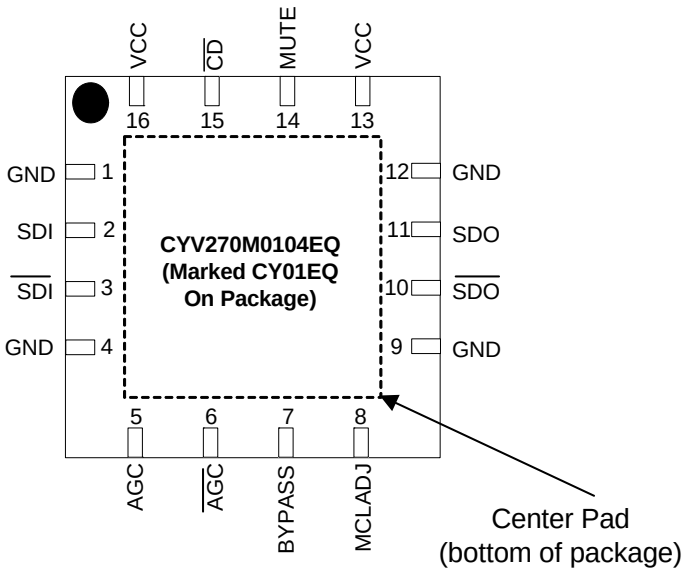


Equalizer Block Diagram



Pinouts

Figure 1. Pin Diagram - 16 Pin QFN (Top View)



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Table 1. Pin Descriptions - CYV270M0104EQ Adaptive Video Cable Equalizer

Name	IO Characteristics	Signal Description
Control Signals		
MUTE	LVTTL Input	**Mute.** When the MUTE pin is set LOW, the equalizer's differential serial outputs are not muted. When the MUTE pin is set HIGH, the equalizer's differential serial outputs are muted. The BYPASS setting is ignored when MUTE is HIGH. Connecting $\overline{CD}$ to the MUTE pin enables automatic muting of the equalizer when the signal is lost. Do not leave an unused MUTE pin floating. Always drive it to a known state.
$\overline{CD}$	LVTTL Output	**Carrier Detect.** When the incoming data stream is present and maximum cable length set by MCLADJ is not exceeded, $\overline{CD}$ outputs a voltage less than 0.8V. When the incoming data stream is not present or maximum cable length set by MCLADJ is exceeded, $\overline{CD}$ outputs a voltage greater than 2.8V. Connecting $\overline{CD}$ to the MUTE pin enables automatic muting of the equalizer when the signal is lost.
MCLADJ	Analog Input	**Maximum Cable Length Adjust.** The maximum cable length to equalize is set by the voltage applied to the MCLADJ input. When the maximum cable length set by MCLADJ is reached, the $\overline{CD}$ indicator deasserts. If MCLADJ functionality is not required, then this pin should be left floating or tied to ground to allow maximum equalized cable length.
BYPASS	LVTTL Input	**Equalizer Bypass.** When BYPASS is set HIGH, the signal presented at the equalizer's differential serial inputs (SDI, $\overline{SDI}$) is routed to the equalizer's differential serial outputs (SDO, $\overline{SDO}$) without performing equalization. When BYPASS is set LOW, the incoming video data stream is equalized and presented at the equalizer's serial differential outputs (SDO, $\overline{SDO}$). When MUTE is set HIGH, the BYPASS setting is ignored and the serial outputs are muted.
AGC, $\overline{AGC}$	Analog	**Automatic Gain Control.** Place a 1 µF capacitor between the AGC and $\overline{AGC}$ pins.
SDO, $\overline{SDO}$	Differential Output	**Differential Serial Outputs.** The equalized serial video data stream is presented at the SDO/$\overline{SDO}$ differential serial CML output.
SDI, $\overline{SDI}$	Differential Input	**Differential Serial Inputs.** SDI/$\overline{SDI}$ accepts either a single-ended or differential serial video data stream over 75Ω coaxial cable.
Power		
VCC	Power	**Power Supply for Device**. Connect to +3.3V DC.
GND	Gnd	**Connect to Ground.**
Center Pad	–	**Connect to PCB Ground for Maximum Thermal Dissipation.**

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Equalizer Operation

The CYV270M0104EQ is an adaptive video cable equalizer that equalizes standard definition (SD) serial digital interface (SDI) video data streams. The CYV270M0104EQ equalizer is optimized to equalize up to 350m of Belden 1694A and Canare L-5CFB cable at 270 Mbps. The device contains one power supply and typically consumes 160 mW power at 3.3V. The adaptive equalizer meets the SMPTE 259M and DVB-ASI video standards. It meets all pathological requirements for SMPTE 259M as defined by RP178. The CYV270M0104EQ Video Cable Equalizer is auto adaptive from 143 Mbps to 360 Mbps.

The CYV270M0104EQ equalizer has multiple variable gain equalization stages that reverse the effects of the cable. This equalization is achieved by separate regulation of the lower and higher frequency components in the signal to give a clean output eye diagram. The CYV270M0104EQ has DC restoration for compensating the DC content of the SMPTE pathological patterns.

SDI, $\overline{\text{SDI}}$

CYV270M0104EQ accepts single-ended or differential serial video data streams over 75Ω coaxial cable. It is recommended to AC couple the SDI and $\overline{\text{SDI}}$ inputs because they are internally biased to 1.2V.

SDO, $\overline{\text{SDO}}$

The CYV270M0104EQ has differential serial output interface drivers that use Current Mode Logic (CML) drivers to provide source matching for the transmission line. These outputs are either AC coupled or DC coupled to HOTLink II receivers.

MCLADJ

Maximum Cable Length Adjust (MCLADJ) sets the approximate maximum amount of cable to equalize. When the maximum cable length set by MCLADJ is reached, the $\overline{\text{CD}}$ pin deasserts. To enable automatic muting of the device when the signal is lost, tie $\overline{\text{CD}}$ directly to MUTE.

The graph in Figure 2 on page 7 illustrates the voltage required at MCLADJ input to equalize various Belden 1694A cables. The same graph applies for Canare L-5CFB cables. If MCLADJ functionality is not required, this pin should be left floating or tied to ground to allow maximum equalized cable length.

MUTE

MUTE is an input pin that controls the muting of the equalizer's output.

If MUTE is set LOW, then the equalizer serial outputs are not muted. If MUTE is set HIGH, then the equalizer serial outputs are muted. When MUTE is active, the BYPASS setting is also ignored.

Connecting $\overline{\text{CD}}$ to MUTE enables automatic muting of the equalizer when the signal is lost.

Do not leave the MUTE pin floating. Always drive it to a known state.

Carrier Detect ($\overline{\text{CD}}$)

Carrier Detect is an active LOW output pin that indicates the presence of a valid incoming data signal. When the incoming data signal is present and maximum cable length does not exceed the length that is set by MCLADJ, $\overline{\text{CD}}$ outputs a voltage less than 0.8V.

When the incoming data stream is not present or maximum cable length exceeds the length that is set by MCLADJ, $\overline{\text{CD}}$ outputs a voltage greater than 2.8V.

Connecting $\overline{\text{CD}}$ to MUTE enables automatic muting of the equalizer when the signal is lost.

BYPASS

The CYV270M0104EQ has a bypass mode that enables the user to bypass the equalizer's equalization and DC restoration functions. When BYPASS is set HIGH, the signal presented at the equalizer's differential serial inputs (SDI, $\overline{\text{SDI}}$) is routed to the equalizer's differential serial outputs (SDO, $\overline{\text{SDO}}$) without equalizing.

When BYPASS is set LOW, the incoming video data stream is equalized and presented at the equalizer's differential serial outputs (SDO, $\overline{\text{SDO}}$).

AGC

Place a 1 µF capacitor between the AGC and $\overline{\text{AGC}}$ pins of the CYV270M0104EQ equalizer.

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Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage to Ground Potential.....–0.5V to +3.8V

DC Voltage Applied to Outputs in High Z State ..... –0.5V to V_{CC} + 0.5V

DC Input Voltage ..... –0.5V to V_{CC} + 0.5V

Electro Static Discharge (ESD) HBM (JEDEC EIA/JESD-A114A)..... > 2000V

Latch Up Current ..... > 200 mA

Power Up Requirements

The CYV270M0104EQ contains one power supply. The voltage on any input or IO pin must not exceed the power pin during power up.

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	+3.3V ±5%

DC Electrical Characteristics

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{CC}	Supply Voltage[1]	–	3.135	3.3	3.465	V
P_D	Power Consumption[2]	–	125	160	190	mW
I_S	Supply Current[1]	–	38	48	60	mA
V_{CMOUT}	Output Common Mode Voltage[1]	Load = 50Ω	–	$V_{CC} - \Delta V_{SDO}/2$ = 2.9	–	V
V_{CMIN}	Input Common Mode Voltage[1] (Bypass = High)	–	1		1.4	V
	Input Common Mode Voltage[1] (Bypass = Low)	–	0		2.9	V
–	Floating MCLADJ DC Voltage[1]	–		1.3		V
–	MCLADJ Range[3]	–	0.4	0.72	1.02	V
$V_{\overline{CD}(OH)}$	$\overline{CD}$ Output Voltage[1]	Carrier Not Present	2.8	–	–	V
$V_{\overline{CD}(OL)}$		Carrier Present	–	–	0.8	V
V_{MUTE}	MUTE Input Voltage Required to Force Outputs to Mute[1]	Min to Mute	2.5		–	V
V_{MUTE}	MUTE Input Voltage Required to Force Active[1]	Max to Activate	–	–	1	V

Notes
1. Production test.
2. Calculated results from production test.
3. Not tested. Based on characterization.

[+] Feedback

AC Electrical Characteristics

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
–	Serial Input Data Rate[1]	–	143	–	360	Mbps
V_{SDI}	Input Voltage Swing	Single-ended, at the transmitter, SD data rate	500[5]		1200	mV
ΔV_{SDO}	Output Voltage Swing[1]	Differential$_{p-p}$, 50Ω load	450	700	950	mV
–	Output Jitter for Various Cable Lengths and Data Rates	270 Mbps Belden 1694A: 0-350m Canare L-5CFB: 0-350m 800 mV transmit amplitude Equalizer pathological pattern	–	0.2[1]	–	UI
–	Output Rise/Fall Time[3, 4]	20% - 80%	80	120	350	ps
–	Mismatch in Rise/Fall Time[3, 4]	–	–	–	30	ps
–	Duty Cycle Distortion[3, 4]	SD color bar pattern	–	0.03	–	UI
–	Overshoot[3, 4]	–	–	–	10	%
–	Input Return Loss[3]	–	-15	–	–	dB
–	Input Resistance[3, 4]	Single-ended	–	2.5	–	kΩ
–	Input Capacitance[3, 4]	Single-ended	–	1	–	pF
–	Output Resistance[3, 4]	Single-ended	–	50	–	Ω

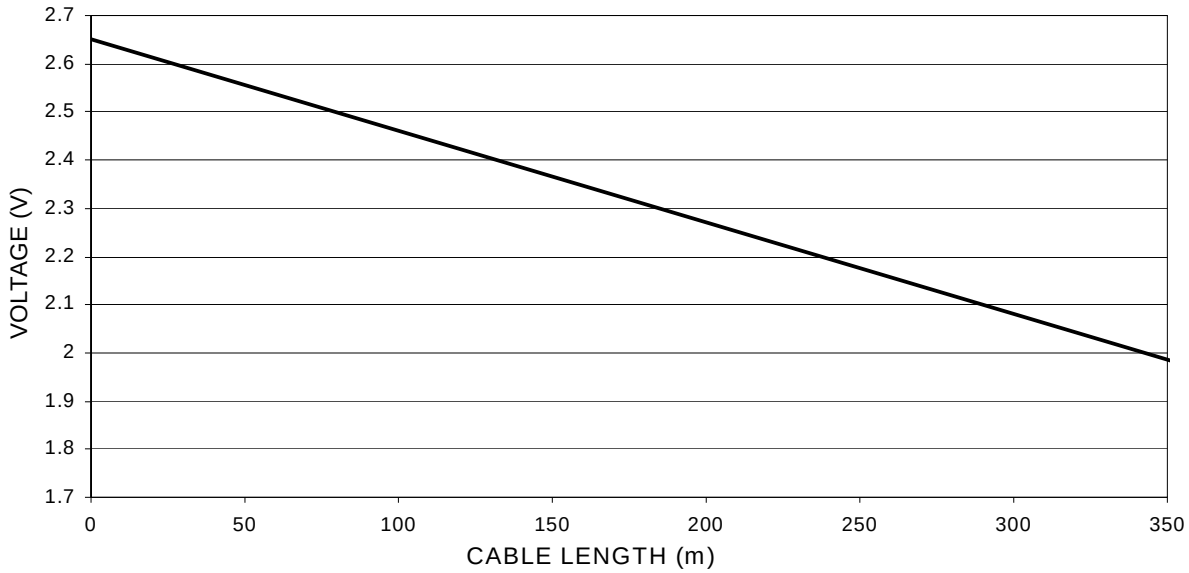
Notes
4. Not tested. Guaranteed by design simulations.
5. Based on characterization across temperature and voltage with 350m of Belden 1694A and Canare L-5CFB cable, transmitting SMPTE Equalizer Pathological Test Pattern.

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Typical Performance Graphs

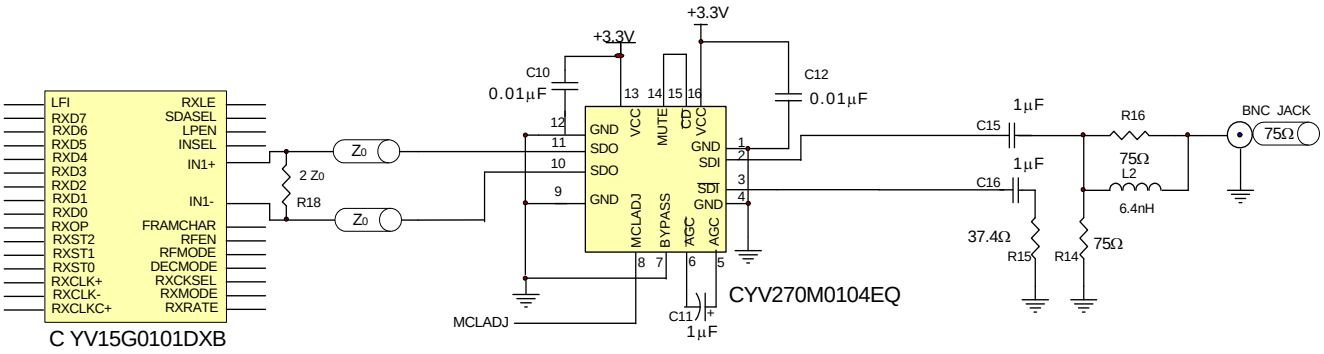
(Unless otherwise stated, V_{CC} = 3.3V, T_A = 25°C)

Figure 2. MCLADJ Input Voltage vs Belden 1694A Cable Length at SD-SDI Data Rate



Typical Application Circuit

Figure 3. Interfacing CYV270M0104EQ to the HOTLink II SerDes



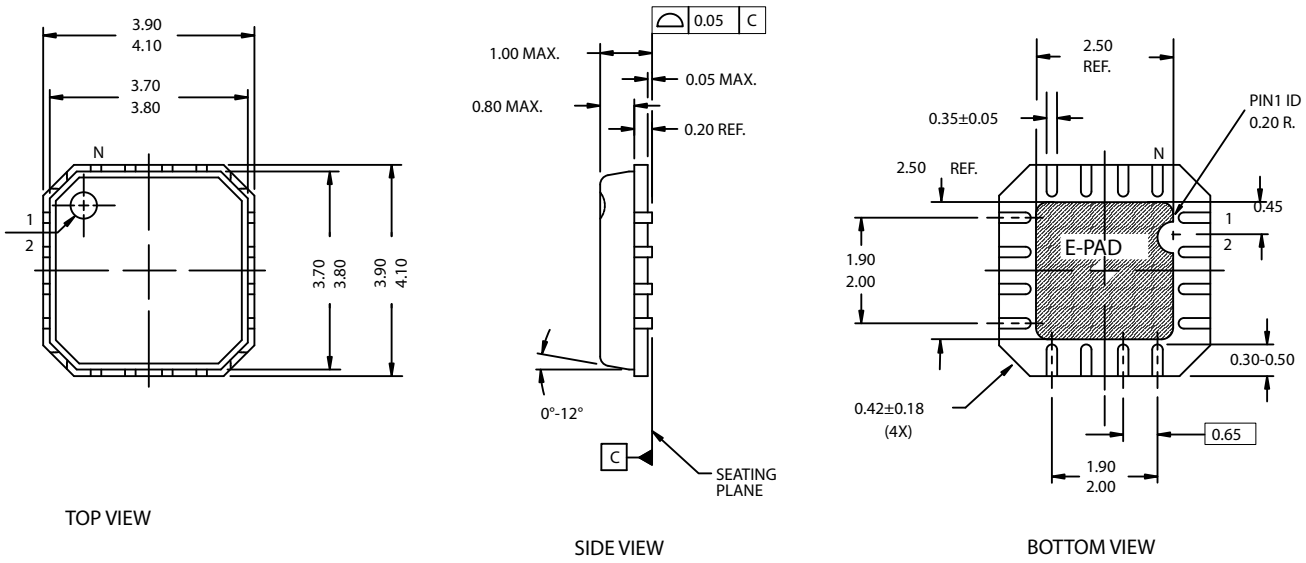
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Ordering Information

Ordering Code	Package Marking	Package Name	Package Type	Operating Range
CYV270M0104EQ-LXC	CY01EQ	LY16A	Pb-free 16-Pin QFN	0 to 70°C

Package Dimension

Figure 4. 16-Pin QFN (4x4 mm) Package LY16A



DIMENSION IN mm MIN.
MAX.

REFERENCE JEDEC MO-220

PKG. WEIGHT 0.04gms

PART #	
LF16A	STANDARD PKG.
LY16A	LEAD FREE PKG.

001-04468-*A

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Document History Page

Document Title: CYV270M0104EQ Adaptive Video Cable Equalizer Document Number: 001-12875				
REV.	**ECN NO.**	**ISSUE DATE**	**ORIG. OF CHANGE**	**DESCRIPTION OF CHANGE**
**	1396423	SEE ECN	UKK/AESA	New datasheet

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