

# HEF4015B

## Dual 4-bit static shift register

Rev. 8 — 21 November 2011

Product data sheet

## 1. General description

The HEF4015B is a dual edge-triggered 4-bit static shift register (serial-to-parallel converter). Each shift register has a serial data input (D), a clock input (CP), four fully buffered parallel outputs (Q0 to Q3) and an overriding asynchronous master reset input (MR). Information present on D is shifted to the first register position, and all the data in the register is shifted one position to the right on the LOW-to-HIGH transition of CP. A HIGH on MR clears the register and forces Q0 to Q3 to LOW, independent of CP and D. The clock input's Schmitt trigger action makes the input highly tolerant of slower clock rise and fall times.

It operates over a recommended  $V_{DD}$  power supply range of 3 V to 15 V referenced to  $V_{SS}$  (usually ground). Unused inputs must be connected to  $V_{DD}$ ,  $V_{SS}$ , or another input.

## 2. Features and benefits

- Tolerant of slow clock rise and fall times
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ .
- Complies with JEDEC standard JESD 13-B

## 3. Applications

- Serial-to-parallel converter
- Buffer stores
- General purpose register

## 4. Ordering information

**Table 1. Ordering information**

All types operate from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ .

Type number	Package	Description	Version
	Name		
HEF4015BP	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
HEF4015BT	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1



5. Functional diagram

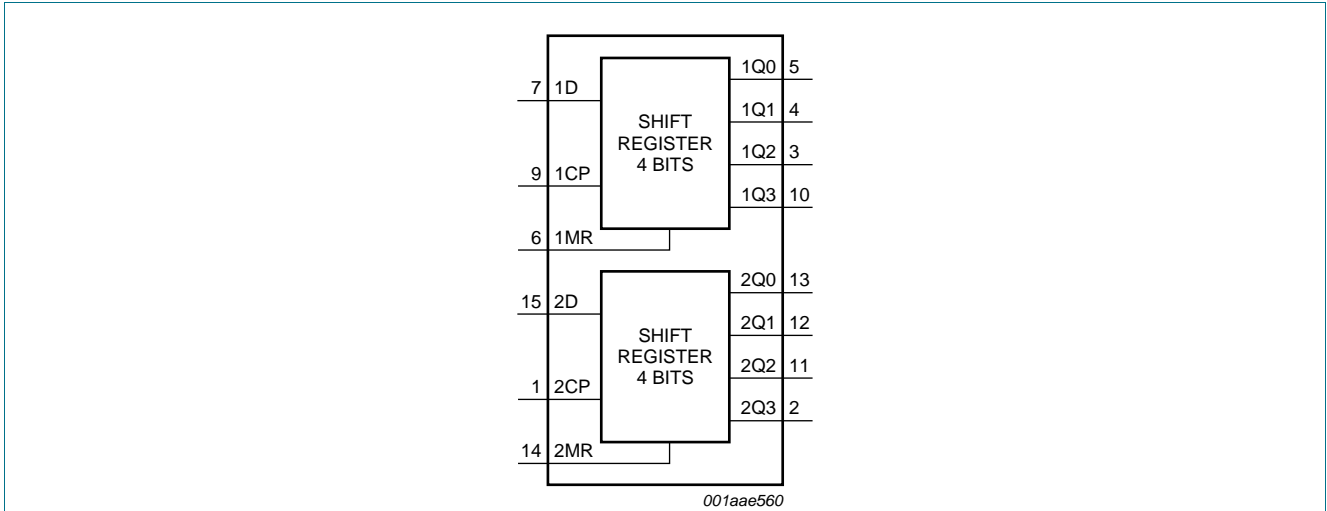


Fig 1. Functional diagram

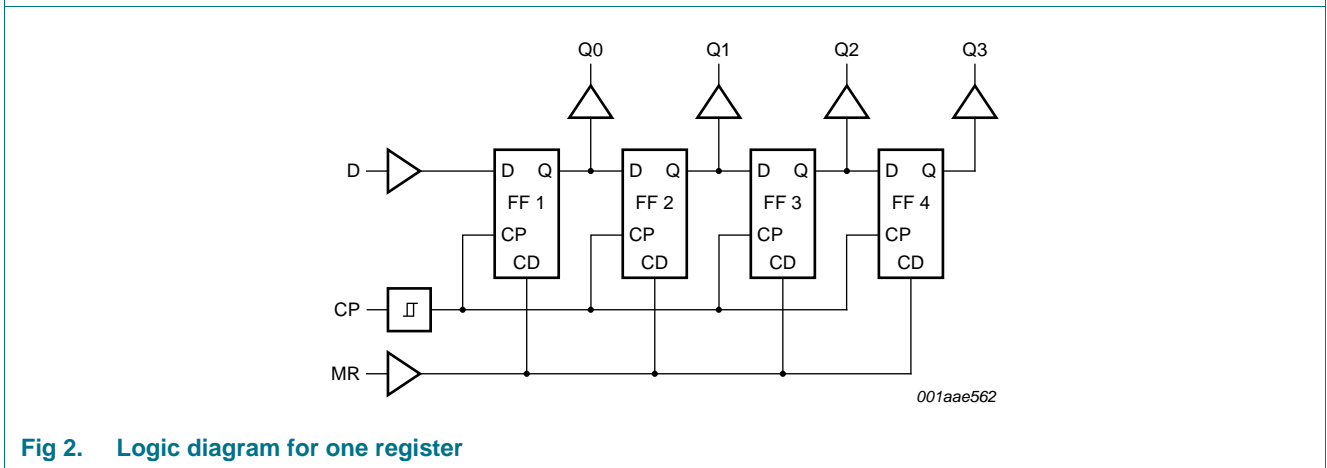


Fig 2. Logic diagram for one register

## 6. Pinning information

### 6.1 Pinning

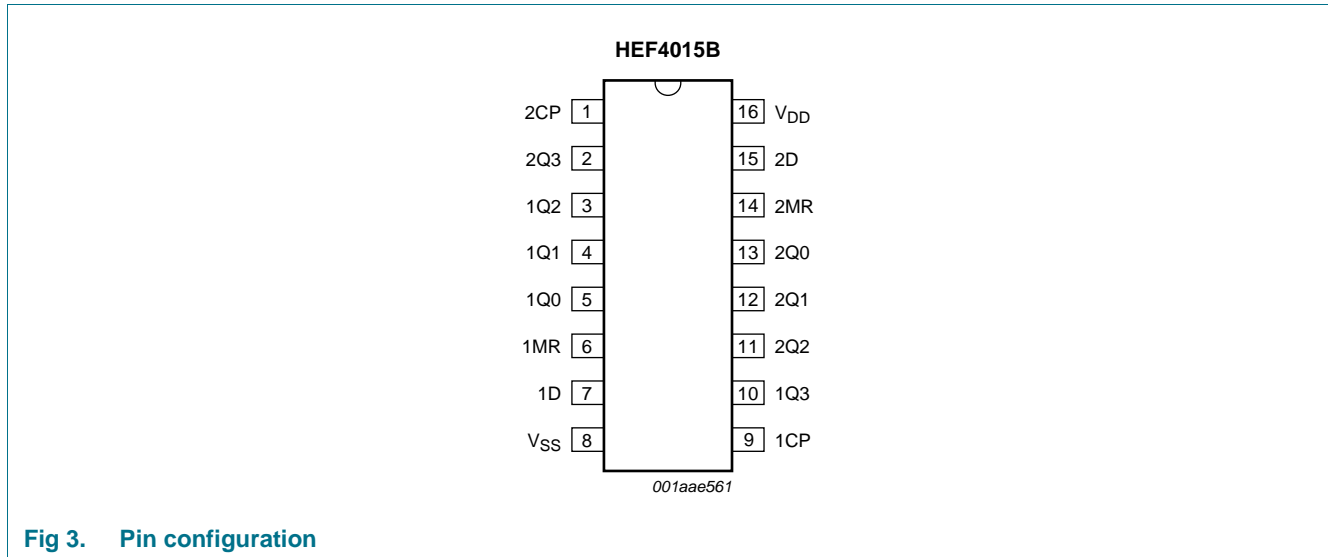


Fig 3. Pin configuration

### 6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1Q0 to 1Q3	5, 4, 3, 10	parallel output
2Q0 to 2Q3;	13, 12, 11, 2	parallel output
1MR, 2MR	6, 14	master reset input (active HIGH)
1D, 2D	7, 15	serial data input
V <sub>SS</sub>	8	ground supply voltage
1CP, 2CP	9, 1	clock input (LOW-to-HIGH edge-triggered)
V <sub>DD</sub>	16	supply voltage

## 7. Functional description

Table 3. Function table [1]

number of clock pulse transitions	Input			Output			
	CP	D	MR	Q0	Q1	Q2	Q3
1	↑	D1	L	D1	X	X	X
2	↑	D2	L	D2	D1	X	X
3	↑	D3	L	D3	D2	D1	X
4	↑	D4	L	D4	D3	D2	D1
	↓	X	L	no change	no change	no change	no change
	X	X	H	L	L	L	L

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; D<sub>n</sub> = either HIGH or LOW; ↑ = positive-going transition; ↓ = negative-going transition.

## 8. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
$V_{DD}$	supply voltage		-0.5	+18	V	
$I_{IK}$	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{DD} + 0.5\text{ V}$	-	$\pm 10$	mA	
$V_I$	input voltage		-0.5	$V_{DD} + 0.5$	V	
$I_{OK}$	output clamping current	$V_O < -0.5\text{ V}$ or $V_O > V_{DD} + 0.5\text{ V}$	-	$\pm 10$	mA	
$I_{I/O}$	input/output current		-	$\pm 10$	mA	
$I_{DD}$	supply current		-	50	mA	
$T_{stg}$	storage temperature		-65	+150	°C	
$T_{amb}$	ambient temperature		-40	+85	°C	
$P_{tot}$	total power dissipation	$T_{amb} = -40\text{ °C}$ to $+85\text{ °C}$				
		DIP16 package	[1]	-	750	mW
		SO16 package	[2]	-	500	mW
$P$	power dissipation	per output	-	100	mW	

[1] For DIP16 package:  $P_{tot}$  derates linearly with 12 mW/K above 70 °C.

[2] For SO16 package:  $P_{tot}$  derates linearly with 8 mW/K above 70 °C.

## 9. Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD}$	supply voltage		3	-	15	V
$V_I$	input voltage		0	-	$V_{DD}$	V
$T_{amb}$	ambient temperature	in free air	-40	-	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{DD} = 5\text{ V}$	-	-	3.75	$\mu\text{s/V}$
		$V_{DD} = 10\text{ V}$	-	-	0.5	$\mu\text{s/V}$
		$V_{DD} = 15\text{ V}$	-	-	0.08	$\mu\text{s/V}$

## 10. Static characteristics

**Table 6. Static characteristics**

$V_{SS} = 0\text{ V}$ ;  $V_I = V_{SS}$  or  $V_{DD}$  unless otherwise specified.

Symbol	Parameter	Conditions	$V_{DD}$	$T_{amb} = -40\text{ }^{\circ}\text{C}$		$T_{amb} = 25\text{ }^{\circ}\text{C}$		$T_{amb} = 85\text{ }^{\circ}\text{C}$		Unit
				Min	Max	Min	Max	Min	Max	
$V_{IH}$	HIGH-level input voltage	$ I_O  < 1\text{ }\mu\text{A}$	5 V	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	V
$V_{IL}$	LOW-level input voltage	$ I_O  < 1\text{ }\mu\text{A}$	5 V	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	V
$V_{OH}$	HIGH-level output voltage	$ I_O  < 1\text{ }\mu\text{A}$	5 V	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	V
$V_{OL}$	LOW-level output voltage	$ I_O  < 1\text{ }\mu\text{A}$	5 V	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	V
$I_{OH}$	HIGH-level output current	$V_O = 2.5\text{ V}$	5 V	-	-1.7	-	-1.4	-	-1.1	mA
		$V_O = 4.6\text{ V}$	5 V	-	-0.52	-	-0.44	-	-0.36	mA
		$V_O = 9.5\text{ V}$	10 V	-	-1.3	-	-1.1	-	-0.9	mA
		$V_O = 13.5\text{ V}$	15 V	-	-3.6	-	-3.0	-	-2.4	mA
$I_{OL}$	LOW-level output current	$V_O = 0.4\text{ V}$	5 V	0.52	-	0.44	-	0.36	-	mA
		$V_O = 0.5\text{ V}$	10 V	1.3	-	1.1	-	0.9	-	mA
		$V_O = 1.5\text{ V}$	15 V	3.6	-	3.0	-	2.4	-	mA
$I_I$	input leakage current		15 V	-	$\pm 0.3$	-	$\pm 0.3$	-	$\pm 1.0$	$\mu\text{A}$
$I_{DD}$	supply current	$I_O = 0\text{ A}$	5 V	-	20	-	20	-	150	$\mu\text{A}$
			10 V	-	40	-	40	-	300	$\mu\text{A}$
			15 V	-	80	-	80	-	600	$\mu\text{A}$
$C_I$	input capacitance		-	-	-	-	7.5	-	-	pF

## 11. Dynamic characteristics

**Table 7. Dynamic characteristics**
 $V_{SS} = 0\text{ V}; C_L = 50\text{ pF}; T_{amb} = 25\text{ }^\circ\text{C}.$ 

Symbol	Parameter	Conditions	V <sub>DD</sub>	Extrapolation formula <sup>[1]</sup>	Min	Typ	Max	Unit
t <sub>PHL</sub>	HIGH to LOW propagation delay	nCP to Qn; see <a href="#">Figure 4</a>	5 V	103 ns + (0.55 ns/pF)C <sub>L</sub>	-	130	260	ns
			10 V	44 ns + (0.23 ns/pF)C <sub>L</sub>	-	55	110	ns
			15 V	32 ns + (0.16 ns/pF)C <sub>L</sub>	-	40	80	ns
		nMR to Qn; see <a href="#">Figure 6</a>	5 V	78 ns + (0.55 ns/pF)C <sub>L</sub>	-	105	210	ns
			10 V	34 ns + (0.23 ns/pF)C <sub>L</sub>	-	45	90	ns
			15 V	27 ns + (0.16 ns/pF)C <sub>L</sub>	-	35	70	ns
t <sub>PLH</sub>	LOW to HIGH propagation delay	nCP to Qn see <a href="#">Figure 4</a>	5 V	93 ns + (0.55 ns/pF)C <sub>L</sub>	-	120	240	ns
			10 V	44 ns + (0.23 ns/pF)C <sub>L</sub>	-	55	110	ns
			15 V	32 ns + (0.16 ns/pF)C <sub>L</sub>	-	40	80	ns
t <sub>t</sub>	transition time	see <a href="#">Figure 4</a>	5 V	10 ns + (1.00 ns/pF)C <sub>L</sub>	-	60	120	ns
			10 V	9 ns + (0.42 ns/pF)C <sub>L</sub>	-	30	60	ns
			15 V	6 ns + (0.28 ns/pF)C <sub>L</sub>	-	20	40	ns
t <sub>su</sub>	set-up time	nD to nCP; see <a href="#">Figure 5</a>	5 V		+25	-15	-	ns
			10 V		+25	-10	-	ns
			15 V		+20	-5	-	ns
t <sub>h</sub>	hold time	nD to nCP; see <a href="#">Figure 5</a>	5 V		40	20	-	ns
			10 V		20	10	-	ns
			15 V		15	8	-	ns
t <sub>w</sub>	pulse width	nCP LOW; minimum width; see <a href="#">Figure 5</a>	5 V		60	30	-	ns
			10 V		30	15	-	ns
			15 V		20	10	-	ns
		nMR HIGH; minimum width; see <a href="#">Figure 6</a>	5 V		80	40	-	ns
			10 V		30	15	-	ns
			15 V		24	12	-	ns
t <sub>rec</sub>	recovery time	pin nMR; see <a href="#">Figure 6</a>	5 V		50	20	-	ns
			10 V		30	10	-	ns
			15 V		20	5	-	ns
f <sub>max</sub>	maximum frequency	see <a href="#">Figure 5</a>	5 V		7	15	-	MHz
			10 V		15	30	-	MHz
			15 V		22	44	-	MHz

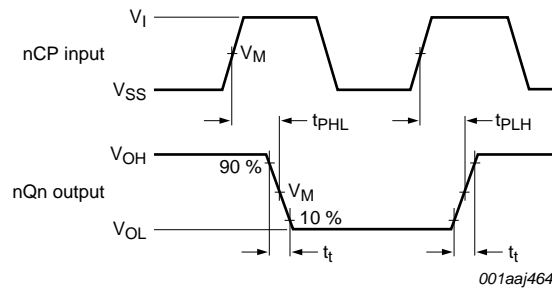
[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown (C<sub>L</sub> in pF).

**Table 8. Dynamic power dissipation  $P_D$**

$P_D$  can be calculated from the formulas shown.  $V_{SS} = 0\text{ V}$ ;  $t_r = t_f \leq 20\text{ ns}$ ;  $T_{amb} = 25\text{ }^\circ\text{C}$ .

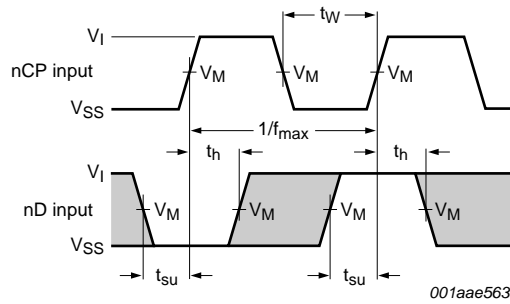
Symbol	Parameter	$V_{DD}$	Typical formula for $P_D$ ( $\mu\text{W}$ )	where:
$P_D$	dynamic power dissipation	5 V	$P_D = 1500 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	$f_i$ = input frequency in MHz;
		10 V	$P_D = 6300 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	$f_o$ = output frequency in MHz;
		15 V	$P_D = 17000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	$C_L$ = output load capacitance in pF;
				$V_{DD}$ = supply voltage in V;
				$\Sigma(C_L \times f_o)$ = sum of the outputs.

## 12. Waveforms



Measurement points are given in [Table 9](#).

**Fig 4. Waveforms showing nCP propagation delays and nQn transition times**

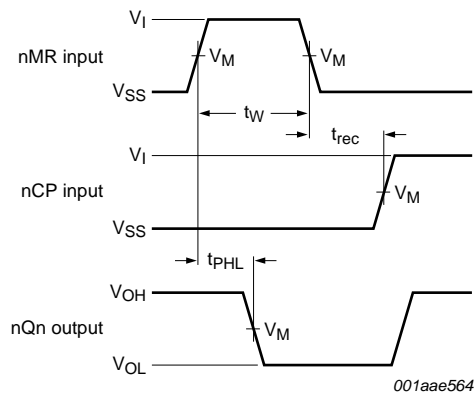


The shaded area indicates where the input is permitted to change for predictable output performance.

Set-up and hold times are shown as positive values but may be specified as negative values;

Measurement points are given in [Table 9](#).

**Fig 5. Waveforms showing set-up times, hold times, and minimum clock pulse width**



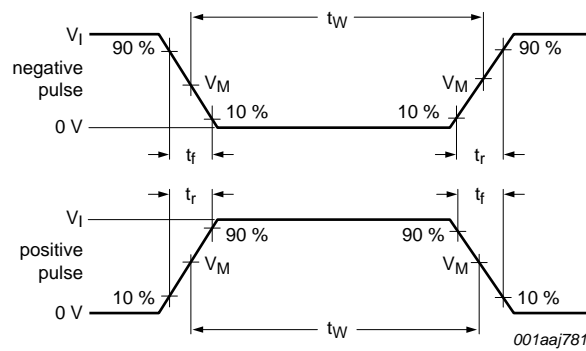
Measurement points are given in [Table 9](#).

**Fig 6. Waveforms showing MR recovery time, propagation delay and minimum pulse width**

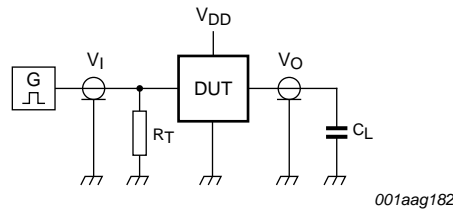
**Table 9. Measurement points**

Supply voltage	Input	Output
$V_{DD}$	$V_M$	$V_M$
5 V to 15 V	$0.5V_{DD}$	$0.5V_{DD}$





a. Input waveforms



b. Test circuit

Test data is given in [Table 10](#).

Definitions for test circuit:

DUT = Device Under Test;

$C_L$  = load capacitance including jig and probe capacitance;

$R_T$  = termination resistance should be equal to the output impedance  $Z_o$  of the pulse generator.

Fig 7. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Input	Load
$V_{DD}$	$V_I$	$C_L$
5 V to 15 V	$V_{SS}$ or $V_{DD}$	50 pF
	$t_r, t_f$	$\leq 20$ ns

13. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4

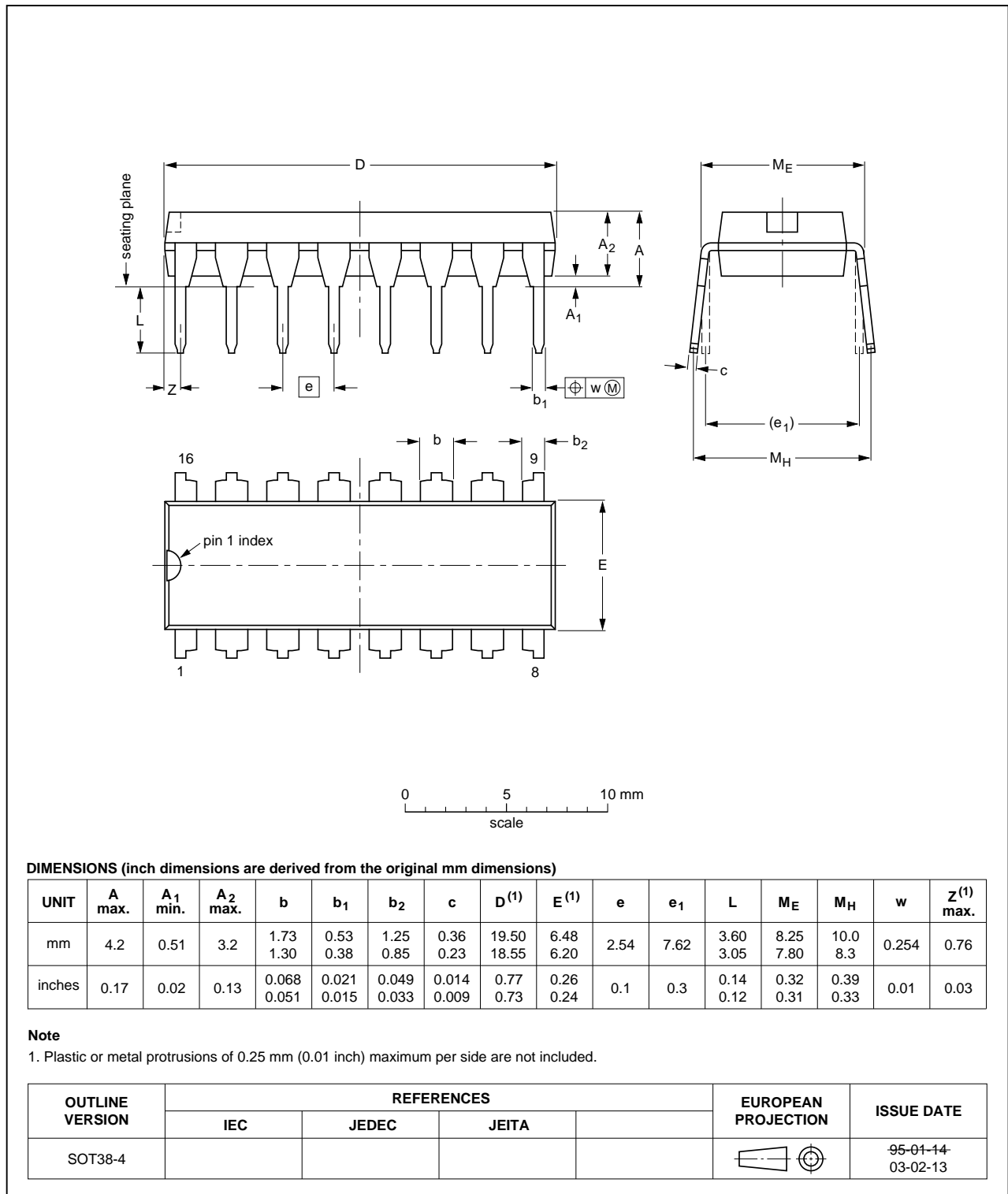


Fig 8. Package outline SOT38-4 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

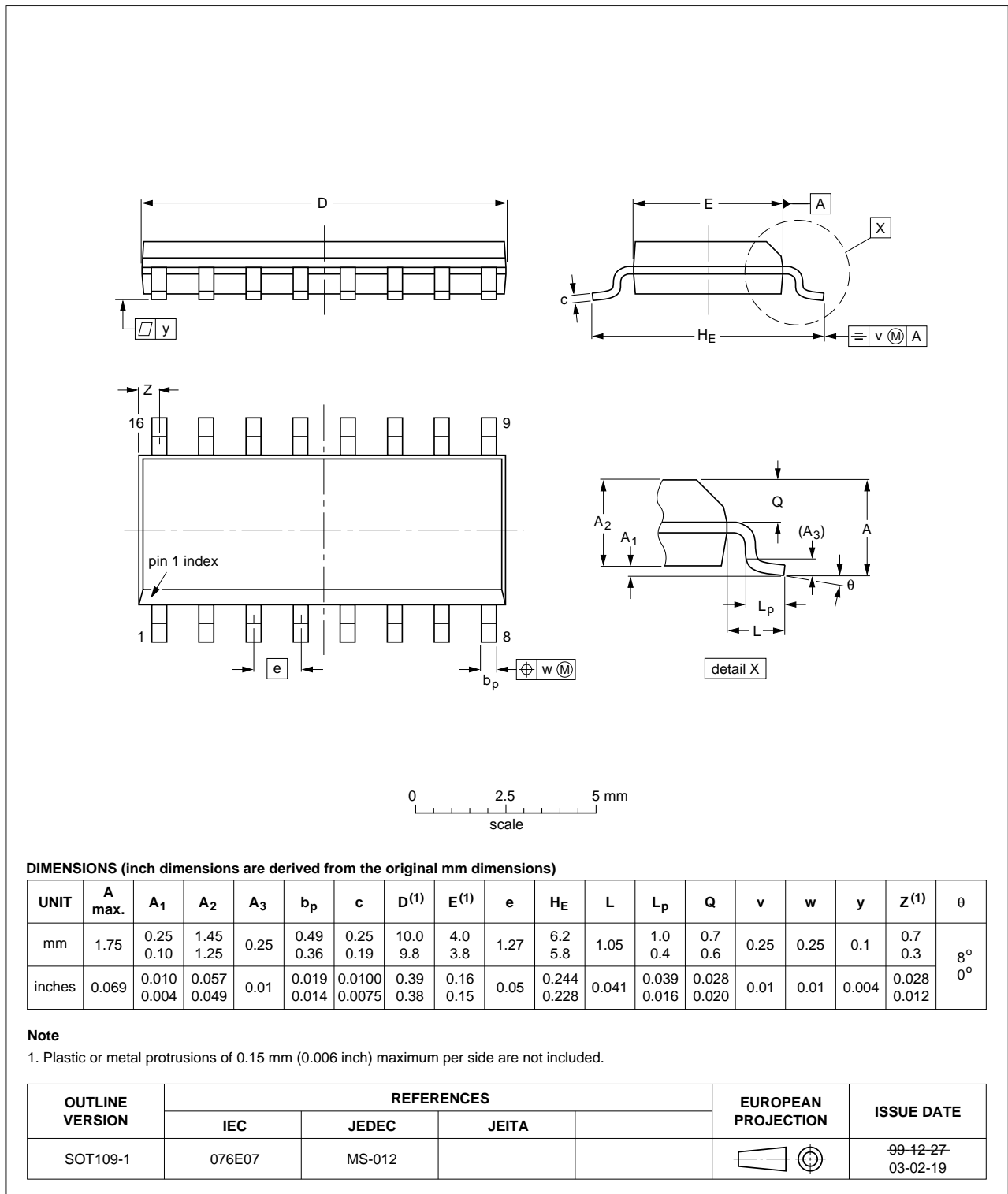


Fig 9. Package outline SOT109-1 (SO16)

## 14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4015B v.8	20111121	Product data sheet	-	HEF4015B v.7
Modifications:	<ul style="list-style-type: none"><li>• Legal pages updated.</li><li>• Changes in “General description” and “Features and benefits”.</li></ul>			
HEF4015B v.7	20110914	Product data sheet	-	HEF4015B v.6
HEF4015B v.6	20091103	Product data sheet	-	HEF4015B v.5
HEF4015B v.5	20090624	Product data sheet	-	HEF4015B v.4
HEF4015B v.4	20090127	Product data sheet	-	HEF4015B_CN V v.3
HEF4015B_CN V v.3	19950101	Product specification	-	HEF4015B_CN V v.2
HEF4015B_CN V v.2	19950101	Product specification	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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