

NIS6111

Product Preview

Better Efficiency Rectifier System

Ultra Efficient, High Speed Diode

The NIS6111 ORing diode is a high speed, high efficiency, hybrid rectifier, designed for low voltage, high current systems, such as those required for today's digital circuits. It couples a high speed integrated circuit with a power MOSFET to create a diode with the same forward drop characteristics as a MOSFET. It offers increased efficiency for switching power supplies as well as in ORing diode applications.

It offers a low on resistance that can be further reduced by the addition of external MOSFETs. It features the highest reverse recovery speed of any device in the industry.

Features

- Low Forward Drop Improves System Efficiency
- Ultra High Speed
- Can be used in High Side and Low Side Configurations
- 24 V Rating
- Allows use of External MOSFETs for Extended Current Handling Capacity

Applications

- Redundant Power Supplies for High-Availability Systems
- Static ORing Diodes
- Low Voltage, Isolated Outputs
- Flyback, Forward Converter, Half Bridge Converters

PIN ASSIGNMENT

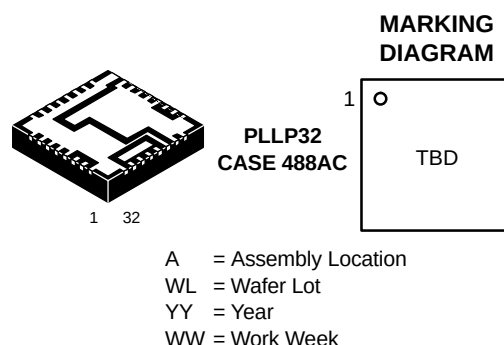
Pin	Symbol	Function
1	Anode	Power Input Connected to System
2	Internal 5.0 V	Output of Internal Voltage Regulator provides power for internal only. No external components required at this pin.
3	Gate	Gate Driver Output for Internal and External N-Channel MOSFET
4	Cathode	Power Output Connected to System
5	Reg In	Input of Internal Voltage Regulator

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PIN CONNECTIONS

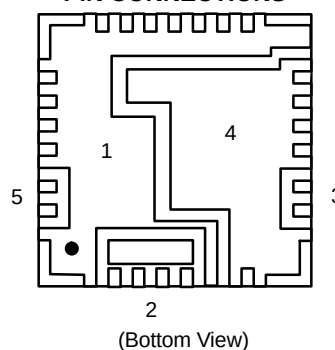
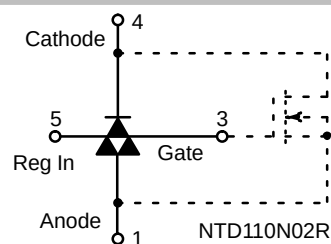


Figure 1. Equivalent Circuit

ORDERING INFORMATION

Device	Package	Shipping†
NIS6111QPT1	PLLP32	2000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NIS6111

MAXIMUM RATINGS ($T_J = 25^{\circ}\text{C}$, unless otherwise noted.)

Rating	Symbol	Value	Unit
Peak Repetitive Reverse Voltage (V_K to V_A)	V_{RRM}	24	V
Peak Regulator Input (Reg In) Voltage	$V_{reg_{max}}$	28	V
Average Rectified Forward Current	I_{FAV}	30	A
Non-repetitive Peak Surge Current	I_{FSM}	90	A
Analog Die Thermal Resistance (Min Copper Area)	$\theta_{A j-a}$	83	$^{\circ}\text{C/W}$
MOSFET Die Thermal Resistance (Min Copper Area)	$\theta_{M j-a}$	78	$^{\circ}\text{C/W}$
Analog Die Thermal Resistance (Junction-to-Top of Board)	$\theta_{A j-t}$	4.9	$^{\circ}\text{C/W}$
MOSFET Die Thermal Resistance (Junction-to-Top of Board)	$\theta_{M j-t}$	0.6	$^{\circ}\text{C/W}$
Analog Die Thermal Resistance (Junction-to-Bottom of Board) (Note 4)	$\theta_{A j-b}$	30	$^{\circ}\text{C/W}$
MOSFET Die Thermal Resistance (Junction-to-Bottom of Board) (Note 4)	$\theta_{M j-b}$	7.0	$^{\circ}\text{C/W}$
Storage Temperature Range	T_{stg}	-55 to 150	$^{\circ}\text{C}$
Operating Temperature Range	T_J	-20 to 125	$^{\circ}\text{C}$

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

NIS6111

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$, Reg In = 8.0 V, unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
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SYNCHRONOUS RECTIFIER

ON STATE

Conduction Mode ON Resistance	($I = 55\text{ A dc}$, $V_{GS} = 4.5\text{ V}$) ($I = 20\text{ A dc}$, $V_{GS} = 4.5\text{ V}$)	R_{ON}	– –	4.9 4.7	– –	$\text{m}\Omega$
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OFF STATE

Reverse Leakage Current ($V_R = 28\text{ VDC}$)	I_{DSS}	–	–	1.5	μA
Reverse Leakage Current ($V_R = 28\text{ VDC}$, $T_J = 150^\circ\text{C}$)	I_{DSS}	–	–	10	μA

SWITCHING (See Figures 2 and 4) (Note 2)

FET Turn-on Time ($I_{max} = 3.0\text{ A}$, $I_{rev} = 1.0\text{ A}$, $V_{rev} = 5.0\text{ V}$)	t_{sat}	–	45	–	ns
Reverse Recovery Time ($I_{max} = 3.0\text{ A}$, $I_{rev} = 1.0\text{ A}$, $V_{rev} = 5.0\text{ V}$)	t_{rev}	–	35	–	ns

BODY DIODE

Forward On-Voltage (Notes 1 and 3) I = 20 Adc, VGS = 0 V I = 55 Adc, VGS = 0 V	VSD	– –	0.82 0.99	1.2 –	Vdc
Reverse Recovery Time (IS = 30 Adc, di/dt = 100 A/μs)	t _{rr} t _a t _b	– – –	36.5 17.7 18.8	– – –	ns

POWER SUPPLY ($V_R = 20\text{ V}$, $T_J = 25^\circ\text{C}$)

Supply Voltage (Pin 2 to Pin 1), Internal Bias Voltage	V_{CC}	4.7	4.9	5.1	V
Cap Charge Time (Zero Initial Charge, 5.0 V @ Reg In, to UVLO Threshold, $C = 0.22\text{ }\mu\text{F}$) $T_J = -20^\circ\text{C}$ to 125°C	t_{chg} t_{chg}	– –	2.7 3.3	– –	μs μs
Headroom (for $V_{cap} = 4.7\text{ V}$)	V_{hd}	–	1.0	–	V
Minimum Duty Cycle for Operation (Freq = 100 kHz)	d_{min}	–	2.0	–	%
Charge Current	–	250	300	–	mA
Delay Time ($T_{amb} = 20^\circ\text{C}$)	T_d		51		ns

Reg In Voltage (Pin 5 to Pin 1)

Minimum Voltage Required for Operation ($V_{SD} + V_{hd}$)			4.65		V
Minimum Voltage Required for Fall Gate Drive ($V_{CC} + V_{hd}$)			5.9		

CONTROL CIRCUIT

Bias Supply Current ($f_{sw} = 100\text{ kHz}$)	I_{BIAS}	–	2.0	4.0	mA
Input Offset Voltage	I_{OS}	–	2.0	5.0	mV
Shutdown Voltage (UVLO)	V_{SD}	–	3.65	–	V

1. Pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
2. Pulse width $2.0\text{ }\mu\text{s}$, duty cycle $< 5\%$.
3. Switching characteristics are independent of operating junction temperature.
4. Based on 0.062" FR4 board, double-sided 1 oz copper.

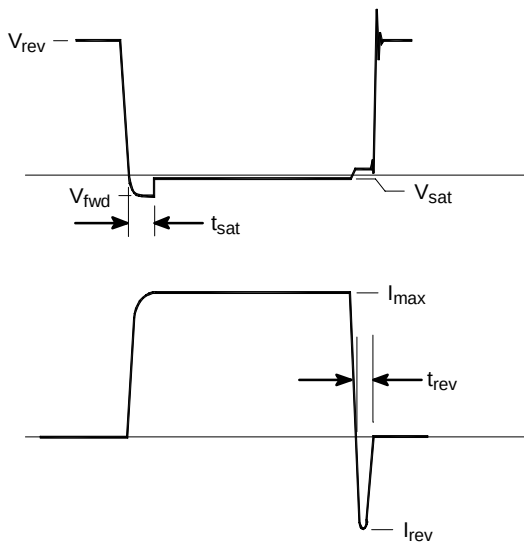


Figure 2. Switching Waveform

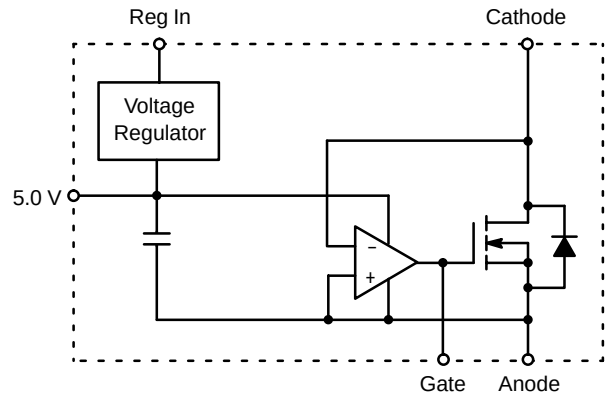


Figure 3. Functional Block Diagram

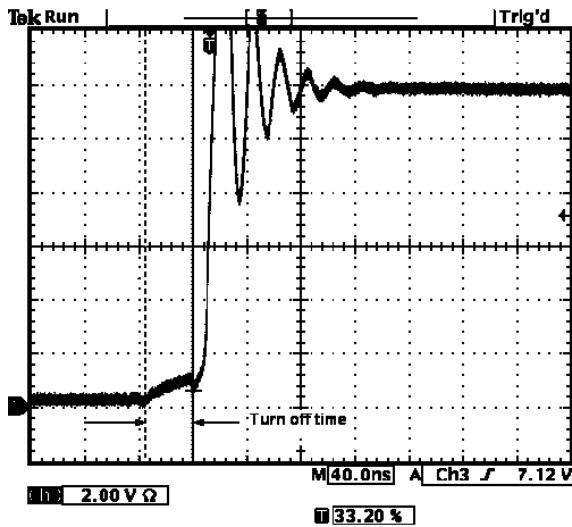


Figure 4. Synchronous Buck Turn Off Delay

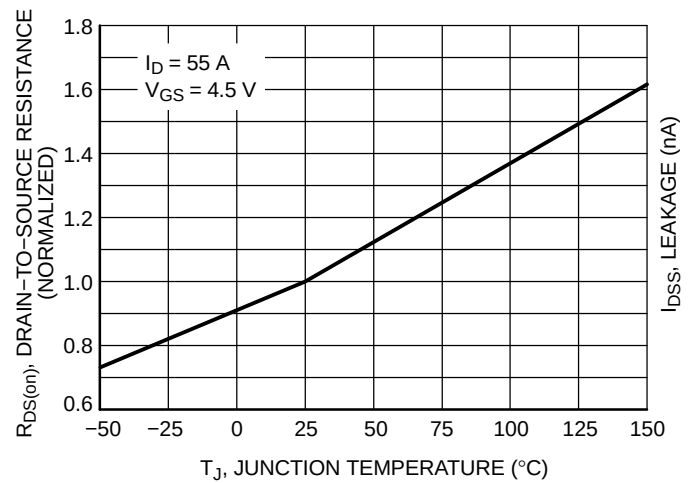


Figure 5. On-Resistance Variation with Temperature

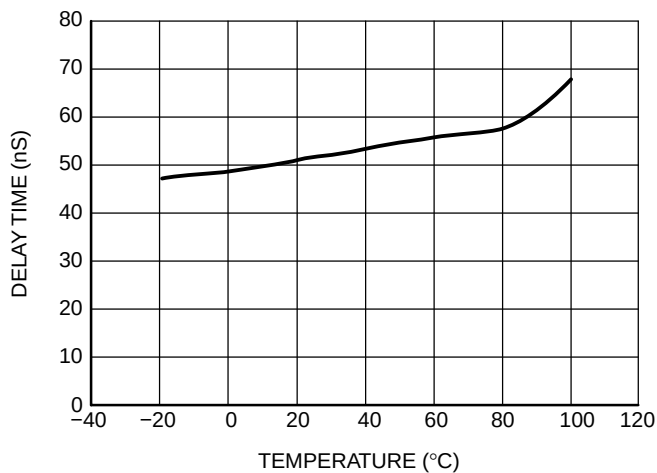


Figure 6. Delay Time versus Temperature

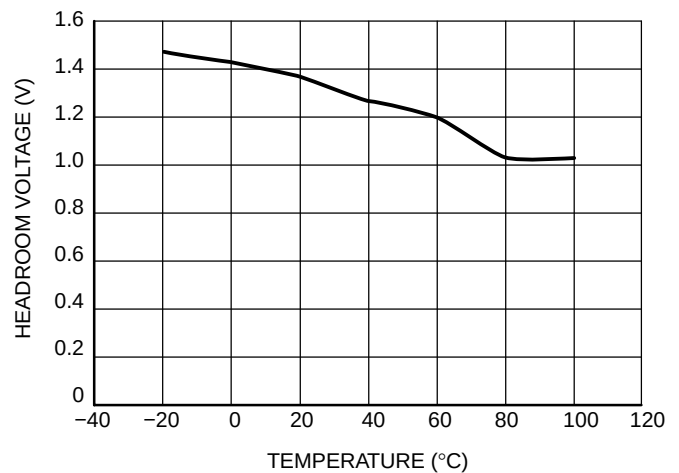


Figure 7. Headroom versus Temperature

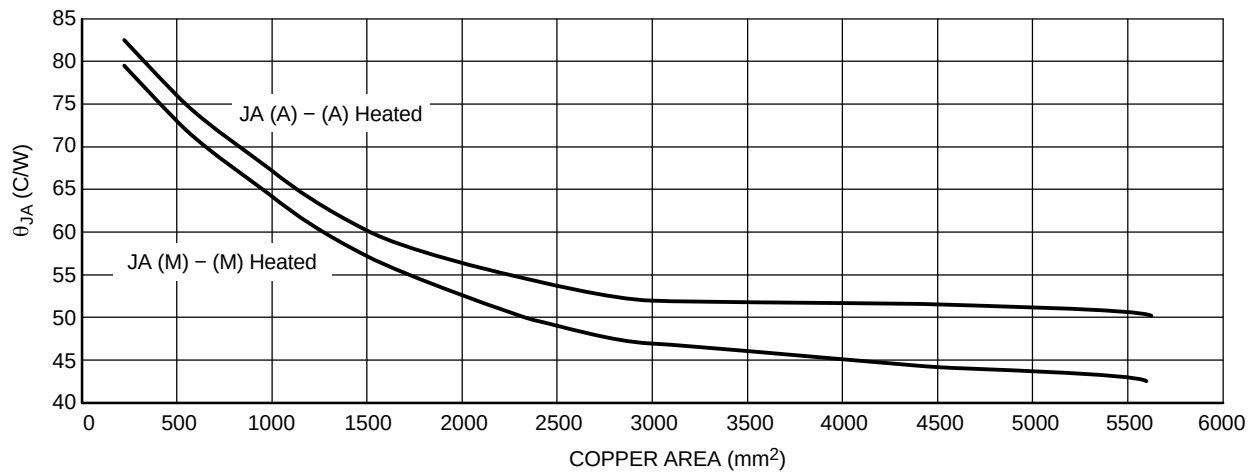


Figure 8. Thermal Resistance vs. Copper Area for MOSFET (M) and Analog Die (A)

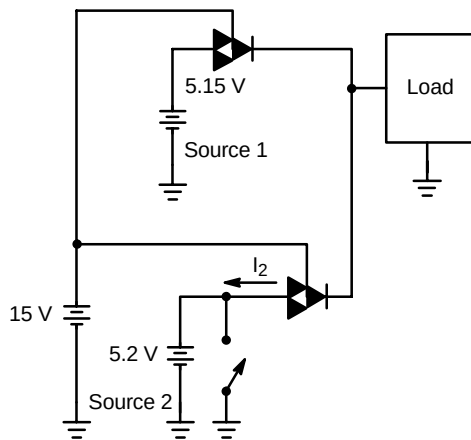


Figure 9. Test Circuit for Short Circuit ORing Test

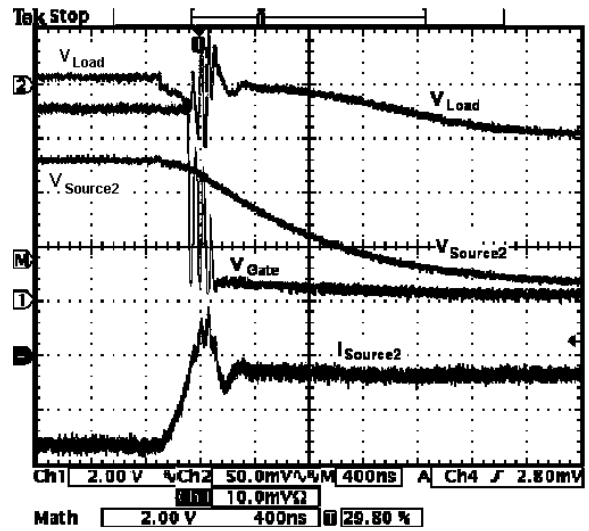


Figure 10. Waveforms from Short Circuit ORing Test

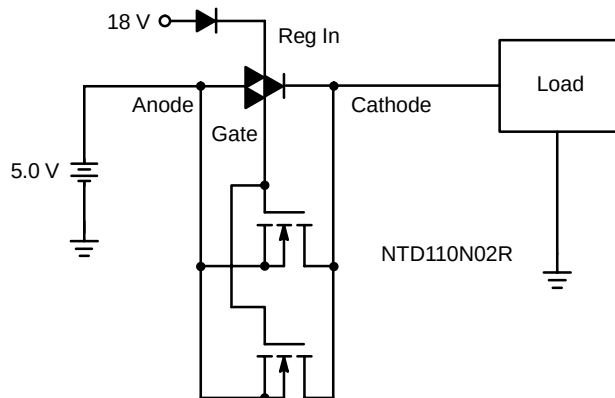


Figure 11. Positive ORing Diode Connection with Additional External FETs

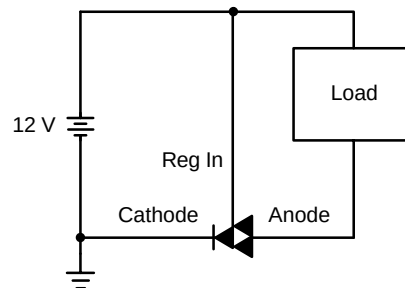


Figure 12. Negative ORing Diode Connection

OPERATING DESCRIPTION

Introduction

The BERS rectifier offers a new concept in rectification for low voltage, high current outputs. This product combines a high speed integrated circuit with a power MOSFET, to create a device with speeds better than an ultrafast silicon rectifier, and a forward drop that is less than that of a Schottky diode.

This device is specifically designed for the low voltage outputs required by today's digital circuits. Current digital products operate on voltages of less than 5.0 V and currents in the tens to hundreds of amperes. BERS can greatly increase the efficiency of low voltage, high current converters, by reducing the rectifier drop to several hundred millivolts.

This device consists of four major circuits as well as a capacitor. BERS contains a power supply to regulate the voltage on the bias supply cap, a high speed comparator to sense the conduction state of the device, a high speed driver, a power FET and a capacitor.

Bias Supply

The internal bias supply is a high current, switching regulator. It will maintain a regulated voltage on the internal capacitor as long as sufficient voltage is available at the Reg In pin. When this pin is high, a current limited switch allows current to charge the capacitor. When the

maximum charge voltage is reached, the switch is turned off. If there is not sufficient reverse voltage to maintain a 5.0 V charge on the capacitor, the bias supply will charge it to within 1.0 V of the reverse voltage.

The Regulator Input pin can be connected to the cathode and will recharge the internal capacitor when the BERS is reversed biased. This input requires a minimum voltage of 4.7 V to operate. In some cases this amount of reverse voltage may not be available. When this is the case, the Reg In pin can be connected to a higher voltage source. It is not necessary that this source be synchronous with the cathode voltage.

The Reg In voltage should not be allowed to go more negative than the anode of the device. If this scenario can occur, a small switching diode should be placed in series with the Reg In pin.

Comparator/Driver

The polarity comparator is a medium gain, ultra high speed design. It is integrated with the driver circuit, to optimize the switching speed of the device. The comparator input has a low offset voltage which biases the inverting input several millivolts above ground. This is to assure that at zero (or very low) current levels, the device is off.

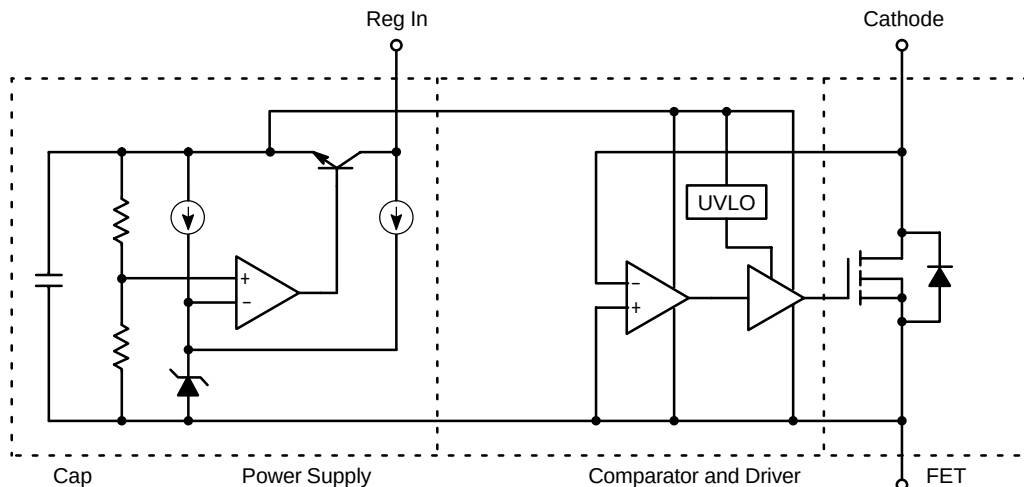
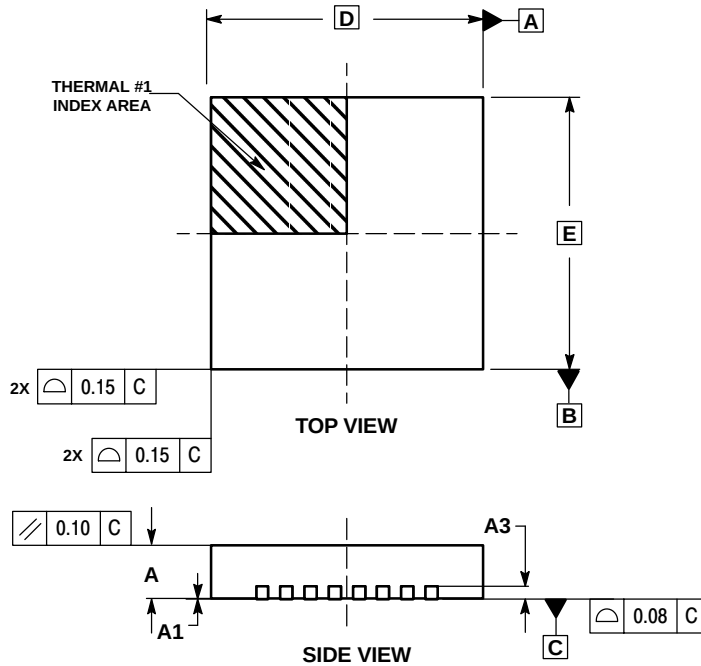
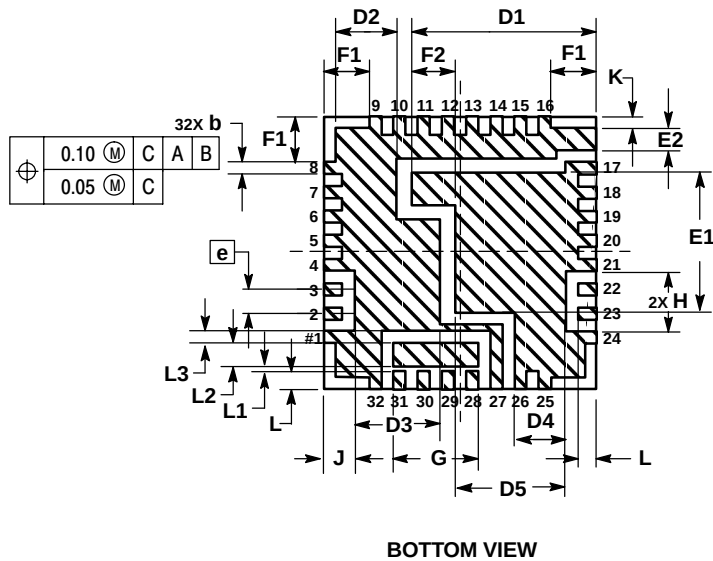


Figure 13. Detailed Block Diagram

PACKAGE DIMENSIONS

PLLP32
CASE 488AC-01
ISSUE A



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 MM AND 40 MM FROM TERMINAL TIP
4. UNILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THEIR TERMINALS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	1.750	1.850	1.950
A1	0.000	----	0.050
A3	0.254 REF		
b	0.350	0.400	0.450
D	9.000 BSC		
D1	5.987	6.087	6.187
D2	1.924	2.024	2.124
D3	2.713	2.813	2.913
D4	1.584	1.684	1.784
D5	3.547	3.647	3.747
E	9.000 BSC		
E1	4.472	4.572	4.672
E2	0.638	0.738	0.838
e	0.800 BSC		
F1	1.500 REF		
F2	1.324	1.424	1.524
G	2.700	2.800	2.900
H	2.000 REF		
J	1.016 BSC		
K	0.381 REF		
L	0.500	0.600	0.700
L1	0.062	0.162	0.262
L2	0.760	0.770	0.870
L3	0.281	0.381	0.481

The product described herein (NIS6111), may be covered by U.S. patents including 6,271,712. There may be other patents pending.

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