CY24130

HOTLink II™ SMPTE Receiver Training Clock

Features

- Integrated phase-locked loop
- Low-jitter, high-accuracy outputs
- 3.3V operation

Benefits

- Internal PLL with up to 400-MHz internal operation
- Meets critical timing requirements in complex system designs
- Enables application compatibility

Table 1. Frequency table

Part Number	Outputs	Input Frequency	Output Frequency Range
CY24130-1	2	27 MHz (Driven Reference)	1 copy 27-MHz reference clock output 1 copy of 27-/36-/54-/148.5-/74.25-MHz (frequency selectable)
CY24130-2	2	27 MHz (Crystal Reference)	1 copy 27-MHz reference clock output 1 copy of 27-/36-/54-/148.5-/74.25-MHz (frequency selectable)

Logic Block Diagram

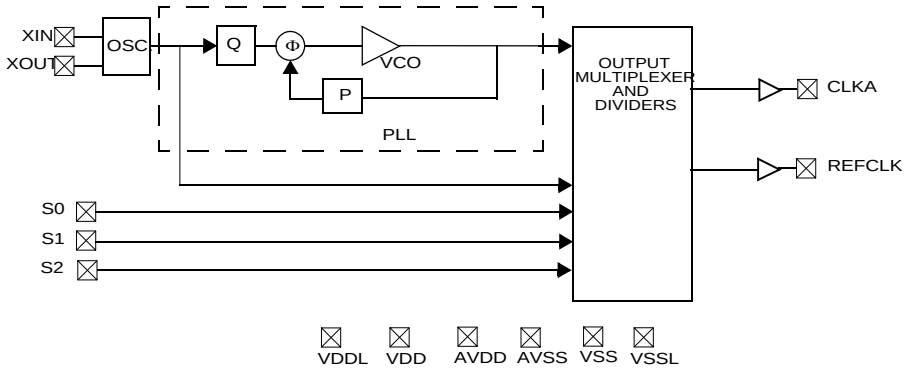


Table 2. Frequency Select Options

S2	S1	S0	CLKA	REFCLK	Units
0	0	0	27	27	MHz
0	0	1	36	27	MHz
0	1	0	54	27	MHz
0	1	1	148.50	27	MHz
1	0	0	74.25	27	MHz
1	0	1	OFF, pulled low	27	MHz
1	1	0	OFF, pulled low	27	MHz
1	1	1	OFF, pulled low	27	MHz

Pin Configuration

Figure 1. CY24130-1, -2, 16-pin TSSOP

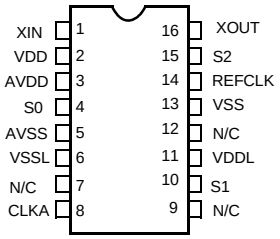


Table 3. Pin Definition

Name	Pin Number	Description
XIN	1	Reference Crystal Input.
V_{DD}	2	Voltage Supply.
AV_{DD}	3	Analog Voltage Supply.
S0	4	Frequency Select 0.
AV_{SS}	5	Analog Ground.
V_{SSL}	6	VDDL Ground.
N/C	7	No Connect.
CLKA	8	27-/36-/54-/148.50-/74.25-MHz Clock Output (frequency selectable).
N/C	9	No Connect.
S1	10	Frequency Select 1.
V_{DDL}	11	Voltage Supply.
N/C	12	No Connect.
VSS	13	Ground.
REFCLK	14	Reference Clock Output.
S2	15	Frequency Select 2.
XOUT	16	Reference Crystal Output. Leave floating for -1.

Absolute Maximum Conditions

Parameter	Description	Min.	Max.	Unit
$V_{DD,}$ AV_{DD}	Supply Voltage	–0.5	7.0	V
V_{DDL}	I/O Supply Voltage	–	7.0	V
T_J	Junction Temperature	–	125	°C
	Digital Inputs	AV_{SS} – 0.3	AV_{DD} + 0.3	V
	Electro-Static Discharge	2	–	kV

Recommended Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Unit
$V_{DD}/AV_{DDL}/V_{DDL}$	Operating Voltage	3.135	3.3	3.465	V
T_A	Ambient Temperature	0	–	70	°C
C_{LOAD}	Max. Load Capacitance	–	–	15	pF
f_{REF}	Reference Frequency	–	27	–	MHz
C_{LNOM}	Nominal Parallel Crystal Load Capacitance for -2	–	18	–	pF

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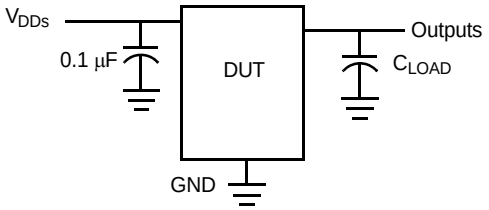
DC Electrical Specifications

Parameter[1]	Name	Description	Min.	Typ.	Max.	Unit
I_{OH}	Output High Current	$V_{OH} = V_{DD} – 0.5$, $V_{DD}/V_{DDL} = 3.3V$	12	24	–	mA
I_{OL}	Output Low Current	$V_{OL} = 0.5$, $V_{DD}/V_{DDL} = 3.3V$	12	24	–	mA
I_{IH}	Input High Current	$V_{IH} = V_{DD}$	–	5	10	µA
I_{IL}	Input Low Current	$V_{IL} = 0V$	–	–	10	µA
V_{IH}	Input High Voltage	CMOS levels, 70% of V_{DD}	0.7	–	–	V
V_{IL}	Input Low Voltage	CMOS levels, 30% of V_{DD}	–	–	0.3	V
I_{VDD}	Supply Current	AV_{DD}/V_{DD} Current	–	16	–	mA
I_{VDDL}	Supply Current	V_{DDL} Current	–	14	–	mA

AC Electrical Specifications

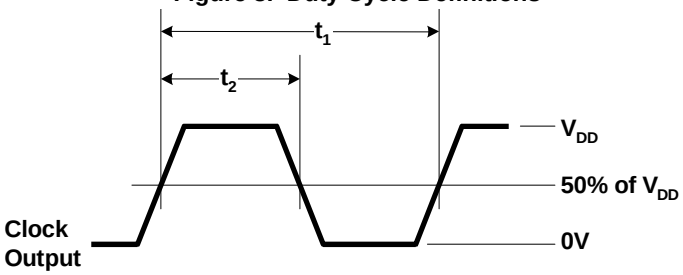
Parameter[1]	Name	Description	Min.	Typ.	Max.	Unit
DC	Output Duty Cycle	Duty Cycle is defined in Figure 3; t_1/t_2, 50% of V_{DD}	45	50	55	%
ER	Rising Edge Rate	Output Clock Edge Rate, Measured from 20% to 80% of V_{DD}, C_{LOAD} = 15 pF. See Figure 4.	0.8	1.4	–	V/ns
EF	Falling Edge Rate	Output Clock Edge Rate, Measured from 80% to 20% of V_{DD}, C_{LOAD} = 15 pF. See Figure 4.	0.8	1.4	–	V/ns
t_9	Clock Jitter	CLKA Peak-Peak Period Jitter	–	100	–	ps
t_{10}	PLL Lock Time		–	–	3	ms

Figure 2. Test and Measurement Setup



Voltage and Timing Definitions

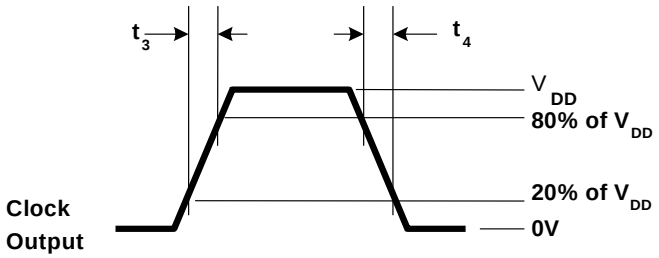
Figure 3. Duty Cycle Definitions



Note
1. Not 100% tested.

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Figure 4. ER = (0.6 x V_{DD}) /t_3, EF = (0.6 x V_{DD}) /t_4



Ordering Information

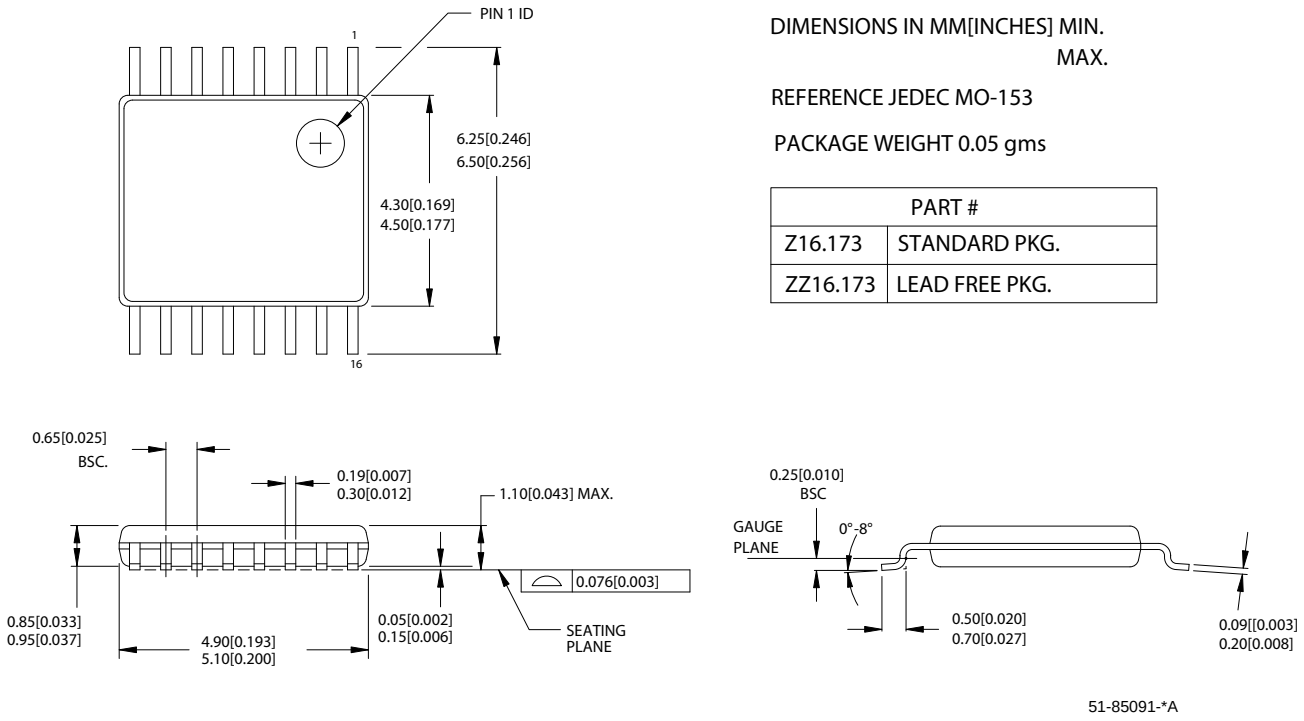
Ordering Code	Package Type	Operating Range	Operating Voltage
Pb-free			
CY24130ZXC-1[2]	16-Pin TSSOP	Commercial	3.3V
CY24130ZXC-1T[2]	16-Pin TSSOP – Tape and Reel	Commercial	3.3V
CY24130ZXC-2[2]	16-Pin TSSOP	Commercial	3.3V
CY24130ZXC-2T[2]	16-Pin TSSOP – Tape and Reel	Commercial	3.3V
CY24130KZXC-1	16-Pin TSSOP	Commercial	3.3V
CY24130KZXC-1T	16-Pin TSSOP – Tape and Reel	Commercial	3.3V

Note
2. Not recommended for new design.

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Package Drawing and Dimensions

Figure 5. 16-lead TSSOP 4.40 MM Body Z16.173



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Document History Page

Document Title: CY24130 HOTLink II™ SMPTE Receiver Training Clock Document Number: 38-07711				
REV.	**ECN NO.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	314514	RGL	See ECN	New Data Sheet
*A	2442066	AESA	See ECN	Updated template. Added Note “Not recommended for new designs.” Added part number CY24130KZXC-1, and CY24130KZXC-1T in ordering information table.

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