FEATURES

- **USB On-the-Go (OTG) Controller Core**
  - **Uses Mentor Graphics USB 2.0 OTG Core**
  - **Dual-Role Controller Can Operate Either as a Function Controller for a USB Peripheral or as the Host/Peripheral in Point-to-Point or Multipoint Communications With Other USB Functions**
  - **Compliant With the USB 2.0 Standard for High-Speed (480-Mbps) Functions and With OTG Supplement to USB 2.0 Specification**
  - **Supports OTG Communications With One or More High-, Full-, or Low-Speed Devices**
  - **Supports Session Request Protocol (SRP) and Host Negotiation Protocol (HNP)**
  - **Supports Suspend-and-Resume Signaling**
  - **Configurable for up to 4 Transmit Endpoints or up to 4 Receive Endpoints**
  - **Configurable FIFOs, Including the Option of Dynamic FIFO Sizing**
  - **16k-Byte RAM for USB Endpoint FIFO Shared by USB In/Out Endpoints**
  - **Support for External Direct Memory Access (DMA) to FIFOs**
  - **Soft Connect/Disconnect Option**
  - **Performs All Transaction Scheduling in Hardware**
- **System Control Module**
  - **Controls Clock and Reset Generation and Distribution**
  - **Controls and Observes Device Power States**
  - **Supports External Power Management**
- **Integrated USB 2.0 OTG PHY**
  - **Fully Compliant with USB 2.0 Standard and USB 2.0 Transceiver Macrocell Interface (UTMI) Revision 1.05**
  - **Optimized One-Port Operation at Low Speed (1.5 Mbps), Full Speed (12 Mbps), and High Speed (480 Mbps)**
  - **Supports UTMI+3 Level 3 (Host and OTG Devices, High/Full/Low Speed and Preamble Packet)**
  - **Protection Circuitry to Withstand Possible VBUS Short**
  - **Use 19.200-MHz or 24.000-MHz Reference Clock Input as a Crystal or External Clock Driver**
  - **At-Speed Built-In Self Test (BIST) With Internal Asynchronous Capability Through Loopback**
  - **On-Chip Integrated Accurate 45-Ω High-Speed Termination, 1.5-kΩ Pullup, and 15-kΩ Pulldown Resistors**
  - **On-Chip Phase-Locked Loop (PLL) to Reduce Noise on High-Speed Clocks**
  - **Active Power Consumption Less Than 100 mW**
- **VLYNQ 2.0 Interface to External Host Controller**
  - **High-Speed (150-MHz) Point-to-Point Serial Interface for Direct Connection to Other VLYNQ Interface**
  - **Supports 4 Receive (RX) and 4 Transmit (TX) Lines**
  - **Memory-Mapped Master/Slave**
  - **Hardware Flow Control Internal Loopback Mode**
  - **Multichannel DMA Controller**
  - **Integrated List Processor Capable of Parsing Communications Port Programming Interface (CPPI) 3.0-Compliant Buffer Descriptors**
- **High-Performance 80-Pin MicroStar BGA™/MicroStar Junior™ ZQE Package**
- **High-Performance 80-Pin PFC Package**

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DESCRIPTION/ORDERING INFORMATION

The TUSB6020 is a USB 2.0 high-speed, on-the-go (OTG) dual-role controller designed for a seamless interface to the VLYNQ serial interface, and is ideal for a wide range of applications. The USB OTG dual-role controller can operate either as a function controller for a USB peripheral or as the host/peripheral in point-to-point or multipoint communications with other functions. The integrated USB 2.0 PHY provides one-port operation at low speed (1.5 Mbps), full speed (12 Mbps), and high speed (480 Mbps). The VLYNQ serial interface is a low pin count, high-speed, point-to-point interface.

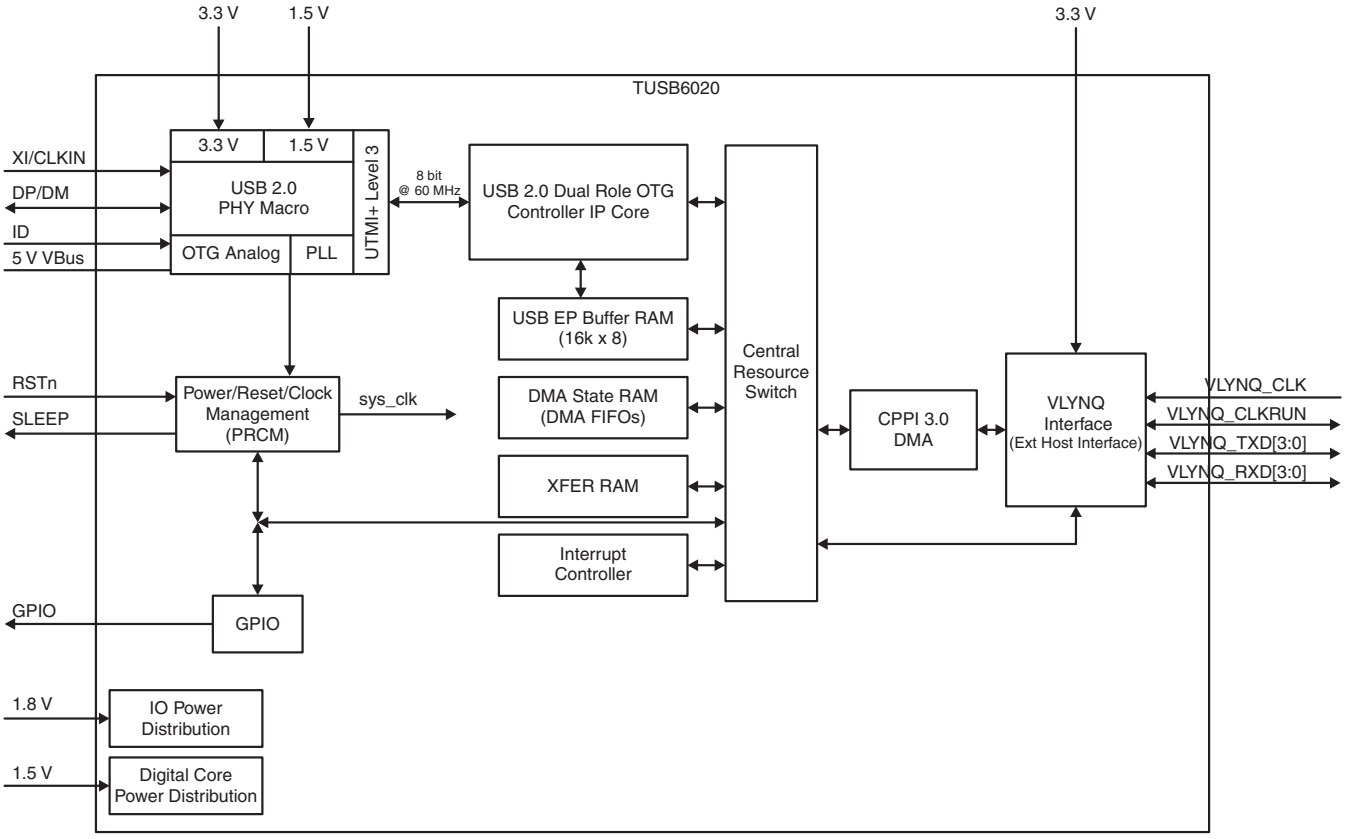
The device is fully compliant with *Universal Serial Bus Specification Revision 2.0* and *On-the-Go Supplement to the USB Specification* Revision 1.3.

ORDERING INFORMATION

T_A	PACKAGE(1)(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	MicroStar BGA™ – ZQE	Reel of 360	TUSB6020ZQE	PREVIEW
	TQFP – PFC	Tube of 96	TUSB6020PFC	PREVIEW

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

BLOCK DIAGRAM



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TERMINAL FUNCTIONS

TERMINAL			TYPE	I/O	RESET STATE	DESCRIPTION
NAME	ZQE NO.	PFC NO.				
1.5V_SWEN	G2	18	LVCMOS	O	0	Switch enable for 1.5-V LDO for VBAT/VBUS switch
3.3V_SWEN	G3	19	LVCMOS	O	0	Switch enable for 3.3-V CP/LDO for VBAT/VBUS switch
CLKIN	A5	71	LVCMOS failsafe(1)	I	In	19.2-MHz system clock in. Connect directly to ground if not used.
CPEN	H2	22	LVCMOS	O	0	5-V power distribution switch enable
DM	E2	10	USB	I/O	–	USB differential pair
DP	D1	9	USB	I/O	–	USB differential pair
GPIO0	H4	26	LVCMOS	I/O	In with pullup	GPIO 0
GPIO1	D5	68	LVCMOS	I/O	In with pullup	GPIO 1
GPIO2	B6	66	LVCMOS	I/O	In with pullup	GPIO 2
GPIO3	E6	54	LVCMOS	I/O	In with pullup	GPIO 3
GPIO4	C4	79	LVCMOS	I/O	In with pullup	GPIO 4
GPIO5	C9	55	LVCMOS	I	In with pullup	GPIO 5
GPIO6	F5	27	LVCMOS	I/O	In with pullup	GPIO 6. Input clock source select at reset. GPIO6 = HIGH, CLKIN is reference clock. GPIO6 = LOW, XI is reference clock.
GPIO7	B2	2	LVCMOS	I/O	In with pullup	GPIO 7. Must be pulled low for proper operation. It is recommended to tie this signal directly to GND.
ID	F2	15	USB	I	–	Indicates default master for OTG. For more information, see *On-the-Go Supplement to the USB Specification*, *Revision 1.2*.
R1	C2	5	Bias	I	–	High-precision external resistor used for calibration (R1 value: 10.7 kΩ ±1%)
RSTn	H1	20	LVCMOS	I	In with pullup	Reset active low
RSVD	A8, B7, B8, B9, C6, C7, C8, D6, D8, E7, G4, J5	64, 65, 62, 58, 63, 60, 57, 59, 53, 50, 23, 31	–	–	–	Reserved, must be pulled low by individual pulldown resistors. A 1-kΩ value is recommended.
RSVD – NC	G5, H5, J4, F6	29, 30, 28, 32	–	–	–	Reserved, should be left unconnected
SLEEP	H3	24	LVCMOS	O	0	OTG sleep
TEST	D4	80	LVCMOS	I	–	Test mode. Under normal operation, this signal should be tied directly to GND.
VBUS	F3	16	USB	I	–	Charged, discharged, and monitored for OTG host negotiation protocol and session request protocol. External power distribution switch provides up to 500 mA.
VDD15	A1, A9, B3, C5, D7, J3	1, 25, 56, 61, 72, 77	Supply	–	–	Digital core power supply, 1.5 V
VDD18	A7, B5, E8, J1	21, 49, 67, 70	Supply	–	–	I/O power supply, 1.8 V
VDDA1P5	E3	11	Supply	–	–	1.5-V analog supply
VDDA3P3	C1	7	Supply	–	–	3.3-V analog supply
VDDCM1P5	D2	6	Supply	–	–	1.5-V PLL supply
VDDD1P5	F1	14	Supply	–	–	1.5-V digital supply
VDDS3P3	F8, G6, J9	33, 39, 44	Supply	–	–	VLYNQ supply, 3.3 V

(1) Failsafe means that CLKIN can toggle when VDD18 is not present without damaging the part.

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TERMINAL FUNCTIONS (continued)

TERMINAL			TYPE	I/O	RESET STATE	DESCRIPTION
NAME	ZQE NO.	PFC NO.				
VLYNQ_CLK	F9	45	LVCMOS 3.3-V VLYNQ	I	In with pullup	VLYNQ clock
VLYNQ_CRUN	E9	48	LVCMOS 3.3-V VLYNQ open drain	I/O	In with pullup	VLYNQ clock run
VLYNQ_RXD0	H7	38	LVCMOS 3.3-V VLYNQ	I	In with pullup	VLYNQ receive data bit 0
VLYNQ_RXD1	J7	37	LVCMOS 3.3-V VLYNQ	I	In with pullup	VLYNQ receive data bit 1
VLYNQ_RXD2	H6	35	LVCMOS 3.3-V VLYNQ	I	In with pullup	VLYNQ receive data bit 2
VLYNQ_RXD3	J6	34	LVCMOS 3.3-V VLYNQ	I	In with pullup	VLYNQ receive data bit 3
VLYNQ_TXD0	H9	40	LVCMOS 3.3-V VLYNQ	O	In with pullup	VLYNQ transmit data bit 0
VLYNQ_TXD1	G9	42	LVCMOS 3.3-V VLYNQ	O	In with pullup	VLYNQ transmit data bit 1
VLYNQ_TXD2	H8	43	LVCMOS 3.3-V VLYNQ	O	In with pullup	VLYNQ transmit data bit 2
VLYNQ_TXD3	F7	47	LVCMOS 3.3-V VLYNQ	O	In with pullup	VLYNQ transmit data bit 3
VSS	A2, A6, B4, D9, E5, G1, G7, G8, J2, J8	17, 36, 41, 46, 51, 52, 69, 74, 76, 78	Supply	–	–	Ground
VSSA1P5	E1	12	Supply	–	–	1.5-V analog ground
VSSA3P3	E4	8	Supply	–	–	3.3-V analog ground
VSSCM1P5	D3	3	Supply	–	–	1.5-V PLL ground
VSSD1P5	F4	13	Supply	–	–	1.5-V digital ground
VSSREF	B1	4	Supply	–	–	Ground for the reference circuits
XI	A4	73	Crystal	I	In	Crystal input. Should be left unconnected if not used.
XO	A3	75	Crystal	O	In	Crystal output. Should be left unconnected if not used.

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ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{DDA3P3}	3.3-V supply voltage		–0.5	4.2	V
V_{DDS3P3}					
V_{DD18}	1.8-V supply votlage		–0.5	2.1	V
V_{DD15}	1.5-V supply voltage		–0.5	2.1	V
V_{DDD1P5}					
$V_{DDCM1P5}$					
V_{DDA1P5}					
V_I	Input voltage range	3.3-V USB	–0.5	V_{DDA3P3} +0.5	V
$V_{I\text{-}VLYNQ}$		3.3-V VLYNQ	–0.5	V_{DDS3P3} +0.5	
V_O	Output voltage range	3.3-V USB	–0.5	V_{DDA3P3} +0.5	V
$V_{O\text{-}VLYNQ}$		3.3-V VLYNQ	–0.5	V_{DDS3P3} +0.5	
V_{DD}	Core supply voltage		–0.5	2.1	mA
I_{IK}	Input clamp current			±20	mA
I_{OK}	Output clamp current			±20	mA
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

			MIN	TYP	MAX	UNIT
V_{DDA3P3}	Supply voltage	OTG PHY analog	3	3.3	3.6	V
V_{DDS3P3}		VLYNQ digital				
V_{DD18}	Supply voltage	Digital I/O	1.62	1.8	1.98	V
V_{DD15}	Supply voltage	Digital core	1.35	1.5	1.65	V
V_{DDD1P5}		OTG PHY digital				
$V_{DDCM1P5}$		OTG PHY common module				
V_{DDA1P5}		OTG PHY analog				
T_A	Operating temperature		0		70	°C
T_J	Operating junction temperature		0			°C

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DIGITAL I/O

Electrical Characteristics

T_A = 0°C to 70°C, V_{DD18} = 1.8 V ± 10%, V_{DDS3P3} = 3.3 V ± 10%, V_{SS} = 0 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{I\text{-}VLYNQ}$	Input voltage	3.3-V LVCMOS (VLYNQ only)		0		V_{DDS3P3}	V
V_I		LVCMOS		0		V_{DD18}	
$V_{O\text{-}VLYNQ}$	Output voltage	3.3-V LVCMOS (VLYNQ only)		0		V_{DDS3P3}	V
V_O		LVCMOS		0		V_{DD18}	
$V_{IH\text{-}VLYNQ}$	High-level input voltage	3.3-V LVCMOS (VLYNQ only)		$0.7 \times V_{DDS3P3}$		V_{DDS3P3}	V
V_{IH}		LVCMOS		$0.7 \times V_{DD18}$		V_{DD18}	
$V_{IL\text{-}VLYNQ}$	Low-level input voltage	3.3-V LVCMOS (VLYNQ only)		0		$0.3 \times V_{DDS3P3}$	V
V_{IL}		LVCMOS		0		$0.3 \times V_{DD18}$	
V_{OH}	High-level output voltage	LVCMOS		$0.8 \times V_{DD18}$			V
V_{OL}	Low-level output voltage	LVCMOS open drain	I_{OL} = 4 mA			$0.22 \times V_{DDS3P3}$	V
		LVCMOS	I_{OL} = 8 mA			$0.22 \times V_{DD18}$	
		LVCMOS (1.5V_SWEN, 3.3V_SWEN only)	I_{OL} = 100 µA		10		mV
I_{IH}	High-level input current	LVCMOS	$V_I = V_I$ max			±1	µA
I_{IL}	Low-level input current	LVCMOS	$V_I = V_I$ min			±1	µA
I_{OZ}	Output leakage current (high Z)		$V_I = V_I$ max or V_{SS}			±20	µA
C_i	Input capacitance				2		pF
t_r, t_f	Input rise/fall time			0		25	ns

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SUPPLY CURRENT

Device Power Consumption(1)

T_A = 0°C to 70°C, V_{DD15} = 1.5 V ± 10%, V_{DD18} = 1.8 V ± 10%, V_{DDA1P5} = 1.5 V ± 10%, V_{DDA3P3} = 3.3 V ± 10%, V_{DDS3P3} = 3.3 V ± 10%, V_{DDD1P5} = 1.5 V ± 10%, $V_{DDCM1P5}$ = 1.5 V ± 10%, V_{SS} = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	I_{DD} = 1.5 V (TOTAL)			I_{DD} = 1.8 V			I_{DD} = 3.3 V (TOTAL)			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
I_{DD}	Input supply current	Power down (Idle)(2)		2.6	5.0		0.26	10.5		4.1	4.8	mA
		No bus activity(3)		60.1	71.2		0.21	10.5		12.7	14.5	
		Active (transmit/receive)(4)		66.2	78.1		0.22	10.5		14.4	16.6	
		Reset(5)										

(1) Minimum, typical, and maximum current values are average values.
(2) PmIdle bit set in Device PRCM management register
(3) Normal operation with no USB connection
(4) Bulk IN and OUT on one endpoint. Packet size is 512 bytes.
(5) Device RSTn asserted

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INTEGRATED USB 2.0 TRANSCEIVER

Electrical Characteristics – V_{bus}

T_A = 0°C to 70°C, V_{DD15} = 1.5 V ± 10%, V_{DD18} = 1.8V ± 10%, V_{DDA1P5} = 1.5 V ± 10%, V_{DDA3P3} = 3.3 V ± 10%, V_{DDS3P3} = 3.3 V ± 10%, V_{DDD1P5} = 1.5 V ± 10%, $V_{DDCM1P5}$ = 1.5 V ± 10%, V_{SS} = 0 V (unless otherwise noted)(1)

PARAMETER	MIN	MAX	UNIT
V_{bus} input impedance	360	690	kΩ
V_{bus} valid comparator	4.4	4.75	V
V_{bus} SRP charge pullup value	281	1950	Ω
V_{bus} SRP discharge pulldown value	656	1850	Ω
V_{bus} leakage current (when device is powered off)		11	µA

(1) Characterization only. Limits approved by design.

Electrical Characteristics – DP and DM

T_A = 0°C to 70°C, V_{DD15} = 1.5 V ± 10%, V_{DD18} = 1.8 V ± 10%, V_{DDA1P5} = 1.5 V ± 10%, V_{DDA3P3} = 3.3 V ± 10%, V_{DDS3P3} = 3.3 V ± 10%, V_{DDD1P5} = 1.5 V ± 10%, $V_{DDCM1P5}$ = 1.5 V ± 10%, V_{SS} = 0 V (unless otherwise noted)(1)

PARAMETER		MIN	MAX	UNIT
Input Levels for Full Speed				
V_{DI}	Full-speed differential input threshold	0.2		V
V_{CM}	Input (was differential) common mode range	0.8	2.5	V
Input Levels for High Speed				
$V_{(HSSQ)}$	High-speed squelch detection threshold (differential signal amplitude)	100	1520	mV
V_{DI}	High-speed differential input threshold voltage	100		mV
Output Levels for Full Speed				
V_{OL}	Low-level output voltage	0	0.3	V
V_{OH}	High-level output voltage (driven)	2.8	3.6	V
$V_{O(SE1)}$	Output voltage on SE1	0.8		V
$V_{O(CRS)}$	Output signal crossover voltage	1.3	2	V
Output Levels for High Speed				
$V_{(HSOI)}$	High-speed idle level	–10	10	mV
$V_{(HSOH)}$	High-speed data signaling high	360	440	mV
$V_{(HSOL)}$	High-speed data signaling low	–10	10	mV
$V_{ID(CHIRPJ)}$	Chirp J level (differential voltage)	700	1100	mV
$V_{ID(CHIRPK)}$	Chirp K level (differential voltage)	–900	–500	mV
Driver Characteristics (Full Speed)				
t_r	Full-speed rise time	4	20	ns
t_f	Full-speed fall time	4	20	ns
$t_{(RFM)}$	Full-speed rise/fall time matching	90%	110%	
Driver Characteristics (High Speed)				
t_r	Rise time (10%-90%)	500		ps
t_f	Fall time (10%-90%)	500		ps
$ro_{(HSDRV)}$	Driver output resistance (serves as a high-speed termination)	40.5	49.5	Ω
$t_{(RFM)}$	Differential rise and fall time matching	90%	111.11%	
Clock Timings				
$t_{(HSDRAT)}$	High-speed data rate	479.76	480.24	Mb/s

(1) Characterization only. Limits approved by design.

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Electrical Characteristics – DP and DM (continued)

T_A = 0°C to 70°C, V_{DD15} = 1.5 V ± 10%, V_{DD18} = 1.8 V ± 10%, V_{DDA1P5} = 1.5 V ± 10%, V_{DDA3P3} = 3.3 V ± 10%, V_{DDS3P3} = 3.3 V ± 10%, V_{DDD1P5} = 1.5 V ± 10%, $V_{DDCM1P5}$ = 1.5 V ± 10%, V_{SS} = 0 V (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
Single-Ended Receiver				
V_{IT+}	Positive-going input threshold voltage		2.0	V
V_{IT-}	Negative-going input threshold voltage	0.8		V
V_{hys}	Hysteresis voltage	200	500	mV
Input Leakage				
DP	Measurement taken with pulldown disabled and device in idle mode		10	nA
DM	Measurement taken with pulldown disabled and device in idle mode		10	nA

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VLYNQ INTERFACE

Electrical Characteristics

T_A = 0°C to 70°C, V_{DD15} = 1.5 V ± 10%, V_{DD18} = 1.8 V ±10%, V_{DDA1P5} = 1.5 V ± 10%, V_{DDA3P3} = 3.3 V ± 10%, V_{DDS3P3} = 3.3 V ± 10%, V_{DDD1P5} = 1.5 V ± 10%, $V_{DDCM1P5}$ = 1.5 V ± 10%, V_{SS} = 0 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{OL}	Low-level input current	LVCMOS			8		mA
I_{OH}	High-level input current	LVCMOS			–8		mA
V_{OH}	High-level output voltage	LVCMOS	I_O = –100 µA	V_{DDS3P3} – 0.2			V
			$I_O = I_{OH}$	$0.8 \times V_{DDSS3P3}$			
V_{OL}	Low-level output voltage	LVCMOS	I_O = 100 µA			0.2	V
			$I_O = I_{OL}$			$0.22 \times V_{DDS}S3P3$	
V_{hys}	Hysteresis	LVCMOS	$V_{I\text{-}VLYNQ} = V_{IH\text{-}VLYNQ}$		$0.13 \times V_{DDSS3P3}$		V
I_{IH}	High-level input current	Receiver only	$V_{I\text{-}VLYNQ} = V_{I\text{-}VLYNQ}$ max			±1	µA
I_{IL}	Low-level input current	Receiver only	$V_{I\text{-}VLYNQ} = V_{I\text{-}VLYNQ}$ min			±1	µA
I_{OZ}	Output leakage current (Hi-Z)	Driver only	Driver disabled			±20	µA

Switching Characteristics

T_A = 0°C to 70°C, V_{DD15} = 1.5 V ± 10%, V_{DD18} = 1.8 V ±10%, V_{DDA1P5} = 1.5 V ± 10%, V_{DDA3P3} = 3.3 V ± 10%, V_{DDS3P3} = 3.3 V ± 10%, V_{DDD1P5} = 1.5 V ± 10%, $V_{DDCM1P5}$ = 1.5 V ± 10%, V_{SS} = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYP	UNIT
Driver Characteristics				
t_r	Rise time (between 10% and 90% swing of 3.3 V)	Load: C_L = 10 pF	1.68	ns
		Load: C_L = 50 pF	6.56	
		Load: C_L = 125 pF	15.78	
t_f	Fall time (between 90% and 10% swing of 3.3 V)	Load: C_L = 5 pF	2.09	ns
		Load: C_L = 5 pF	8.19	
		Load: C_L = 15 pF	19.75	

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APPLICATION INFORMATION

Power-On Reset

The system reset function ensures an orderly start-up sequence for the TUSB6020. There is one active-low external system reset (RSTn) input . The reset initializes the power/reset/clock manager (PRCM) module, which in turn generates all the internal resets to initialize USB 2.0 OTG PHY macro and synchronous logic in the core. While reset is asserted (active low), dual functional pins are sampled to determine device configuration after reset. Since the TUSB6020 relies on dual function pins to configure the device during reset, the reset must be sufficiently long for (external) marginal pullup/pulldown to achieve the intended levels. Reset pulse duration should be at least three times actual RC constant time (with typical 22 kΩ marginal pull-up resistor with 50-pF load, reset pulse should be at least 3.3 μs). All functional pins remain in the same state even after RSTn is deasserted and stay in that state until the internal core reset is cleared. The internal core reset is held for 16 system clock cycles following the low-to-high RSTn transition. Upon power-on reset, the system reference clock source and the active external host interface must be determined for proper device initialization.

Table 1. Dual-Function GPIOs

EXTERNAL PIN	FUNCTION	DESCRIPTION
GPIO6	Reference clock source select	Determines the system reference clock source: 0 – XI (24 MHz) 1 – CLKIN (19.2 MHz)Dual
GPIO7	External host interface select	Determines the external host interface type: 0 – VLYNQ host interface 1 – Reserved

The TUSB6020 uses dual-mode pins to determine initial setup. Dual-function pins are latched during the reset. After the reset, these terminals assumes the normal functionality. Figure 1 shows the power-up sequence.

Upon exiting reset, the USB 2.0 OTG PHY is not in the suspend state and the clocks are enabled and free running. The USB 2.0 HS OTG dual role controller core powers up without a session enabled, thus the state machines are in the idle state. After reset is deasserted, the TUSB6020 sends an interrupt to the external host to indicate that it is ready to be programmed. The host reads registers and decides how to proceed based on the device's current status.

Device Power States

The TUSB6020 has three device states typically entered under normal operation:

- RESET
- IDLE
- NORMAL (ACTIVE)

RESET State

The device is in the RESET state when the RSTn input signal is driven low. In RESET state:

- All output ports are tri-stated or initialized to inactive state.
- All bidirectional ports are configured as inputs.
- All registers are set to their reset value.
- PHY macro is enabled and its reference clock output is active.

The TUSB6020 always enters the RESET state asynchronously, but exits the state synchronously. System reset deassertion is always synchronized with active system clock. Upon asserted system reset, the device requires an active system clock to exit the RESET state.

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IDLE State

The TUSB6020 enters IDLE state when external host sets DevIdle bit in the device power management register. The external host may decide to place the device into IDLE state if:

- No USB cable is attached.
- The type-B connector is attached, but the type-A device did not charge V_{BUS}.
- The type-A connector is attached, but the external host may decide to wait for an SRP request from the type-B device.

In IDLE state:

- All output signals are driven to state with minimum I/O current leakage (pullup/pulldowns are controllable through Pullup/Pulldown Control registers).
- All controllable bidirectional pins are placed into minimum current leakage state.
- All registers and memories retain the content and any read/write registers access is disabled.
- All clock sources are disabled.
- PHY macro is suspended:
  1. Low-power V_{BUS} sense comparator is enabled and all regular V_{BUS} comparators are disabled to minimize current consumption.
  2. ID detection circuitry is enabled.
  3. Remaining analog circuitry is disabled.

In IDLE state, the device asserts the SLEEP output pin to the companion power-management device to place it into low-power/sleep mode if the PmIdle and DevIdle bits are set in the PRCM power management register. The power-management device can be put into the sleep state only if the device is placed in IDLE state (DevIdle bit set).

If the application requires the companion power-management device to remain in NORMAL state, the PmIdle bit will not be set, while the DevIdle bit can be set to place the device into the idle state. TUSB6020 stays in the IDLE state until a valid wake-up event occurs and transitions into NORMAL (ACTIVE) State. If system reset is asserted (RSTn), the device transitions to RESET state.

NORMAL (ACTIVE) State

A transition to NORMAL state is required for normal device operation. All circuitry is enabled. In NORMAL state:

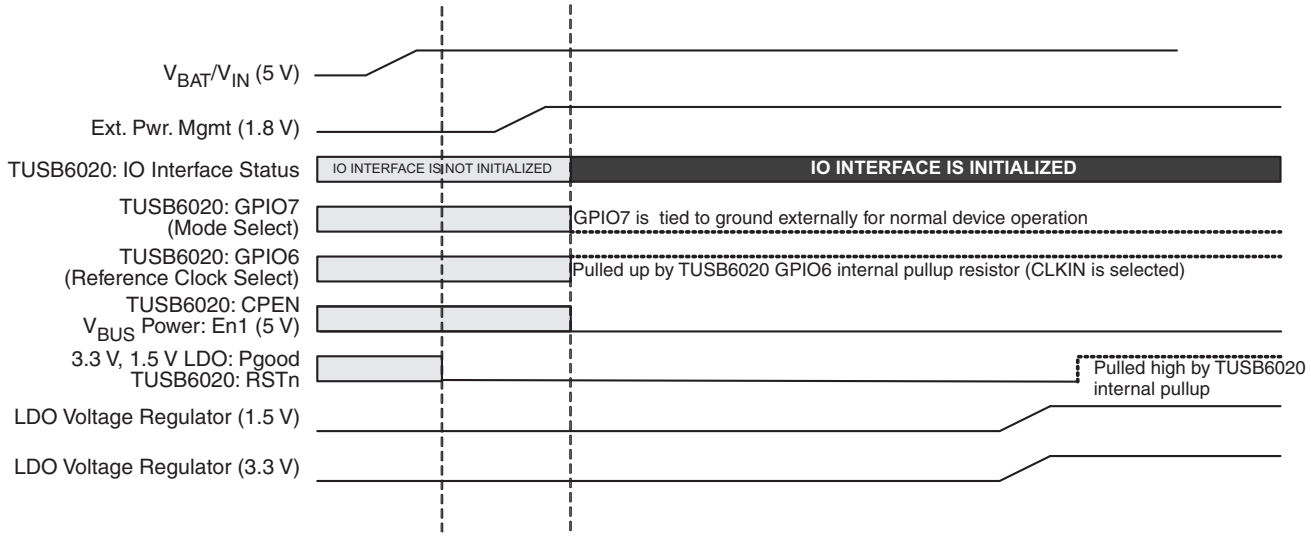
- All I/Os are enabled.
- All registers and memories are accessible.
- Clock source are enabled.
- PHY macro is enabled.
- Session end V_{BUS} detect circuitry is enabled.
- V_{BUS} detection circuitry is enabled.
- ID detection circuitry is enabled.

The external host enables IDpullup and the V_{BUS} sense comparator. It reads the Device Status register to confirm the USB cable connection.

- If no USB cable is attached, IDpullup should be high and V_{BUS} should be low.
- If the type-B USB connector is attached, IDpullup should be high. The V_{BUS} status depends on whether the type-A device on the other side of the cable is charging V_{BUS}.
- If the type-A USB connector is attached, IDpullup should be low and V_{BUS} should be low. The external host decides when to charge V_{BUS}.

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Power-Sequencing Guidelines



NOTE: Host mode and reference clock source selection is latched on RSTn rising edge. No external components are required to select normal mode and CLKIN as a reference clock source.

NOTE: CPEN is used to drive the enable of the V_{BUS} power switch. The TUSB6020 does not power up with CPEN asserted. CPEN is asserted when TUSB6020 is recognized as an A device.

Signal state cannot be ensured.

Signal state is stable and valid.

Figure 1. System Power-Up Sequence

Table 2. INPUT CLOCK REQUIREMENTS

PARAMETER	VALUE
Nominal clock frequency	19.200 (CLKIN), 24.000 (XI)
Frequency accuracy	±100 ppm
Maximum rise/fall time	5 ns (10% to 90%)
Voltage level	1.8 V
Input clock type	Square wave, Sine wave
Duty cycle	40% to 60%
Input capacitance loading	4 pF
Jitter	–95 dBc at 1 MHz –120 dBc at 100 MHz

Crystal Requirements

Frequency

The required frequency of oscillation for the crystal can be 19.200 or 24.000 MHz.

Frequency Tolerance

Frequency tolerance is the maximum allowable deviation from the nominal crystal frequency at a specified temperature, usually 25°C. The recommended frequency tolerance of the crystal over the manufacturing process is ±50 ppm. The maximum acceptable frequency tolerance of the crystal over the manufacturing process is ±100 ppm.

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NOTE:

The total system frequency tolerance from the crystal, load capacitors, capacitive load of the board, capacitive load of the device pins, variation over temperature, variation with age, and circuitry of the PHY must be less than ±500 ppm. Consequently, the individual tolerance for the crystal must be ≤ ±100 ppm.

Load Capacitance

The oscillator of the USB device may have difficulty driving a large load capacitance, so crystals that specify large load capacitances should be avoided. For more information on crystal requirements, see *Selection and Specification of Crystals for Texas Instruments USB 2.0 Devices* (literature number SLLA122).

Mechanical Characteristics

The TUSB6020 controller uses an 80-pin MicroStar BGA™ package. The lead-free solder ball composition is Sn/Ag1.2Cu0.5 (proportions by weight). The substrate plating on the die side where the die bonds to is NiAu. The substrate finish on the bottom side where the solder balls attach to is bare Cu.

Reflow Conditions - ZQE Package

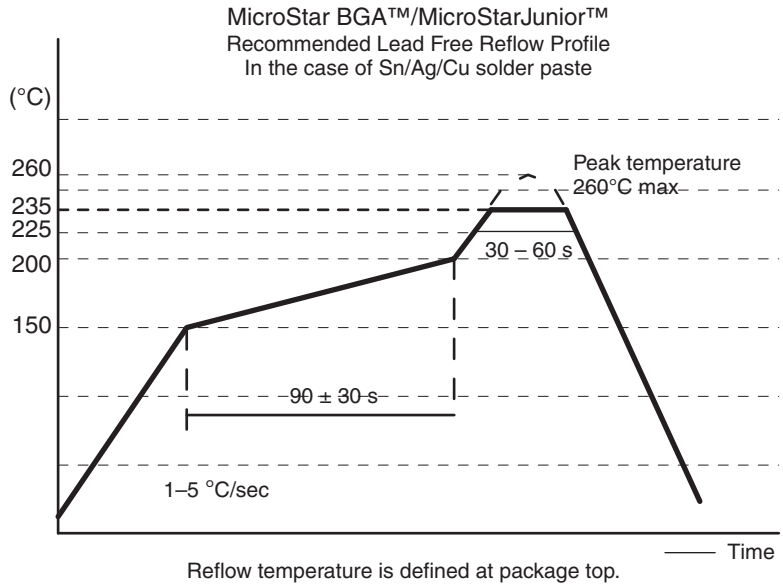


Figure 2. Reflow Conditions

The TUSB6020 controller can also use an 80-pin PFC (TQFP) package.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TUSB6020PFC	ACTIVE	TQFP	PFC	80	96	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR
TUSB6020PFCG4	ACTIVE	TQFP	PFC	80	96	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR
TUSB6020PFCR	ACTIVE	TQFP	PFC	80	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR
TUSB6020PFCRG4	ACTIVE	TQFP	PFC	80	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-4-260C-72 HR
TUSB6020ZQE	ACTIVE	BGA MICROSTAR JUNIOR	ZQE	80	360	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR
TUSB6020ZQER	ACTIVE	BGA MICROSTAR JUNIOR	ZQE	80	2500	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-260C-168 HR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

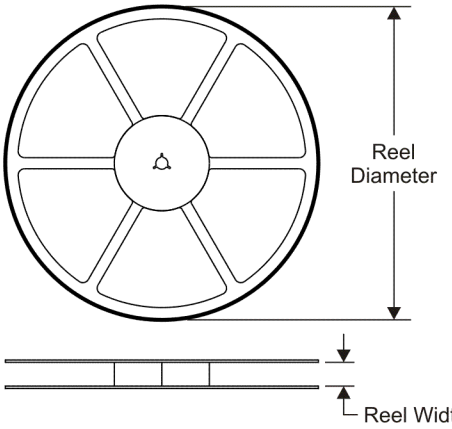
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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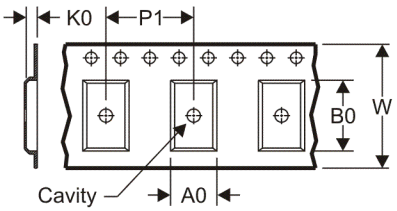
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

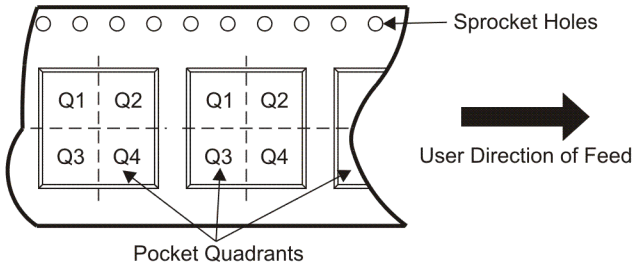


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

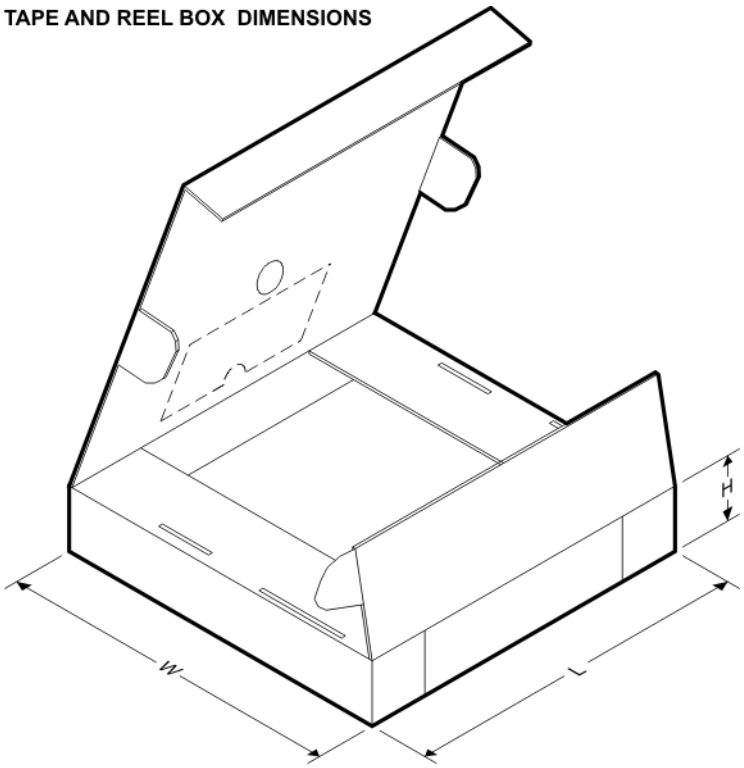
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TUSB6020PFCR	TQFP	PFC	80	2500	330.0	24.4	15.0	15.0	2.0	20.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS

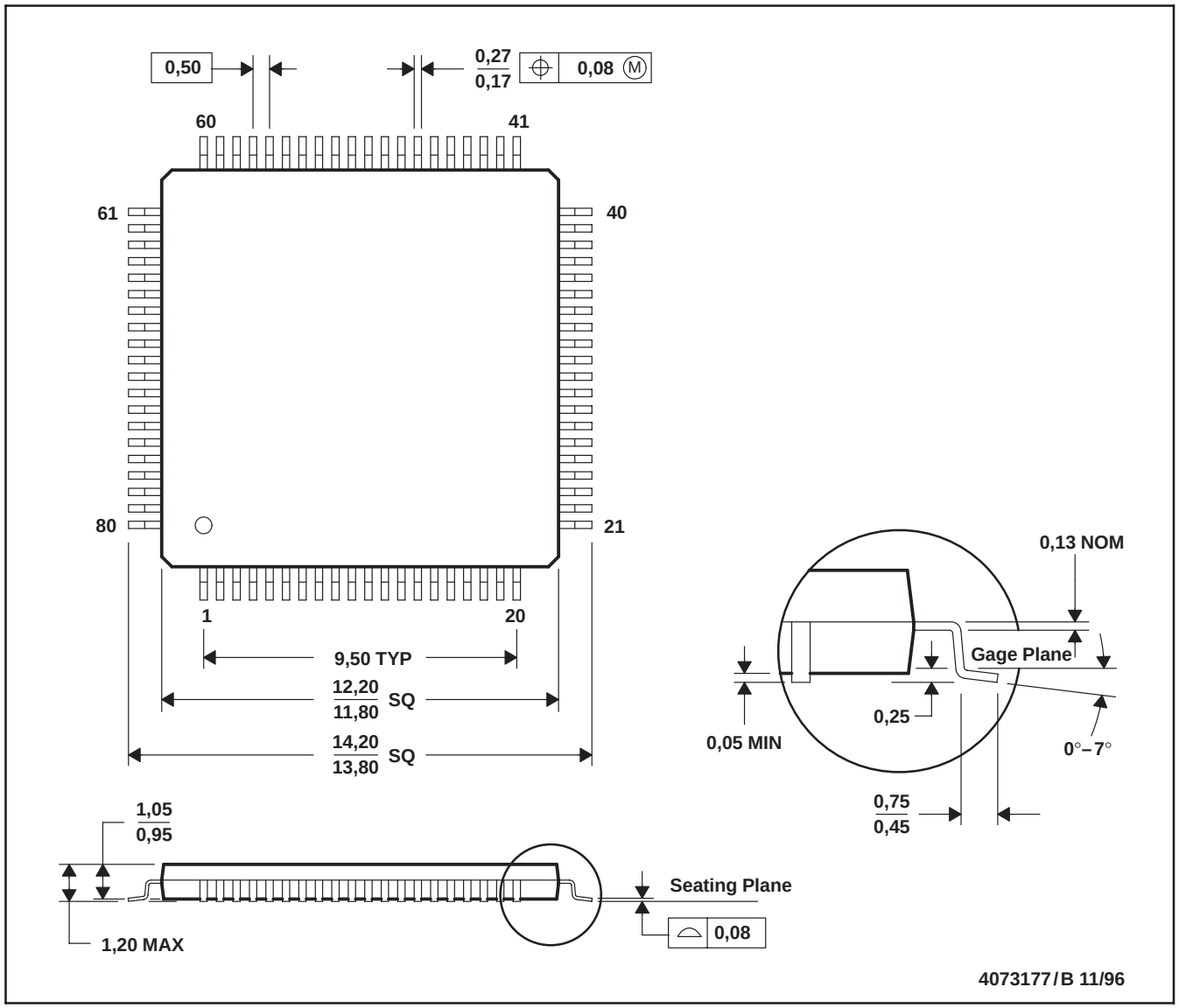


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TUSB6020PFCR	TQFP	PFC	80	2500	346.0	346.0	41.0

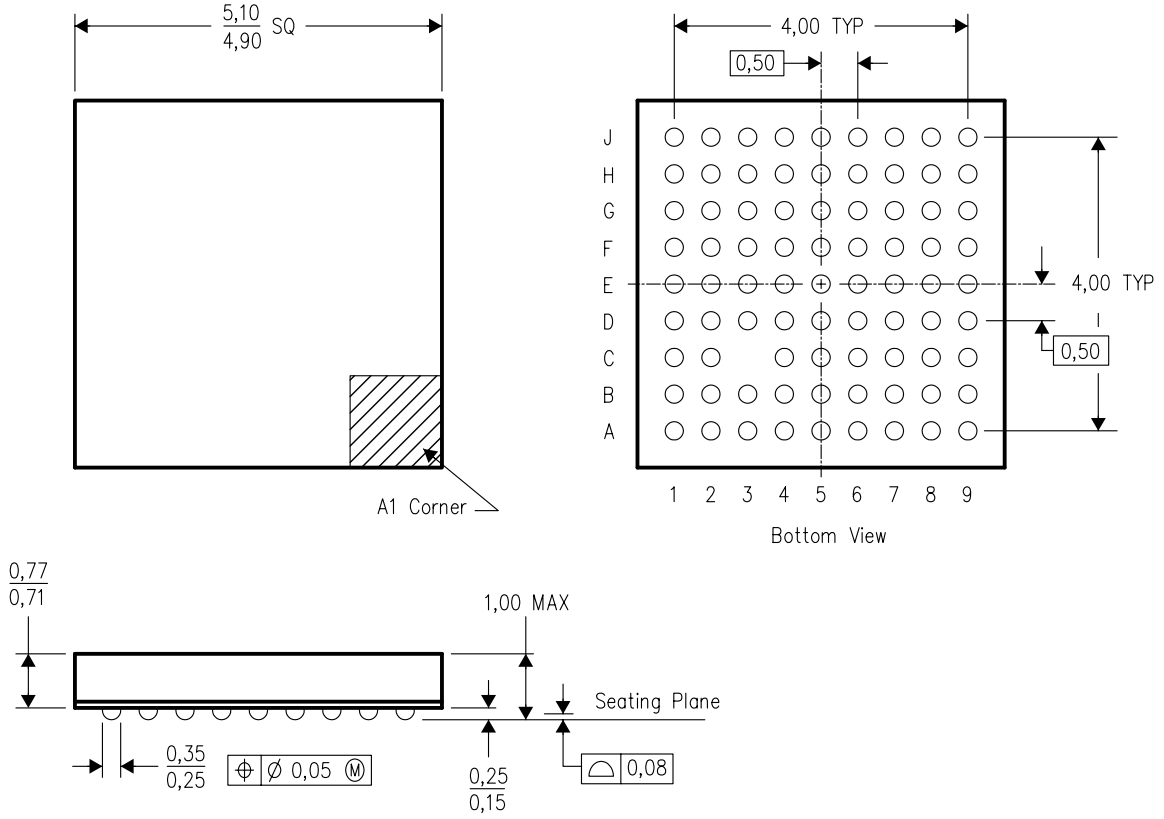
MTQF009A – OCTOBER 1994 – REVISED DECEMBER 1996

PFC (S-PQFP-G80) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

ZQE (S–PBGA–N80) PLASTIC BALL GRID ARRAY



4204334–4/D 10/05

NOTES:
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B. This drawing is subject to change without notice.
C. Falls within JEDEC MO–225
D. This is a lead–free solder ball design.

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