# M50743-PGYS

## PIGGYBACK for M50743-XXXSP

## DESCRIPTION

The M50743-PGYS is an EPROM mounted-type microcomputer employing a silicon gate CMOS process and was designed for developing programs for single-chip, 8-bit microcomputer M50743-XXXSP. The M50743-PGYS, being housed in a piggyback-type 64-pin shrink DIP, is compatible with the M50743-XXXSP.

There is a 28-pin socket on the upper surface so that the M5L2764K or the M5L27128K EPROM may be used.

The M50743-PGYS simplifies the development of programs for the M50743-XXXSP and is excellent for making prototypes.

## DISTINCTIVE FEATURES

- Differences with the M50743-XXXSP are:

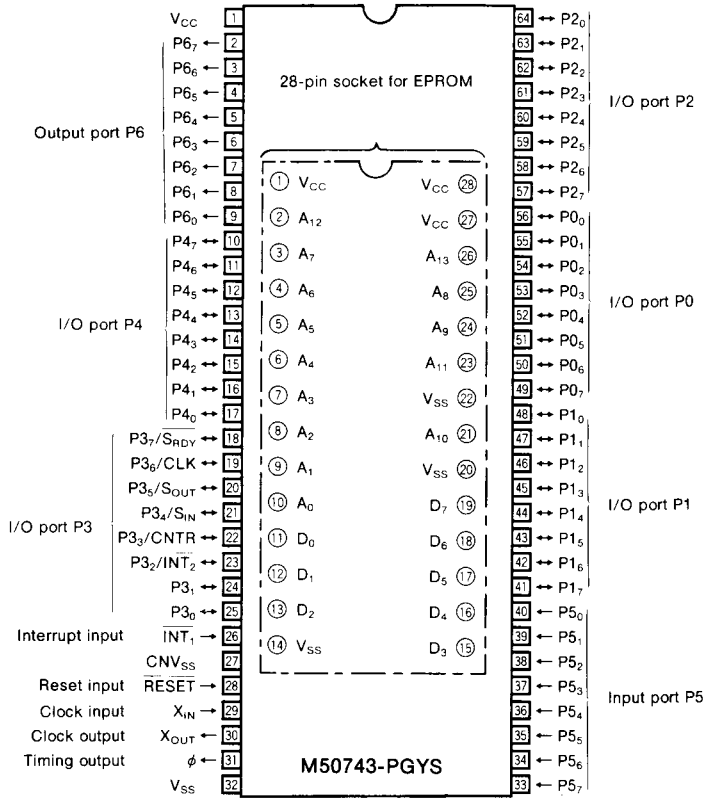
(1) ROMless, EPROM is attached externally

(2) Suitable EPROM is the M5L2764K or the M5L27128K.

## APPLICATION

Development of programs for VCR, tuners, and audio equipment.

## PIN CONFIGURATION (TOP VIEW)




Outline 64S1M

The symbol "○" indicates sockets for EPROM.

## PIN DESCRIPTION

| Pin | Name | Input/ Output | Functions |
|---|---|---|---|
| $V_{CC}$<br>$V_{SS}$ | Supply voltage | | Power supply inputs 5V±5% to $V_{CC}$, and 0V to $V_{SS}$. |
| $CNV_{SS}$ | $CNV_{SS}$ | | This is usually connected to $V_{SS}$. |
| $\overline{RESET}$ | Reset input | Input | To enter the reset state, the reset input pin must be kept at a "L" for more than 2$\mu$s (under normal $V_{CC}$ conditions). If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time. |
| $X_{IN}$ | Clock input | Input | This chip has an internal clock generating circuit. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the $X_{IN}$ and $X_{OUT}$ pins. If an external clock is used, the clock source should be connected the $X_{IN}$ pin and the $X_{OUT}$ pin should be left open. |
| $X_{OUT}$ | Clock output | Output | |
| $\phi$ | Timing output | Output | This is the timing output pin. |
| CNTR | Timer I/O | I/O | This is an output pin for the timer X. |
| $\overline{INT_1}$ | Interrupt input | Input | This is the highest order interrupt input pin. |
| $P0_0$~$P0_7$ | I/O port P0 | I/O | Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode.<br>The output structure is CMOS output. |
| $P1_0$~$P1_7$ | I/O port P1 | I/O | Port P1 is an 8-bit I/O port and has basically the same functions as port P0. |
| $P2_0$~$P2_7$ | I/O port P2 | I/O | Port P2 is an 8-bit I/O port and has basically the same functions as port P0. |
| $P3_0$~$P3_7$ | I/O port P3 | I/O | Port P3 is an 8-bit I/O port and has basically the same functions as port P0. When serial I/O is used, $P3_7$, $P3_6$, $P3_5$, and $P3_4$ work as $\overline{S_{RDY}}$, CLK, $S_{OUT}$, and $S_{IN}$ pins, respectively.<br>Also $P3_3$ and $P3_2$ work as CNTR pin and the lowest order order interrupt input pin ($\overline{INT_2}$), respectively. |
| $P4_0$~$P4_7$ | I/O port P4 | I/O | Port P4 is an 8-bit I/O port and has basically the same functions as port P0. |
| $P5_0$~$P5_7$ | Input port P5 | Input | Port P5 is an 8-bit input port. |
| $P6_0$~$P6_7$ | Output port P6 | Output | Port P6 is an 8-bit output port. The output structure is CMOS output. |
| $A_0$~$A_{13}$ | Output port A | Output | Port A outputs to the address of the EPROM mounted on top of the package. |
| $D_0$~$D_7$ | Input port D | Input | Port D inputs from the address of the EPROM mounted on top of the package. |

## EXPLANATION OF FUNCTION BLOCK OPERATION

The differences between the M50743-PGYS and the M50743-XXXSP are explained below. As all other points are the same, only the differences are explained.

## MEMORY

The memory map is shown in Figure 1. Instead of an internal ROM, an EPROM is mounted. The address of EPROM is $E000_{16}$ to $FFFF_{16}$, having 8k bytes. Other than this, the M50743-PGYS has the same functions as the M50743-XXXSP has.

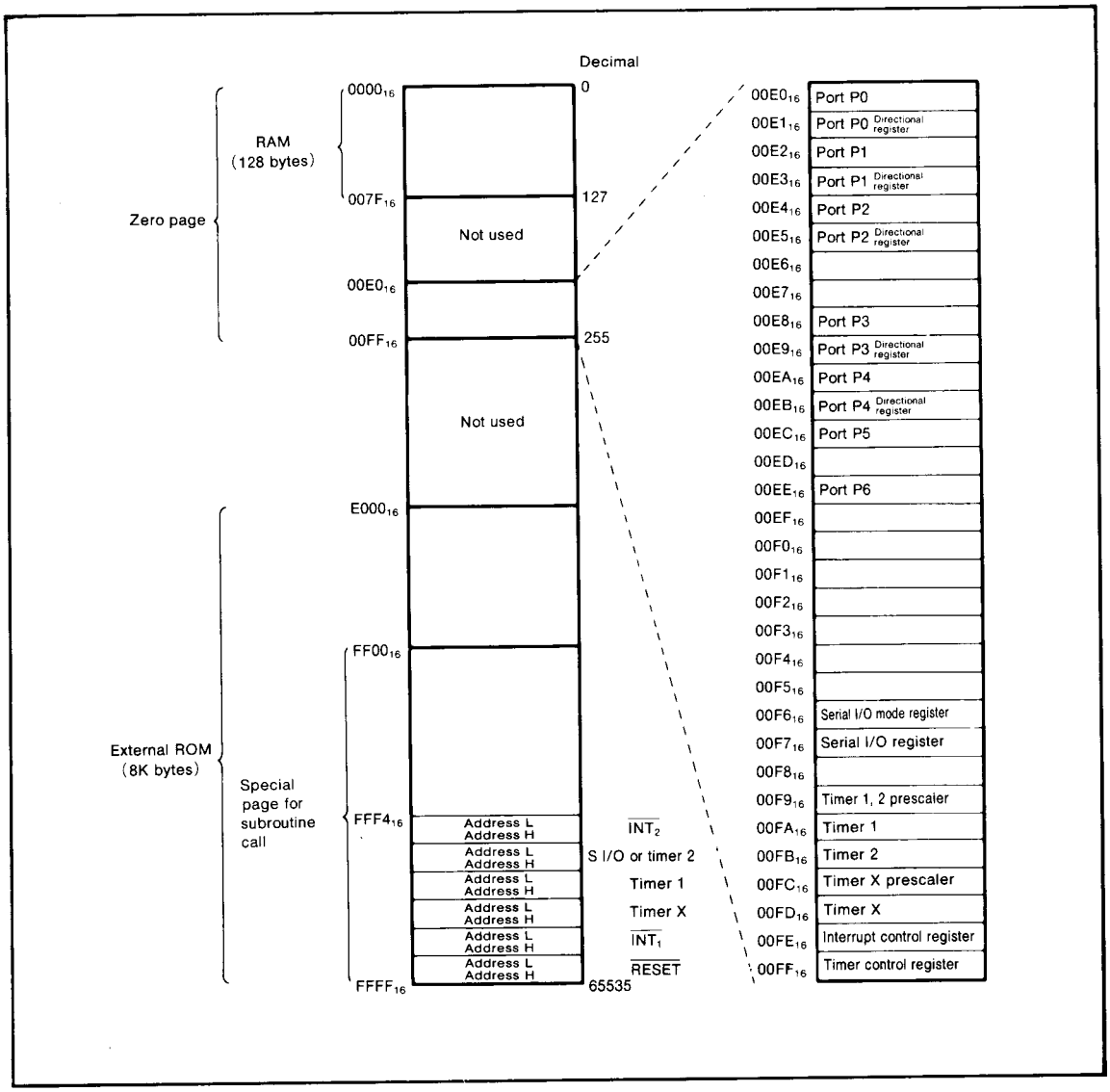



Fig.1 Memory map

## PROCESSOR MODE

External memory area differs from the M50743-XXXSP only in the memory expanding mode of the processor mode. Figure 2 shows the external memory area when the M50743-PGYS is in the memory expanding mode. All other processor modes are identical to those of the M50743-XXXSP.

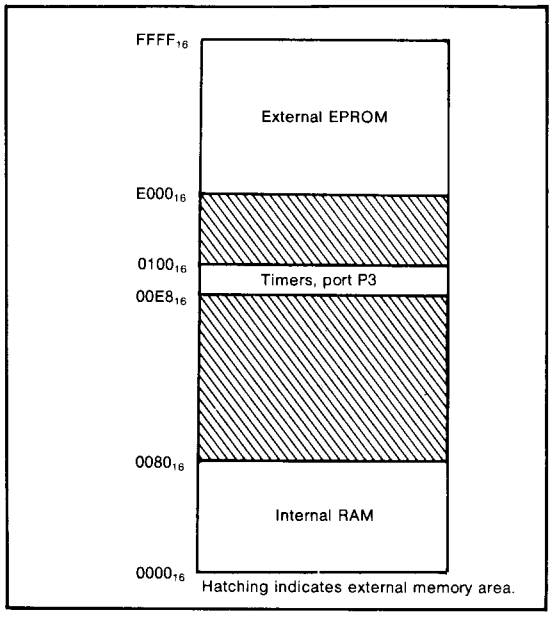



Fig.2 Memory map in memory expanding mode

## PRECAUTION FOR USE

When developing programs with the M50743-PGYS, carefully consider the ROM capacity of the M50743-XXXSP.

In the case of the M50743-XXXSP, use the ROM area from $F000_{16}$ to $FFFF_{16}$.

(In the case of the M5L2764K and the M5L27128K use the areas from $1000_{16}$ to $1FFF_{16}$ and from $3000_{16}$ to $3FFF_{16}$, respectively.)

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Conditions | Ratings | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | With respect to $V_{SS}$<br>With the output transistor isolated. | −0.3~7 | V |
| $V_I$ | Input voltage, $\overline{RESET}$, $X_{IN}$, $\overline{INT_1}$, $P5_0$~$P5_7$, $D_0$~$D_7$ | | −0.3~7 | V |
| $V_I$ | Input voltage, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$ $P3_0$~$P3_7$, $P4_0$~$P4_7$ | | −0.3~$V_{CC}$+0.3 | V |
| $V_I$ | Input voltage, $CNV_{SS}$ | | −0.3~13 | V |
| $V_O$ | Output voltage, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$ $P4_0$~$P4_7$, $P6_0$~$P6_7$, $X_{OUT}$, $\phi$, $A_0$~$A_{13}$ | | −0.3~$V_{CC}$+0.3 | V |
| $P_d$ | Power dissipation | $T_a$ = 25°C | 1000 | mW |
| $T_{opr}$ | Operating temperature | | −10~70 | °C |
| Tstg | Storage temperature | | −40~125 | °C |

## RECOMMENDED OPERATING CONDITIONS ($V_{CC}$=5V±5%, $T_a$ = −10~70°C unless otherwise noted)

| Symbol | Parameter | Limits Min. | Limits Nom. | Limits Max. | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 4.75 | 5 | 5.25 | V |
| $V_{SS}$ | Supply voltage | | 0 | | V |
| $V_{IH}$ | "H" input voltage, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $\overline{INT_1}$, $\overline{RESET}$, $X_{IN}$, $CNV_{SS}$ | 0.8$V_{CC}$ | | $V_{CC}$ | V |
| $V_{IH}$ | "H" input voltage, $D_0$~$D_7$ | 0.45$V_{CC}$ | | $V_{CC}$ | V |
| $V_{IL}$ | "L" input voltage, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $INT_1$, $CNV_{SS}$ | 0 | | 0.2$V_{CC}$ | V |
| $V_{IL}$ | "L" input voltage, $\overline{RESET}$ | 0 | | 0.12$V_{CC}$ | V |
| $V_{IL}$ | "L" input voltage, $X_{IN}$ | 0 | | 0.16$V_{CC}$ | V |
| $V_{IL}$ | "L" input voltage, $D_0$~$D_7$ | 0 | | 0.15$V_{CC}$ | V |
| $I_{OL(peak)}$ | "L" peak output current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P6_0$~$P6_7$ | | | 10 | mA |
| $I_{OL(avg)}$ | "L" average output current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P6_0$~$P6_7$ (Note 1) | | | 5 | mA |
| $I_{OH(peak)}$ | "H" peak output current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P6_0$~$P6_7$ | | | −10 | mA |
| $I_{OH(avg)}$ | "H" average output current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P6_0$~$P6_7$ (Note 1) | | | −5 | mA |
| $f(X_{IN})$ | Internal clock oscillating frequency | | | 8 | MHz |

Note 1 : The average output currents $I_{OL(avg)}$ and $I_{OH(avg)}$ are the average value of a period of 100ms.

2 : Do not allow the combined current of the fllowing ports to exceed stated values.
$I_{OL(peak)}$ of P0, P1, P2, P3, P4 and P6 not to exceed 80mA. $I_{OH(peak)}$ of P2 not to exceed 50mA.
$I_{OH(peak)}$ of P0 and P1 not to exceed 30mA. $I_{OH(peak)}$ of P3, P4 and P6 not to exceed 30mA.

## ELECTRICAL CHARACTERISTICS ($T_a$ = 25°C, $V_{CC}$ = 5V, $V_{SS}$ = 0V, $f(X_{IN})$ = 8MHz, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits Min. | Limits Typ. | Limits Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{OH}$ | "H" output voltage, $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P6_0$~$P6_7$ | $I_{OH}$ = −10mA | 3 | | | V |
| $V_{OH}$ | "H" output voltage, $\phi$, $A_0$~$A_{13}$ | $I_{OH}$ = −2.5mA | 3 | | | V |
| $V_{OL}$ | "L" output voltage, $P0_0$~ $P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P6_0$~$P6_7$ | $I_{OL}$ = 10mA | | | 2 | V |
| $V_{OL}$ | "L" output voltage, $\phi$, $A_0$~$A_{13}$ | $I_{OL}$ = 5mA | | | 2 | V |
| $V_{T+}-V_{T-}$ | Hysteresis, $P3_6$ | When used as CLK input | 0.3 | | 1 | V |
| $V_{T+}-V_{T-}$ | Hysteresis, $\overline{INT_1}$ | | 0.3 | | 1 | V |
| $V_{T+}-V_{T-}$ | Hysteresis, $P3_2$ | When used as $\overline{INT_2}$ input | 0.3 | | 1 | V |
| $V_{T+}-V_{T-}$ | Hysteresis, $P3_3$ | When used as CNTR input | 0.3 | | 1 | V |
| $V_{T+}-V_{T-}$ | Hysteresis, $\overline{RESET}$ | | | 0.5 | 0.7 | V |
| $V_{T+}-V_{T-}$ | Hysteresis, $X_{IN}$ | | 0.1 | | 0.5 | V |
| $I_{IL}$ | "L" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$, $\overline{INT_1}$, $\overline{RESET}$, $X_{IN}$, $D_0$~$D_7$ | $V_I$ = 0V | | | −5 | μA |
| $I_{IH}$ | "H" input current $P0_0$~$P0_7$, $P1_0$~$P1_7$, $P2_0$~$P2_7$, $P3_0$~$P3_7$, $P4_0$~$P4_7$, $P5_0$~$P5_7$, $P6_0$~$P6_7$, $\overline{INT_1}$, $\overline{RESET}$, $X_{IN}$, $D_0$~$D_7$ | $V_I$ = 5V | | | 5 | μA |
| $I_{CC}$ | Supply current | Output pins opened, input and input/output pins at $V_{SS}$ and a square wave input at $X_{IN}$. | | 6 | 12 | mA |