DATA SHEET

# GPES240B2

## Easy-to-use SOUNDPLUS

JAN. 06, 2009

Version 1.1

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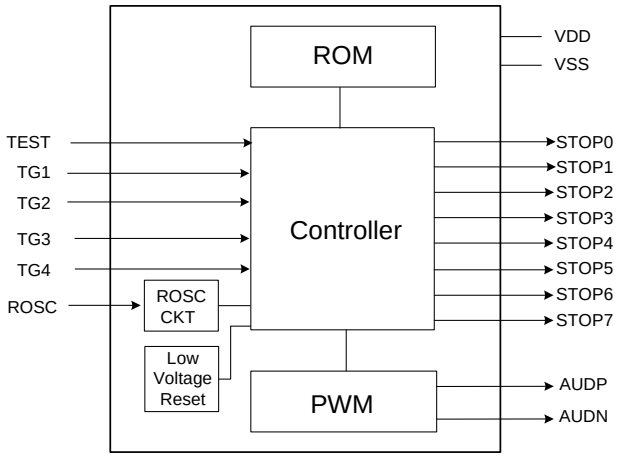
# Easy-to-use SOUNDPLUS

## 1. GENERAL DESCRIPTION

The easy-to-use SOUNDPLUS II (GPESII) is an enhanced version of easy-to-use SOUNDPLUS (GPES). Many features have been added in GPES II to increase its capability and performance. One of the most significant features in GPES II is that no complex program structure is necessary. With only nine instructions and six registers, GPES II is capable of driving sophisticated tasks and playing realistic sound with simple program structure. Programmer can easily implement application rapidly and increase productivity efficiently.

The GPES240B2, one of the GPES II families, stores up to 40 seconds of sound data (@ 6.0KHz sample rate). It also contains four trigger pins, eight output pins, PWM audio output, and five LED flash alternations. To assure the system reliability, a watchdog and a Low Voltage Reset (LVR) are also built in for monitoring possible critical conditions. With the high cost/performance ratio, GPES240B2 is one of the most suitable engines in the industry for vocal products.

## 2. BLOCK DIAGRAM



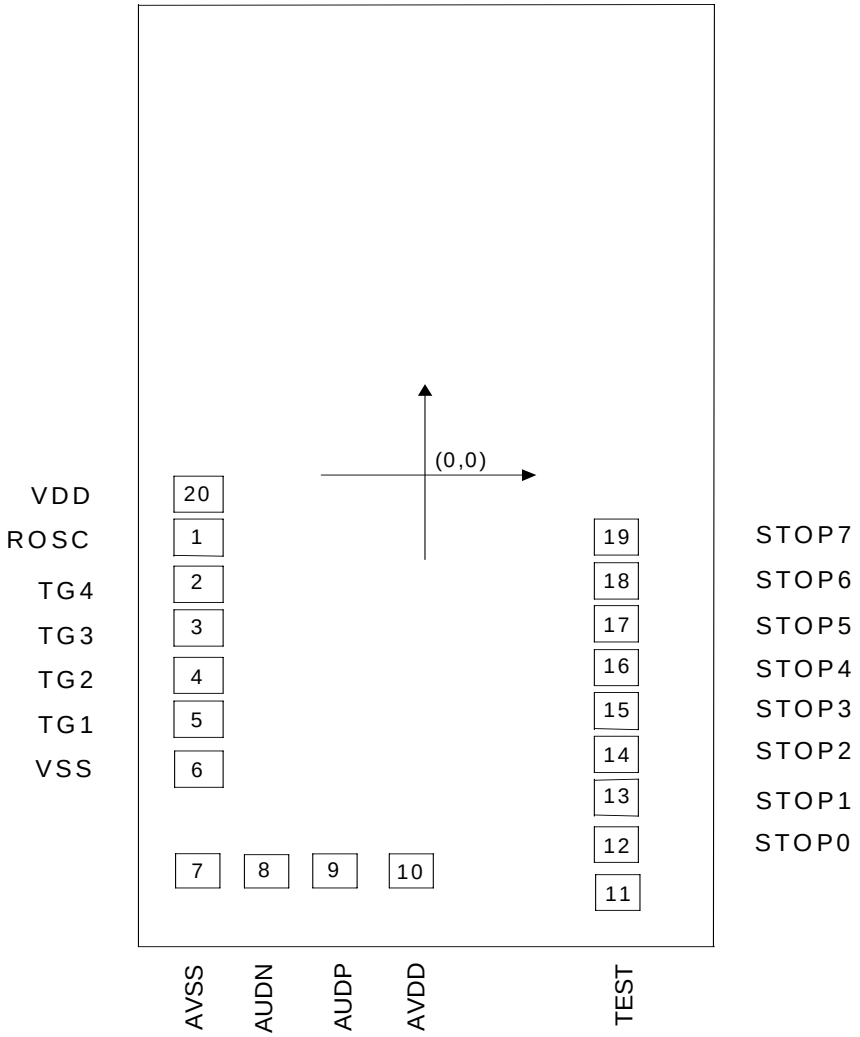

## 3. FEATURES

- 128KB ROM SIZE
- Programmable speech synthesizer
- Operating voltage:
  - 1.9V - 5.5V for 4.0MHz operating clock
  - 3.6V - 5.5V for 6.0MHz operating clock
- 4 direct trigger inputs that can be extended to 36 matrix key
- Up to 8 programmable outputs
- Programmable power on initialization
- 256 voice group entries available
- Mask options: Trigger input debounce time from 5ms to 35ms
- Flexible functions through the following:
  - LD (load), JP (jump) commands
  - 6 registers: R0, R1, R2, R3, EN, STOP
  - Conditional instructions
  - Speech equation
  - END instruction
  - Local repeat setting
  - Output frequency and LED flash type setting
- Approx. 40 sec. speech (6.0KHz sample rate)
- Low voltage reset function
- Watchdog function
- A pair of PWM outputs
- Flexible functions as the follows:
  - Interrupt or non-interrupt for rising or falling edge of each trigger.
  - Eight programmable playing modes:
    - · One shot
    - · Level hold
    - · Single-cycle level hold
    - · Complete-cycle level hold
    - · Sequence
    - · Level-Auto
    - · Random
    - · Non-retrigger
  - Stop signal output setting
- Each voice section provides
  - Programmable sampling frequency:
    - · 2K to 10K for 4.0MHz operating clock
    - · 2K to 15K for 6.0MHz operating clock
  - Five LED flash type : On, Off, Alternatively, Synchronous, Volume-controlled
  - LED: programmable
- Infrared Red (IR) communication Function
- Play Speech with tags, Seven different tags are available

## 4. SIGNAL DESCRIPTIONS

| Mnemonic | PIN No. | Type | Description |
|---|---|---|---|
| TG4 - 1 | 2 - 5 | I | Trigger input pins |
| TEST | 11 | I | TEST pin |
| STOP7 - 6 | 19 - 18 | O | Open drain output pins / LED drive pins |
| STOP5 - 0 | 17 - 12 | O | Output signals pins |
| AUDP, AUDN | 9, 8 | O | A pair of PWM outputs for speak |
| ROSC | 1 | I | Oscillator frequency control pin |
| VDD | 20 | I | Digital circuit power supply pin |
| AVDD | 10 | I | PWM power supply pin |
| VSS | 6 | I | Digital circuit power supply pin |
| AVSS | 7 | I | PWM power supply pin |

### 4.1. PAD Assignment




This IC substrate should be connected to VSS

**Note1:** To ensure that the IC functions properly, bond all VDD and VSS pins.
**Note2:** The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

## 5. FUNCTIONAL DESCRIPTIONS

### 5.1. Instruction Sets

Nine instructions involve *LD, JP, LSR, ADD, SUB, AND, ORR, EOR, and END*. "LD" represents LOAD and "JP" indicates JUMP. "LSR" shifts a register's value one bit to the right. "ADD" and "SUB" are addition and subtraction. "AND", "ORR" and "EOR" are logical operations which indicate AND, OR and, Exclusive OR respectively. "END" ends program and enters into sleep mode for power saving purpose.

### 5.2. I/O Description

GPES II has the following I/O pins: TG1, TG2, TG3, TG4, STOP [0:7]. The TG1, TG2, TG3 and TG4 are input pins and STOP [0:7] are output pins; moreover, STOP [6:7] can be shared with LED drive pins.

| PIN | Configuration |
|---|---|
| TG1 | Input |
| TG2 | Input |
| TG3 | Input |
| TG4 | Input |
| STOP.0 | Output |
| STOP.1 | Output |
| STOP.2 | Output |
| STOP.3 | Output |
| STOP.4 | Output |
| STOP.5 | Output |
| STOP.6 | Output (shared with LED2 pin) |
| STOP.7 | Output (shared with LED1 pin) |

### 5.3. Program Structure Overview

The following description is an overview of GPES II program structure. For more information about GPES II programming method, please refer to GPES II Programming Guide.

#### 5.3.1. Definition area

The beginning of a program is the Definition Area that defines some declarations before Initialization such as IC body, variable, frequency, debounce time and low voltage reset option.

##### 5.3.1.1. IC body

The first element defined in a program is a GPES II body.

Example:

```
        SPES240B        ;select SPES240B
        EXT_CLK_4M
        Freq4           ;Set default speech
                        ;sample frequency to 7.8K
        LVR_DISABLE
        ...
POI:
        ...
        ...
```

##### 5.3.1.2. Debounce

A key debounce time can be defined in Definition Area. The range of debounce time is 5ms ~ 35ms.

##### 5.3.1.3. Variable

A variable can be defined by adding a "#define" in front of a variable. A variable can be the combination of numbers and characters, but not underscore.

Variable Syntax:

```
#define  VariableName  <Register | NUM>
```

Example1:

```
#define var  R0     ;define var as R0
```

Example2:

```
#define const 8     ;define const as 8
```

##### 5.3.1.4. External clock

Users can define one external clock out of the following selections in a program. This option must be defined in definition area.

EXT_CLK_3M; (3.0MHz)
EXT_CLK_4M; (4.0MHz)
EXT_CLK_6M; (6.0MHz)

#### 5.3.1.5. Low voltage reset

The Low Voltage Reset (LVR), prevents system running into malfunction state, will intend to reset all functions back to the initial states if power VDD drops too low. The LVR works the same as Power-on Reset; it can be enabled or disabled via programming and must be defined in the definition area.

LVR_ENABLE; enable
LVR_DISABLE; disable

#### 5.3.1.6. Infrared Red (IR) Function

Some IR parameters must be defined in Definition Area before using IR function. We will only introduce the commands here. For more details on how to use these commands in your program, please refer to GPES II Programming Guide.

### 5.3.2. Entry point (Label)

The essence applied in GPES II is the ENTRY POINT. Each trigger pin is assigned an entry point. *Instructions must be located in a new line under its entry point. Any instruction located with the same line as entry point will cause error when compiling.* Users can also define a label (ID) for an entry point. A label can be the combinations of number and character, but not underscore. In addition, a label can not start with a number.

Example

```
SpeechLoop:
            Sound1+Sound2
            JP  SpeechLoop
```

When a pin is triggered, the program jumps to its corresponding entry point and starts executing. The entry points are fixed values. For instance, '0' is the entry point of TG1 when 1→0. '1' is the entry point of TG2 when 1→0. Users can either use Entry Point ID or Entry Point Abbreviator to express an entry point. A summary of entry point for each trigger pin is as follows:

| Entry Point | Entry Point Abbreviator | Status |
|---|---|---|
| 32 | POI | Power on initialization |
| 0 | TG1F | TG1 1→0 (falling) |
| 1 | TG2F | TG2 1→0 (falling) |
| 2 | TG3F | TG3 1→0 (falling) |
| 3 | TG4F | TG4 1→0 (falling) |
| 4 | TG1R | TG1 0→1 (rising) |
| 5 | TG2R | TG2 0→1 (rising) |
| 6 | TG3R | TG3 0→1 (rising) |
| 7 | TG4R | TG4 0→1 (rising) |
| 8 ~ 253 (except 32) | User-Defined entry point or label | User-Defined |
| *254* | *Speech event* | *User-Defined* |
| *255* | *Timer event* | *User-Defined* |

Example:
An example is introduced here. Also, all words after semi-colon (;) are for comments only.

```
      SPES240B          ;body defined
      EXT_CLK_4M
      LVR_Disable
POI:
      LD  EN, 0x00
      (4000)_3
      LD  EN, 0x 03     ;enable TG1 falling and
                        ;TG2 falling
      END

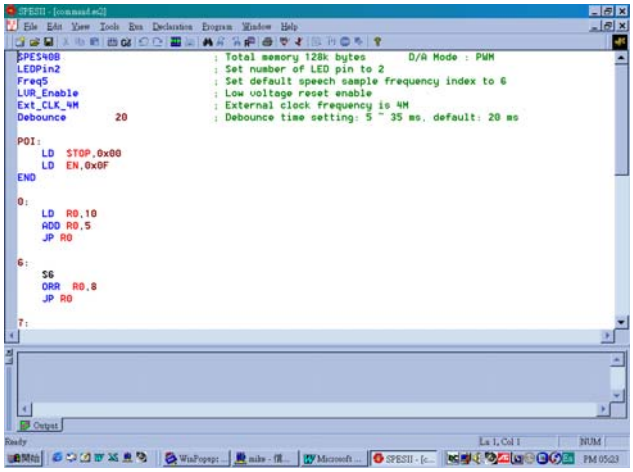
TG1F:
      Sound1            ;when TG1 changes from
                        ;1→0 (High→Low),
                        ;sound1 is played
      END               ;Sleep

TG2F:
      Sound2            ;when TG2 changes from
                        ;1→0, sound2 is played
      END               ;Sleep
```

## 6. GPES II PROGRAMMING TOOL

GENERALPLUS provides a user-friendly interface that allows users to write, edit, compile and debug GPES II programs. GPES II Programming Tool should be executed under Windows 95, Windows 98, Windows Me and Windows 2000. For more information on how to use GPES II Programming Tool, please refer to GPES II Programming Guide.



## 7. ELECTRICAL SPECIFICATIONS

### 7.1. Absolute Maximum Ratings

| Characteristics | Symbol | Ratings |
|---|---|---|
| DC Supply Voltage | $V_+$ | < 7.0V |
| Input Voltage Range | $V_{IN}$ | -0.5V to $V_+$ + 0.5V |
| Operating Temperature | $T_A$ | 0℃ to +60℃ |
| Storage Temperature | $T_{STO}$ | -50℃ to +150℃ |

**Note:** Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

### 7.2. DC Characteristics (VDD = 3.0V, $T_A$ = 25℃)

| Characteristics | Symbol | Limit | | | Unit | Condition |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | |
| Operating Voltage | VDD | 1.9 | - | 5.5 | V | - |
| LED2 - 1 Output Current | $I_{OL}$ | - | 25 | - | mA | VDD = 3.0V, $V_{OUT}$ = 1.0V |
| STOP5 - 0 Output Current | $I_{OL}$ | - | 10 | - | mA | VDD = 3.0V, $V_{OL}$ = 1.0V |
| | $I_{OH}$ | - | -3.5 | - | | VDD = 3.0V, $V_{OH}$ = 2.0V |
| Standby Current | $I_{STBY}$ | - | - | 2.0 | μA | VDD = 3.0V |
| Operating Current | $I_{OP}$ | - | 1.7 | - | mA | VDD = 3.0V, $F_{CPU}$ = 2.0MHz No load |
| PWM Output Current | $I_{OL}$ | - | 100 | - | mA | VDD = 3.0V, $V_{OL}$ = 1.0V |
| | $I_{OH}$ | - | -100 | - | | VDD = 3.0V, $V_{OH}$ = 2.0V |
| $R_{OSC}$ Resistor | $R_{OSC}$ | - | 82 | - | KΩ | VDD = 3.0V, $F_{OSC}$ = 4.0MHZ |
| Input Current for TG4 - 1 | $I_{IN}$ | - | 1.8 | - | μA | VDD = 3.0V, $V_{IN}$ = VSS |

### 7.3. DC Characteristics (VDD = 4.5V, $T_A$ = 25℃)

| Characteristics | Symbol | Limit | | | Unit | Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Operating Voltage | VDD | 3.6 | - | 5.5 | V | - |
| LED2 - 1 Output Current | $I_{OL}$ | - | 30 | - | mA | VDD = 4.5V, $V_{OUT}$ = 1.0V |
| STOP5 - 0 Output Current | $I_{OL}$ | - | 15 | - | mA | VDD = 4.5V, $V_{OL}$ = 1.0V |
| | $I_{OH}$ | - | -7 | - | | VDD = 4.5V, $V_{OH}$ = 3.5V |
| Standby Current | $I_{STBY}$ | - | - | 2.0 | μA | VDD = 4.5V |
| Operating Current | $I_{OP}$ | - | 3.6 | - | mA | VDD = 4.5V, $F_{CPU}$ = 2.0MHz No load |
| PWM Output Current | $I_{OL}$ | - | 130 | - | mA | VDD = 4.5V, $V_{OL}$ = 1.0V |
| | $I_{OH}$ | - | -130 | - | | VDD = 4.5V, $V_{OH}$ = 3.5V |
| $R_{OSC}$ Resistor | $R_{OSC}$ | - | 56 | - | KΩ | VDD = 4.5V, $F_{OSC}$ = 6.0MHz |
| Input Current for TG4 - 1 | $I_{IN}$ | - | 4.4 | - | μA | VDD = 4.5V, $V_{IN}$ = VSS |

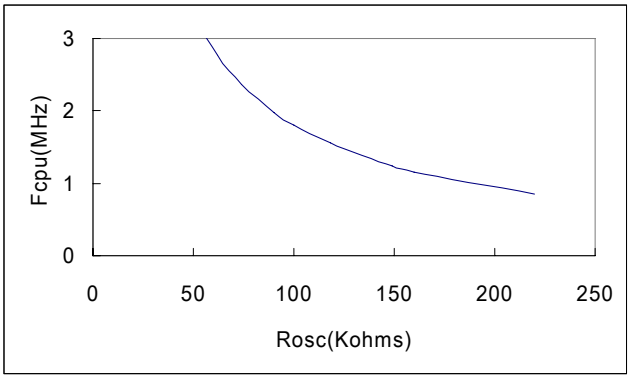
### 7.4. (3volt) R relative $F_{OSC}$ Table (the table is only for reference)

| R(Kohm) | 56KΩ | 82KΩ | 110KΩ |
|---|---|---|---|
| $F_{OSC}^*$ (MHz) | 6 | 4 | 3 |

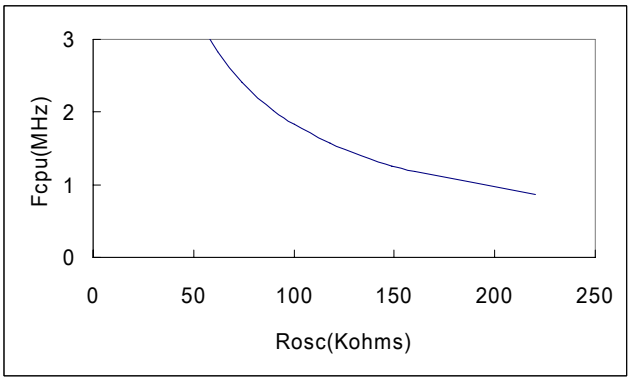
**NOTE*:** $F_{CPU}=F_{OSC}/2$

### 7.5. The Relationships between the $R_{OSC}$ and the $F_{CPU}$

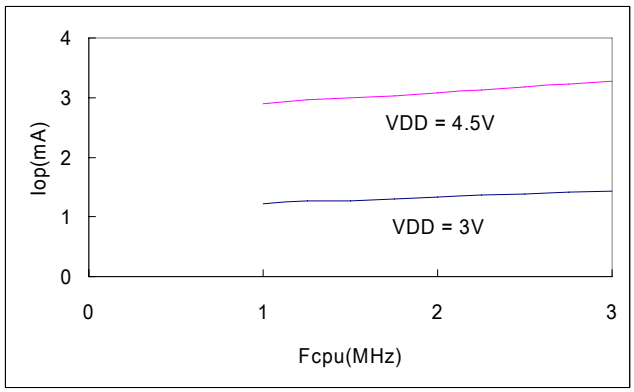
#### 7.5.1. VDD = 3.0V, $T_A$ = 25℃



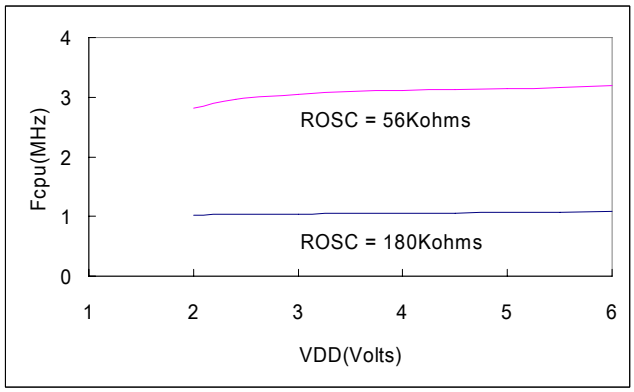

#### 7.5.2. VDD = 4.5V, $T_A$ = 25℃




### 7.6. The Relationships between the $F_{CPU}$ and the $I_{OP}$

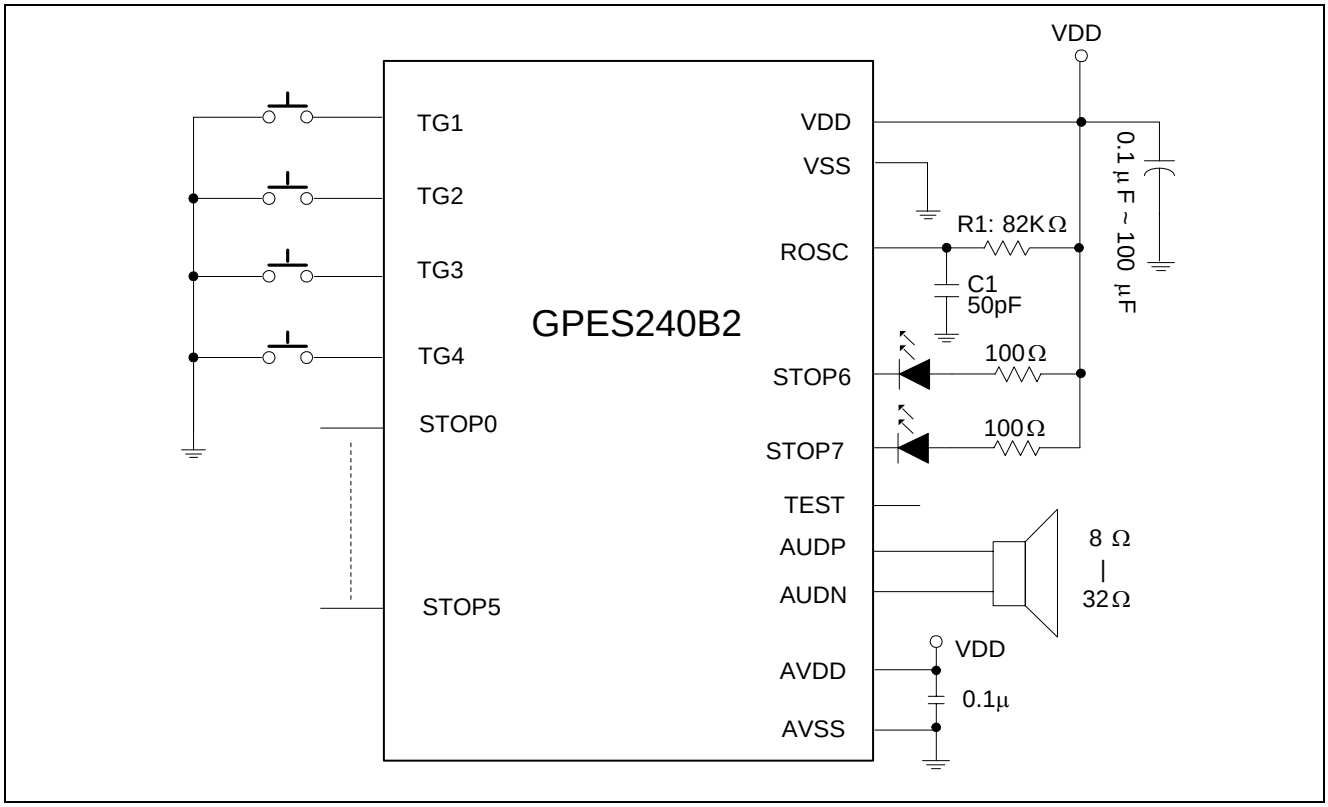



### 7.7. The Relationships between the $F_{CPU}$ and the VDD

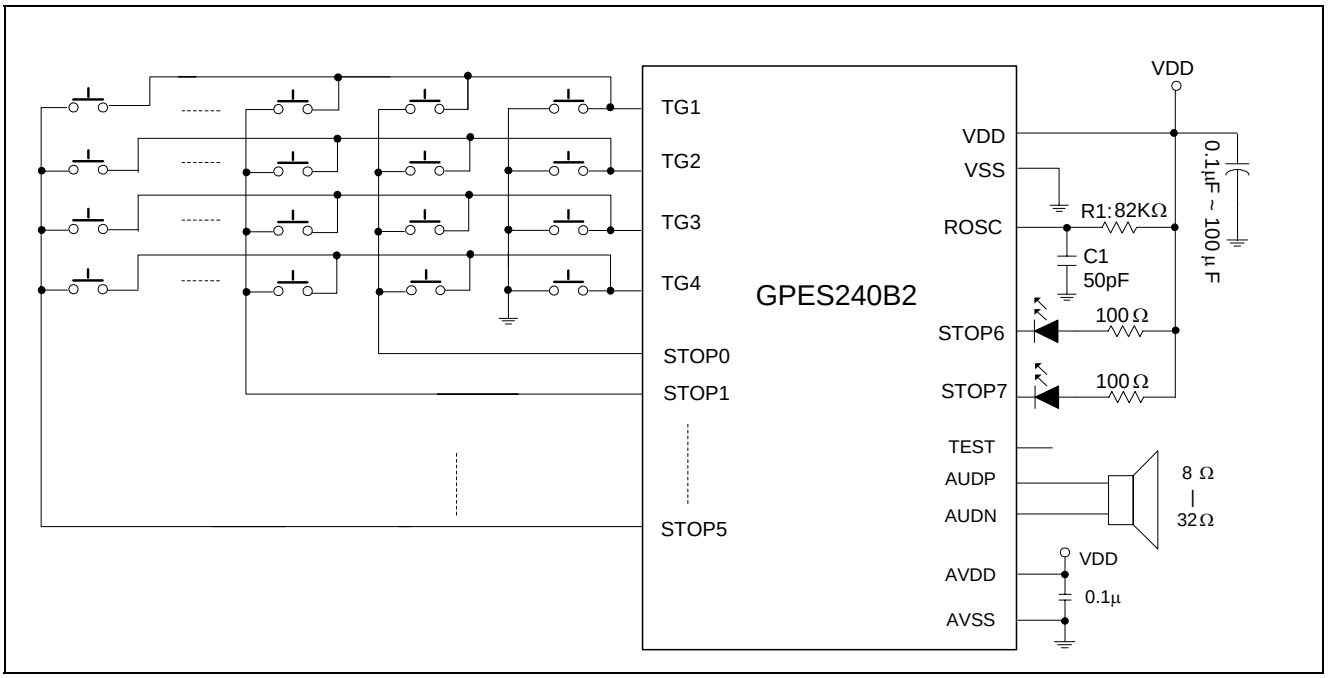


## 8. APPLICATION CIRCUITS

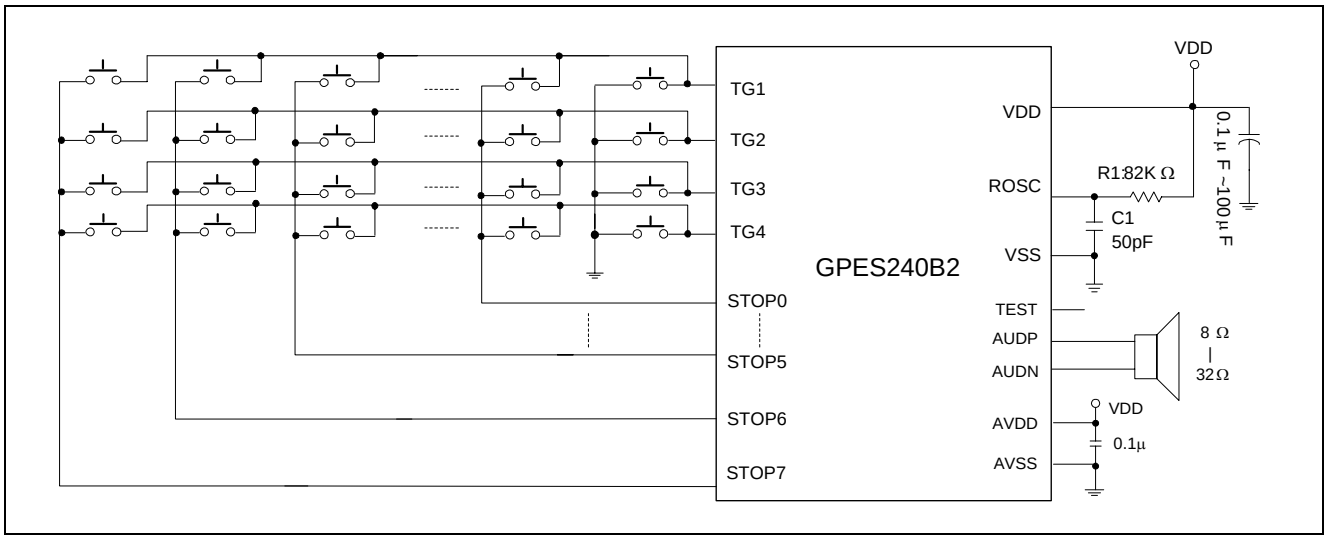
### 8.1. 4 Inputs, 2 LEDS and 6 Outputs




### 8.2. 28 Inputs Key Matrix

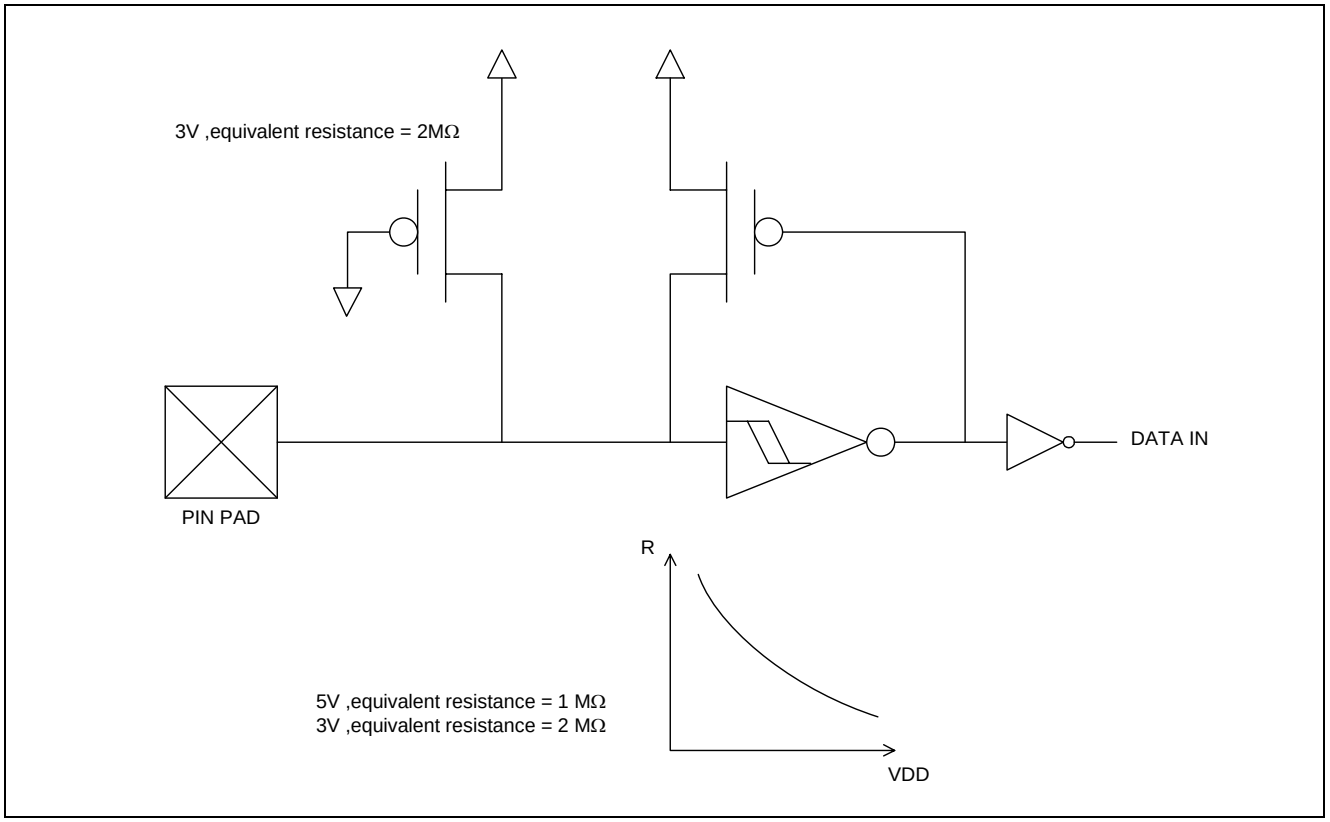


### 8.3. 36 Inputs Key Matrix




**Note:** To avoid the noise interference on PCB around R-oscillator, R1 and C1 should be placed as close as possible to ROSC pin.

### 8.4. PTG pin Pull-High Resistance



## 9. PACKAGE/PAD LOCATIONS

### 9.1. Ordering Information

| Product Number | Package Type |
|---|---|
| GPES240B2-NnnV-C | Chip form |

**Note1:** Code number is assigned for customer.

**Note2:** Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

## 10. DISCLAIMER

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## 11. REVISION HISTORY

| Date | Revision # | Description | Page |
|---|---|---|---|
| JAN. 06, 2009 | 1.1 | 1. Modify 3 FEATURES.<br>2. Modify 6.3.1.5 Low voltage reset.<br>3. Modify 8.2 DC Characteristics. | 3<br>7<br>9 |
| NOV. 03, 2006 | 1.0 | Original | 14 |