MAS9078

AM Receiver IC

- **High Sensitivity**
- **Very Low Power Consumption**
- **Wide Supply Voltage Range**
- **Power Down Control**
- **Control for AGC On**
- **High Selectivity by Crystal Filter**
- **Fast Startup Feature**

DESCRIPTION

The MAS9078 AM-Receiver chip is a highly sensitive, simple to use AM receiver specially intended to receive time signals in the frequency range from 40 kHz to 100 kHz. Only a few external components are required for time signal receiver. The circuit has preamplifier, wide range automatic gain control, demodulator and output comparator built in. The output signal can be processed directly by an additional digital circuitry to extract the data from the received signal. The control for AGC (automatic gain control) can be used to switch AGC on or off if necessary. Unlike MAS1016A and MAS1016B, MAS9078 does not require AGC control procedure in WWVB and JJY systems.

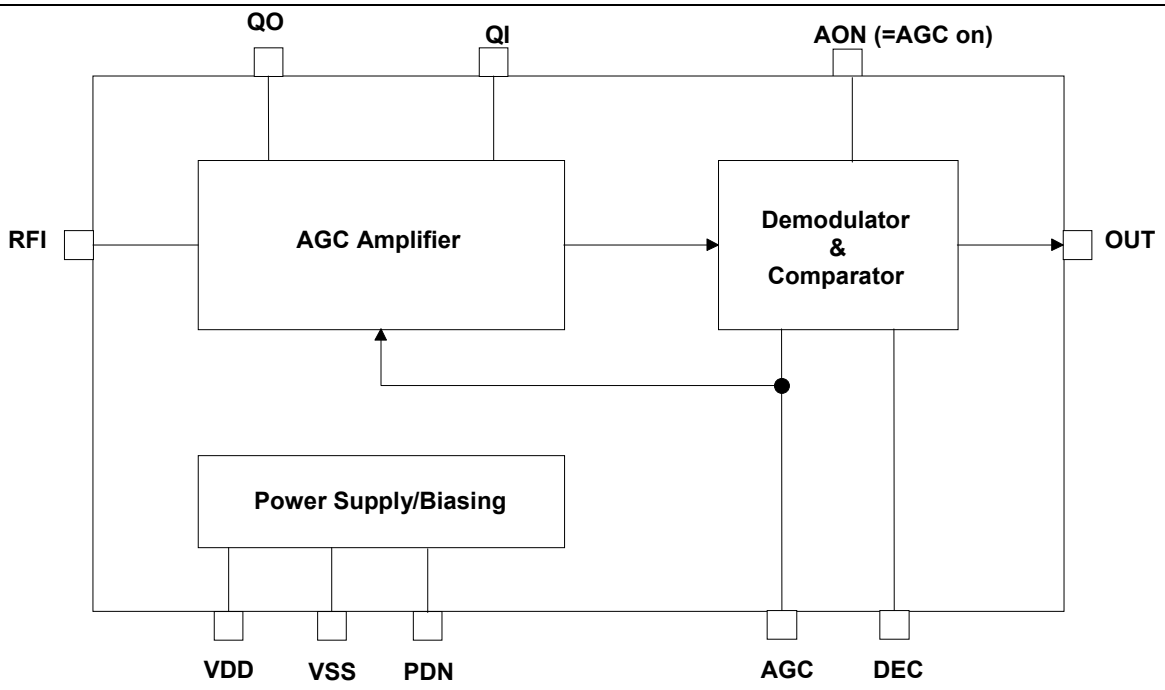
FEATURES

- Highly Sensitive AM Receiver, 0.4 μV_{RMS} typ.
- Wide Supply Voltage Range from 1.1 V to 3.6 V
- Very Low Power Consumption
- Power Down Control
- Fast Startup
- Only a Few External Components Necessary
- Control for AGC On
- Wide Frequency Range from 40 kHz to 100 kHz
- High Selectivity by Quartz Crystal Filter
- Die and TSSOP-16 Package

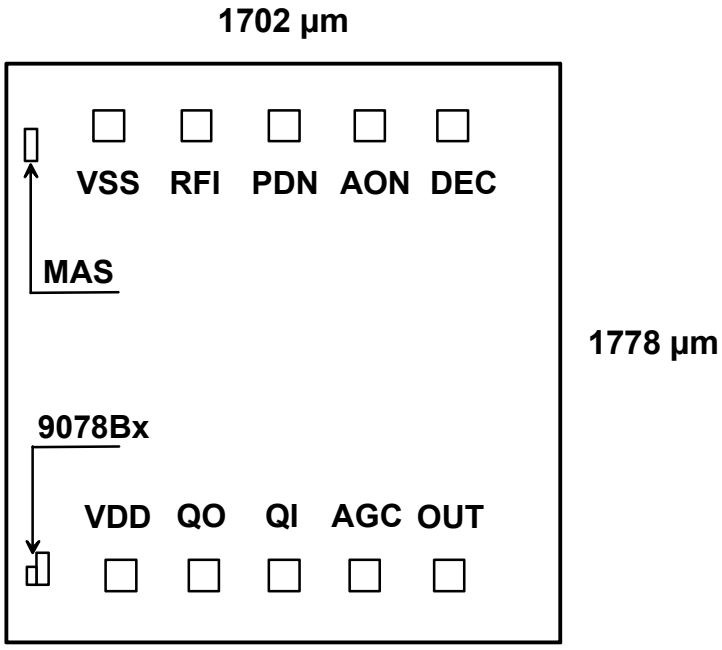
APPLICATIONS

- Time Signal Receiver WWVB (USA), JJY (Japan), DCF77 (Germany) and MSF (UK)
- Receiver for ASK Modulated Data Signals

BLOCK DIAGRAM



PAD LAYOUT



DIE size = 1.70 x 1.78 mm; PAD size = 100 x 100 µm

Note: Because the substrate of the die is internally connected to VDD, the die has to be connected to VDD or left floating. Please make sure that VDD is the first pad to be bonded. Pick-and-place and all component assembly are recommended to be performed in ESD protected area.

Note: Coordinates are pad center points where origin has been located in the center of VDD pad

Note: The on-chip product code 9078Bx identifies internal compensation capacitance option. x has values 1, 2, 3, 4 or 5 refering to capacitance option described in the Table 2 on page 4.

Pin Description	Name	X-coordinate	Y-coordinate	Note
Power Supply Voltage	VDD	0 µm	0 µm	
Quarz Filter Output	QO	306 µm	19 µm	
Quarz Filter Input	QI	586 µm	19 µm	
AGC Capacitor	AGC	866 µm	19 µm	
Receiver Output	OUT	1109 µm	19 µm	1
Demodulator Capacitor	DEC	1109 µm	1428 µm	
AGC On Control	AON	866 µm	1428 µm	2
Power Down Input	PDN	549 µm	1428 µm	3
Receiver Input	RFI	306 µm	1428 µm	
Power Supply Ground	VSS	16 µm	1407 µm	

Notes:
1) OUT = VSS when carrier amplitude at maximum; OUT = VDD when carrier amplitude is reduced (modulated)
   - the output is a current source/sink with $|I_{OUT}| > 5$ µA
   - at power down the output is pulled to VSS (pull down switch)
2) AON = VSS means AGC off (hold current gain level); AON = VDD means AGC on (working)
   - Internal pull-up with current < 1 µA which is switched off at power down
3) PDN = VSS means receiver on; PDN = VDD means receiver off
   - Fast start-up is triggered when the receiver is after power down (PDN=VDD) controlled to power up (PDN=VSS) i.e. at the falling edge of PDN signal.

ABSOLUTE MAXIMUM RATINGS

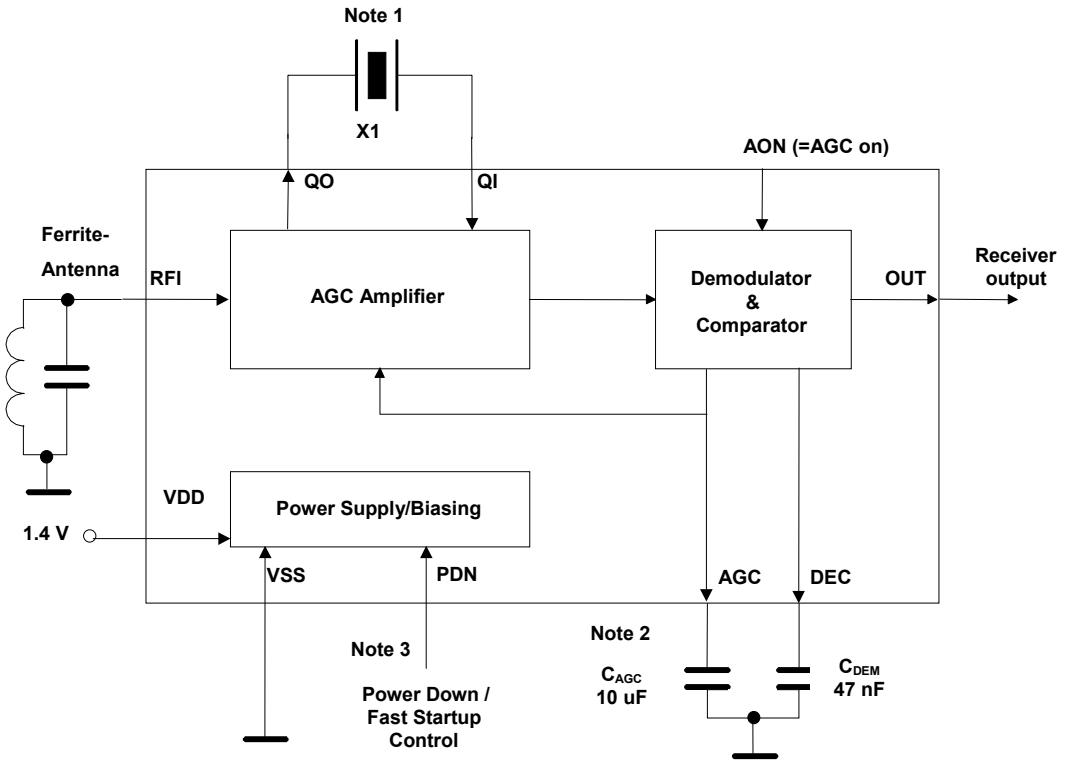
Parameter	Symbol	Conditions	Min	Max	Unit
Supply Voltage	V_{DD}-V_{SS}		-0.3	5.0	V
Input Voltage	V_{IN}		V_{SS}-0.3	V_{DD}+0.3	V
Power Dissipation	P_{MAX}			100	mW
Operating Temperature	T_{OP}		-20	70	°C
Storage Temperature	T_{ST}		-40	120	°C

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 1.4V, Temperature = 25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating Voltage	V_{DD}		1.10		3.60	V
Current Consumption	I_{DD}	VDD=3.6 V, Vin=0 µV VDD=1.4 V, Vin=0 µV	56	76 66	95	µA
Stand-By Current	I_{DDoff}				0.1	µA
Input Frequency Range	f_{IN}		40		100	kHz
Minimum Input Voltage	$V_{IN\ min}$			0.4	1	µVrms
Maximum Input Voltage	$V_{IN\ max}$		20			mVrms
Input Levels $\|I_{IN}\|$<0.5 µA	V_{IL} V_{IH}		 0.8 V_{DD}		0.2 V_{DD}	V
Output Current V_{OL}<0.2 V_{DD};V_{OH} >0.8 V_{DD}	$\|I_{OUT}\|$		5			µA
Output Pulse	T_{100ms}	1 µVrms ≤ V_{IN} ≤ 20 mVrms	50		140	ms
	T_{200ms}	1 µVrms ≤ V_{IN} ≤ 20 mVrms	150		230	ms
	T_{500ms}	1 µVrms ≤ V_{IN} ≤ 20 mVrms	400	500	600	ms
	T_{800ms}	1 µVrms ≤ V_{IN} ≤ 20 mVrms	700	800	900	ms
Startup Time	T_{Start}	Fast Start-up Without Fast Start-up		12 3		s min
Output Delay Time	T_{Delay}			50	100	ms

TYPICAL APPLICATION



Note 1: Crystal

The crystal as well as ferrite antenna frequencies are chosen according to the time-signal system (Table 1). The crystal shunt capacitance C_0 should be matched as well as possible with the internal shunt capacitance compensation capacitance C_C. MAS9078 has five compensation capacitance options. Capacitance values and suitable crystals are described in Table 2. See also Ordering Information (p.10).

Time-Signal System	Location	Antenna Frequency	Recommended Crystal Frequency
DCF77	Germany	77.5 kHz	77.503 kHz
MSF	United Kingdom	60 kHz	60.003 kHz
WWVB	USA	60 kHz	60.003 kHz
JJY	Japan	40 kHz and 60 kHz	40.003 kHz and 60.003 kHz

Table 1 Time-Signal System Frequencies

Device	C_C	Crystal Description
MAS9078B1	0.75 pF	For single low C_0 crystal (Nominal value)
MAS9078B2	1.25 pF	For single high C_0 crystal
MAS9078B3	1.625 pF	For two parallel low C_0 crystals (dual band receiver)
MAS9078B4	2.5 pF	For two parallel high C_0 crystals (dual band receiver)
MAS9078B5	3.875 pF	Any crystal with parallel external compensation capacitor

Table 2 Compensation Capacitance Options

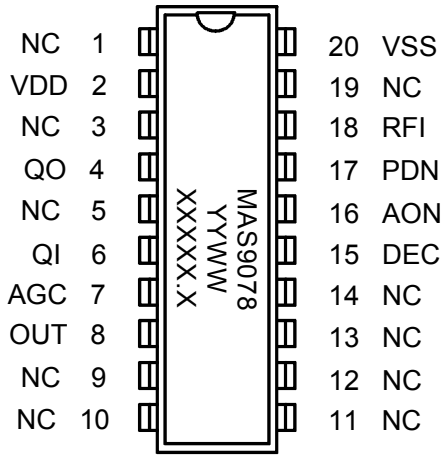
Note 2: AGC Capacitor

The AGC and DEC capacitors must have low leakage currents due to very small 40 nA signal currents through the capacitors. The insulation resistance of these capacitors should be higher than 70 MΩ. Also probes with at least 100 MΩ impedance should be used for voltage probing of AGC and DEC pins.

Note 3: Power Down / Fast Startup Control

Both power down and fast startup are controlled using the PDN pin. The device is in power down (turned off) if PDN = VDD and in power up (turned on) if PDN = VSS. Fast startup is triggered by the falling edge of PDN signal, i.e., controlling device from power down to power up. The startup time without using the fast startup control can be several minutes but with fast startup it is shortened typically to 12 s.

SAMPLES IN SBDIL 20 PACKAGE



Top Marking Definitions:
YYWW = Year Week
XXXXX.X = Lot Number

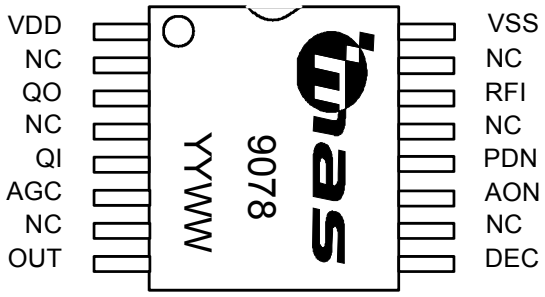
PIN DESCRIPTION

Pin Name	Pin	Type	Function	Note
NC	1			
VDD	2	P	Positive Power Supply	
NC	3			
QO	4	AO	Quartz Filter Output	
NC	5			1
QI	6	AI	Quartz Filter Input	
AGC	7	AO	AGC Capacitor	
OUT	8	DO	Receiver Output	2
NC	9			
NC	10			
NC	11			
NC	12			
NC	13			
NC	14			
DEC	15	AO	Demodulator Capacitor	
AON	16	DI	AGC On Control	3
PDN	17	AI	Power Down Input	4
RFI	18	AI	Receiver Input	
NC	19			
VSS	20	G	Power Supply Ground	

Notes:

1) Pin 5 between quartz crystal filter pins must be connected to VSS to eliminate DIL package leadframe parasitic capacitances disturbing the crystal filter performance. All other NC (Not Connected) pins are also recommended to be connected to VSS to minimize noise coupling.
2) OUT = VSS when carrier amplitude at maximum; OUT = VDD when carrier amplitude is reduced (modulated)
   - the output is a current source/sink with $|I_{OUT}| > 5\ \mu A$
   - at power down the output is pulled to VSS (pull down switch)
3) AON = VSS means AGC off (hold current gain level); AON = VDD means AGC on (working)
   - Internal pull-up with current < 1 µA which is switched off at power down
4) PDN = VSS means receiver on; PDN = VDD means receiver off
   - Fast start-up is triggered when the receiver is after power down (PDN=VDD) controlled to power up (PDN=VSS) i.e. at the falling edge of PDN signal.

PIN CONFIGURATION & TOP MARKING FOR PLASTIC TSSOP-16 PACKAGE



Top Marking Definitions:
YYWW = Year Week

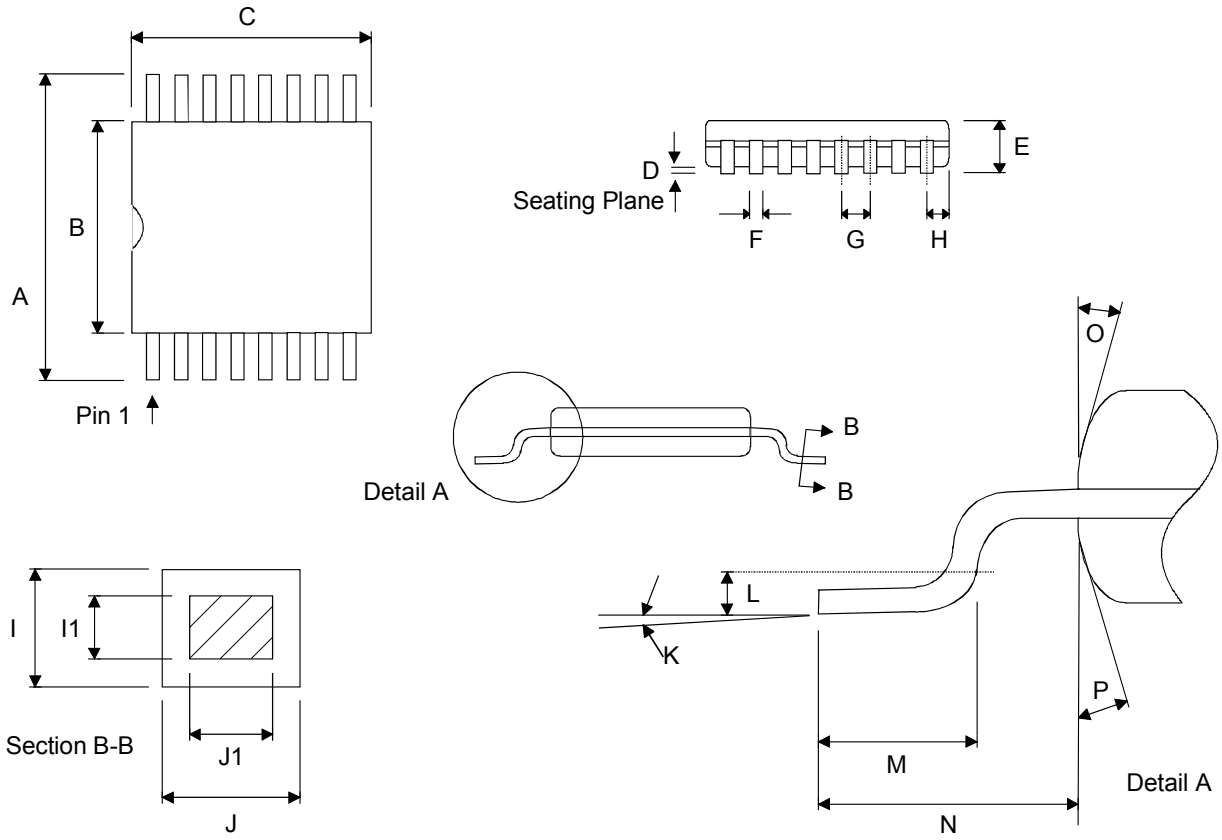
PIN DESCRIPTION

Pin Name	Pin	Type	Function	Note
VDD	1	P	Positive Power Supply	
NC	2			
QO	3	AO	Quartz Filter Output	
NC	4			1
QI	5	AI	Quartz Filter Input	
AGC	6	AO	AGC Capacitor	
NC	7			
OUT	8	DO	Receiver Output	2
DEC	9	AO	Demodulator Capacitor	
NC	10			
AON	11	DI	AGC On Control	3
PDN	12	AI	Power Down Input	4
NC	13			
RFI	14	AI	Receiver Input	
NC	15			
VSS	16	G	Power Supply Ground	

Notes:

1) Pin 4 between quartz crystal filter pins must be connected to VSS to eliminate package leadframe parasitic capacitances disturbing the crystal filter performance. All other NC (Not Connected) pins are also recommended to be connected to VSS to minimize noise coupling.
2) OUT = VSS when carrier amplitude at maximum; OUT = VDD when carrier amplitude is reduced (modulated)
   - the output is a current source/sink with $|I_{OUT}| > 5\ \mu A$
   - at power down the output is pulled to VSS (pull down switch)
3) AON = VSS means AGC off (hold current gain level); AON = VDD means AGC on (working)
   - Internal pull-up (to AGC on) with current < 1 µA which is switched off at power down
4) PDN = VSS means receiver on; PDN = VDD means receiver off
   - Fast start-up is triggered when the receiver is after power down (PDN=VDD) controlled to power up (PDN=VSS) i.e. at the falling edge of PDN signal.

PACKAGE (TSSOP16) OUTLINES



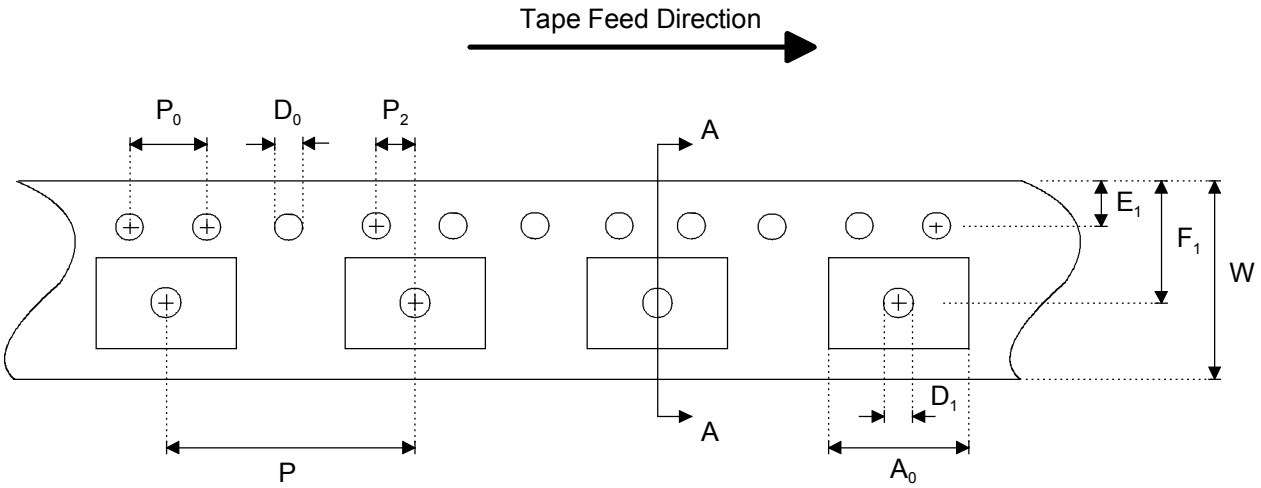
Dimension	Min	Max	Unit
A	6.40 BSC		mm
B	4.30	4.50	mm
C	5.00 BSC		mm
D	0.05	0.15	mm
E		1.10	mm
F	0.19	0.30	mm
G	0.65 BSC		mm
H	0.18	0.28	mm
I	0.09	0.20	mm
I1	0.09	0.16	mm
J	0.19	0.30	mm
J1	0.19	0.25	mm
K	0°	8°	
L	0.24	0.26	mm
M (The length of a terminal for soldering to a substrate)	0.50	0.75	mm
N	1.00 REF		mm
O	12°		
P	12°		

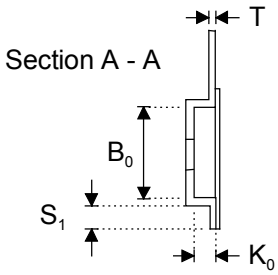
Dimensions do not include mold flash, protrusions, or gate burrs.
All dimensions are in accordance with JEDEC standard MO-153.

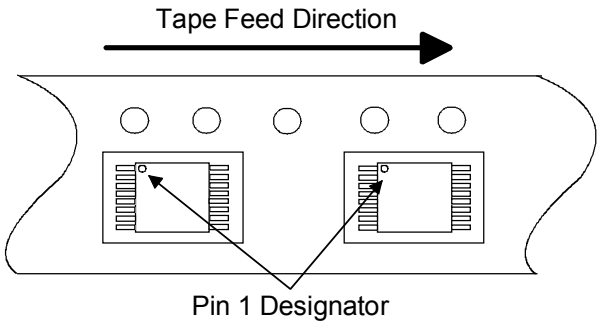
SOLDERING INFORMATION

Resistance to Soldering Heat	According to RSH test IEC 68-2-58/20 2*220°C
Maximum Temperature	240°C
Maximum Number of Reflow Cycles	2
Reflow profile	Thermal profile parameters stated in JESD22-A113 should not be exceeded. http://www.jedec.org
Seating Plane Co-planarity	max 0.08 mm
Lead Finish	Solder plate 7.62 - 25.4 µm, material Sn 85% Pb 15%

EMBOSSED TAPE SPECIFICATIONS

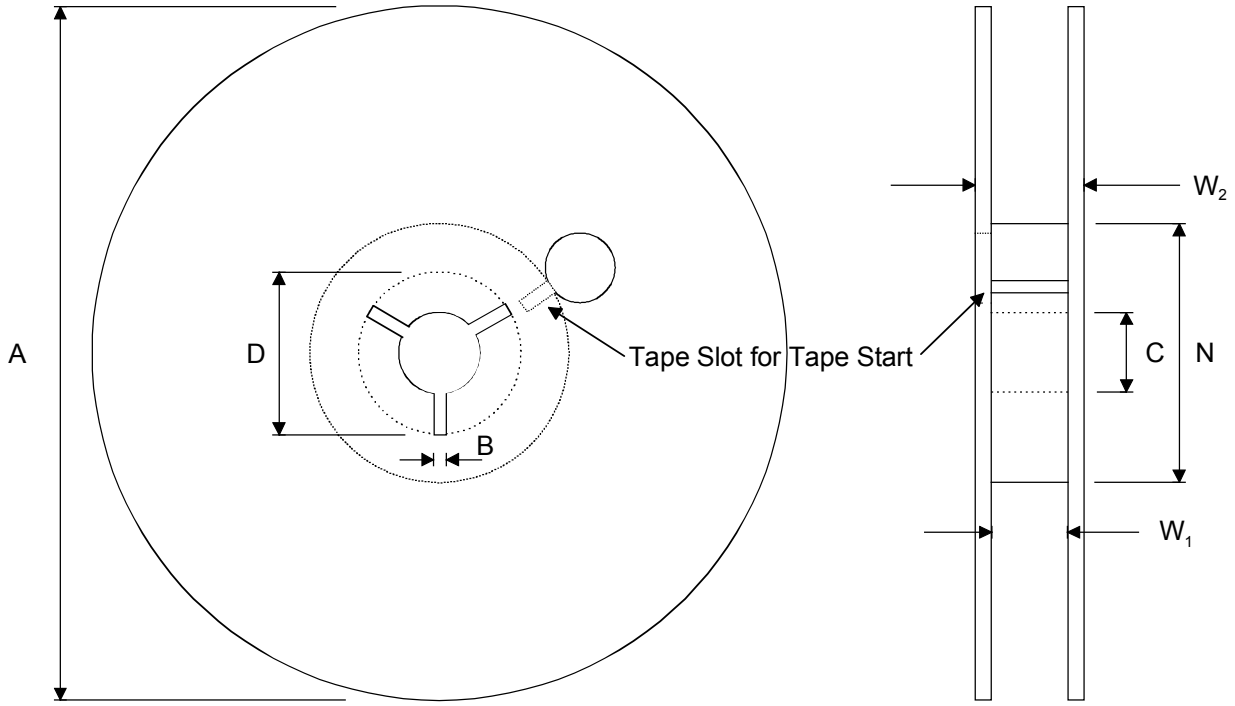






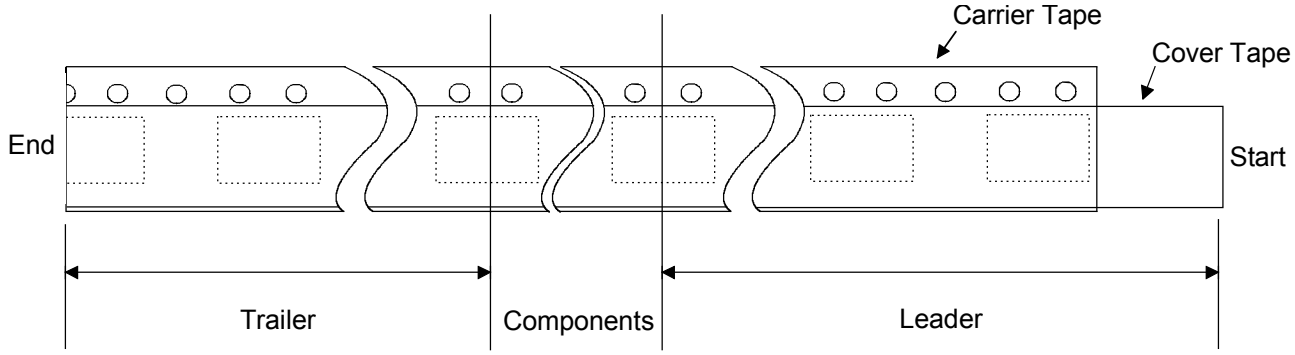
Dimension	Min	Max	Unit
A_0	6.50	6.70	mm
B_0	5.20	5.40	mm
D_0	1.50 +0.10 / -0.00		mm
D_1	1.50		mm
E_1	1.65	1.85	mm
F_1	7.20	7.30	mm
K_0	1.20	1.40	mm
P	11.90	12.10	mm
P_0	4.0		mm
P_2	1.95	2.05	mm
S_1	0.6		mm
T	0.25	0.35	mm
W	11.70	12.30	mm

REEL SPECIFICATIONS



2000 Components on Each Reel

Reel Material: Conductive, Plastic Antistatic or Static Dissipative
Carrier Tape Material: Conductive
Cover Tape Material: Static Dissipative



Dimension	Min	Max	Unit
A		330	mm
B	1.5		mm
C	12.80	13.50	mm
D	20.2		mm
N	50		mm
W_1 (measured at hub)	12.4	14.4	mm
W_2 (measured at hub)		18.4	mm
Trailer	160		mm
Leader	390, of which minimum 160 mm of empty carrier tape sealed with cover tape		mm
Weight		1500	g

ORDERING INFORMATION

Product Code	Product	Package	Capacitance Option
MAS9078BTB1	AM-Receiver IC	EWS-tested wafer, Thickness 480 µm	C_C = 0.75 pF (Nominal)
MAS9078BTB2	AM-Receiver IC	EWS-tested wafer, Thickness 480 µm	C_C = 1.25 pF
MAS9078BTB3	AM-Receiver IC	EWS-tested wafer, Thickness 480 µm	C_C = 1.625 pF
MAS9078BTB4	AM-Receiver IC	EWS-tested wafer, Thickness 480 µm	C_C = 2.5 pF
MAS9078BTB5	AM-Receiver IC	EWS-tested wafer, Thickness 480 µm	C_C = 3.875 pF
MAS9078BTC1	AM-Receiver IC	EWS-tested wafer, Thickness 400 µm	C_C = 0.75 pF
MAS9078BTC2	AM-Receiver IC	EWS-tested wafer, Thickness 400 µm	C_C = 1.25 pF
MAS9078BTC3	AM-Receiver IC	EWS-tested wafer, Thickness 400 µm	C_C = 1.625 pF
MAS9078BTC4	AM-Receiver IC	EWS-tested wafer, Thickness 400 µm	C_C = 2.5 pF
MAS9078BTC5	AM-Receiver IC	EWS-tested wafer, Thickness 400 µm	C_C = 3.875 pF
MAS9078BUA1-T	AM-Receiver IC	TSSOP-16, Tape & Reel	C_C = 0.75 pF (Nominal)

Contact Micro Analog Systems Oy for other wafer thickness options.

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