National Semiconductor

January 1988

MM54HCT190/MM74HCT190 Synchronous Decade Up/Down Counters with Mode Control. MM54HCT191/MM74HCT191 Synchronous Binary Up/Down Counters with Mode Control

General Description

These high speed synchronous counters utilize advanced silicon-gate CMOS technology. They possess the high noise immunity and low power consumption of CMOS technology, along with the speeds of low power Schottky TTL. These circuits are synchronous, reversible, up/down counters. The MM54HCT191/MM74HCT191 are 4-bit binary counters and the MM54HCT190/MM74HCT190 are BCD counters.

Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change simultaneously when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four master-slave flip-flops are triggered on a low-to-high level transition of the clock input, if the enable input is low. A high at the enable input inhibits counting. The direction of the count is determined by the level of the down/up input. When low, the counter counts up and when high, it counts down.

These counters are fully programmable; that is, the outputs may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change independent of the level of the clock input. This feature allows the counters to be used as divide by N dividers by simply modifying the count length with the preset inputs.

Two outputs have been made available to perform the cascading function; ripple clock and maximum/minimum count. The latter output produces a high level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low level output pulse equal in width to the low level portion of the clock input when an overflow or underflow condition exists. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high speed operation.

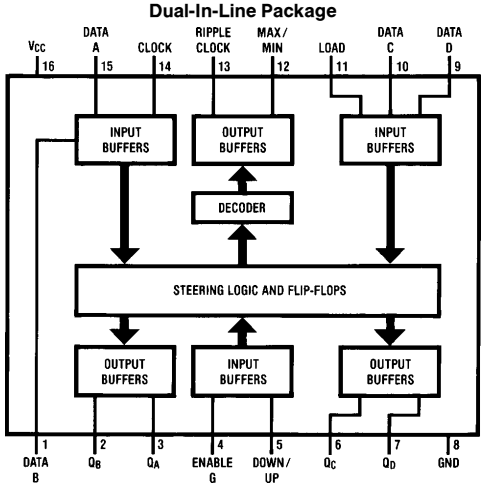
MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS devices. These parts are also plug-in replacements for LS-TTL devices can be used to reduce power consumption in existing designs.

Features

- Level changes on Enable or Down/Up can be made regardless of the level of the clock.
- Low quiescent supply current: 80 μA maximum (74HCT Series)
- Low input current: 1 μA maximum
- TTL compatible inputs

Connection Diagram

Dual-In-Line Package



TL/F/5744–1

Truth Table

Load	Enable G	Down/ Up	Clock	Function
H	L	L	↑	Count Up
H	L	H	↑	Count Down
L	X	X	X	Load
H	H	X	X	No Change

Order Number MM54HCT190/191
or MM74HCT190/191

MM54HCT190/MM74HCT190 Synchronous Decade Up/Down Counters with Mode Control.
MM54HCT191/MM74HCT191 Synchronous Binary Up/Down Counters with Mode Control

©1995 National Semiconductor Corporation

RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings (Notes 1 and 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to + 7.0V
DC Input Voltage (V_{IN})	−1.5V to V_{CC} + 1.5V
DC Output Voltage (V_{OUT})	−0.5V to V_{CC} + 0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per Pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per Pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to + 150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage			
(V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times			
(t_r, t_f)		500	ns

DC Electrical Characteristics V_{CC} = 5V ± 10% unless otherwise specified

Symbol	Parameter	Conditions	T_A = 25°C	74HCT T_A = −40°C to 85°C	54HCT T_A = −55°C to 125°C	Units
			Typ	Guaranteed Limits		
V_{IH}	Minimum High Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High Level Output Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	V_{CC}	V_{CC} − 0.1	V_{CC} − 0.1	V_{CC} − 0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	4.2	3.98	3.84	3.7	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	5.2	4.98	4.84	4.7	V
V_{OL}	Maximum Low Level Voltage	V_{IN} = V_{IH} or V_{IL}					
		$\|I_{OUT}\|$ = 20 μA	0	0.1	0.1	0.1	V
		$\|I_{OUT}\|$ = 4.0 mA, V_{CC} = 4.5V	0.2	0.26	0.33	0.4	V
		$\|I_{OUT}\|$ = 4.8 mA, V_{CC} = 5.5V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND, V_{IH} or V_{IL}		±0.1	±1.0	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 μA		8	80	160	μA
		V_{IN} = 2.4V or 0.5V (Note 4)		1.0	1.2	1.3	mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power dissipation temperature derating—plastic "N" package: −12 mW/°C from 65°C to 85°C; ceramic "J" package: −12 mW/°C from 100°C to 125°C.

Note 4: Measured per pin, all other inputs held at V_{CC} or GND.

AC Electrical Characteristics $T_A = 25°C$, $V_{CC} = 5.0V$, $t_r = t_f = 6$ ns, $C_L = 15$ pF unless otherwise specified

Symbol	Parameter	From Input	To Output	Conditions	Typ	Guaranteed Limits	Units
f_{MAX}	Maximum Clock Frequency				40		MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Load	Q_A, Q_B Q_C, Q_D		30		ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Data A, B, C, D	Q_A, Q_B Q_C, Q_D		27		ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Clock	Ripple Clock		16		ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Clock	Q_A, Q_B Q_C, Q_D		24		ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Clock	Max/Min		30		ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Down/Up	Ripple Clock		29		ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Down/Up	Max/Min		22		ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay Time	Enable	Ripple Clock		22		ns
t_W	Minimum Clock or Load Input Pulse Width				10		ns

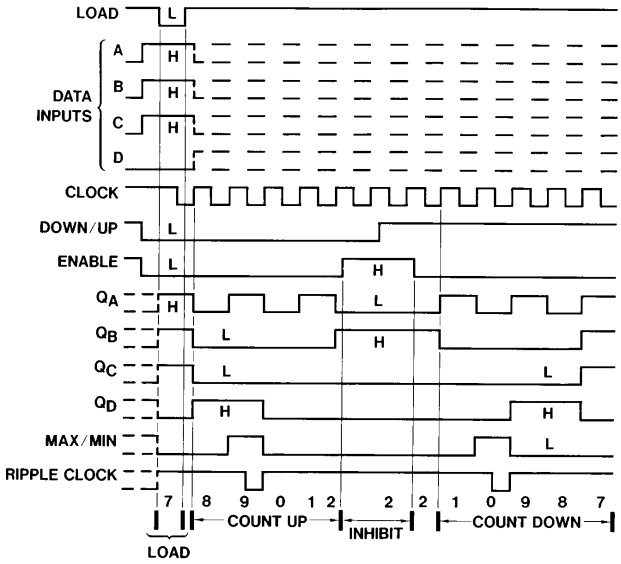
AC Electrical Characteristics $V_{CC}=5V \pm 10\%$, $C_L = 50$ pF, $t_r = t_f = 6$ ns unless otherwise specified

Symbol	Parameter	From Input	To Output	Conditions	$T_A=25°C$	74HCT $T_A=-40°C$ to $85°C$		54HCT $T_A=-55°C$ to $125°C$	Units
					Typ	Guaranteed Limits			
f_{MAX}	Maximum Clock Frequency				28	20	16	13	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Load	Q_A, Q_B Q_C, Q_D		31	44	55	66	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Data A, B, C, D	Q_A, Q_B Q_C, Q_D		30	40	50	60	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Clock	Ripple Clock		24	30	38	45	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Clock	Q_A, Q_B Q_C, Q_D		32	43	54	65	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Clock	Max/Min		45	55	69	83	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Down/Up	Ripple Clock		42	50	63	75	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay Time	Down/Up	Max/Min		30	45	56	68	ns
t_{PHL}, t_{PLH}	Propagation Delay Time	Enable	Ripple Clock		26	33	41	50	ns
t_W	Minimum Clock Pulse Width				15	25	31	38	ns
t_S	Minimum Set-Up Time	Data	Load		10	20	25	30	ns
t_H	Minimum Hold Time	Load	Data		−3	5	6	8	ns
t_S	Minimum Set-Up Time	Down/Up	Clock		23	30	38	45	ns
t_H	Minimum Hold Time	Clock	Down/Up		−7	0	0	0	ns
t_S	Minimum Set-Up Time	Enable	Clock		13	20	25	30	ns
t_H	Minimum Hold Time	Clock	Enable		−5	0	0	0	ns
t_{THL}, t_{TLH}	Maximum Output Rise and Fall Time				10	15	19	22	ns
C_{IN}	Maximum Input Capacitance				5				pF
C_{PD}	Power Dissipation Capacitance (Note 5)				35				pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Timing Diagrams

'HCT190 Synchronous Decade Counters
Typical Load, Count, and Inhibit Sequences

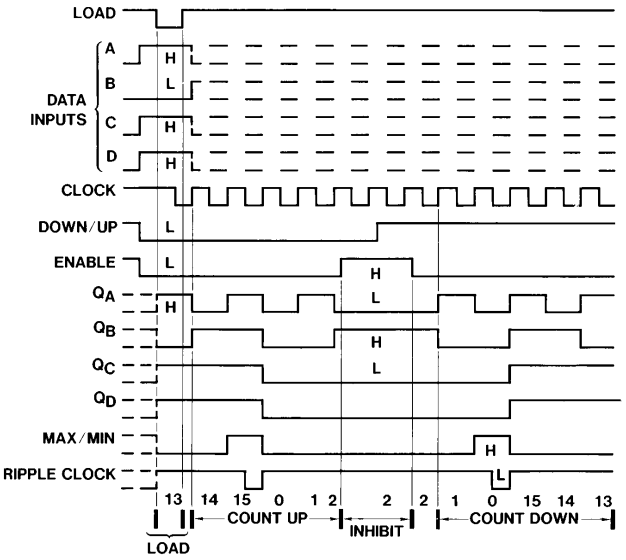


TL/F/5744–5

Sequence:

(1) Load (preset) to BCD seven
(2) Count up to eight, nine, zero, one and two
(3) Inhibit
(4) Count down to one, zero, nine, eight and seven

'HCT191 Synchronous Binary Counters
Typical Load, Count, and Inhibit Sequence



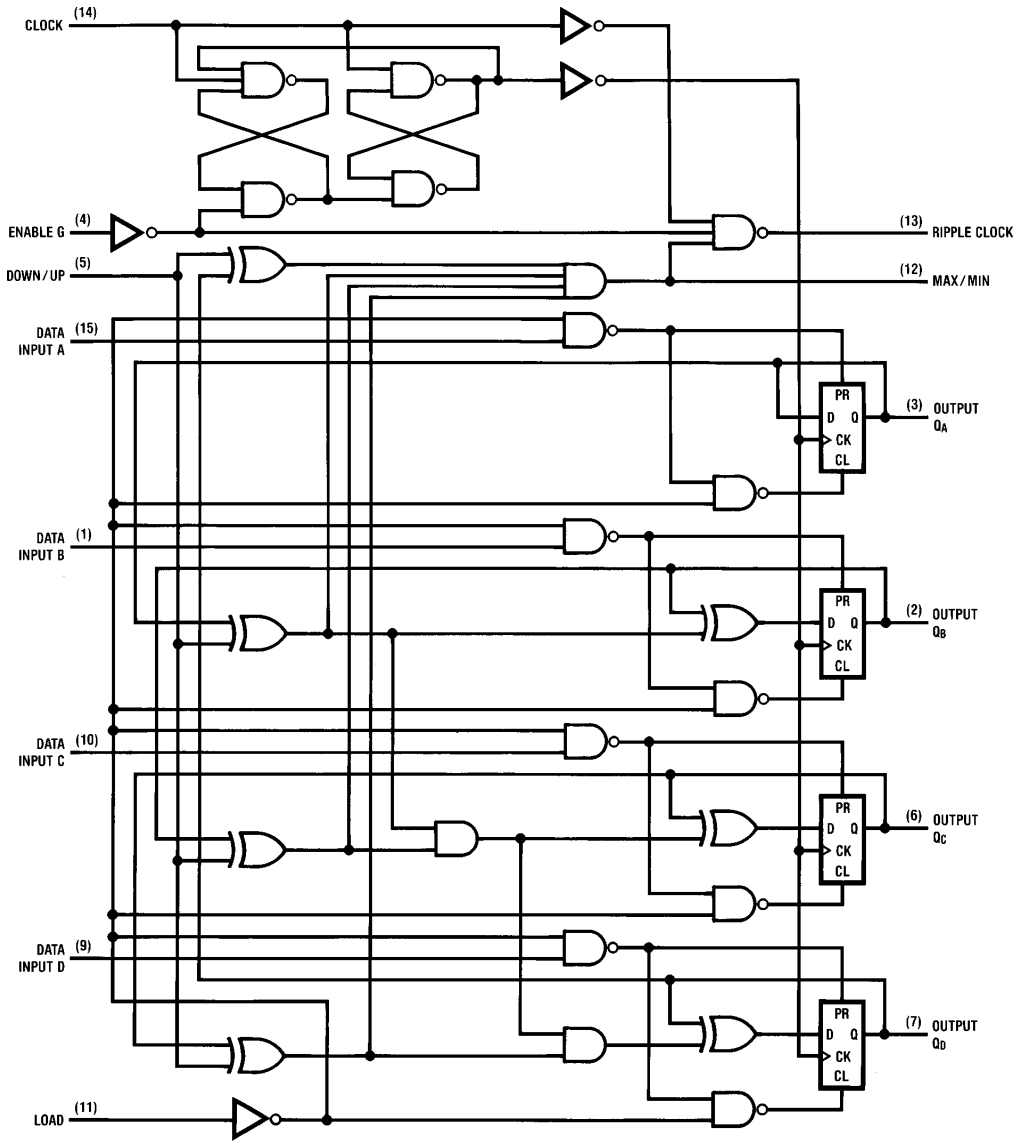
TL/F/5744–6

Sequence:

(1) Load (preset) to binary thirteen
(2) Count up to fourteen, fifteen, zero, one and two
(3) Inhibit
(4) Count down to one, zero, fifteen, fourteen and thirteen

Logic Diagram

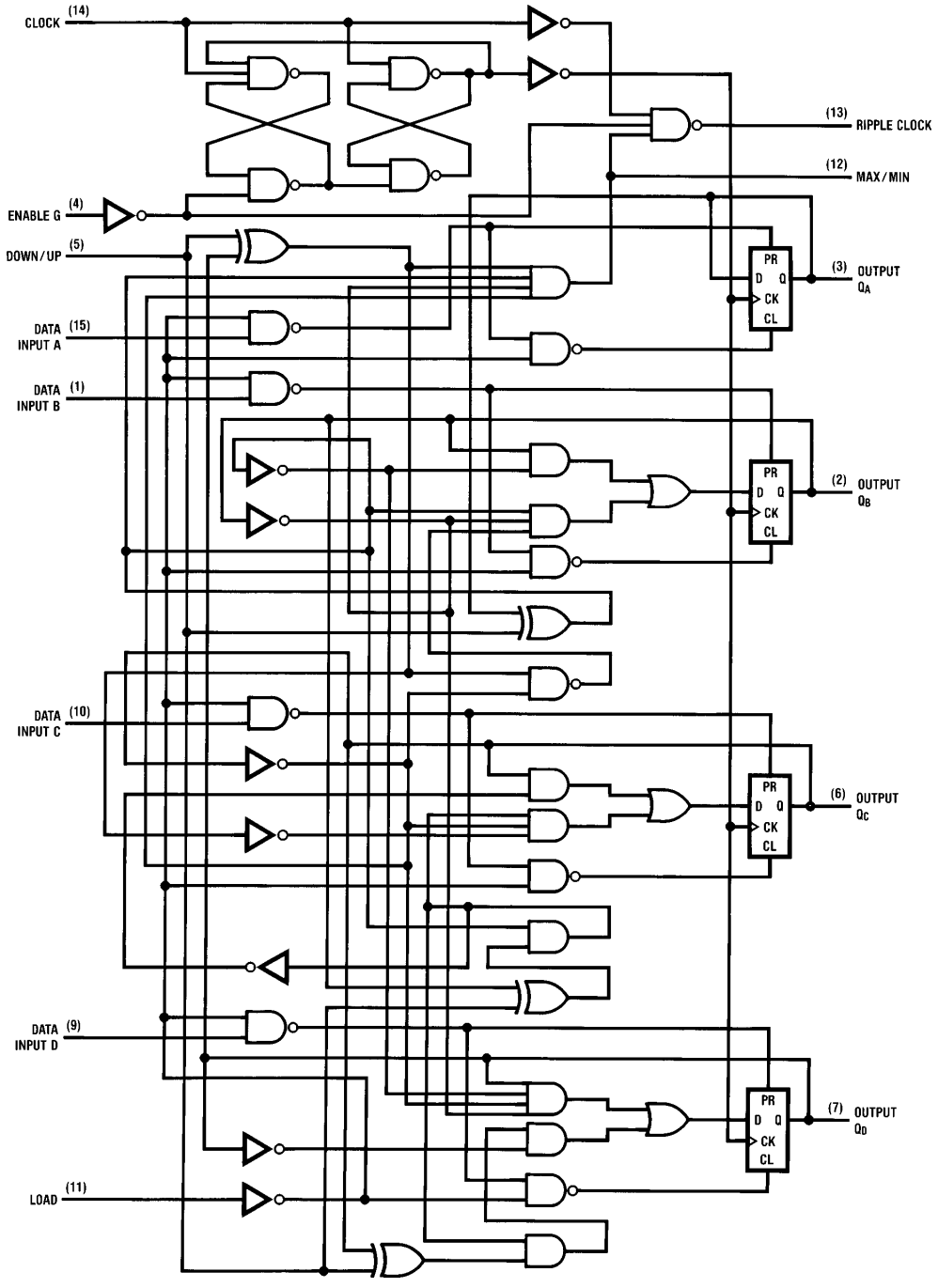
'HCT191



TL/F/5744–3

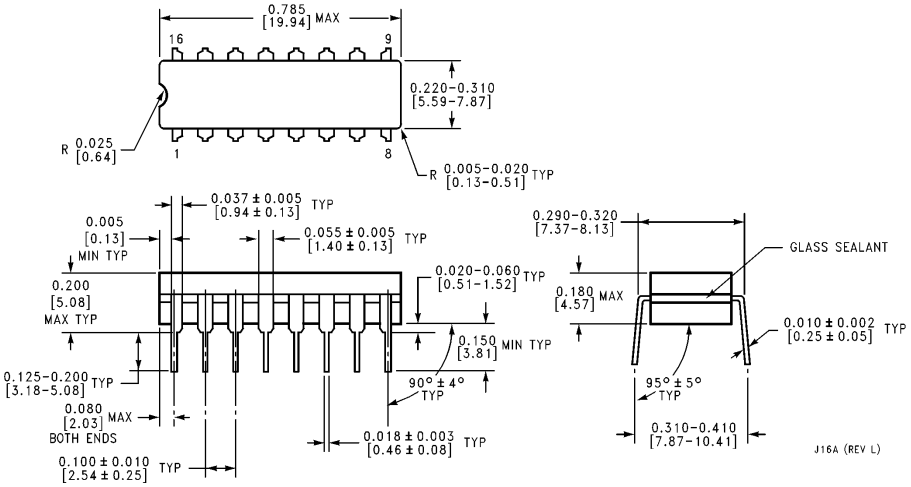
Logic Diagram (Continued)

'HCT190 Decade Counters

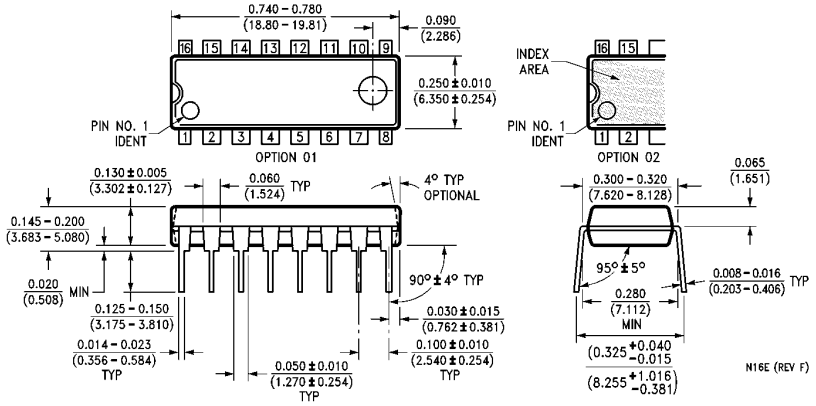


TL/F/5744–7

Physical Dimensions inches (millimeters)



Order Number MM54HCT191J or MM74HCT191J
NS Package J16A



Order Number MM74HCT191N
NS Package N16E

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
Email: cnjwge@tevm2.nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Français Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.