
155 Mbps to 4.25 Gbps Limiting Amplifier With LOS and RSSI

FEATURES

- Multi-Rate Operation from 155 Mbps up to 4.25 Gbps
- 89 mW Power Consumption
- Input Offset Cancellation
- High Input Dynamic Range
- Output Disable
- CML Data Outputs
- Receive Signal Strength Indicator (RSSI)
- Loss of Signal Detection
- Polarity Select
- Single 3.3-V Supply
- Surface Mount Small Footprint 3-mm × 3-mm 16-Pin QFN Package
- Pin-Compatible with the ONET2501PA and ONET3301PA

APPLICATIONS

- Multi-Rate OC3 to OC-48 FEC SONET/SDH Transmission Systems
- 1.0625 Gbps, 2.125 Gbps, and 4.25 Gbps Fibre Channel Receivers
- Gigabit Ethernet Receivers

DESCRIPTION

The ONET4201PA is a versatile high-speed, 3.3-V limiting amplifier for multiple fiber optic applications with data rates up to 4.25 Gbps.

This device provides a gain of about 50 dB, which ensures a fully differential output swing for input signals as low as 3 mV_{p-p}.

The high input signal dynamic range ensures low jitter output signals even when overdriven with input signal swings as high as 1200 mV_{p-p}.

The ONET4201PA provides a loss of signal detection as well as a received signal strength indicator.

The part is available in a small footprint 3-mm × 3-mm 16-pin QFN package and is pin-compatible with the ONET2501PA and ONET3301PA.

This power efficient limiting amplifier typically dissipates less than 89 mW and it is characterized for operation from –40°C to 85°C.



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BLOCK DIAGRAM

A simplified block diagram of the ONET4201PA is shown in Figure 1.

This compact, low power 4.25 Gbps limiting amplifier consists of a high-speed data path with offset cancellation block, a loss of signal and RSSI detection block, and a bandgap voltage reference and bias current generation block.

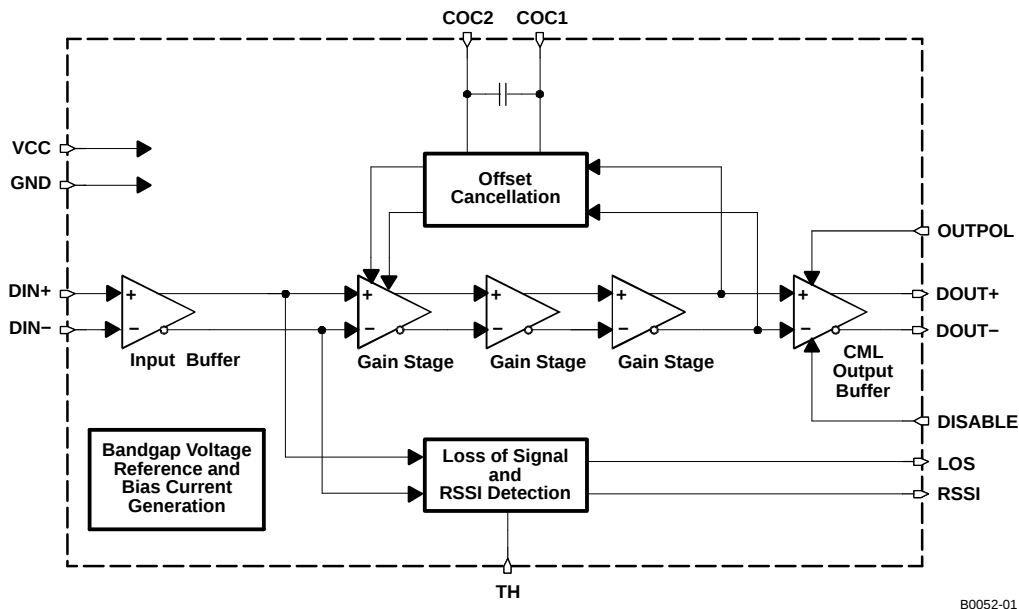


Figure 1. Simplified Block Diagram of the ONET4201PA

HIGH SPEED DATA PATH

The high-speed data signal is applied to the data path by means of the input signal pins DIN+/DIN-. The data path consists of the input stage with $2 \times 50\text{-}\Omega$ on-chip line termination to VCC, three gain stages, which provide the required typical gain of about 50 dB, and a CML output stage. The amplified data output signal is available at the output pins DOUT+/DOUT-, which provide $2 \times 50\text{-}\Omega$ back-termination to VCC. The output stage also includes a data polarity switching function, which is controlled by the OUTPUTPOL input, and a disable function, controlled by the signal applied to the DISABLE input pin.

Offset cancellation compensates for internal offset voltages and thus ensures proper operation even for very small input data signals.

The low frequency cutoff is typically as low as 25 kHz with the built-in filter capacitor.

For applications which require even lower cutoff frequencies, an additional external filter capacitor may be connected to the COC1/COC2 pins.

LOSS OF SIGNAL AND RSSI DETECTION

The output signal of the input buffer is monitored by the loss of signal and RSSI detection circuitry. In this block a signal is generated that is linearly proportional to the input amplitude over a wide input voltage range. This signal is available at the RSSI output pin.

Furthermore, this circuit block compares the input signal to a threshold which can be programmed by means of an external resistor connected to the TH pin. If the input signal falls below the specified threshold, a loss of signal is indicated at the LOS pin.

The relation between the LOS assert voltage V_{AST} (in mV_{p-p}) and the external resistor R_{TH} (in $\text{k}\Omega$) connected to the TH pin can be approximated as given below:

$$R_{TH} \approx \frac{20.8 \text{ k}\Omega}{\left(V_{AST}/\text{mV}_{p-p} - 1\right)} + 300 \text{ }\Omega \quad (1)$$

$$V_{AST} \approx \frac{20.8 \text{ mV}_{p-p}}{R_{TH}/\text{k}\Omega - 0.3} + 1 \text{ mV}_{p-p} \quad (2)$$

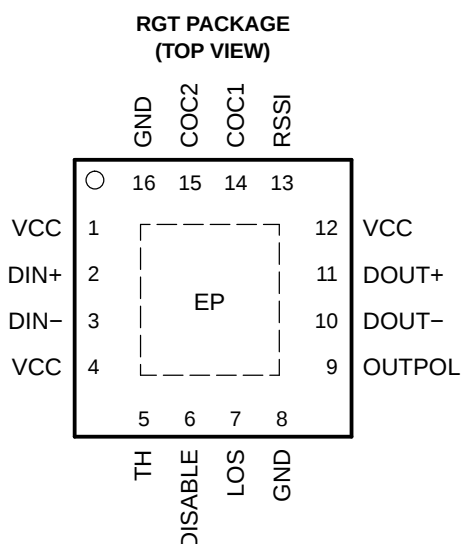
BANDGAP VOLTAGE AND BIAS GENERATION

The ONET4201PA limiting amplifier is supplied by a single 3.3-V±10% supply voltage connected to the VCC pins. This voltage is referred to ground (GND).

An on-chip bandgap voltage circuit generates a supply voltage independent reference from which all other internally required voltages and bias currents are derived.

PACKAGE

For the ONET4201PA a small footprint 3-mm × 3-mm 16-pin QFN package, with a lead pitch of 0,5 mm, is used. The pin out is shown in [Figure 2](#).



P0019-01

Figure 2. Pinout of ONET4201PA in a 3mm x 3mm 16 Pin QFN Package (Top View)

TERMINAL FUNCTIONS

TERMINAL		TYPE	DESCRIPTION
NO.	NAME		
1, 4, 12	VCC	supply	3.3-V ± 10% supply voltage
2	DIN+	analog-in	Non-inverted data input. On-chip 50-Ω terminated to VCC.
3	DIN–	analog-in	Inverted data input. On-chip 50-Ω terminated to VCC.
5	TH	analog-in	LOS threshold adjustment with resistor to GND.
6	DISABLE	CMOS-in	Disables CML output stage when set to high level.
7	LOS	CMOS-out	High level indicates that the input signal amplitude is below the programmed threshold level.
8, 16, EP	GND	supply	Circuit ground. Exposed die pad (EP) must be grounded.
9	OUTPOL	CMOS-in	Output data signal polarity select (internally pulled high). Setting to a high level or leaving the pin open selects normal polarity. Low level selects inverted polarity.
10	DOUT–	CML-out	Inverted data output. On-chip 50-Ω back-terminated to VCC.
11	DOUT+	CML-out	Non-inverted data output. On-chip 50-Ω back-terminated to VCC.

TERMINAL FUNCTIONS (continued)

TERMINAL		TYPE	DESCRIPTION
NO.	NAME		
13	RSSI	analog-out	Analog output voltage proportional to the input data amplitude. Indicates the strength of the received signal (RSSI).
14	COC1	analog	Offset cancellation filter capacitor terminal 1. Connect an additional filter capacitor between this pin and COC2 (pin 15). To disable the offset cancellation loop connect COC1 and COC2 (pins 14 and 15).
15	COC2	analog	Offset cancellation filter capacitor terminal 2. Connect an additional filter capacitor between this pin and COC1 (pin 14). To disable the offset cancellation loop connect COC1 and COC2 (pins 14 and 15).

ABSOLUTE MAXIMUM RATINGSover operating free-air temperature range (unless otherwise noted)⁽¹⁾

		VALUE/UNIT
V_{CC}	Supply voltage ⁽²⁾	–0.3 V to 4.0 V
V_{DIN+} , V_{DIN-}	Voltage at DIN+, DIN– ⁽²⁾	0.5 V to 4.0 V
V_{TH} , $V_{DISABLE}$, V_{LOS} , V_{OUTPOL} , V_{DOUT+} , V_{DOUT-} , V_{RSSI} , V_{COC1} , V_{COC2}	Voltage at TH, DISABLE, LOS, OUTPOL, DOUT+, DOUT–, RSSI, COC1, COC2 ⁽²⁾	–0.3 V to 4.0 V
$V_{COC,DIFF}$	Differential voltage between COC1 and COC2	±1 V
$V_{DIN,DIFF}$	Differential voltage between DIN+ and DIN–	±2.5 V
I_{LOS}	Current into LOS	–1 to 9 mA
I_{DIN+} , I_{DIN-} , I_{DOUT+} , I_{DOUT-}	Continuous current at inputs and outputs	–25 mA to 25 mA
ESD	ESD rating at all pins	2 kV (HBM)
$T_{J(max)}$	Maximum junction temperature	125°C
T_{STG}	Storage temperature range	–65 to 85°C
T_A	Characterized free-air operating temperature range	–40 to 85°C
T_{LEAD}	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
T_A	Operating free-air temperature	–40		85	°C
V_{IH}	CMOS input high voltage	2.1			V
V_{IL}	CMOS input low voltage			0.6	V

DC ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{CC} Supply voltage		3	3.3	3.6	V
I _{VCC} Supply current	DISABLE = low (includes CML output current)		35	45	mA
	DISABLE = low (excludes CML output current)		27	35	
V _{OD} Differential data output voltage swing	DISABLE = high		0.25	10	mV _{p-p}
	DISABLE = low, 5 mV _{p-p} ≤ V _{IN} ≤ 1200 mV _{p-p}	520	760	1200	
R _{IN} , R _{OUT} Data input/output resistance	Single-ended		50		Ω
RSSI output voltage	Input = 8 mV _{p-p} , R _{RSSI} ≥ 10 kΩ		200		mV
	Input = 80 mV _{p-p} , R _{RSSI} ≥ 10 kΩ		1900		
RSSI linearity	8 mV _{p-p} ≤ V _{IN} ≤ 80 mV _{p-p}		±3%		
V _{IN(MIN)} Data input sensitivity	BER < 10 ⁻¹⁰		3	5	mV _{p-p}
V _{IN(MAX)} Data input overload		1200			mV _{p-p}
LOS high voltage	I _{SOURCE} = 30 μA	2.4			V
LOS low voltage	I _{SINK} = 1 mA			0.4	V

AC ELECTRICAL CHARACTERISTICS

over recommended operating conditions, typical operating condition is at V_{CC} = 3.3 V and T_A = 25°C (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Low frequency –3 dB bandwidth	C _{OC} = open		25		kHz
	C _{OC} = 0.54 μF		0.8		
Data rate		4.25			Gb/s
V _{NI} Input referred noise			230		μV _{RMS}
DJ Deterministic jitter	K28.5 pattern at 4.25 Gbps		3	19	ps _{p-p}
	K28.5 pattern at 2.125 Gbps		4	35	
	K28.5 pattern at 1.0625 Gbps		4	72	
RJ Random jitter	Input = 5 mVpp		9		ps _{RMS}
	Input = 10 mVpp		4		
t _R Output rise time	20% to 80%		45	85	ps
t _F Output fall time	20% to 80%		45	85	ps
LOS hysteresis	K28.5 pattern at 4.25 Gbps, 20log (V _{DEA} /V _{AST})	2.5	4.5		dB
R _{TH} LOS threshold adjustment resistor range	See ⁽¹⁾	1.2		6.8	kΩ
V _{AST} LOS assert voltage	R _{TH} = 2.5 kΩ, K28.5 pattern at 4.25 Gbps ⁽¹⁾		10		mV _{p-p}
	R _{TH} = 6.8 kΩ, K28.5 pattern at 4.25 Gbps ⁽¹⁾	2	5		
V _{DEA} LOS de-assert voltage	R _{TH} = 2.5 kΩ, K28.5 pattern at 4.25 Gbps ⁽¹⁾		17		mV _{p-p}
	R _{TH} = 6.8 kΩ, K28.5 pattern at 4.25 Gbps ⁽¹⁾		8	20	
T _{LOS} LOS assert/deassert time		2		100	μs
T _{DIS} Disable response time			20		ns

- (1) For a given external resistor connected to the TH pin the LOS assert voltage value may vary due to part-to-part variations. If high precision is required, adjustment of this resistor for each device is mandatory.

TYPICAL CHARACTERISTICS

Typical operating condition is at $V_{CC} = 3.3\text{ V}$ and $T_A = 25^\circ\text{C}$ (unless otherwise noted).

TRANSFER FUNCTION

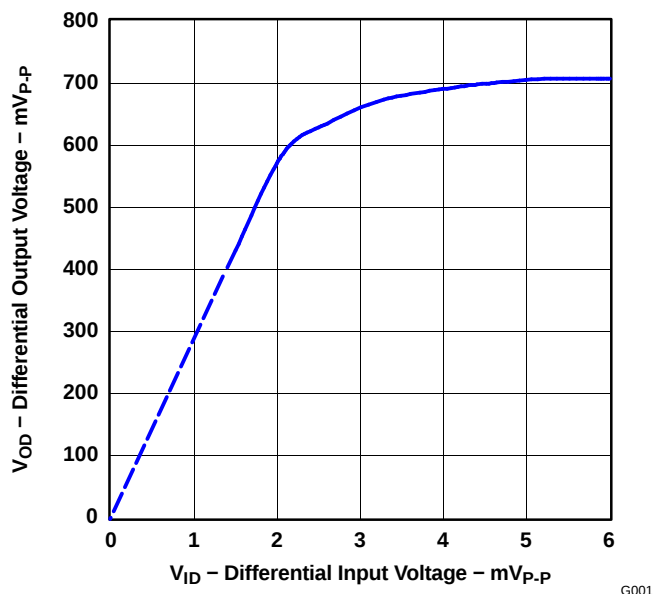


Figure 3.

RANDOM JITTER
vs INPUT AMPLITUDE

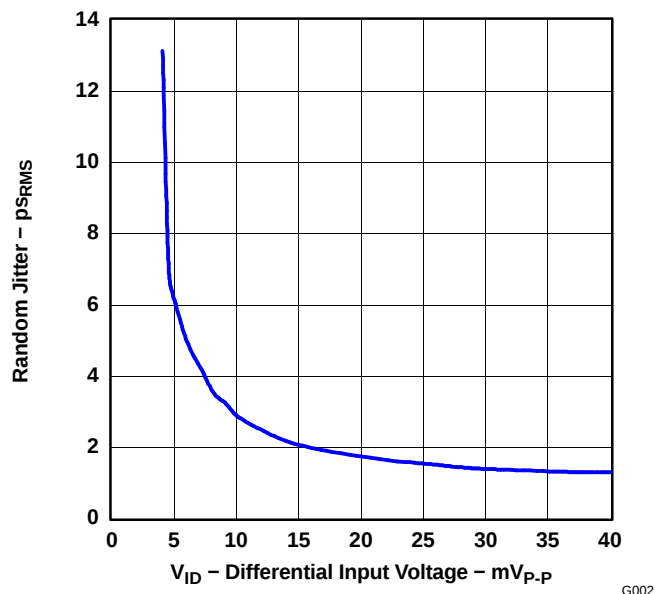


Figure 4.

BIT-ERROR RATIO
INPUT AMPLITUDE

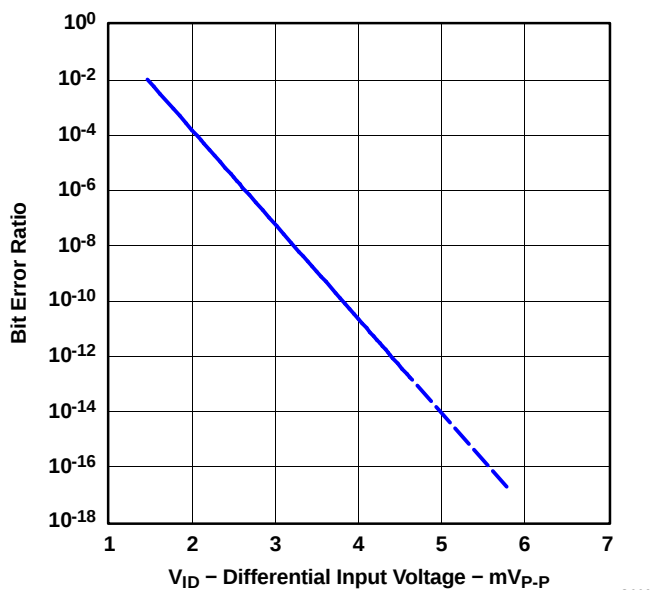


Figure 5.

FREQUENCY RESPONSE

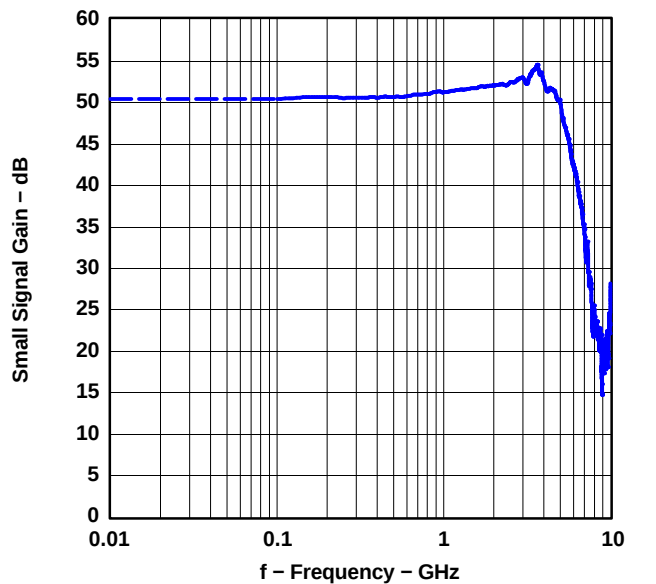


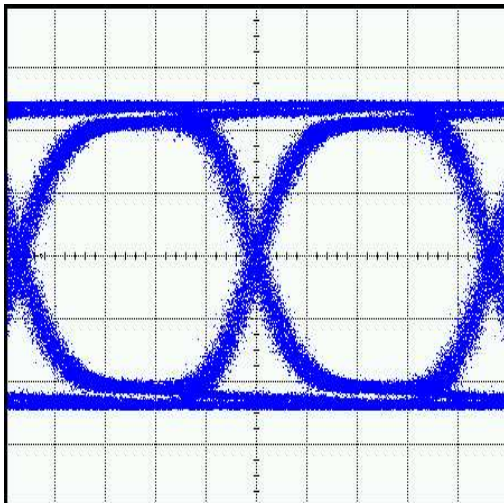
Figure 6.

TYPICAL CHARACTERISTICS (continued)

Typical operating condition is at $V_{CC} = 3.3\text{ V}$ and $T_A = 25^\circ\text{C}$ (unless otherwise noted).

OUTPUT EYE-DIAGRAM AT 4.25 GBPS
AND MINIMUM INPUT VOLTAGE (5 mV_{p-p})

V_{OD} – Differential Output Voltage – 160 mV/Div



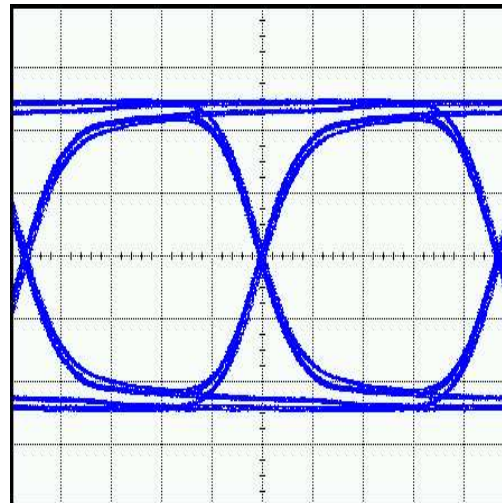
t – Time – 50 ps/Div

G005

Figure 7.

OUTPUT EYE-DIAGRAM AT 4.25 GBPS
AND MAXIMUM INPUT VOLTAGE (1200 mV_{p-p})

V_{OD} – Differential Output Voltage – 160 mV/Div



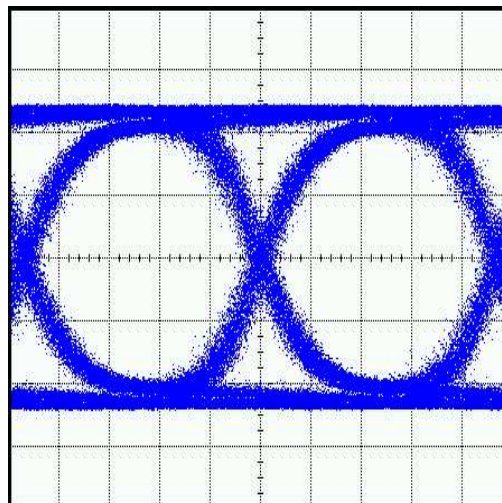
t – Time – 50 ps/Div

G006

Figure 8.

OUTPUT EYE-DIAGRAM AT 4.25 GBPS AND 85°C
AND MINIMUM INPUT VOLTAGE (5 mV_{p-p})

V_{OD} – Differential Output Voltage – 160 mV/Div



t – Time – 50 ps/Div

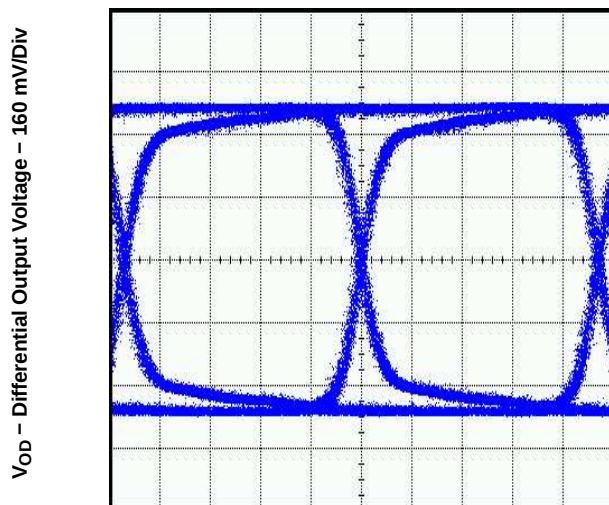
G007

Figure 9.

TYPICAL CHARACTERISTICS (continued)

Typical operating condition is at $V_{CC} = 3.3\text{ V}$ and $T_A = 25^\circ\text{C}$ (unless otherwise noted).

**OUTPUT EYE-DIAGRAM AT 2.125 GBPS
AND MINIMUM INPUT VOLTAGE (5 mV_{p-p})**

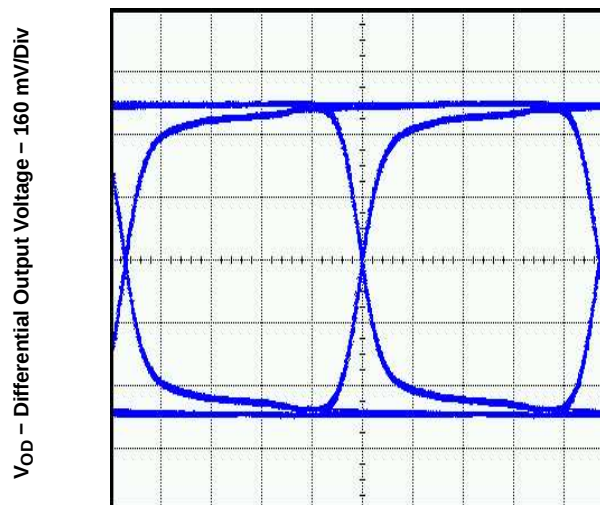


t – Time – 100 ps/Div

G008

Figure 10.

**OUTPUT EYE-DIAGRAM AT 2.125 GBPS
AND MAXIMUM INPUT VOLTAGE (1200 mV_{p-p})**

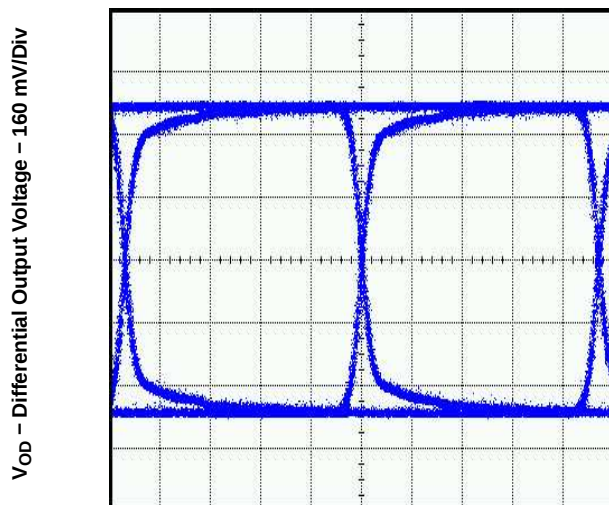


t – Time – 100 ps/Div

G009

Figure 11.

**OUTPUT EYE-DIAGRAM AT 1.0625 GBPS
AND MINIMUM INPUT VOLTAGE (5 mV_{p-p})**

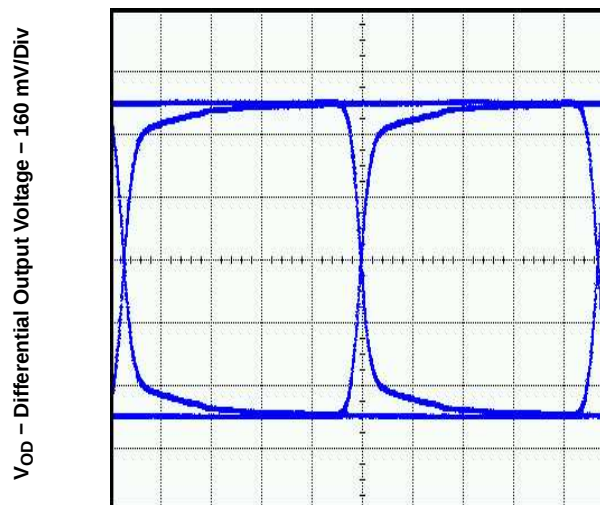


t – Time – 200 ps/Div

G010

Figure 12.

**OUTPUT EYE-DIAGRAM AT 1.0625 GBPS
AND MAXIMUM INPUT VOLTAGE (1200 mV_{p-p})**



t – Time – 200 ps/Div

G011

Figure 13.

TYPICAL CHARACTERISTICS (continued)

Typical operating condition is at $V_{CC} = 3.3\text{ V}$ and $T_A = 25^\circ\text{C}$ (unless otherwise noted).

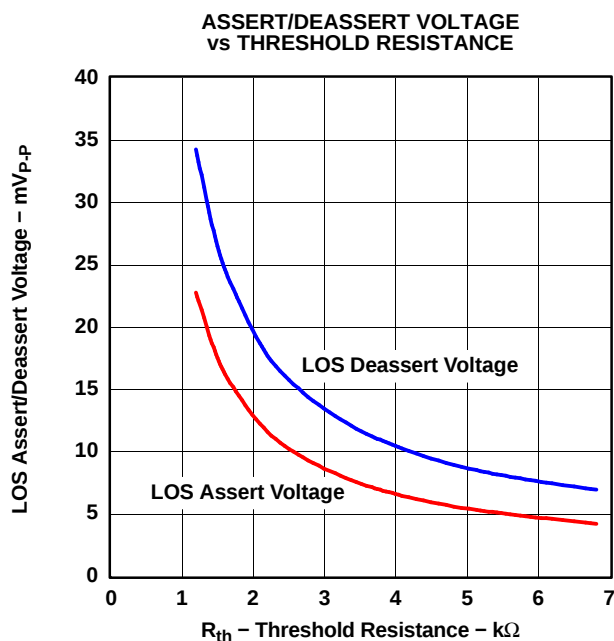


Figure 14.

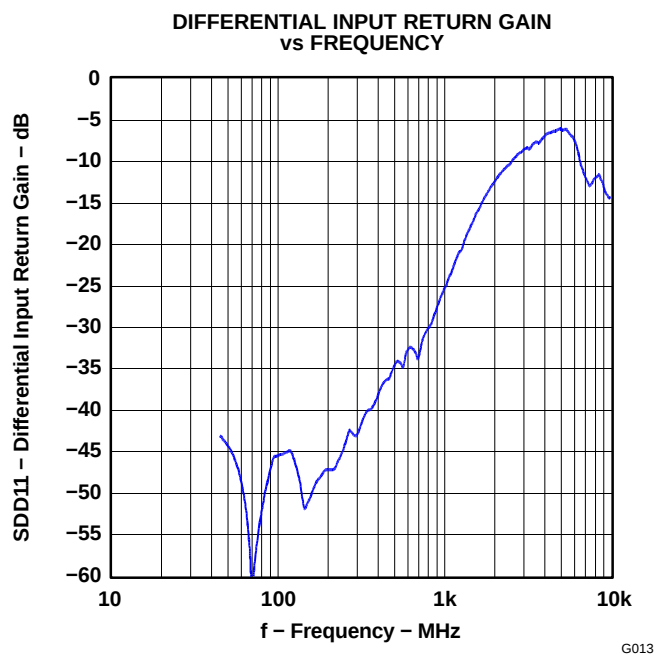


Figure 15.

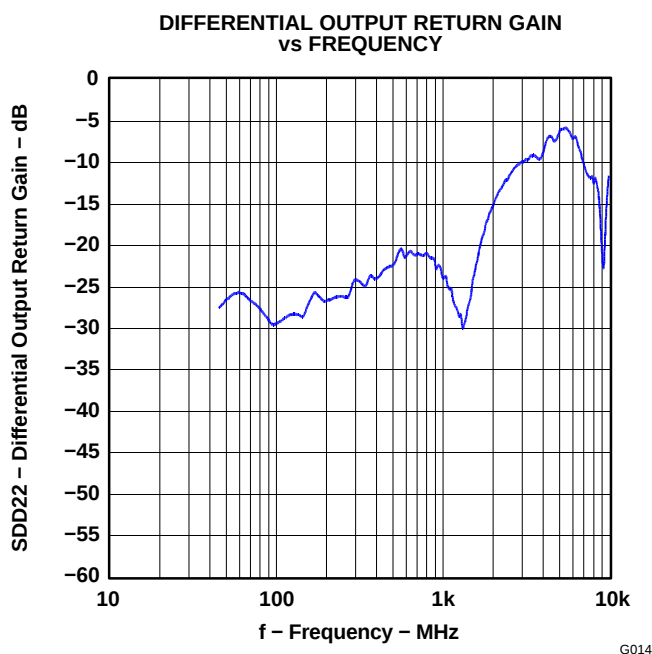


Figure 16.

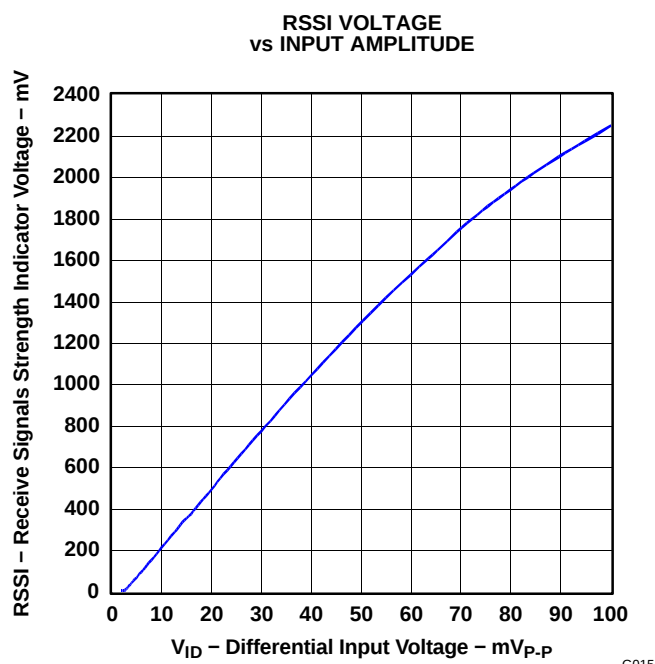
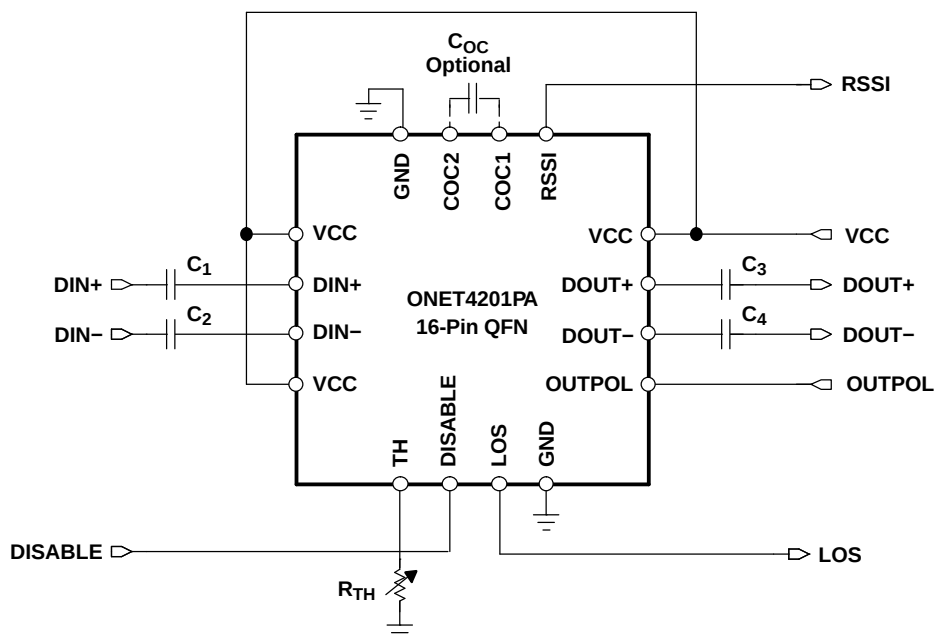


Figure 17.

APPLICATION INFORMATION

Figure 18 shows the ONET4201PA connected with an ac-coupled interface to the data signal source as well as to the output load.

Besides the ac-coupling capacitors C_1 through C_4 in the input and output data signal lines, the only required external component is the LOS threshold setting resistor R_{th} . In addition, an optional external filter capacitor (C_{oc}) may be used if a lower cutoff frequency is desired.



S0072-01

Figure 18. Basic Application Circuit With AC-Coupled I/Os

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
ONET4201PARGTR	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ONET4201PARGTRG4	ACTIVE	QFN	RGT	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ONET4201PARGTT	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ONET4201PARGTTG4	ACTIVE	QFN	RGT	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

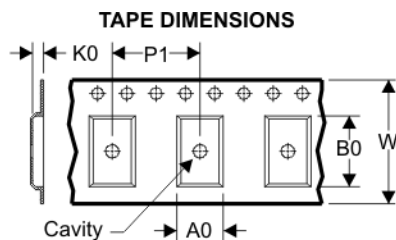
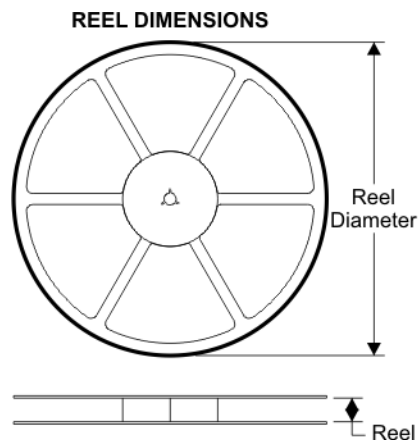
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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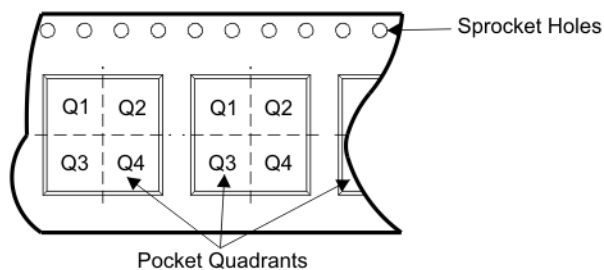
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL BOX INFORMATION



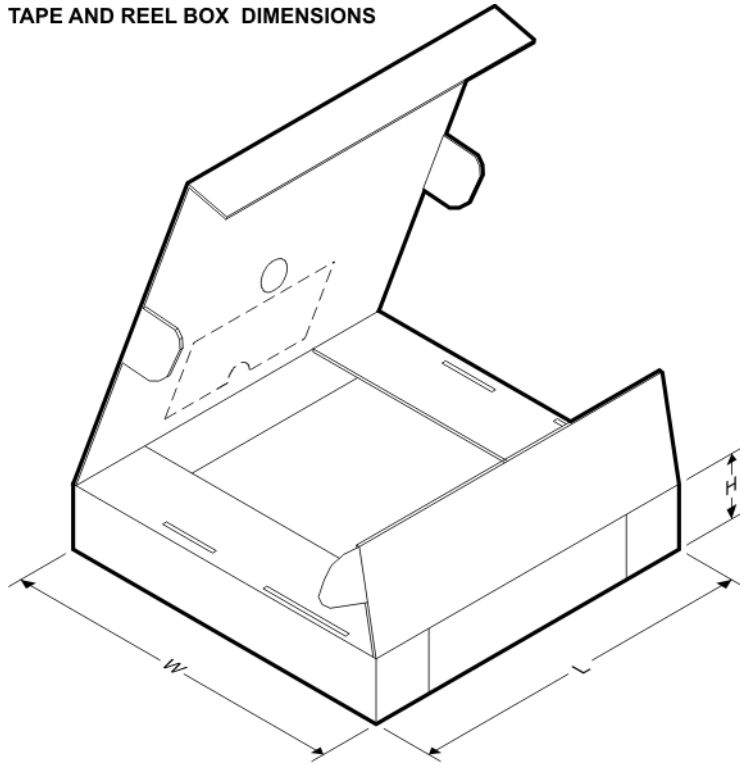
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ONET4201PARGTR	RGT	16	SITE 60	330	12	3.3	3.3	1.1	8	12	Q2
ONET4201PARGTT	RGT	16	SITE 60	330	12	3.3	3.3	1.1	8	12	Q2

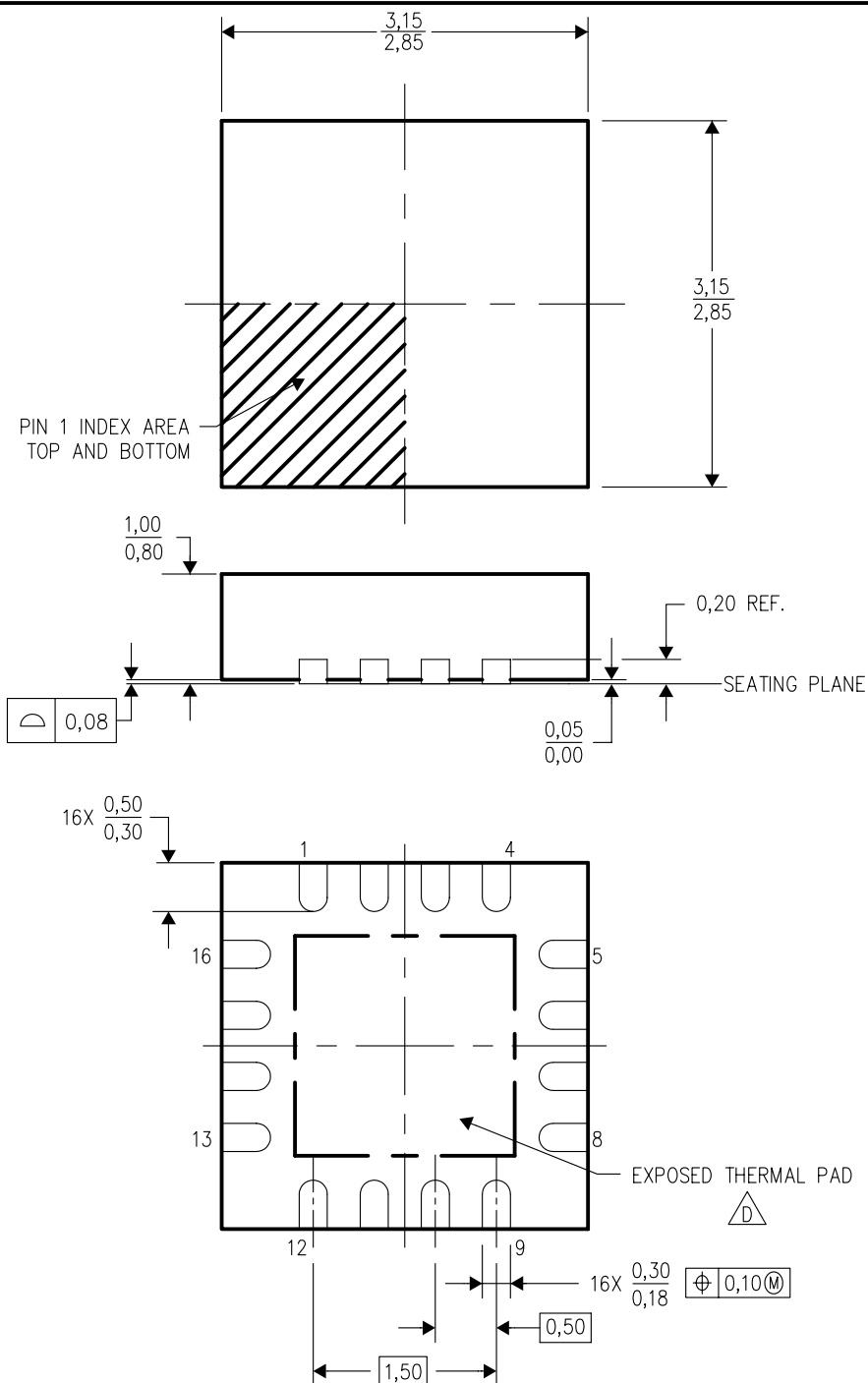
TAPE AND REEL BOX DIMENSIONS



Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
ONET4201PARGTR	RGT	16	SITE 60	342.9	336.6	20.64
ONET4201PARGTT	RGT	16	SITE 60	342.9	336.6	20.64

RGT (S-PQFP-N16)

PLASTIC QUAD FLATPACK



4203495/E 11/04

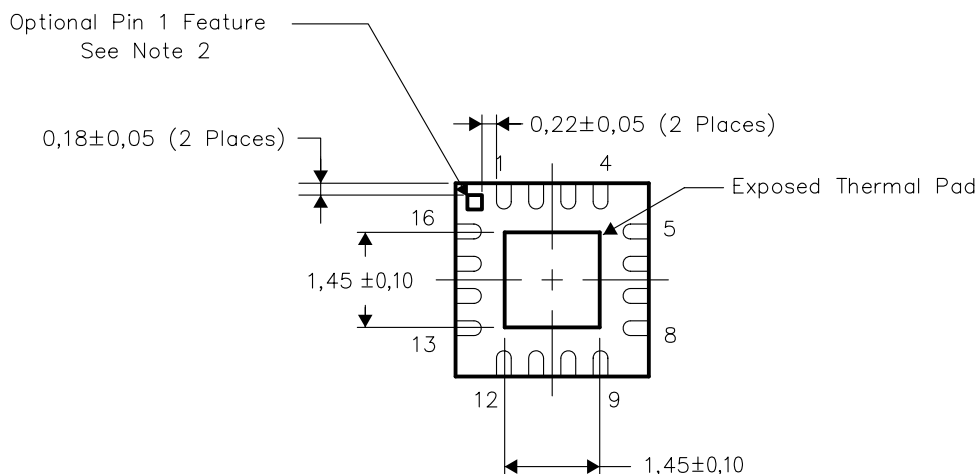
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Quad Flatpack, No-leads (QFN) package configuration.
 -  D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
 - E. Falls within JEDEC MO-220.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No-Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

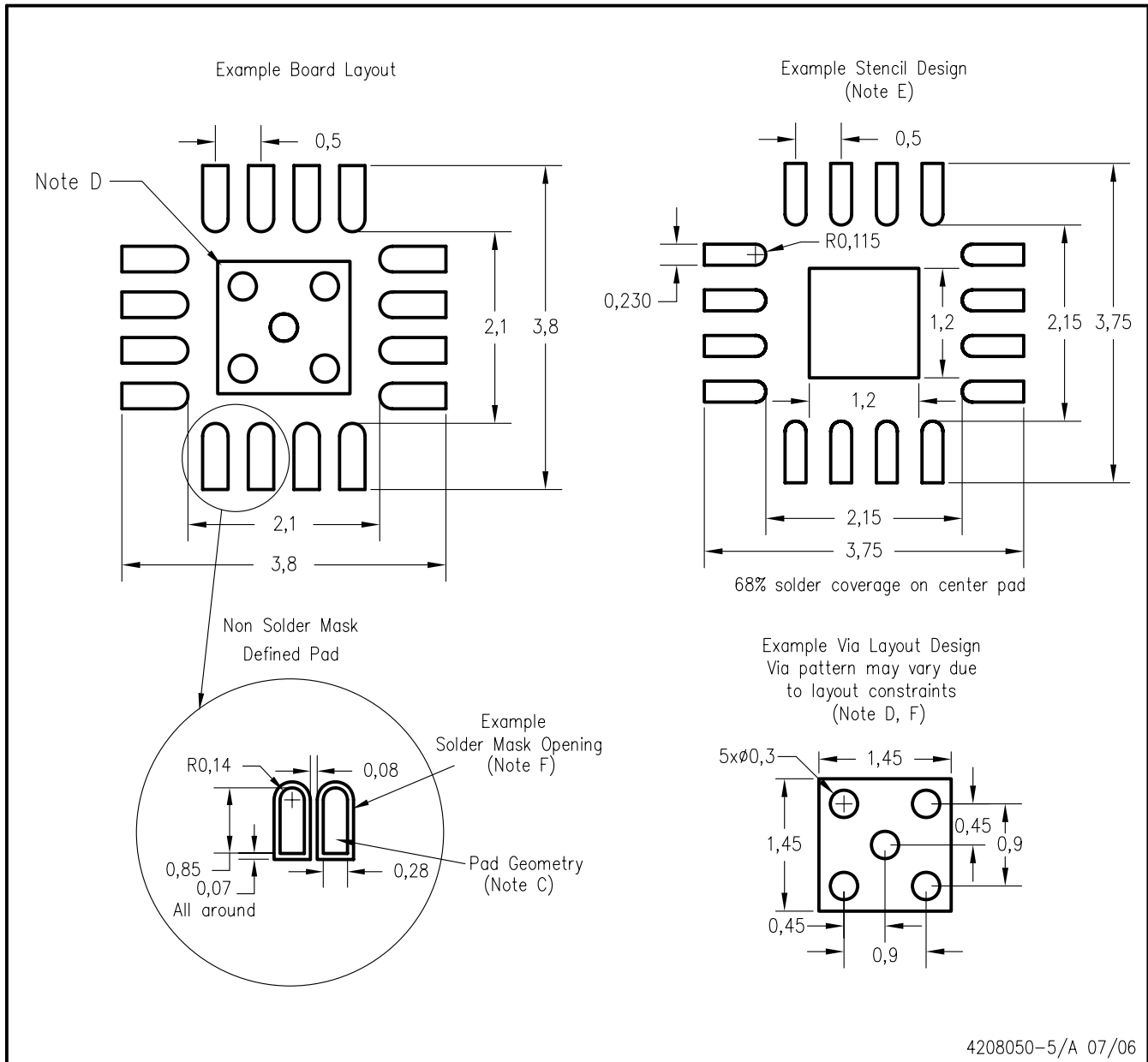


Bottom View
Exposed Thermal Pad Dimensions

NOTES:

- 1) All linear dimensions are in millimeters
- 2) The Pin 1 Identification mark is an optional feature that may be present on some devices
In addition, this Pin 1 feature if present is electrically connected to the center thermal pad and therefore should be considered when routing the board layout.

RGT (S-PQFP-N16)



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

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