NID5003N

Preferred Device

Self-Protected FET with Temperature and Current Limit

42 V, 20 A, Single N−Channel, DPAK

HDPlus™ devices are an advanced series of power MOSFETs which utilize ON Semiconductors latest MOSFET technology process to achieve the lowest possible on−resistance per silicon area while incorporating smart features. Integrated thermal and current limits work together to provide short circuit protection. The devices feature an integrated Drain−to−Gate Clamp that enables them to withstand high energy in the avalanche mode. The Clamp also provides additional safety margin against unexpected voltage transients. Electrostatic Discharge (ESD) protection is provided by an integrated Gate−to−Source Clamp.

Features

- Short Circuit Protection/Current Limit
- Thermal Shutdown with Automatic Restart
- I_{DSS} Specified at Elevated Temperature
- Avalanche Energy Specified
- Slew Rate Control for Low Noise Switching
- Overvoltage Clamped Protection

MOSFET MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain−to−Source Voltage Internally Clamped	V_{DSS}	42	Vdc
Gate−to−Source Voltage	V_{GS}	±14	Vdc
Drain Current Continuous	I_D	Internally Limited	
Total Power Dissipation @ T_A = 25°C (Note 1) @ T_A = 25°C (Note 2)	P_D	 1.3 2.3	W
Thermal Resistance Junction−to−Case Junction−to−Ambient (Note 1) Junction−to−Ambient (Note 2)	 $R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	 3.0 95 54	°C/W
Single Pulse Drain−to−Source Avalanche Energy (V_{DD} = 25 Vdc, V_{GS} = 5.0 Vdc, I_L = 3.2 Apk, L = 120 mH, R_G = 25 Ω)	E_{AS}	600	mJ
Operating and Storage Temperature Range (Note 3)	T_J, T_{stg}	−55 to 150	°C

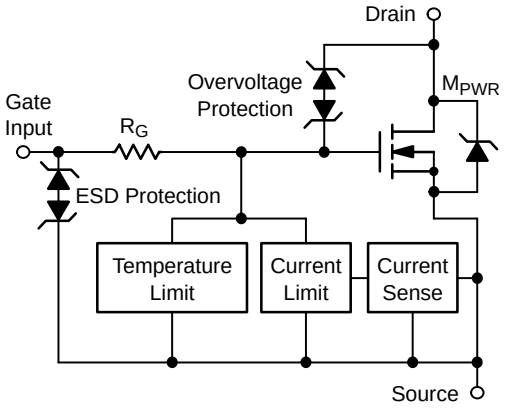
Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Surface mounted onto minimum pad size (0.412″ square) FR4 PCB, 1 oz cu.
2. Mounted onto 1″ square pad size (1.127″ square) FR4 PCB, 1 oz cu.
3. Normal pre−fault operating range. See thermal limit range conditions.

ON Semiconductor®

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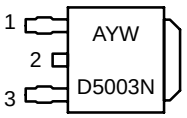
V_{DSS} (Clamped)	$R_{DS(on)}$ TYP	I_D MAX (Limited)
42 V	42 mΩ @ 10 V	20 A*





DPAK
CASE 369C
STYLE 2

MARKING DIAGRAM



D5003N = Device Code
A = Assembly Location
Y = Year
W = Work Week

1 = Gate
2 = Drain
3 = Source

ORDERING INFORMATION

Device	Package	Shipping†
NID5003NT4	DPAK	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Preferred devices are recommended choices for future use and best overall value.

*Max current may be limited below this value depending on input conditions.

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MOSFET ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain−to−Source Clamped Breakdown Voltage (V_{GS} = 0 Vdc, I_D = 250 μAdc) (V_{GS} = 0 Vdc, I_D = 250 μAdc, T_J = −40°C to 150°C)	$V_{(BR)DSS}$	 42 40	 46 45	 51 51	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 32 Vdc, V_{GS} = 0 Vdc, T_J = 150°C)	I_{DSS}	 − −	 0.6 2.5	 5.0 −	μAdc
Gate Input Current (V_{GS} = 5.0 Vdc, V_{DS} = 0 Vdc)	I_{GSSF}	−	50	125	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1.2 mAdc) Threshold Temperature Coefficient	$V_{GS(th)}$	 1.0 −	 1.7 5.0	 2.2 −	Vdc −mV/°C
Static Drain−to−Source On−Resistance (Note 4) (V_{GS} = 10 Vdc, I_D = 3.0 Adc, T_J @ 25°C) (V_{GS} = 10 Vdc, I_D = 3.0 Adc, T_J @ 150°C)	$R_{DS(on)}$	 − −	 42 76	 51 104	mΩ
Static Drain−to−Source On−Resistance (Note 4) (V_{GS} = 5.0 Vdc, I_D = 3.0 Adc, T_J @ 25°C) (V_{GS} = 5.0 Vdc, I_D = 3.0 Adc, T_J @ 150°C)	$R_{DS(on)}$	 − −	 50 88	 58 125	mΩ
Source−Drain Forward On Voltage (I_S = 7.0 A, V_{GS} = 0 V)	V_{SD}	−	0.95	1.1	V
SWITCHING CHARACTERISTICS					
Turn−on Time (V_{in} to 90% I_D)	R_L = 4.7 Ω, V_{in} = 0 to 10 V, V_{DD} = 12 V	$T_{(on)}$	−	16	20	μs
Turn−off Time (V_{in} to 10% I_D)	R_L = 4.7 Ω, V_{in} = 0 to 10 V, V_{DD} = 12 V	$T_{(off)}$	−	80	100	
Slew Rate On	R_L = 4.7 Ω, V_{in} = 0 to 10 V, V_{DD} = 12 V	$-dV_{DS}/dt_{on}$	−	1.4	−	V/μs
Slew Rate Off	R_L = 4.7 Ω, V_{in} = 10 to 0 V, V_{DD} = 12 V	dV_{DS}/dt_{off}	−	0.5	−	V/μs

SELF PROTECTION CHARACTERISTICS (T_J = 25°C unless otherwise noted) (Note 5)

Current Limit	(V_{GS} = 5.0 Vdc) V_{DS} = 10 V (V_{GS} = 5.0 Vdc, T_J = 150°C)	I_{LIM}	12 7	18 13	24 18	Adc
Current Limit	(V_{GS} = 10 Vdc) V_{DS} = 10 V (V_{GS} = 10 Vdc, T_J = 150°C)	I_{LIM}	18 13	22 18	30 25	
Temperature Limit (Turn−off)	V_{GS} = 5.0 Vdc	$T_{LIM(off)}$	150	175	200	°C
Thermal Hysteresis	V_{GS} = 5.0 Vdc	$\Delta T_{LIM(on)}$	−	15	−	°C
Temperature Limit (Turn−off)	V_{GS} = 10 Vdc	$T_{LIM(off)}$	150	165	185	°C
Thermal Hysteresis	V_{GS} = 10 Vdc	$\Delta T_{LIM(on)}$	−	15	−	°C
Input Current during Thermal Fault	V_{DS} = 35 V, (V_{GS} = 5.0 V, T_j = 150°C)	$I_{g(fault)}$	0.6	−	−	mA
Input Current during Thermal Fault	V_{DS} = 35 V, (V_{GS} = 10 V, T_j = 150°C)	$I_{g(fault)}$	2.0	−	−	mA

ESD ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Electro−Static Discharge Capability Human Body Model (HBM) Machine Model (MM)	ESD	 4000 400	 − −	 − −	V

4. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
5. Fault conditions are viewed as beyond the normal operating range of the part.

TYPICAL PERFORMANCE CURVES

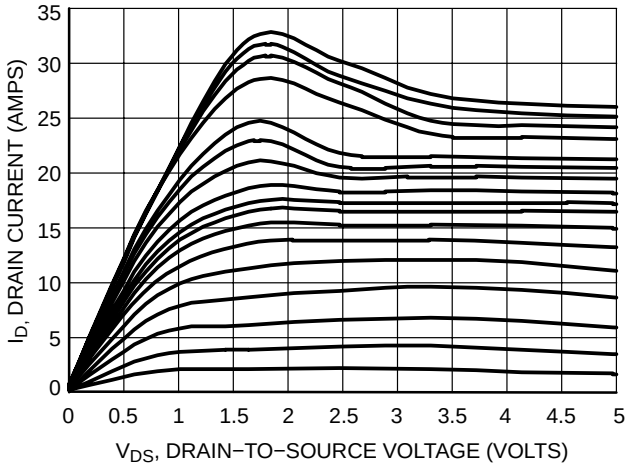


Figure 1. On−Region Characteristics

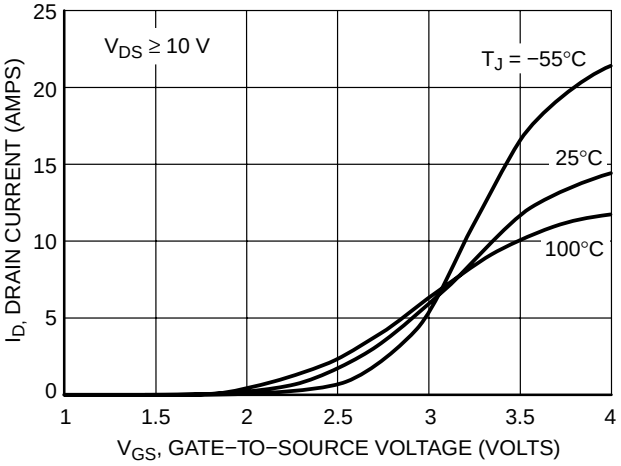


Figure 2. Transfer Characteristics

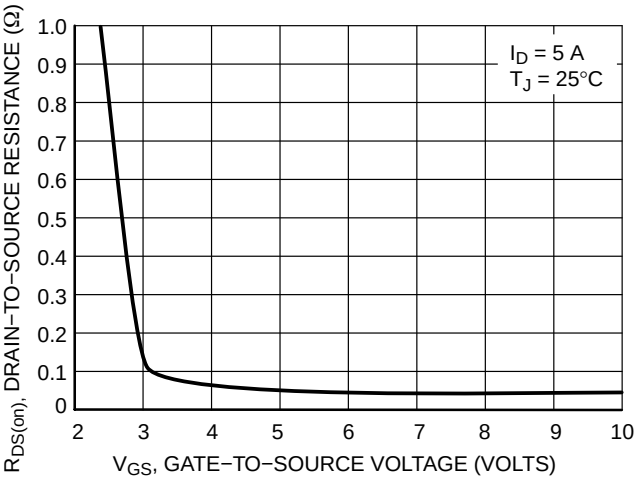


Figure 3. On−Resistance vs. Gate−to−Source Voltage

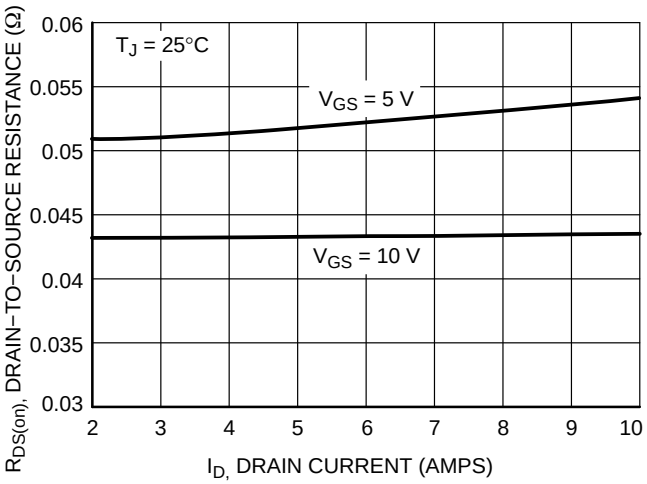


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

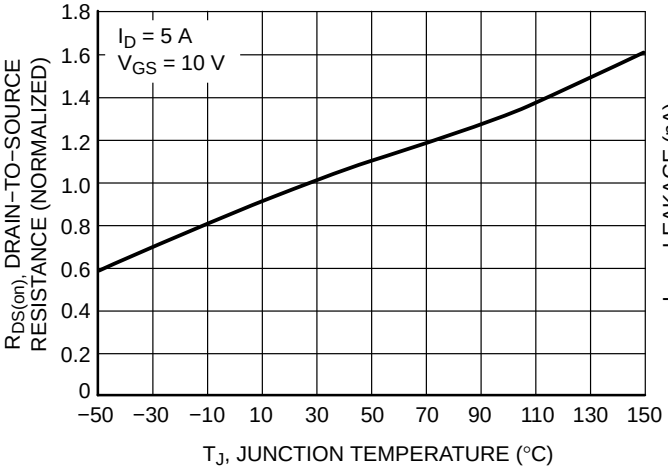


Figure 5. On−Resistance Variation with Temperature

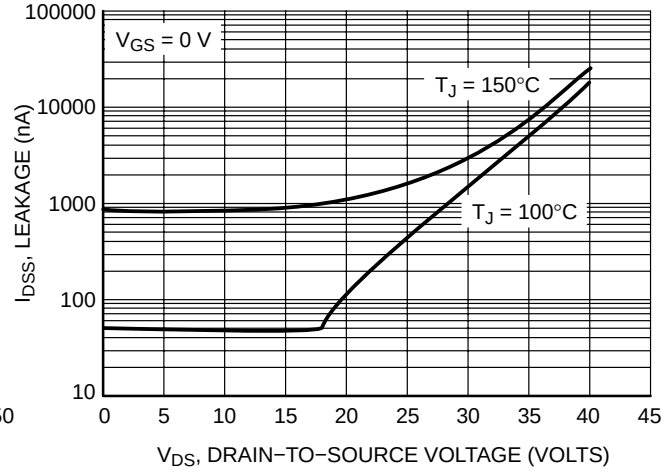


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES

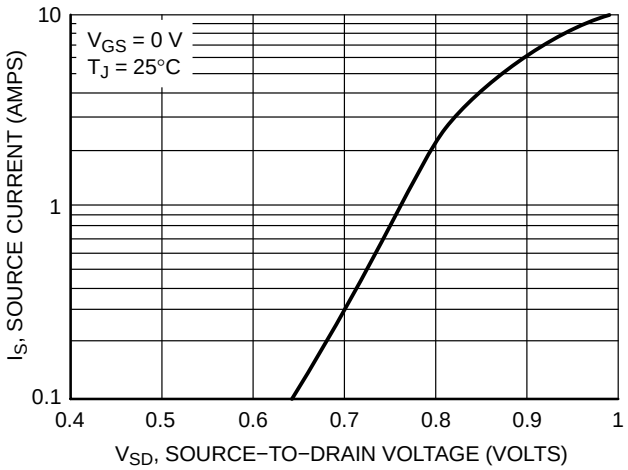
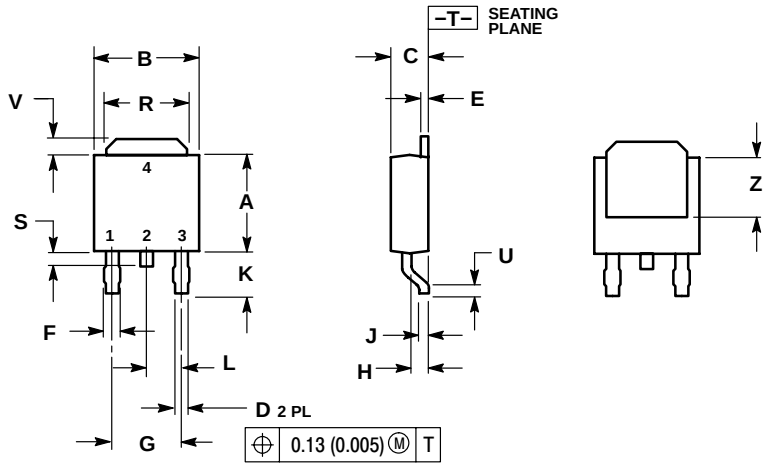


Figure 7. Diode Forward Voltage vs. Current

PACKAGE DIMENSIONS

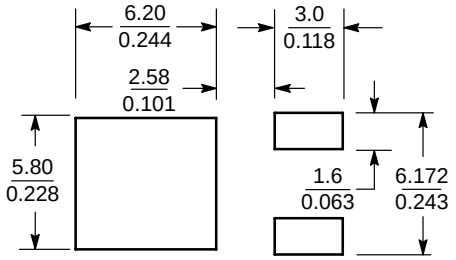
DPAK
CASE 369C−01
ISSUE O



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.180	0.215	4.57	5.45
S	0.025	0.040	0.63	1.01
U	0.020	−−−	0.51	−−−
V	0.035	0.050	0.89	1.27
Z	0.155	−−−	3.93	−−−

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

SOLDERING FOOTPRINT



SCALE 3:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

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