

## Features

- Resolution: 12-Bit  $\pm 0.5$  LSB(DNL)
- Maximum Conversion Rate: 6 MSPS
- Built-in Sample and Hold Function
- Built-in Reference Voltage
- Single +5.0 V Power Supply
- Three-State TTL Compatible Output
- No Missing Code

## Applications

- Video Digitizing
- Personal Computer Video
- Multimedia
- Digital Television

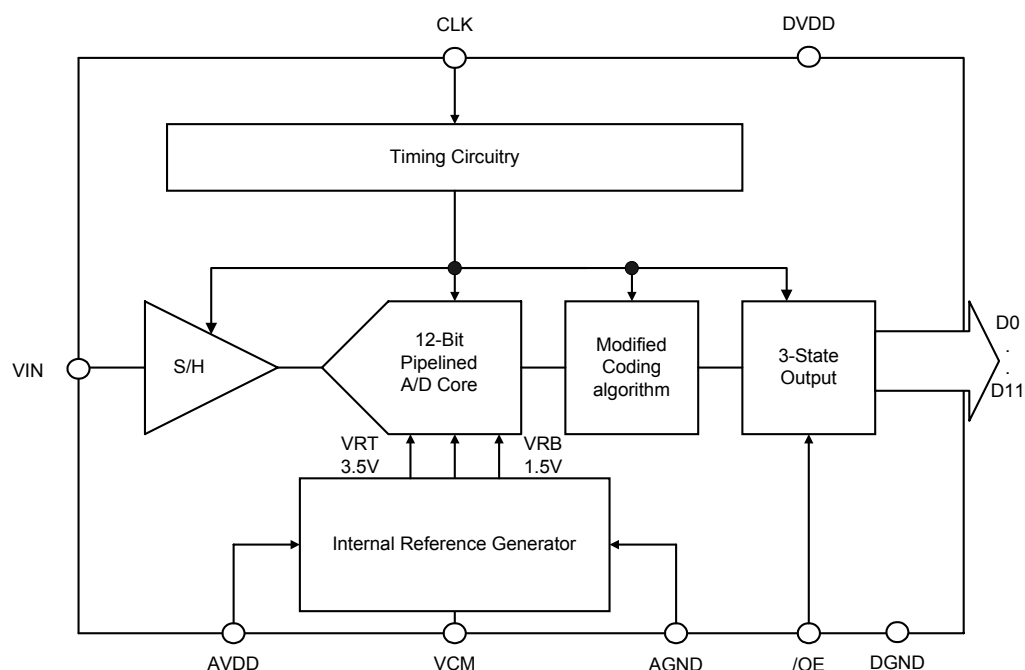
## General Description

The AT2101 is a pipeline CMOS analog-to-digital converter with modified coding algorithm and capable of digitizing full-scale analog input signals into 12-bit digital words at sample rate of 6 MSPS.

This high performance converter includes a 12-bit quantizer, high bandwidth sample/hold, and an internal reference, which eliminates the need for external reference circuitry. The AT2101 employs digital error correction techniques to provide excellent differential linearity for imaging applications.

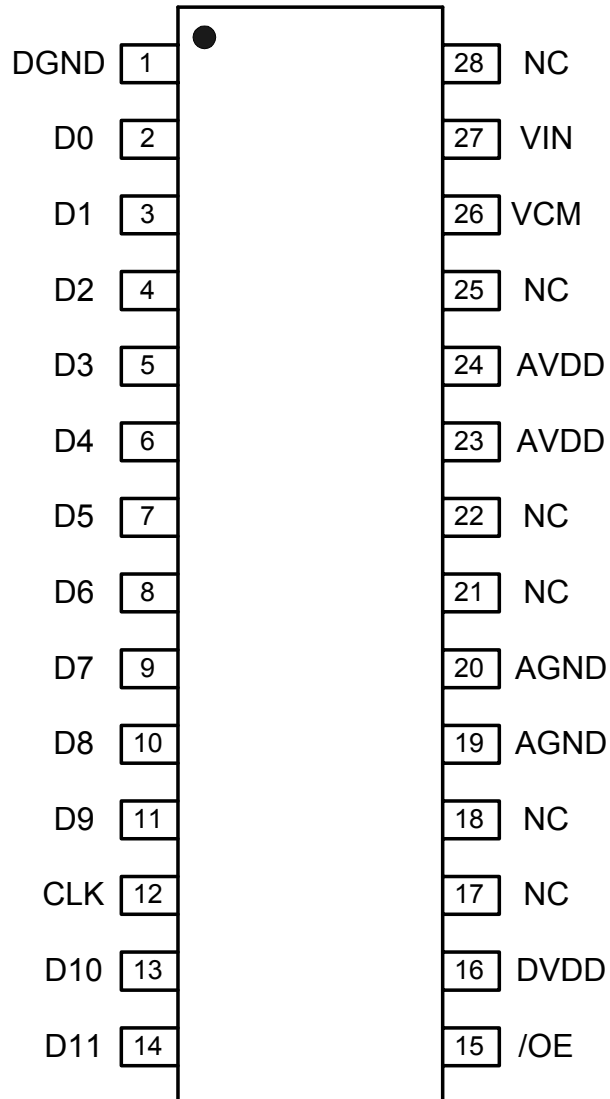
The AT2101 operates from a single +5.0V power supply. All digital inputs are CMOS compatible and the tri-state outputs are TTL-compatible. The AT2101 is ideal for most video and image processing applications that require low power dissipation and low cost.

## Block Diagram



## Pin Configuration

AT2101 (28-Pin 300 mil SOP)



**Pin Description**

| PIN                     | NAME            | FUNCTION                                                                                                                                | PIN      | NAME       | FUNCTION                              |
|-------------------------|-----------------|-----------------------------------------------------------------------------------------------------------------------------------------|----------|------------|---------------------------------------|
| 16                      | DVDD            | Digital +5V Supply                                                                                                                      | 23<br>24 | AVDD       | Analog +5V Supply                     |
| 1                       | DGND            | Digital GND                                                                                                                             | 19<br>20 | AGND       | Analog GND                            |
| 2~11                    | D0~D9           | Digital Output Data<br>D0 (LSB) ~D9                                                                                                     | 13<br>14 | D10<br>D11 | Digital Output Data<br>D10 (MSB) ~D11 |
| 15                      | $\overline{OE}$ | Output Enable Control<br>D0~D11 Output Enabled<br>When $\overline{OE}$ = Low<br>D0~D11 at High Impedance<br>When $\overline{OE}$ = High | 26       | VCM        | Common-Mode Voltage<br>Output         |
| 12                      | CLK             | Clock Input                                                                                                                             | 27       | VIN        | Analog Input                          |
| 17,18<br>21,22<br>25,28 | NC              |                                                                                                                                         |          |            |                                       |

**Absolute Maximum Ratings (Beyond which damage may occur) 25°C**
**Supply Voltages**

V<sub>DD</sub> .....-0.5 to +7.0 V

**Input Voltages**

Analog Input .....AGND to V<sub>DD</sub>

Reference Input Voltage .....AGND to V<sub>DD</sub>

ESD Susceptibility .....± 1,500V

**Temperature**

Operating Temperature .....-20 to +70°C

Junction Temperature .....175°C

Lead Temperature, (Soldering 10 seconds) .....300°C

Storage Temperature .....-55 to +125°C

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### Electrical Specifications

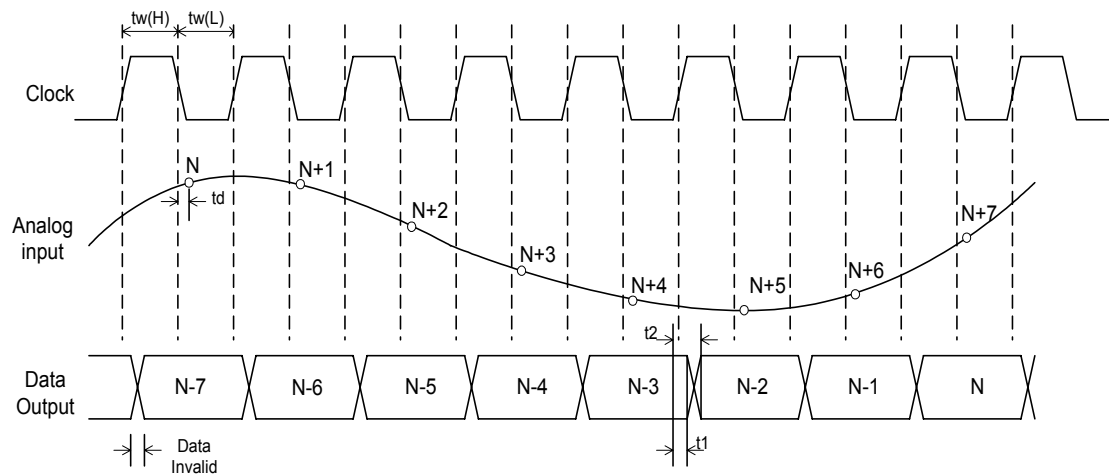
$T_a = +25^{\circ}\text{C}$ ,  $AV_{DD} = DV_{DD} = +5.0\text{V}$ ,  $AGND = DGND = 0.0\text{V}$ ,  $V_{RB} = 1\text{V}$  and  $V_{RT} = 3\text{V}$ , unless otherwise specified.

| PARAMETERS                         | TEST CONDICTION                           | MIN   | TYP        | MAX        | UNITS         |
|------------------------------------|-------------------------------------------|-------|------------|------------|---------------|
| <b>Resolution</b>                  |                                           | 12    |            |            | Bits          |
| <b>DC Accuracy (+25°C)</b>         |                                           |       |            |            |               |
| Integral Nonlinearity              |                                           |       | $\pm 1.5$  |            | LSB           |
| Differential Nonlinearity          |                                           |       | $\pm 0.5$  |            | LSB           |
| No Missing Codes                   |                                           |       | Guaranteed |            |               |
| Zero Error(+25°C)                  |                                           |       |            | $\pm 7.5$  | %FSR          |
| Gain Error(+25°C)                  |                                           |       |            | $\pm 1.25$ | %FSR          |
| <b>Analog Input</b>                |                                           |       |            |            |               |
| Input Voltage Range                |                                           | 1.5   |            | 3.5        | V             |
| Common-Mode Voltage                |                                           |       | 2.5        |            | V             |
| Input Bias Current                 |                                           |       | 5          |            | $\mu\text{A}$ |
| Sample-Hold Input Bandwidth        | -3dBFS                                    |       | 100        |            | MHz           |
| Input Resistance                   |                                           |       | 50         |            | K $\Omega$    |
| Input Capacitance                  |                                           |       | 10         |            | pF            |
| <b>Dynamic Performance</b>         |                                           |       |            |            |               |
| Signal-to-Noise Ratio              | Referred to Full Scale                    |       | 59         |            | dB            |
| $f_{in}=500\text{KHz}$             |                                           | 54    |            |            | dB            |
| $f_{in}=1\text{MHz}$               |                                           |       |            |            |               |
| Spurious Free Dynamic Range        | Referred to Full Scale                    |       | 68         |            | dB            |
| $f_{in}=500\text{KHz}$             |                                           | 58    |            |            | dB            |
| $f_{in}=1\text{MHz}$               |                                           |       | 66         |            |               |
| <b>Timing Characteristics</b>      |                                           |       |            |            |               |
| Output Data Delay (td)             |                                           |       | 18         | 30         | ns            |
| Output Data Delay (tdsl)           | (High 'Z')                                |       |            | 100        | ns            |
| Data Valid Time                    | Tri-state circuit                         |       |            | 100        | ns            |
| Sampling Time Offset               |                                           |       | 5          | 10         | ns            |
| <b>Digital Inputs</b>              |                                           |       |            |            |               |
| Input Current, Logic High          | $V_{DD}=5.25\text{V}$ , $V_{IH}=V_{DD}$   |       |            | 100        | $\mu\text{A}$ |
| Input Current, Logic Low           | $V_{DD}=5.25\text{V}$ , $V_{IL}=DGND$     |       |            | 10         | $\mu\text{A}$ |
| Pulse Width High (CLK)             |                                           | 83    |            |            | ns            |
| Pulse Width Low (CLK)              |                                           | 83    |            |            | ns            |
| Voltage, Logic High                |                                           | 4.0   |            |            | V             |
| Voltage, Logic Low                 |                                           |       |            | 1.0        | V             |
| <b>Digital Outputs</b>             |                                           |       |            |            |               |
| Output Current, Logic High         | $V_{DD}=\text{min}$ $V_{OH}=4.25\text{V}$ | -1.1  |            |            | mA            |
| Output Current, Logic Low          | $V_{DD}=\text{min}$ $V_{OL}=0.4\text{V}$  | 3.7   |            |            | mA            |
| Voltage, Logic High                |                                           |       |            | 4.0        | V             |
| Voltage, Logic Low                 |                                           |       |            | 0.4        | V             |
| <b>Power Supply Requirements</b>   |                                           |       |            |            |               |
| $AV_{DD}$ (Analog Supply Voltage)  |                                           | +4.75 | +5.0       | +5.25      | V             |
| $DV_{DD}$ (Digital Supply Voltage) |                                           | +4.75 | +5.0       | +5.25      | V             |
| Supply Voltage Difference          | $(AV_{DD}-DV_{DD})$                       | -0.1  | 0.0        | 0.1        | V             |
| Supply Current                     | $f_s=6\text{MSPS}$                        |       | 65         |            | mA            |
| Power Dissipation                  |                                           |       | 325        |            | mW            |

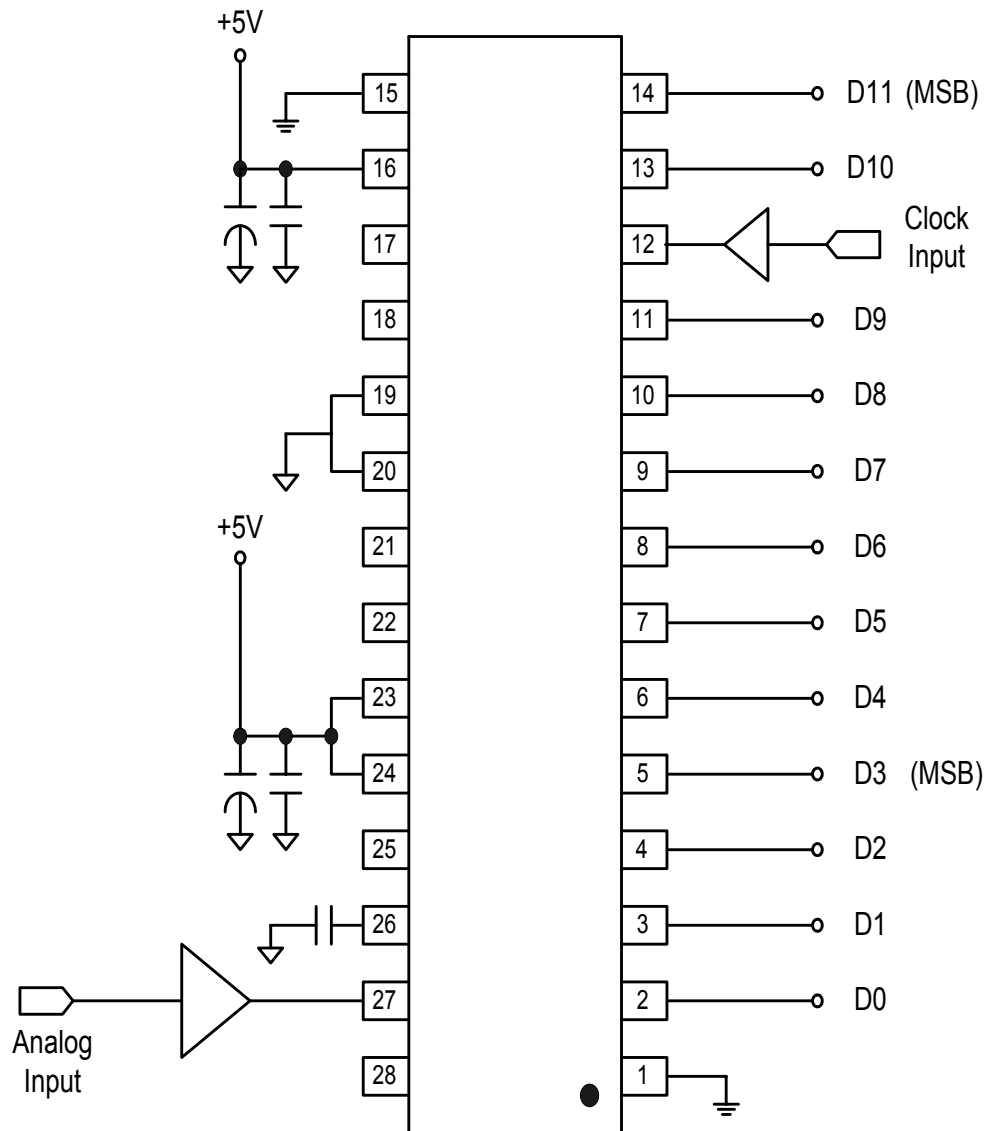
## Timing Specifications

Operating characteristic at  $V_{DD}=5V$ ,  $V_{RT}=3.0V$ ,  $V_{RB}=1.0V$ ,  $f_{(CLK)}=20MHz$ ,  $T_A=25^{\circ}C$  (unless otherwise noted)

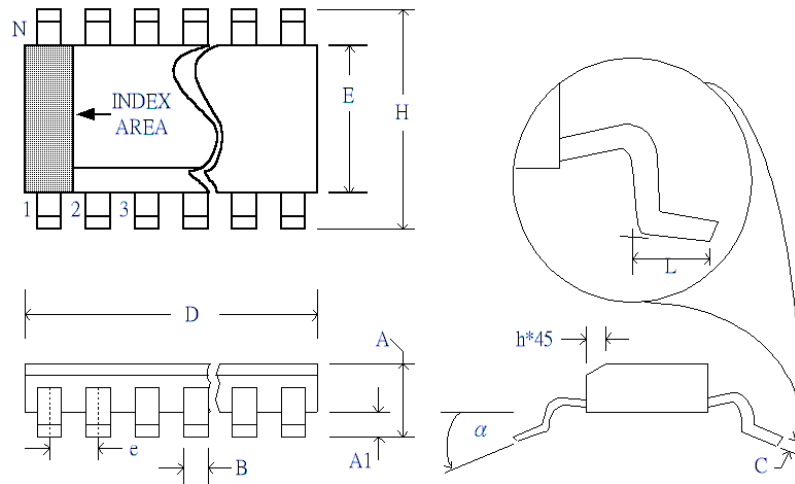
| PARAMETERS                         | TEST CONDICTION | MIN | TYP | MAX | UNITS |
|------------------------------------|-----------------|-----|-----|-----|-------|
| $f_{CONV}$ Maximum conversion rate |                 | 6   |     |     | MSPS  |
| $t_d$ Sampling delay time          |                 |     | 4   |     | ns    |
| $t_{AJ}$ Aperture jitter time      |                 |     | 30  |     | ps    |
| $tw(H)$ Clock pulse High           |                 | 83  |     |     | ns    |
| $tw(L)$ Clock Pulse Low            |                 | 83  |     |     | ns    |
| $t_1$ Data Hold time               | $C_L=10pF$      |     | 15  |     | ns    |
| $t_2$ New Data delay time          | $C_L=10pF$      |     |     | 20  | ns    |



**Typical Application Schematic**



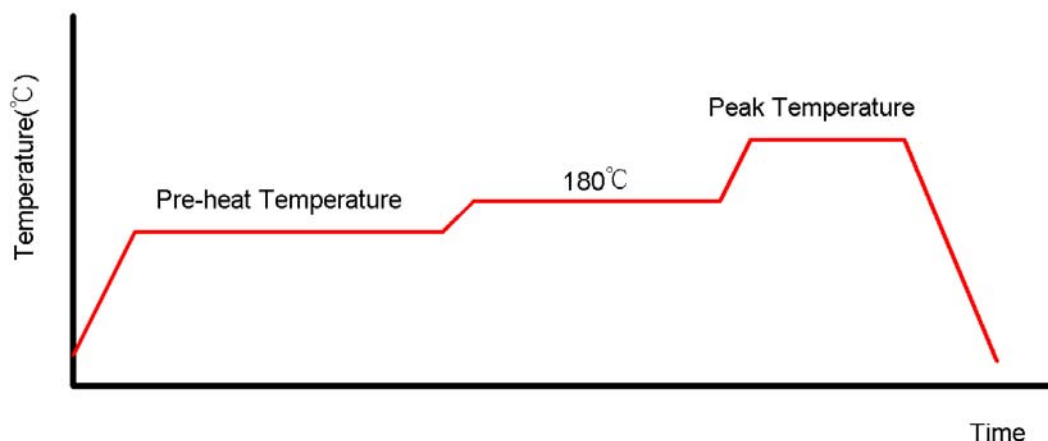
**Package Outline (28-pin 300 mil SSOP)**



| SYMBOLS | DIMENSIONS IN MILLIMETERS |       |       | DIMENSIONS IN INCHES |       |       |
|---------|---------------------------|-------|-------|----------------------|-------|-------|
|         | MIN                       | NOM   | MAX   | MIN                  | NOM   | MAX   |
| A       | 2.36                      | 2.49  | 2.64  | 0.093                | 0.098 | 0.104 |
| A1      | 0.10                      | -     | 0.30  | 0.004                | -     | 0.012 |
| A2      | -                         | 2.34  | -     | -                    | 0.092 | -     |
| B       | 0.33                      | 0.41  | 0.51  | 0.013                | 0.016 | 0.020 |
| C       | 0.23                      | 0.25  | 0.33  | 0.009                | 0.010 | 0.012 |
| D       | 17.70                     | -     | 18.10 | 0.697                | -     | 0.713 |
| E       | 7.39                      | 7.49  | 7.59  | 0.291                | 0.295 | 0.299 |
| e       | -                         | 1.27  | -     | -                    | 0.050 | -     |
| H       | 10.01                     | 10.31 | 10.64 | 0.394                | 0.406 | 0.419 |
| L       | 0.38                      | 0.81  | 1.27  | 0.015                | 0.032 | 0.050 |
| y       | 0                         | -     | 8     | 0                    | -     | 8     |
| h       | 0.25                      | -     | 0.75  | 0.01                 | -     | 0.029 |
|         |                           |       |       |                      |       |       |

## Reflow Condition (IR/Convection or VPR Reflow)

Reference JEDEC Standard J-STD-020A



## Classification Reflow Profiles

|                                            | Convection or IR/Convection | VPR                    |
|--------------------------------------------|-----------------------------|------------------------|
| Average Heating Rate(180°C to peak)        | 5°C/second max.             | 10°C/second max.       |
| Preheat Temperature(125±20°C)              | 120 seconds max.            |                        |
| Temperature maintained above 180°C         | 10~150 seconds              |                        |
| Time within 5°C of actual Peak Temperature | 10~20 seconds               | 60 seconds             |
| Peak Temperature Range(Note 1)             | 219~225°C or 235~240°C      | 219~225°C or 235~240°C |
| Cooling Rate                               | 6°C /second max.            | 10°C/second max.       |
| Time 25°C to Peak Temperature              | 6 minutes max.              |                        |

\*1 The maximum peak temperatures for IR and VP reflow are depending on package dimensions.

## Package Reflow Conditions

| Pkg. Thickness ≥2.5mm and all bags | Pkg. Thickness <2.5mm and Pkg. Volume ≥350 mm <sup>3</sup> | Pkg. Thickness <2.5mm and Pkg. Volume <350 mm <sup>3</sup> |
|------------------------------------|------------------------------------------------------------|------------------------------------------------------------|
| Convection 219~225°C               |                                                            | Convection 235~240°C                                       |
| VPR 219~225°C                      |                                                            | VPR 235~240°C                                              |
| IR/Convection 219~225°C            |                                                            | IR/Convection 235~240°C                                    |