AN2657
Application note

An innovative verilog model for predicting LDMOS DC, small and large signal behavior

Introduction

To reduce the design cycle time and cost for wireless applications it is useful to have models that can help RF Engineers predict and simulate the behavior of RF power transistors. Recently, STMicroelectronics has been strongly focused on developing new models for RF LDMOS power transistors.

The model introduced here is simple in concept, and describes with good approximation DC, small signal S-parameter and large signal behavior, and could be a starting point for designers in developing their new applications. This model has been implemented in Agilent Advanced Design System, in verilog Language, and includes the parasitic elements of the package, as well as a thermal node which takes self heating effects into account.

In this applicatio note we will briefly describe how to extract the model parameters for the PD54003L-E device, which is a 3 W - 7.2 V - 500 MHz LDMOS housed in a PowerFLAT plastic package (5 x 5 mm). As an internally unmatched device, the PD54003L-E can be used in various portable applications over HF, VHF and UHF frequency bands. At the end of this note we will validate this new model using ST's DB-54003L-175 demoboard, especially designed for 2-way portable radio applications using PD54003L-E over the 135-175 MHz frequency band.

Thanks to their cost effectiveness and high performance, LDMOS devices are widely used in radio frequency applications, ranging from digital communication infrastructures (cellular base stations) to low cost portable radios (private mobile radios) commonly known as walkie-talkies.

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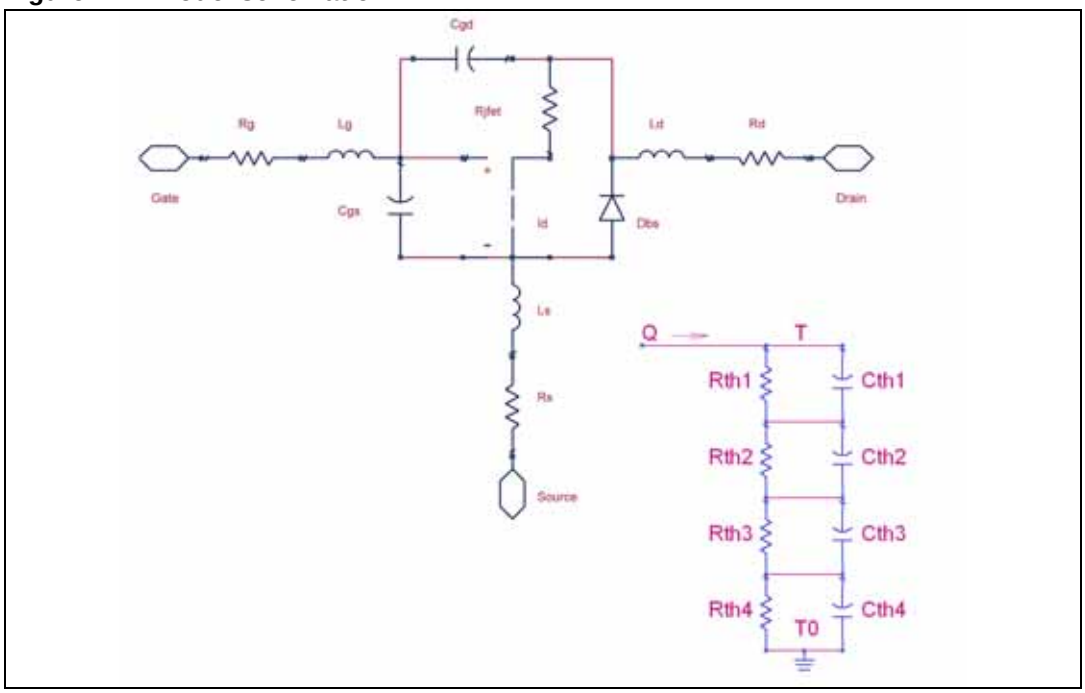
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1 Model description and parameter extraction

The model introduced in this application note is a behavioral model with the equations written in verilog language [1] [2].

Figure 1. Model schematic



By observing the equivalent model schematic of *Figure 1*, the following elements can be noted:

- Parasitic elements associated with the device
- Nonlinear current generator
- JFET resistance
- Substrate-body diode

Parasitic elements

To model the parasitic elements of the device, a resistor and an inductor are placed in series at each terminal. The model can change the resistance and inductance values according to the simulation temperature.

Parameter P in *Equation 1* is the temperature dependence, where T_c is its temperature coefficient, T is the temperature used in the simulation and Tnom is the temperature used to measure the parameter value.

Equation 1

$$P(T) = P(T_{NOM}) \cdot (1 + T_C \cdot (T - T_{NOM}))$$

Nonlinear current generator

The nonlinear current generator controlled by V_{gs} and Vds is the most important factor used to calculate the static and dynamic current of the device. Moreover, the static current is required to define the working region of the MOS.

Table 1. Parameters required for the extraction of the current generator equations

Name	Description
VT0	Threshold voltage [V]
ETA	Drain induce barrier lowering (DIBL) [V^{-1}]
KP0	Transconduttance [$A*V^{-2}$]
THETA	Mobility degradation [$V^{-VGTHETA}$]
VGTHETA	Mobility degradation exponent [-]
THETA2..9	From 2nd to 9th degradation polynomial factor [V^{-2}]
XN	Slope subthreshold current [V^{-1}]
DEL	Body effect linearization coefficient [-]
DELVG	Body effect linearization coefficient independent of Vgs [V^{-1}]
L0	Critical length [m]
L	Channel length [m]
EPS	Output conductance factor if L0>L [m]
KE	Output conductance factor if L0<L [Vm]
DT_KP	Mobility thermal coefficient [-]
DT_VT	Thermal coefficient of threshold voltage [$°C^{-1}$]

Table 1 reports all the parameters required to extract the equations of the current generator. To get the generator current equation, a set of equations must be defined. An important parameter to consider is the threshold voltage of the device shown in *Equation 2*.

Equation 2

$$V_{TH} = V_{T0} - \eta \cdot V_{DS} + DV_VT \cdot (T - T_{NOM})$$

Moreover, a new threshold voltage formula is necessary to describe the weak and strong inversion region in a single equation (*Equation 3*).

Equation 3

$$VR = V_{TH} - 2 \cdot XN \cdot U_{TH}$$

$$U_{TH} = \frac{K \cdot T}{q}$$

To describe both regions, a new gate voltage can be defined as in *Equation 4*.

Equation 4

$$V_{gg} = \begin{cases} V_{TH} + 2 \cdot XN \cdot U_{TH} \cdot e^{\frac{V_{gs} - VR}{2 \cdot XN \cdot U_{TH}}} \\ V_{gs} \end{cases}$$

Equation 5

$$KP = KP0 \cdot \left(\frac{T(°K)}{T_{NOM}(°K)}\right)^{DT_KP}$$

Another important parameter to define is the gain factor with zero bias. Referring to *Equation 5*, *6* and *7*, the gain factor degrades according to the V_{gs} voltage (mobility degradation). *Equation 8* and *9*, which define the drain saturation voltage, complete the set of equations needed to define the generator current (*Equation 10* and *11*).

Equation 6

$$F(V_{gst}) = \begin{cases} 1 & V_{gst} \le 0 \\ 1 + T \cdot V^{vgT}_{gst} + \sum_{I=2}^{9} T_I \cdot V^{I}_{gst} & V_{gst} > 0 \end{cases}$$

Equation 7

$$KP_{EFF} = \frac{KP}{F(V_{gst})}$$

Equation 8

$$A = L0^2 - L^2$$

$$B = \frac{L}{\delta} \cdot L0^2$$

$$C = KE \cdot L^3$$

$$\delta = \Delta + \Delta VG \cdot Vgg \qquad \delta = \Delta + \Delta VG \cdot Vgg$$

$$D_1 = (B - A) \cdot (Vgg - V_{TH}) - C \cdot (1 - \delta)$$

$$D_2 = D^2_1 - 4 \cdot C \cdot (Vgg - V_{TH}) \cdot (1 + \delta) \cdot (0.5 \cdot A - B)$$

Equation 9

$$VDSAT = \frac{\sqrt{D_2} + D_1}{(1 + \delta) \cdot (2 \cdot B - A)}$$

Equation 10

$$I_{DS} = \begin{cases} KP_{EFF} \cdot Vds \cdot (Vgg - V_{TH} - 0.05 \cdot Vds \cdot (1 + \Delta)) & V_{DS} < VDSAT \\ IDSS \cdot \left(1 + A \cdot \frac{Vds - VDSAT}{B \cdot VDSAT + C}\right) & V_{DS} \ge VDSAT \end{cases}$$

Equation 11

$$IDSS = KP_{EFF} \cdot VDSAT \cdot (Vgg - V_{TH} - 0.5 \cdot VDSAT \cdot (1 + \Delta))$$

The automatic ADS optimizer was used to extract the parameters for the current generator. The threshold voltage and the gain factor have been extracted from the input characteristics with Vds at a low voltage level. Concerning mobility degradation, the transconductance parameter was used varying Vds and with Vgs at a high voltage level. The sub-threshold voltage was extracted from the input characteristics with a gate voltage level below the threshold voltage level.

L is the physical channel length of the MOS, while L0 influences the output conductance which depends on KE and EPS. DEL and DELVG affect the VDSAT and are extracted from the output characteristics in the saturation region. As mentioned previously, all the equations have been implemented in verilog language.

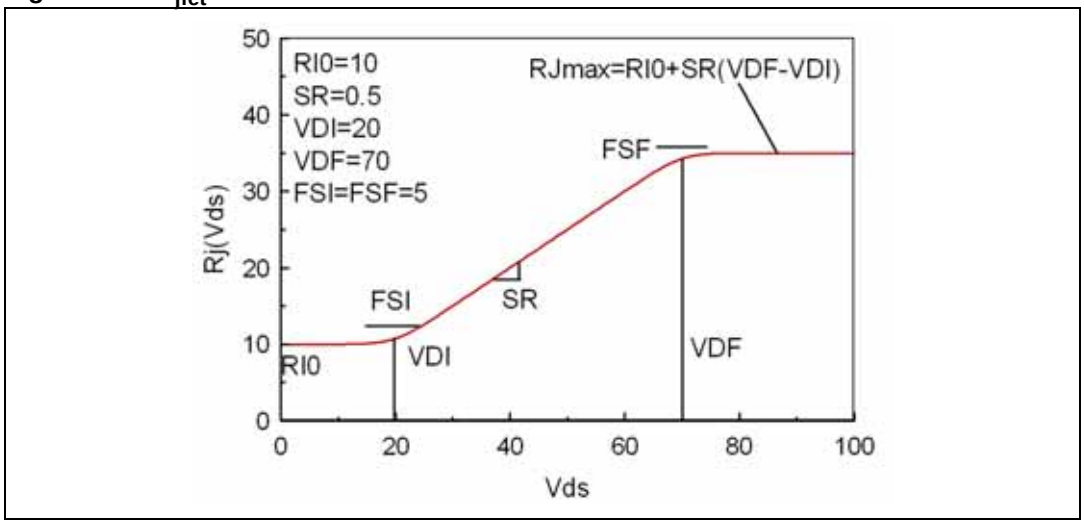
JFET resistance

The quasi-saturation region is modeled by a nonlinear JFET resistor. The mathematical empirical equation is defined in *Equation 12*, where pres depends on the current and on the drop voltage across R_j.

Equation 12

$$R_j = f(Vds, Vgs) \cdot g(pres) \cdot h(T)$$

Figure 2. R_{ifet} vs. Vds



Useful to delete any convergence problem, *Figure 2* shows the resistor law for the variation of Vds (using the right hand function approach) (*Equation 13*). A similar graph and function can be obtained by varying Vgs [*3*].

Equation 13

$$R_j(Vds) = RI0 + SR \cdot \left[FSI \cdot Log_{10}\left(1 + 10^{\frac{Vds - VDI}{FSI}}\right) - FSF \cdot Log_{10}\left(1 + 10^{\frac{Vds - VDF}{FSF}}\right)\right]$$

The function g(pres) was created to bind the Rj to the current Id. This is accomplished by introducing a new parameter linked to the dissipated power on R_j (*Equation 14*), where pres is linked to the dissipated power on Rj through RPWR.

Equation 14

$$g(pres) = 1 + (PCR1 + PCR2 \cdot pres) \cdot pres$$

h(T) (*Equation 15*), introduces the temperature dependence of R_j, where TCR1 and TCR2 are temperature coefficients in the linear region.

R_j is extracted from the DC output characteristics in the linear region with high bias current.

Equation 15

$$h(T) = 1 + (T - T_{NOM}) \cdot (TCR1 + (T - T_{NOM}) \cdot TCR2)$$

Substrate-body diode

The body-substrate diode is employed to describe the breakdown, the drain current leakage and the capacitance between the drain and source.

The thermal variations are shown by *Equation 16*.

Equation 16

$$\begin{aligned} CjT &= CJ \cdot (1 + TC_CJ \cdot (T - T_{NOM})) \\ VjT &= VJ \cdot (1 + TC_VJ \cdot (T - T_{NOM})) \\ Cj_parT &= CJPAR \cdot (1 + TC_CJPAT \cdot (T - T_{NOM})) \\ BVT &= BV \cdot (1 + TC_BV \cdot (T - T_{NOM})) \\ BVVGT &= BVVG \cdot (1 + TC_BVVG \cdot (T - T_{NOM})) \\ R_{LEAKT} &= R_{LEAK} \cdot (1 + TC_R_{LEAK} \cdot (T - T_{NOM})) \end{aligned}$$

To include the temperature in the saturation current refer to *Equation 17*.

Equation 17

$$IsT = + \begin{cases} IS \cdot \left(\frac{T}{T_{NOM}}\right)^{\frac{XTI}{N}} \cdot \exp\left(\frac{q \cdot EG}{K} \cdot \left(\frac{1}{T_{NOM}} - \frac{1}{T}\right)\right) & T \le 200\,°C \\ Is200 + \left(\frac{dIs}{dT}\right)_{T200} \cdot (T(°K) - T200) & T > 200\,°C \end{cases}$$

The diode current is implemented in *Equation 18*, *19*, *20*, *21* and *22*. The charge equation is given by *Equation 23*.

Equation 18

$$Id = \begin{cases} IsT \cdot \left(\exp\left(\frac{Vd}{N \cdot Vt}\right) - 1\right) \\ Ir1 + Ir2 + Ir3 \end{cases}$$

Equation 19

$$Ir1 = IsT \cdot \left[\exp\left(\frac{Vd}{N \cdot Vt}\right) - 1\right]$$

Equation 20

$$Ir2 = \frac{Vd}{R_{LEAKT}}$$

Equation 21

$$Ir3 = sgn(Vd) \cdot Ibv \cdot \exp\left(-\frac{Vd + BVT + BVVGT \cdot Vgs}{NBV \cdot Vt}\right)$$

Equation 22

$$Ibv = \begin{cases} I_{BV} & I_{BV} > 0\,A \\ I_s \cdot \frac{BV}{V_T} & I_{BV} \le 0\,A \end{cases}$$

Equation 23

$$\begin{cases} f1 = \frac{CjT \cdot VjT}{1 - MJ} & V_D \le FCP \\ Qd = TT \cdot Id + f1 \cdot \left(1 + \left(\frac{1 - Vd}{VjT}\right)^{(1-MJ)}\right) + Cj_parT \cdot Vd & \\ f1 = \frac{CjT}{(1 - FCP)^{(1-MJ)}} & \\ f2 = 1 - FCP \cdot (1 + MJ) & V_D > FCP \\ Qd = TT \cdot Id + f1 \cdot \left(f2 \cdot Vd + 0.5 \cdot \frac{MJ \cdot Vd^2}{VjT}\right) + Cj_parT \cdot Vd & \end{cases}$$

The remaining model parameters are the capacitances Cgs and Cgd of the MOSFET. The gate-source capacitance is modeled with a constant capacitance, because it is related to a highly doped MOSFET (*Equation 24*).

Equation 24

$$Qgs = CgsT \cdot Vgs$$

Moreover, the gate-drain capacitance can be considered as a classic MOSFET model capacitance, where the equations of the charged capacitance (*Equation 25*, *26*, *27*, *28*) can be divided into four regions (*Figure 3*). Even in this case, capacitance variation depends on temperature (*Equation 29*).

Equation 25

$$Cgd = \frac{Cgx0}{\left(1 - \frac{Vgx - VFB}{Vjx}\right)^{Mjx}} + CgdovlT$$

$$Qgd = \frac{Cgx0 \cdot Vjx}{1 - Mjx} \cdot \left(\left(1 + \frac{VFB}{Vjx}\right)^{1-Mjx} - \left(1 + \frac{VFB - Vgx}{Vjx}\right)^{1-Mjx}\right) + CgdovlT \cdot Vgd$$

Equation 26

$$Qgd = Cgx0 \cdot (Vgd - VFB) + \frac{Cgx0 \cdot Vjx}{1 - Mjx} \cdot \left(\left(1 + \frac{VFB}{Vjx}\right)^{1-Mjx} - 1\right) + CgdovlT \cdot Vgd$$

Equation 27

$$Cgd = \frac{Cgx0}{\left(1 - \frac{Vgx - VFB}{Vjx}\right)^{Mjx}} + CgdovlT$$

$$Qgd = Cgx0 \cdot VFB + \frac{Cgx0 \cdot Vjx}{1 - Mjx} \cdot \left(\left(1 + \frac{VFB - Vgx}{Vjx}\right)^{1-Mjx} - 1\right) + CgdovlT \cdot Vgd$$

Equation 28

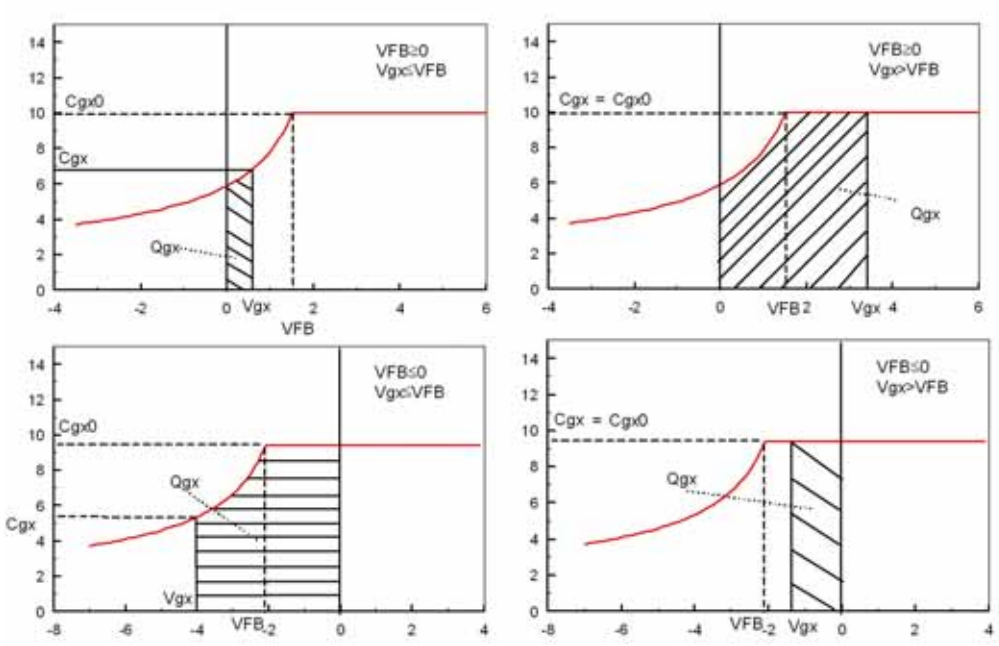
$$Cgd = Cgx0 + CgdovlT$$

$$Qgd = (Cgx0 + CgdovlT) \cdot Vgd$$

Equation 29

$$GgxT = CGX0 \cdot (1 + CGXTC1 \cdot (T - T_{NOM}) + CGXTC2 \cdot (T - T_{NOM})^2)$$
$$VfbT = VFB \cdot (1 + VFBTC1X \cdot (T - T_{NOM}))$$
$$CgdovlT = CGDOVL \cdot (1 + CGDOVLTC \cdot (T - T_{NOM}))$$

Figure 3. Gate-drain charge variation vs. Vds



To extract the capacitance variables, a classic configuration has been used to measure the C_{iss}, C_{oss} and C_{rss}.

Thermal node

A "thermal node" has been introduced to consider the self-heating effect (*Figure 1*).

The voltage between the external thermal circuit port and the source node is related to the junction temperature rise. The current source of the circuit is equal to the dissipated power [*4*] [*5*]. In this first model implementation we have not considered the temperature dependent variables.

Package simulation

To include all the parasitic elements of the package in the model, several electromagnetic simulations were performed [*6*].

Figure 4. Generic internal RF package structure

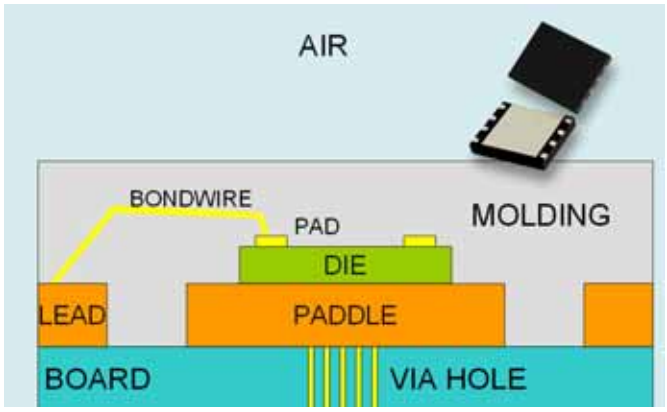
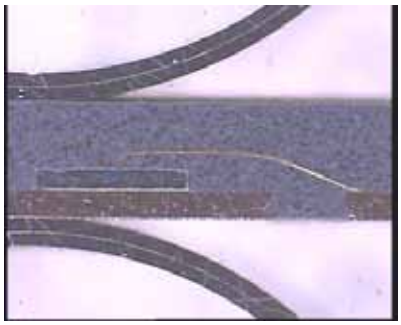


Figure 5. PowerFLAT cross-section



The molding resin has a dielectric constant equal to 4 and a dielectric loss tangent of 0.005. The leads of the package are made of copper, while the bonding wires are made of gold.

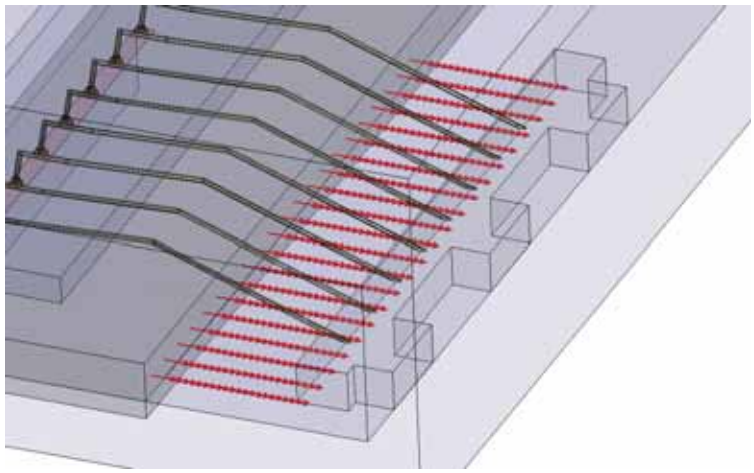
During the simulation, the device contact pads and the paddle are considered as a PEC (perfect electric conductive surface lossless). Instead, along the external sides of the air box containing the package, an electric and magnetic field total wave absorption condition was set to consider the radiation losses (*Equation 30*).

Equation 30

$$(\nabla \times E)_{tan} = j \cdot k_0 - \frac{j}{k_0} \cdot \nabla_{tan} \times (\nabla_{tan} \times E_{tan}) + \frac{j}{k_0} \cdot \nabla_{tan} \times (\nabla_{tan} \cdot E_{tan})$$

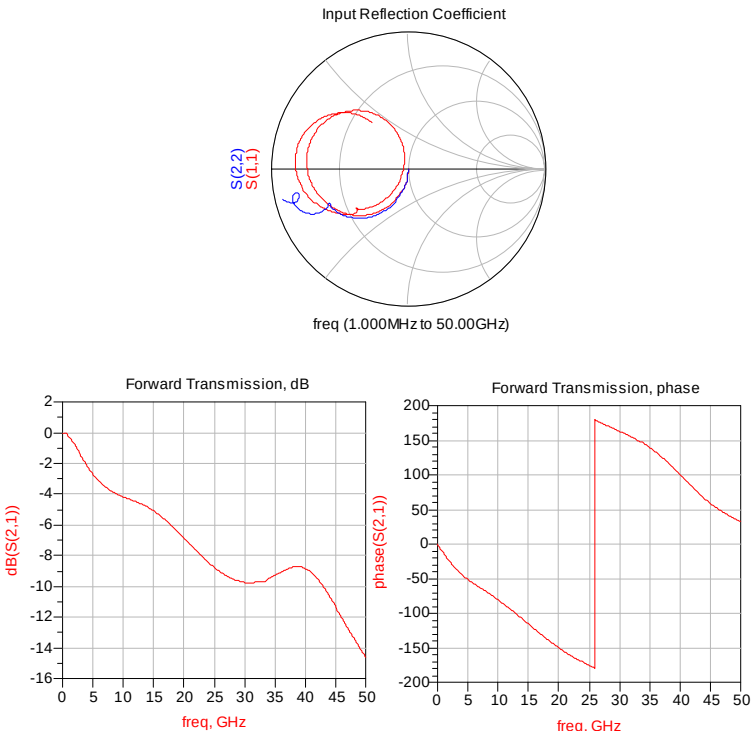
During the simulation lumped ports were used to excite the fields (*Figure 6*) [*7*]. The package simulation performed was in the frequency range from 1 MHz to 50 GHz.

Figure 6. Simulated version of the PowerFLAT



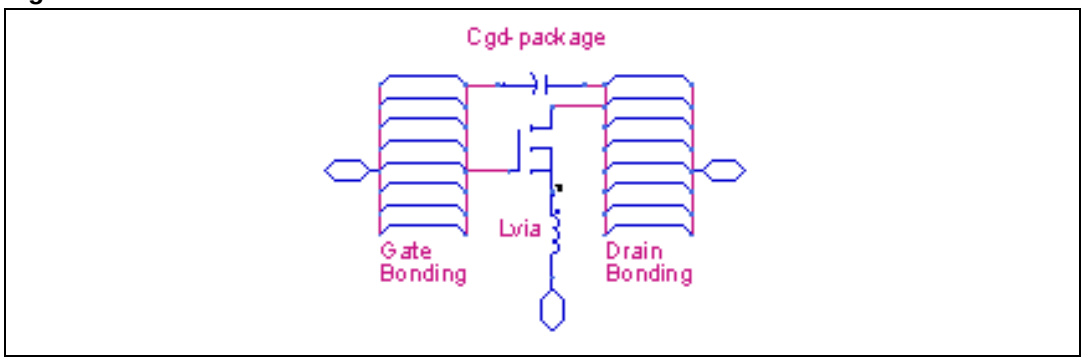
To minimize the simulation time and increase accuracy, the structure was split into two parts (drain and gate). In this way, the reciprocal coupling between the input and output parts are not considered. To take into account such effect, an extra capacitor (Cgd-package) has been used. To complete the package model an extra inductor (Lvia) associated with the source has been added. This inductor represents the effect created by the "via holes"[*8*] [*9*]. The S-parameters concerning the electromagnetic simulation of the gate section of the package are shown in *Figure 7*.

Figure 7. S-parameters of the simulated package



Moreover, using the measured S-parameters of the packaged device, it was possible to extract the Cgd-package and the Lvia. Observing *Figure 8*, it is possible to see the circuit representing the union between the package model and the device model.

Figure 8. Overall model schematic



DC and RF small signal validation

Figure 9, *10*, and *11* compare the measured DC and RF small signal parameters with the simulated parameters (C_{iss}, C_{oss}, C_{rss}, low signal S-parameters, and input and output DC curves). The simulations predict with good approximation the above mentioned parameters, including S21 and S22 which are the most difficult to predict.

Figure 9. Measured C_{iss}, C_{oss}, C_{rss} vs. simulated parameters

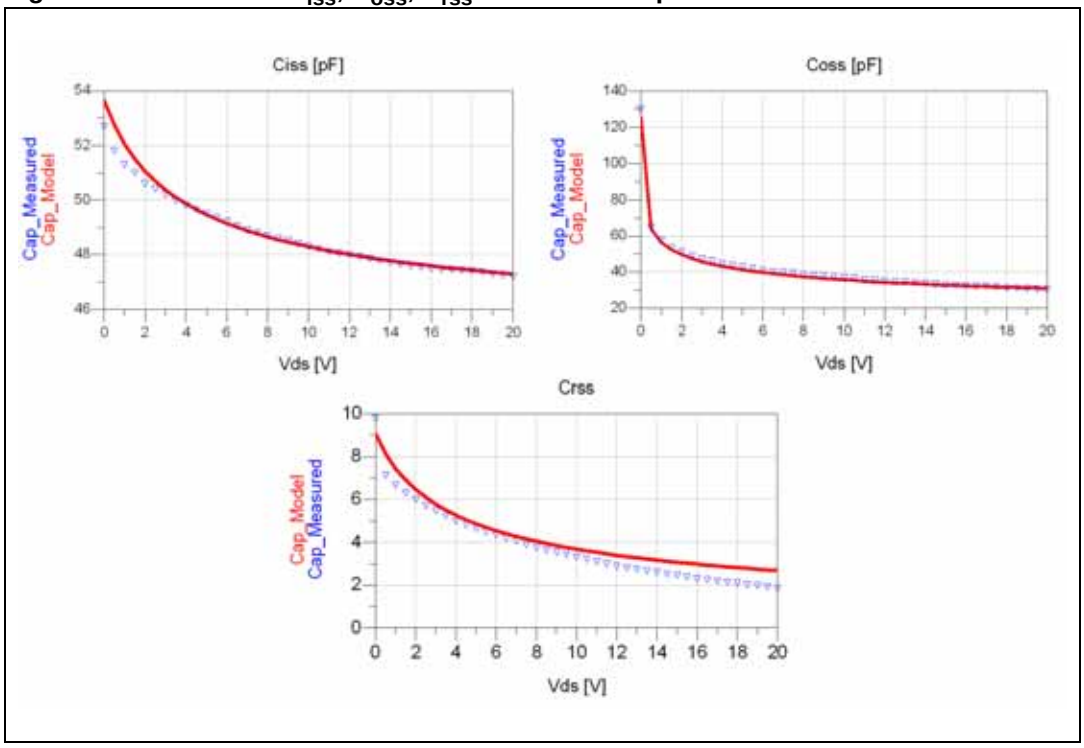


Figure 10. Measured S-parameters vs. simulated parameters (Vds= 7.2 V; Idq= 100 mA)

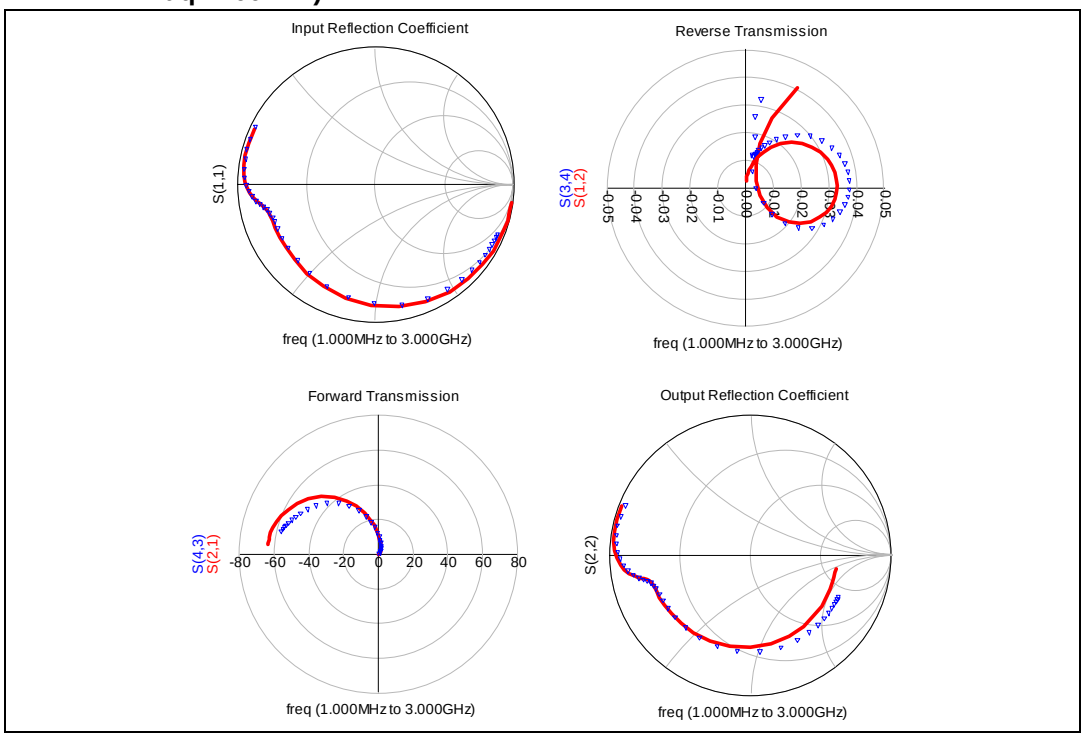
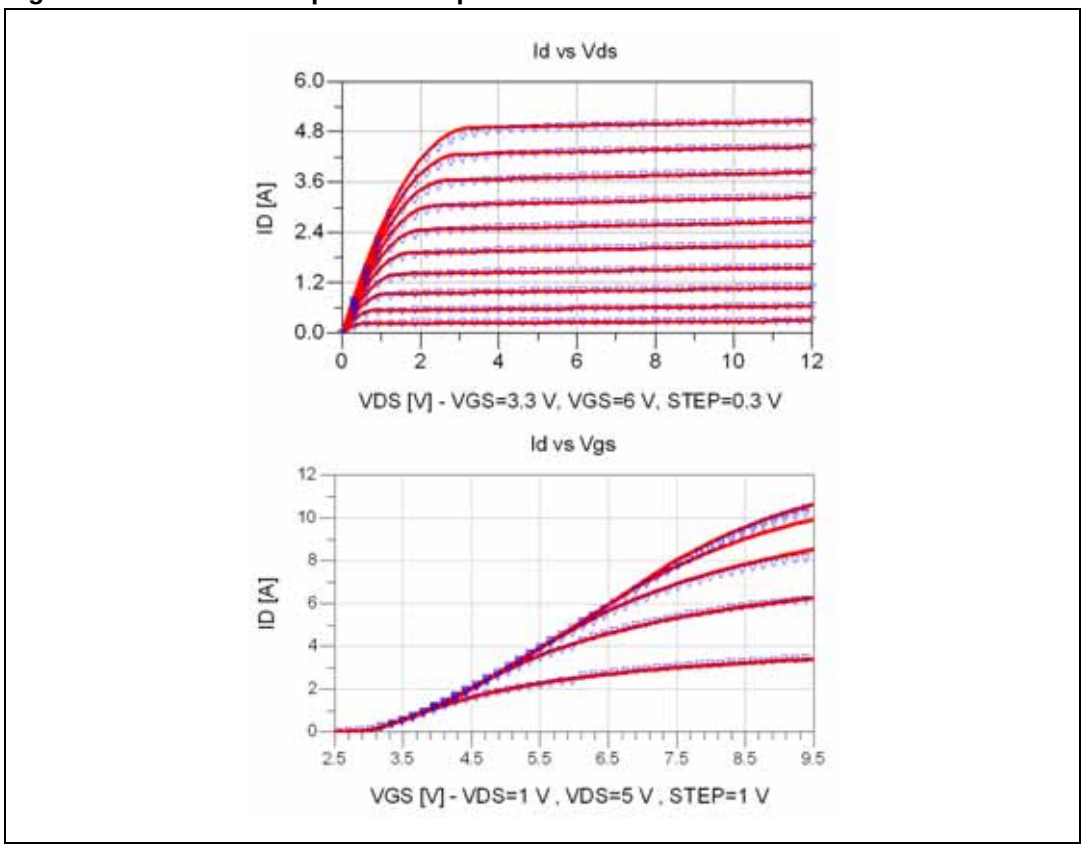


Figure 11. Measured input and output DC curves vs. simulated curves

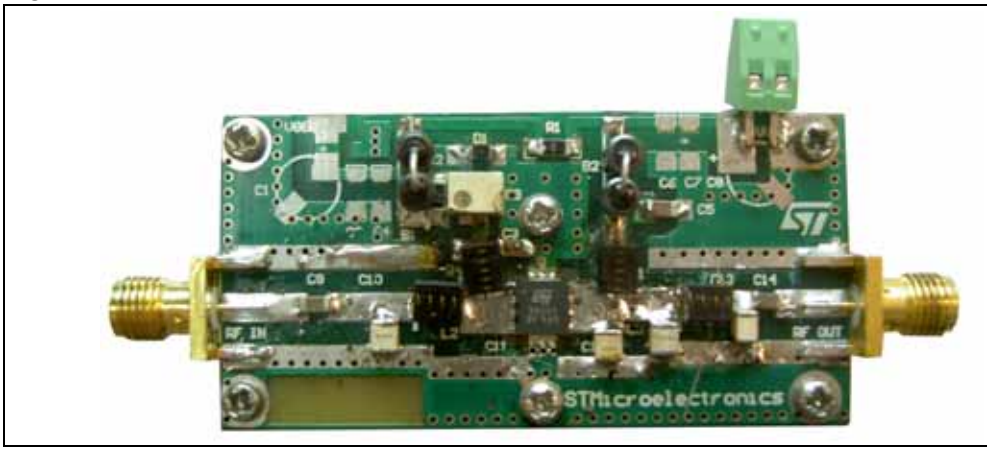


Large signal validation

Using the ADS with harmonic balance engine simulator [*10*], the model has been simulated in conjunction with the DC network and the input and output matching network of ST's demonstration board DB-54003L-175 (*Figure 12*).

The DB-54003L-175 demonstration board was developed to demonstrate the best broadband performance of PD54003L-E.

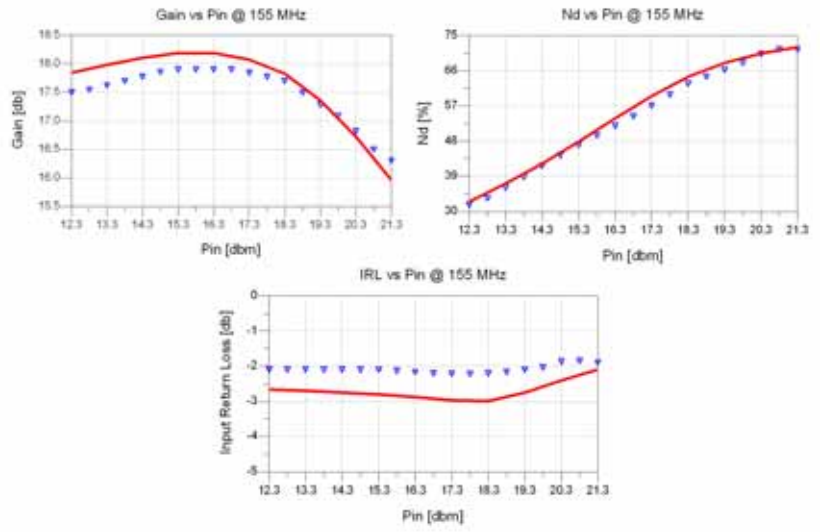
Figure 12. DB-54003L-175 demoboard



In the harmonic balance simulations we used all the information relative to the board and the S-parameters of the lumped capacitors and inductors. *Figure 13* compares the simulations and measurements of the demonstration board at 155 MHz, varying the power delivered by the generator at the input port.

P_{IN} is the power available from the generator, Nd is the drain efficiency, IRL (input return loss) is the ratio between the power reflected from the device and the power available from the generator, and Gain is the ratio between the power dissipated on the load and the power available from the generator.

Figure 13. Measured RF demonstration board performance vs simulated performance



2 Conclusions

Thanks to this new verilog model, customers will now be able to predict and simulate the behavior of STMicroelectronics' RF DMOS and LDMOS products, reducing design cycle time and time-to-market.

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4 Revision history

Table 2. Document revision history

Date	Revision	Changes
27-Nov-2007	1	Initial release

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