SONY

CXA2503AR

Decoder/Driver/Timing Generator for Color LCD Panels

For the availability of this product, please contact the sales office.

Description

The CXA2503AR is an IC designed exclusively to drive color LCD panels LCX005BK/BKB and LCX009AK/AKB.

This IC greatly reduces the number of circuits and parts required to drive LCD panels by incorporating RGB decoder functions for video signals, driver functions, and a timing generator for driving panels onto a single chip.

This chip has a built-in serial interface circuit and electronic attenuators which allow various mode settings and adjustments to be performed through direct control from an external microcomputer, etc.

Features

- Color LCD panels LCX005BK/BKB and LCX009AK/AKB driver
- Supports NTSC and PAL systems
- Supports 16:9 wide display
- Supports composite inputs, Y/C inputs and Y/color difference inputs
- Serial interface circuit
- Electronic attenuators (D/A converter)
- BPF, trap and delay line
- Sharpness function
- 2-point γ correction circuit
- R, G, B signal delay time adjustment circuit
- Polarity inversion circuit (line inverted mode)
- Supports external RGB input
- Supports AC drive for LCD panel during no signal

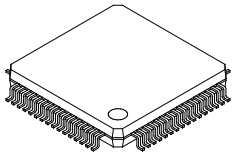
Applications

- LCD viewfinders
- Compact liquid crystal projectors
- Compact LCD monitors

Structure

Bipolar CMOS IC

64 pin LQFP (Plastic)



Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	$V_{CC}1$ – GND1, 3	6	V
	$V_{CC}2$ – GND2	14	V
	$V_{DD}1$ – $V_{SS}1$	4.5	V
	$V_{DD}2$ – $V_{SS}2$	4.5	V
• Analog input pin voltage	VINA	–0.3 to $V_{CC}1$	V
• Digital input pin voltage	VIND	–0.3 to $V_{DD}1$ + 0.3	V
• Operating temperature	Topr	–15 to +75	°C
• Storage temperature	Tstg	–40 to +125	°C

• Allowable power dissipation

P_D (Ta ≤ 75°C) 350mW **Note)**

Operating conditions

Supply voltage	$V_{CC}1$ – GND1, 3	4.25 to 5.25	V
	$V_{CC}2$ – GND2	11.0 to 13.5	V
	$V_{DD}1$ – $V_{SS}1$	2.7 to 3.6	V
	$V_{DD}2$ – $V_{SS}2$	2.7 to 3.6	V

Note) With substrate

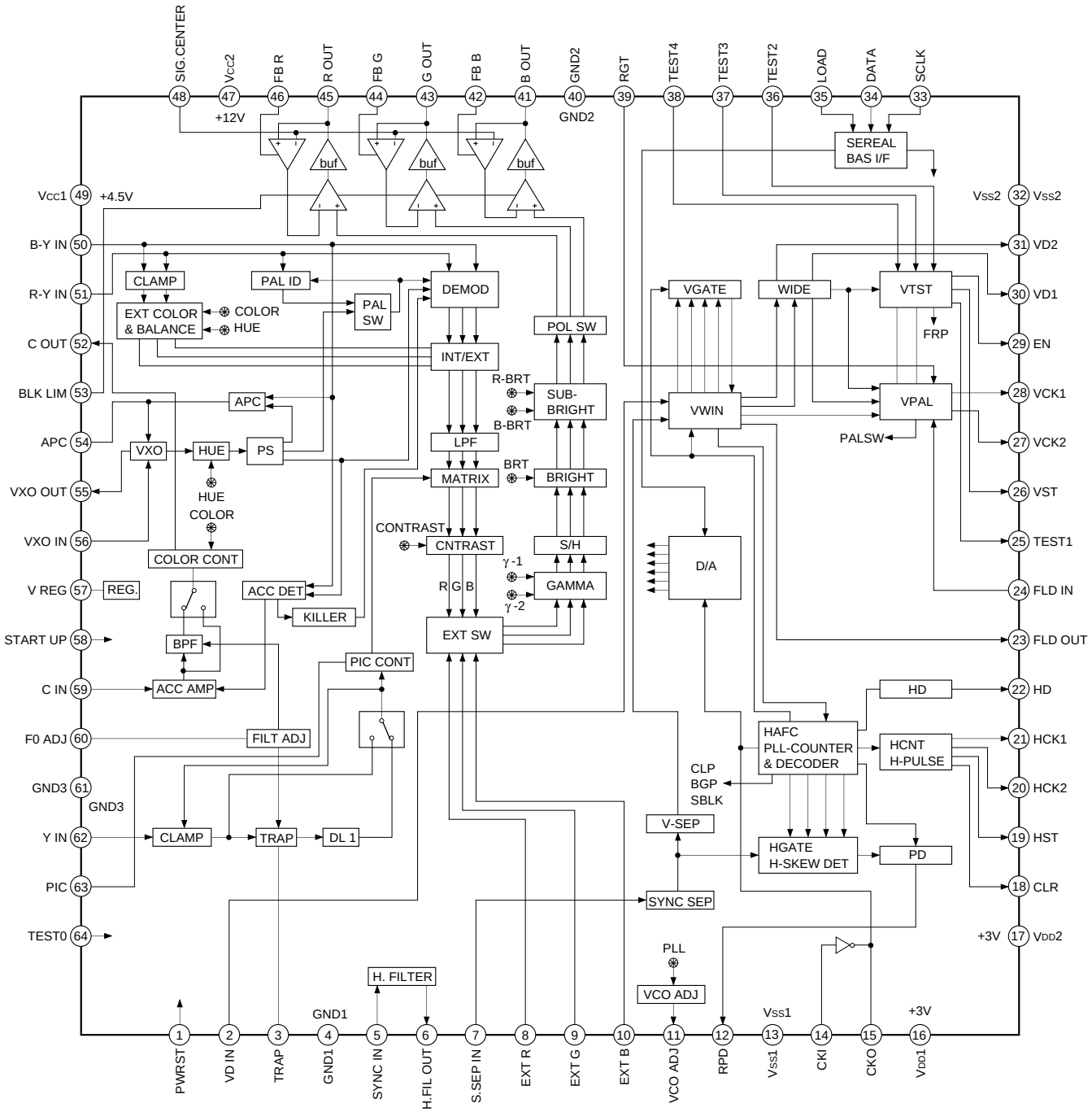
Size: 114.3 × 76.1 × 1.5mm

Material: Glass fabric base epoxy

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E97910-PS

Block Diagram



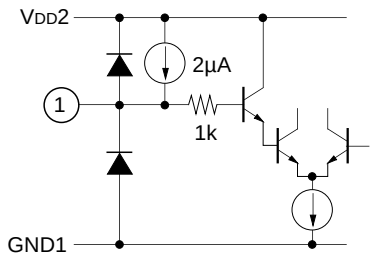
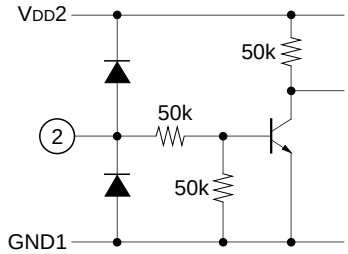
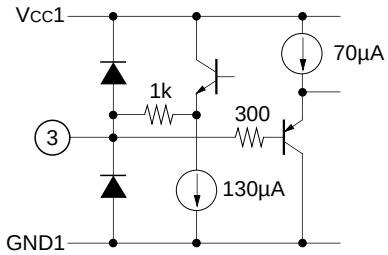
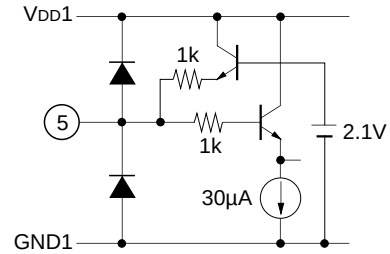
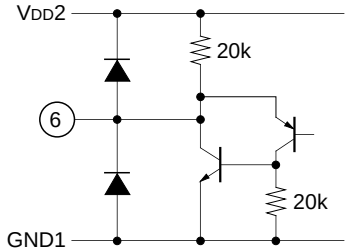
Pin Description

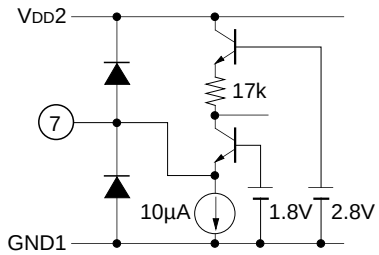
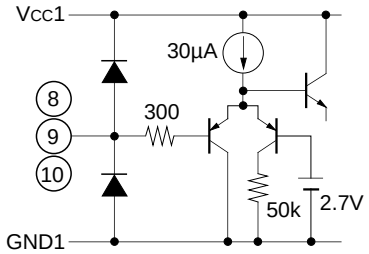
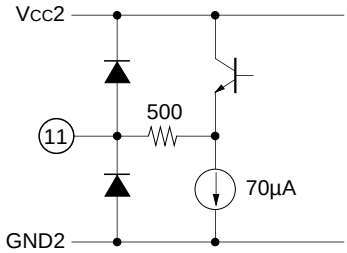
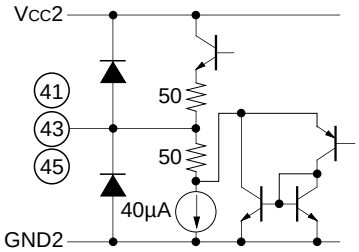
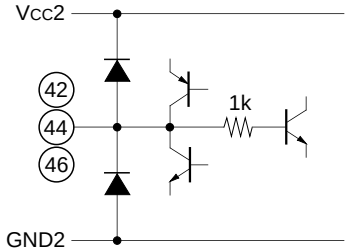
Pin No.	Symbol	I/O	Description	Input pin for open status
1	PWRST	—	System reset	
2	VD IN	I	External vertical sync input	
3	TRAP		External trap connection	
4	GND1		Analog 4.5V GND	
5	SYNC IN	I	Video input for sync separation	
6	H.FIL OUT	O	Video output for sync input	
7	S.SEP IN	I	Sync separation circuit input	
8	EXT R	I	External digital input R	
9	EXT G	I	External digital input G	
10	EXT B	I	External digital input B	
11	VCO ADJ	O	VCO adjustment voltage output	
12	RPD	O	Phase comparator output	
13	$V_{SS}1$		Digital 3V GND for oscillation cell	
14	CKI	I	Oscillation cell input	
15	CKO	O	Oscillation cell output	
16	$V_{DD}1$		Digital 3V power supply for oscillation cell	
17	$V_{DD}2$		Digital 3V power supply	
18	CLR	O	CLR pulse output	
19	HST	O	H start pulse output	
20	HCK2	O	H clock pulse 2 output	
21	HCK1	O	H clock pulse 1 output	
22	HD	O	HD pulse output	
23	FLD OUT	O	Field identification output	
24	FLD IN	I	Field identification input	
25	TEST1		Test (Leave this pin open.)	
26	VST	O	V start pulse output	
27	VCK2	O	V clock pulse 2 output	
28	VCK1	O	V clock pulse 1 output	
29	EN	O	EN pulse output	
30	VD1	O	VD1 pulse output	
31	VD2	O	VD2 pulse output	
32	$V_{SS}2$		Digital 3V GND	

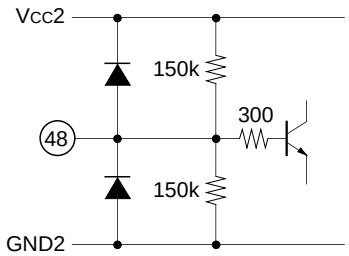
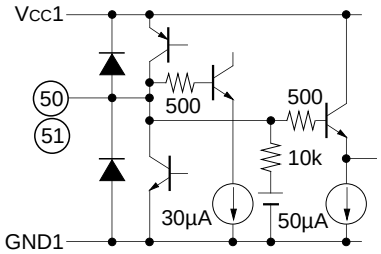
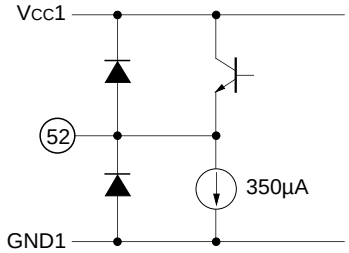
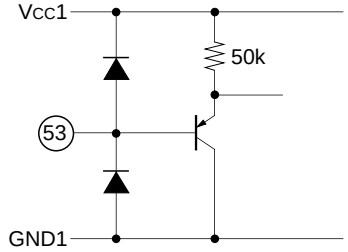
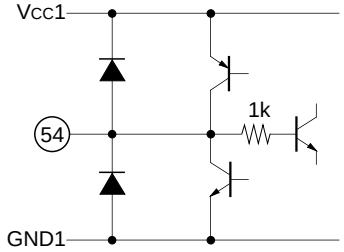
Pin No.	Symbol	I/O	Description	Input pin for open status
33	SCLK	I	Serial interface clock input	H
34	DATA	I	Serial interface data input	H
35	LOAD	I	Serial interface load input	H
36	TEST2		Test (Leave this pin open.)	
37	TEST3		Test (Leave this pin open.)	
38	TEST4		Test (Leave this pin open.)	
39	RGT	I	Switches between Normal scan (H) and Reverse scan (L)	H
40	GND2		Analog 12V GND	
41	B OUT	O	B output	
42	FB B	O	B signal DC voltage feedback circuit capacitor connection	
43	G OUT	O	G output	
44	FB G	O	G signal DC voltage feedback circuit capacitor connection	
45	R OUT	O	R output	
46	FB R	O	R signal DC voltage feedback circuit capacitor connection	
47	$V_{CC}2$		Analog 12V power supply	
48	SIG.CENTER	I	RGB output DC voltage adjustment	
49	$V_{CC}1$		Analog 4.5V power supply	
50	B-Y IN	I	B-Y demodulator input (or B-Y color difference signal input)	
51	R-Y IN	I	R-Y demodulator input (or R-Y color difference signal input)	
52	C OUT	O	Chroma signal output	
53	BLK LIM	I	Black peak limiter level adjustment	
54	APC	O	APC detective filter connection	
55	VXO OUT	O	VXO output	
56	VXO IN	I	VXO input	
57	V REG	O	Constant voltage capacitor connection	
58	START UP	O	Startup time constant connection	
59	C IN	I	Chroma signal input	
60	F0 ADJ	O	Internal filter adjusting resistor connection	
61	GND3		Analog 4.5V GND	
62	Y IN	I	Y signal input	
63	PIC	I	Y signal frequency response adjustment	
64	TEST0	I	Test (Leave this pin open.)	

(H: Pull up)

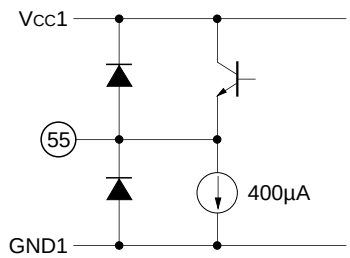
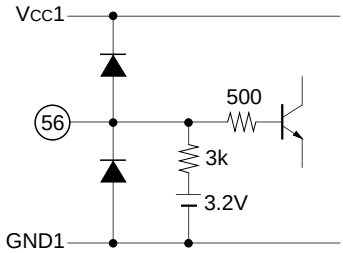
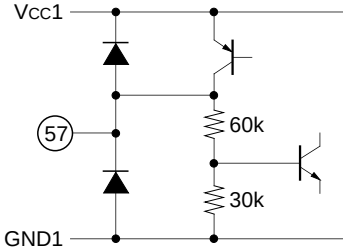
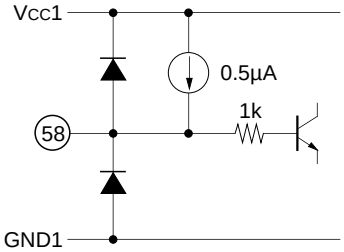
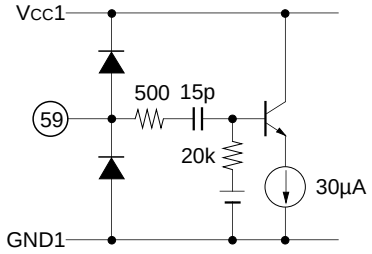
Analog Block Pin Description

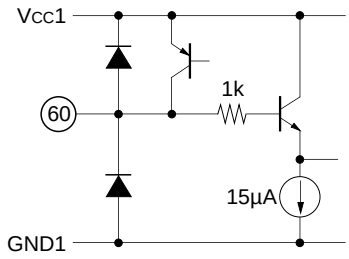
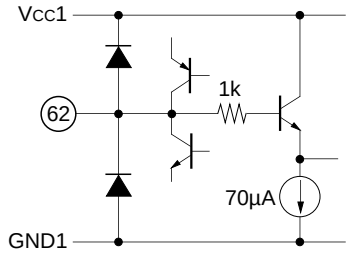
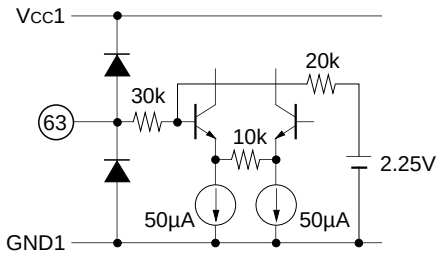
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
1	PWRST	—		TG block system reset pin. The system is reset when this pin is connected to GND. Connect a capacitor between this pin and GND.
2	VDIN	—		External vertical sync signal input.
3	TRAP	2.2V		External trap connection. Connect the trap between this pin and GND to remove the chroma component.
5	SYNC IN	1.5V		Sync input. Normally inputs the Y signal. The standard signal input level is 0.5Vp-p (100% white level from the sync tip).
6	H.FIL OUT	2.5V		Outputs the video signal for input to the sync separation circuit.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
7	S.SEP IN	1.0V		Sync separation circuit input. Input the H FILTER output signal.
8	EXT-R	—		External digital signal inputs. There are two threshold values: Vth1 (= 1.0V) and Vth2 (= 2.0V). When one of the RGB signals exceeds Vth1, all of the RGB outputs go to black level; when an input exceeds Vth2, only the corresponding output goes to white level.
9	EXT-G			
10	EXT-B			
11	VCO ADJ	—		VCO adjustment voltage output.
41	B OUT	$\frac{Vcc2}{2}$		RGB signal outputs.
43	G OUT			
45	R OUT			
42	FB B	2.5V		Smoothing capacitor connection for the feedback circuit of RGB output DC level control. Use a low-leakage capacitor because of high impedance.
44	FB G			
46	FB R			

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
48	SIG. CENTER	6.0V		RGB output DC voltage control. When used with a Vcc2 of 12V or more, apply 6V from an external source.
50	B-Y IN	—		Color difference demodulation circuit inputs. Color difference signal is input when using Y/color difference input. At this time, the clamp level is approximately 2.8V. Pin 52 signal is input in other modes. (except D-PAL*1) At this time, the DC level is approximately 2.0V.
51	R-Y IN			
52	C OUT	1.3V		Color adjusted chroma signal output. The burst level is approximately 140mVp-p (typ.). (420mVp-p during D-PAL.)
53	BLK LIM	—		Sets the RGB output amplitude (black-black) clip level.
54	APC	2.7V		APC detective filter connection.

*1 D-PAL is a demodulation method that uses an external delay line during demodulation; S-PAL is a demodulation method that internally processes chroma demodulation.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
55	VXO OUT	2.9V		VXO output.
56	VXO IN	3.2V		VXO input.
57	V REG	3.6V		Smoothing capacitor connection for the internally generated constant voltage source circuit. Connect a capacitor of 1µF or more.
58	START UP	—		Prevents output of the HST and VST pulses for driving LCD panels for a certain time during power-on. Connect a capacitor between this pin and GND. When not using this pin, connect to Vcc1.
59	C IN	—		Video signal input when using composite signal input. Chroma signal input when using Y/C signal input. Leave this pin open when using Y/color difference input.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
60	F0 ADJ	2.4V		Connect resistance of 82kΩ between this pin and GND1 to adjust the internal filters using the outflow current value.
62	Y IN	3.1V		Y signal input. The standard signal input level is 0.5Vp-p (100% white level from the sync tip). Input at low impedance (75Ω or less).
63	PIC	2.25V		Adjusts frequency response of luminance signal. Increasing the voltage emphasizes contours.

Setting Conditions for Measuring Electrical Characteristics

When measuring the electrical characteristics, the TG (timing generator) block must be initialized by performing Settings 1 and 2 below.

Setting 1. System reset

After turning on the power, set SW1 to ON and start up V1 from GND in order to activate the TG block system reset. (See Fig. 1-1.)

Setting 2. Horizontal AFC adjustment

Input SIG5 (VL = 0mV) to (A) and adjust serial bus register PLL ADJ so that WL and WH of the TP12 output waveform are the same. (See Fig. 1-2.)

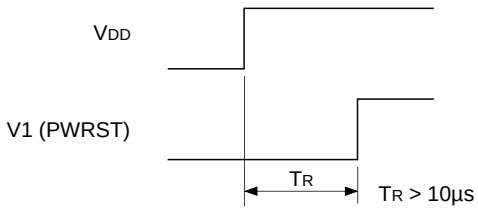


Fig. 1-1. System reset

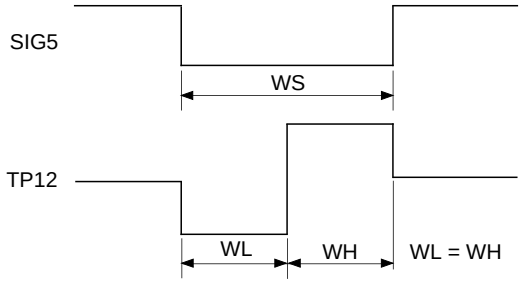


Fig. 1-2. Horizontal AFC adjustment

Electrical Characteristics – DC Characteristics

Unless otherwise specified, Settings 1 and 2 and the following setting conditions are required.

$V_{CC}1$ = 4.5V, $V_{CC}2$ = 12.0V, GND1 = GND2 = GND3 = 0V, $V_{DD}1$ = $V_{DD}2$ = 3.0V, $V_{SS}1$ = $V_{SS}2$ = 0V, Ta = 25°C

SW1, SW53, SW63 = ON

SW8, SW9, SW10, SW59 = A

SW50, SW51 = B

V53 = 0V, V63 = 2.2V

Set the serial bus registers to the "Serial Bus Register Initial Settings".

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply characteristics						
Current consumption $V_{CC}1$	$I_{CC}11$	Input SIG4 to (A) and SIG2 (0dB) to (B). Measure the $I_{CC}1$ current value. COMP input mode	20	27	34	mA
	$I_{CC}12$	Input SIG4 to (A) and SIG2 (0dB) to (B). Measure the $I_{CC}1$ current value. Y/C input mode	19	26	33	mA
	$I_{CC}13$	Input SIG4 to (A), (D) and (E). Measure the $I_{CC}1$ current value. SW50, SW51 = A, SW59 = B Y/color difference input mode	15	21	27	mA
Current consumption $V_{CC}2$	$I_{CC}2$	Input SIG4 to (A) and SIG2 (0dB) to (B). Measure the $I_{CC}2$ current value.	3	5	8	mA
Current consumption V_{DD}	$I_{DD}1$	Input SIG4 to (A) and SIG2 (0dB) to (B). Measure the IDD current value. LCX009 mode	4	6	8	mA
	$I_{DD}2$	Input SIG4 to (A) and SIG2 (0dB) to (B). Measure the I_{DD} current value. LCX005 mode	3.5	5	6.5	mA

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Digital block I/O characteristics							
Input current FLDIN pin	II1	Normal input pin	VIN = V_{DD}	–10			µA
			VIN = V_{SS}			10	
Input current	II2	Input pin with pull-up resistor*1 VIN = V_{SS}		–145	–60	–24	µA
High level input voltage	VIH	CMOS input cell*3		0.7V_{DD}			V
Low level input voltage	VIL	CMOS input cell*3				0.3V_{DD}	V
High level output voltage Output pins except CKO and RPD	VOH1	IOH = –1mA*2		2.8			V
Low level output voltage Output pins except CKO and RPD	VOL1	IOL = 1mA*2				0.3	V
High level output voltage CKO pin	VOH2	IOH = –3mA		0.5V_{DD}			V
Low level output voltage CKO pin	VOL2	IOL = 3mA				0.5V_{DD}	V
High level output voltage RPD pin	VOH3	IOH = –0.5mA		V_{DD} – 1.2			V
Low level output voltage RPD pin	VOL3	IOL = 0.7mA				1.0	V
Output off leak current RPD pin	IOFF	High impedance status VOUT = V_{SS} or VOUT = V_{DD}		–40		40	µA

*1 Input pins with pull-up resistors: SCLK, DATA, LOAD, RGT

*2 Output pins except CKO and RPD: CLR, HST, HCK1, HCK2, HD, VD1, VD2, FLDOUT, VST, VCK1, VCK2, EN

*3 CMOS input cells: FLDIN, SCLK, DATA, LOAD, RGT

Electrical Characteristics – AC Characteristics

Unless otherwise specified, Settings 1 and 2 and the following setting conditions are required.
$V_{CC}1$ = 4.5V, $V_{CC}2$ = 12.0V, GND1 = GND2 = GND3 = 0V, $V_{DD}1$ = $V_{DD}2$ = 3.0V, $V_{SS}1$ = $V_{SS}2$ = 0V, Ta = 25°C
SW1, SW53, SW63 = ON
SW8, SW9, SW10 = A
SW50, SW51, SW59 = B
V53 = 0V, V63 = 2.2V
Set the serial bus registers to the "Serial Bus Register Initial Settings".
Unless otherwise specified, measure the non-inverted outputs for TP41, TP43 and TP45.

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Y signal system							
Video maximum gain	GV	Input SIG4 to (A) and measure the ratio between the output amplitude (white – black) and input amplitude at TP43.		19	22	25	dB
Contrast characteristics TYP	GCNTTP	Input SIG4 to (A) and measure the ratio between the output amplitude (white – black) and input amplitude at TP43.		13	17	21	dB
Contrast characteristics MIN	GCNTMN	Input SIG4 to (A) and measure the ratio between the output amplitude (white – black) and input amplitude at TP43.		–9	–5	–1	dB
Y signal frequency characteristics	FCYYC	Assume the output amplitude at TP43 when SIG1 (0dB, no burst, 100kHz) is input to (A) as 0dB. Vary the frequency of the input signal to obtain the frequency with an output amplitude of –3dB.	Y/C input, V63 = 1.5V	5.0			MHz
	FCYCMN		Composite input (NTSC), V63 = 2.2V	2.5			MHz
	FCYCMP		Composite input (PAL), V63 = 2.2V	3.0			MHz
Picture adjustment variable amount 1 (composite input, LCX005 mode)	GSHP1X	Assume the output amplitude at TP43 when SIG7 (100kHz) is input to (A) as 0dB. Set SIG7 to 1.8MHz and measure GSHP1X and GSHP1N as the amounts by which the output amplitude at TP43 changes when V63 = 4V and 0V, respectively.		8	12		dB
	GSHP1N				–3	1	dB
Picture adjustment variable amount 2 (composite input, LCX009 mode)	GSHP2X	Assume the output amplitude at TP43 when SIG7 (100kHz) is input to (A) as 0dB. Set SIG7 to 2.0MHz and measure GSHP2X and GSHP2N as the amounts by which the output amplitude at TP43 changes when V63 = 4V and 0V, respectively.		6	9		dB
	GSHP2N				–4	2	dB
Picture adjustment variable amount 3 (Y/C input, LCX005 mode)	GSHP3X	Assume the output amplitude at TP43 when SIG7 (100kHz) is input to (A) as 0dB. Set SIG7 to 1.8MHz and measure GSHP3X and GSHP3N as the amounts by which the output amplitude at TP43 changes when V63 = 4V and 0V, respectively.		10	15		dB
	GSHP3N				–1	2	dB
Picture adjustment variable amount 4 (Y/C input, LCX009 mode)	GSHP4X	Assume the output amplitude at TP43 when SIG7 (100kHz) is input to (A) as 0dB. Set SIG7 to 2.5MHz and measure GSHP4X and GSHP4N as the amounts by which the output amplitude at TP43 changes when V63 = 4V and 0V, respectively.		10	14		dB
	GSHP4N				–2	0	dB
Carrier leak (residual carrier)	CRLEKY	Input SIG2 (0dB) to (A). Using a spectrum analyzer, measure the input and the 3.58MHz or 4.43MHz component of TP43, and obtain $CRLEKY = 150mV \times 10^{\Delta CLK/20}$ using their difference ΔCLK.				30	mV
Y signal I/O delay time	TDYYC	Input SIG9 (VL = 150mV) to (A). Measure the delay time from the 2T pulse peak of the input signal to the peak of the non-inverted output at TP43.	Y/C input	230	330	430	ns
	TDYCMN		Composite input (NTSC)	430	530	630	ns
	TDYCMP		Composite input (PAL)	430	530	630	ns

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Chroma signal block							
ACC amplitude characteristics 1	ACC1	Input SIG5 (VL = 150mV) to (A) and SIG2 (0dB/+6dB/–20dB, 3.58MHz burst/chroma phase = 180°, or 4.43MHz burst/chroma phase = ±135°) to (B). Measure the output amplitude at TP52, assuming the output corresponding to 0dB, +6dB and –20dB as V0, V1 and V2, respectively. ACC1 = 20 log (V1/V0) ACC2 = 20 log (V2/V0) SW59 = A	NTSC	–3	0	3	dB
			PAL	–3	0	3	dB
ACC amplitude characteristics 2	ACC2		NTSC	–3	0	3	dB
			PAL	–3	0	3	dB
APC pull-in range	FAPCN	Input SIG5 (VL = 150mV) to (A) and SIG2 (0dB, 3.58MHz burst/chroma phase = 180°, or 4.43MHz burst/chroma phase = ±135°) to (B). Changing the SIG2 burst frequency, measure the frequency fl at which the TP41 output appears (the killer mode is canceled). NTSC: FAPCN = fl – 3579545Hz PAL: FAPCP = fl – 4433619Hz SW59 = A	NTSC	±500			Hz
	FAPCP		PAL	±500			Hz
Color adjustment characteristics MAX	GCOLMX	Input SIG5 (VL = 150mV) to (A) and SIG2 (0dB, 3.58MHz burst/chroma phase = 180°) to (B). Assume the chroma output when serial bus register COLOR = 80H, 0FFH and 0H as V0, V1 and V2, respectively. GCOLMX = 20 log (V1/V0) GCOLMN = 20 log (V2/V0) SW59 = A		4	6		dB
Color adjustment characteristics MIN	GCOLMN				–25	–15	dB
HUE adjustment range MAX	HUEMX	Input SIG5 (VL = 150mV) to (A) and SIG2 (0dB, burst/chroma phase variable) to (B). Assume the phase at which the output amplitude at TP41 reaches a minimum when serial bus register HUE = 80H, 0FFH and 0H as $\theta 0$, $\theta 1$ and $\theta 2$, respectively. HUEMX = $\theta 1 - \theta 0$ HUEMN = $\theta 2 - \theta 0$ SW59 = A		–30	–40		deg
HUE adjustment range MIN	HUEMN			30	60		deg
Killer operation input level	ACKN	Input SIG5 (VL = 150mV) to (A) and SIG2 (level variable, 3.58MHz burst/chroma phase = 180°, or 4.43MHz burst/chroma phase = ±135°) to (B), and measure the output amplitude at TP41. Gradually reduce the SIG2 amplitude level and measure the level at which the killer operation is activated. SW59 = A	NTSC		–36	–30	dB
	ACKP		PAL		–34	–28	dB

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Demodulation output amplitude ratio (NTSC)	VRBN	Input SIG5 (VL = 150mV) to (A) and SIG2 (0dB, 3.58MHz) to B and change the chroma phase. Assume the maximum amplitude at TP41 as VB, the maximum amplitude at TP43 as VG, and the maximum amplitude at TP45 as VR. VRBN = VR/VB, VGBN = VG/VB SW59 = A	0.53	0.63	0.73	
	VGBN		0.25	0.32	0.39	
Demodulation output phase difference (NTSC)	θRBN	Input SIG5 (VL = 150mV) to (A) and SIG2 (0dB, 3.58MHz) to B and change the chroma phase. Assume the phase at which the amplitude at TP41, TP43 and TP45 reaches a maximum as θB, θG and θR, respectively. θRBN = θR – θB, θGBN = θG – θB SW59 = A	99	109	119	deg
	θGBN		230	242	254	deg
Demodulation output amplitude ratio (PAL)	VRBP	Input SIG5 (VL = 150mV) to (A) and SIG2 (0dB, 4.43MHz) to B and change the chroma phase. Assume the maximum amplitude at TP41 as VB, the maximum amplitude at TP43 as VG, and the maximum amplitude at TP45 as VR. VRBP = VR/VB, VGBP = VG/VB SW59 = A	0.65	0.75	0.85	
	VGBP		0.33	0.40	0.47	
Demodulation output phase difference (PAL)	θRBP	Input SIG5 (VL = 150mV) to (A) and SIG2 (0dB, 4.43MHz) to B and change the chroma phase. Assume the phase at which the amplitude at TP41, TP43 and TP45 reaches a maximum as θB, θG and θR, respectively. θRBP = θR – θB, θGBP = θG – θB SW59 = A	80	90	100	deg
	θGBP		232	244	256	deg
Color difference input color adjustment characteristics MAX	GEXCMX	Input SIG5 (VL = 150mV) to (A) and SIG1 (0dB, 100kHz, no burst) to (D). Assume the output amplitude at TP41 when serial bus register COLOR = 80H as VC0, when COLOR = 0H as VC2, and when SIG1 is set to –10dB and COLOR = 0FFH as VC1. GEXCMX = 20 log (VC1/VC0) + 10 GEXCMN = 20 log (VC2/VC0) SW50, SW51 = A	4	6		dB
Color difference input color adjustment characteristics MIN	GEXCMN			–20	–15	dB
Color difference balance	VEXCBL	Input SIG5 (VL = 150mV) to (A) and SIG1 (0dB, 100kHz, no burst) to (D) and (E). Assume the output amplitude at TP41 as VB and the output amplitude at TP45 as VR. VEXCBL = VR/VB SW50, SW51 = A	0.8	1.0	1.2	
Color difference input balance adjustment R	GEXRMX	Input SIG5 (VL = 150mV) to (A) and SIG1 (–6dB, 100kHz, no burst) to (D) and (E). Assume the output amplitude at TP45 and TP41 when serial bus register HUE = 80H as VR0 and VB0, respectively, when HUE = 0FFH as VR1 and VB1, respectively, and when HUE = 0H as VR2 and VB2, respectively. GEXRMX = 20 log (VR1/VR0) GEXRMN = 20 log (VR2/VR0) GEXBMX = 20 log (VB1/VB0) GEXBMN = 20 log (VB2/VB0) SW50, SW51 = A	2	3		dB
	GEXRMN			–3	–2	dB
Color difference input balance adjustment B	GEXBMX			–3	–2	dB
	GEXBMN		2	3		dB

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
G-Y matrix characteristics	VEXGB	Input SIG5 (VL = 150mV) to (A) and SIG1 (0dB, 100kHz, no burst) to (D). Assume the output amplitude at TP41 as VEXB and the output amplitude at TP43 as VEXBG. VEXGB = VEXBG/VEXB SW50, SW51 = A	NTSC	0.23	0.25	0.28	
			PAL	0.17	0.19	0.21	
	VEXGR	Input SIG5 (VL = 150mV) to (A) and SIG1 (0dB, 100kHz, no burst) to (E). Assume the output amplitude at TP45 as VEXR and the output amplitude at TP43 as VEXRG. VEXGR = VEXRG/VEXR SW50, SW51 = A		0.48	0.53	0.58	
RGB signal output block							
RGB signal output DC voltage	VOUT	Input SIG5 (VL = 0mV) to (A). Adjust serial bus register BRIGHT so that the output (black-black) at TP43 is 9Vp-p and measure the DC voltage at TP41, TP43 and TP45.		5.85	6.00	6.15	V
RGB signal output DC voltage difference	ΔVOUT	Input SIG5 (VL = 0mV) to (A). Adjust serial bus register BRIGHT so that the output (black-black) at TP43 is 9Vp-p, measure the DC voltage at TP41, TP43 and TP45, and obtain the maximum difference between these values.			0	100	mV
RGB output limiter operation voltage	VLIMMX	Input SIG3 to (A). Vary V53 and measure the maximum value VLIMMX and minimum value VLIMMN of the voltage range (black – black) over which the black limiter operates for the TP41, TP43 and TP45 outputs. Assume the value when V53 = 0V as VLIMMX, and when V53 = 4.5V as VLIMMN.		9.0			Vp-p
	VLIMMN					5.2	Vp-p
Amount of change in brightness	BRTMX	Input SIG5 (VL = 0mV) to (A) and measure the output (black – black) at TP41, TP43 and TP45 when serial bus register BRIGHT = 0H.		9.0			Vp-p
	BRTMN	Input SIG5 (VL = 0mV) to (A) and measure the output (black – black) at TP41, TP43 and TP45 when serial bus register BRIGHT = 0FFH.				4.0	Vp-p
Amount of change in sub-brightness	SBBRT	Input SIG5 (VL = 0mV) to (A) and measure the difference between the outputs (black-black) at TP41 and TP45 and the output (black – black) at TP43 when serial bus registers R-BRT = B-BRT = 0H and when R-BRT = B-BRT = 0FFH.		±1.5	±2.0		V
Difference in gain between RGB output signals	ΔGRGB	Input SIG4 to (A) and obtain the level difference between the maximum and minimum non-inverted output amplitudes (white – black) at TP41, TP43 and TP45.		–0.5	0	0.5	dB
Difference in RGB output inverted/ non-inverted gain	ΔGINV	Input SIG4 to (A) and obtain the level difference between the non-inverted output amplitudes (white – black) and the inverted output amplitudes at TP41, TP43 and TP45.		–0.5	0	0.5	dB
Difference in black level potential between RGB output signals	ΔVBL	Input SIG4 to (A) and obtain the level difference between the maximum and minimum black levels of both the inverted and non-inverted outputs at TP41, TP43 and TP45.				300	mV

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
γ gain	Gγ1	Input SIG8 to (A). Adjust the non-inverted output black level at TP43 to 6 – 4.5V with serial bus register BRIGHT and the non-inverted output amplitude (white – black) at TP43 to 3.5V with serial bus register CONTRAST. Measure VG1, VG2 and VG3. Gγ1 = 20 log (VG1/0.0357) Gγ2 = 20 log (VG2/0.0357) Gγ3 = 20 log (VG3/0.0357) (See Fig. 5 for definitions of VG1, VG2 and VG3.)	23.0	26.0	29.0	dB
	Gγ2		12.0	15.0	18.0	dB
	Gγ3		18.0	22.0	26.0	dB
γ1 adjustment variable range	Vγ1MN	Input SIG8 to (A) and adjust serial bus register BRIGHT so that the output at TP43 is 9Vp-p (black – black). Read the point where the gain of the non-inverted output at TP43 changes when serial bus register γ1 = 0H and 0FFH from the input signal IRE level. Vγ1MN when γ1 = 0H, and Vγ1MX when γ1 = 0FFH.			0	IRE
	Vγ1MX		100			IRE
γ2 adjustment variable range	Vγ2MN	Input SIG8 to (A) and adjust serial bus register BRIGHT so that the output at TP43 is 9Vp-p (black – black). Read the point where the gain of the non-inverted output at TP43 changes when serial bus register γ2 = 0H and 0FFH from the input signal IRE level. Vγ2MN when γ2 = 0H, and Vγ2MX when γ2 = 0FFH.	100			IRE
	Vγ2MX				0	IRE
Filter characteristics						
Amount of BPF attenuation	ATBPF	Assume the chroma amplitude at TP52 when SIG5 (VL = 0mV) is input to (A) and SIG1 (0dB at input center frequency (3.58MHz or 4.43MHz)) is input to (B) as 0dB. Obtain the amount by which the output at TP52 is attenuated when the frequencies noted on the right are input. SW59 = A — NTSC 1.5MHz		–16	–10	dB
		PAL 2.0MHz		–16	–10	dB
		NTSC 5.5MHz		–7	–2	dB
		PAL 6.8MHz		–8	–3	dB
Amount of TRAP attenuation	ATRAPN	Input SIG2 (0dB, 3.58MHz or 4.43MHz) to (A) and measure the output at TP43. Assume the amplitude at TP43 during Y/C input mode as 0dB, and obtain the amount of attenuation during COMP input mode. — NTSC		–40	–30	dB
	ATRAPP	PAL		–40	–30	dB
R-Y, B-Y and LPF characteristics	DEMLPF	Assume the amplitude of the 100kHz component of the output at TP43 when SIG5 (VL = 150mV) is input to (A) and SIG2 (0dB, 3.58MHz + 100kHz) is input to (B) as 0dB. Obtain the frequency which attenuates the beat component of the output by 3dB when the SIG2 frequency is increased with respect to 3.58MHz.	0.8	1.0	1.3	MHz
Sync separation, TG block						
Input sync signal width sensitivity	WSSEP	Input SIG5 (VL = 0mV, VS = 143mV, WS variable) to (A) and confirm that it is synchronized with the HD output at TP22. Gradually narrow the WS of SIG5 from 4.7µs and obtain the WS at which synchronization with the HD output at TP22 is lost.	2.0			µs
Sync separation input sensitivity	VSSEP	Input SIG5 (VL = 0mV, WS = 4.7µs, VS variable) to (A) and confirm that it is synchronized with the HD output at TP22. Gradually reduce the VS of SIG5 from 143mV and obtain the VS at which synchronization with the HD output at TP22 is lost.		40	60	mV

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Sync separation output delay time	TDSYL	Input SIG5 (VL = 0mV, WS = 4.7µs, VS = 143mV) to (A) and measure the delay time with the RPD output at TP12. TDSYL is from the falling edge of the input HSYNC to the falling edge of the RPD output at TP12, and TDSYH is from the falling edge of the input HSYNC to the rising edge of the RPD output at TP12.		430	630	830	ns
	TDSYH			4.7	5.0	5.3	µs
Horizontal pull-in range	HPLLN	Input SIG5 (VL = 0mV, WS = 4.7µs, VS = 143mV, horizontal frequency variable) to (A) and confirm that it is synchronized with the HD output at TP22. Obtain the frequency fH at which the input and output are synchronized by changing the horizontal frequency of SIG5 from the non-synchronized condition. HPLLN = fH – 15734 HPLLP = fH – 15625	NTSC	±500			Hz
	HPLLP		PAL	±500			Hz
Output transition time (*2 pins)	tTLH	Input SIG5 (VL = 0mV) to (A). Load = 30pF (See Fig. 3.)				30	ns
	tTHL					30	ns
Cross-point time difference	ΔT	Input SIG5 (VL = 0mV) to (A). Measure HCK1/HCK2 and VCK1/VCK2. Load = 30pF (See Fig. 4.)				10	ns
HCK duty	DTYHC	Input SIG5 (VL = 0mV) to (A). Measure the HCK1/HCK2 duty. Load = 30pF		47	50	53	%
External I/O characteristics							
External RGB input threshold voltage	VTEXTB	Input SIG5 (VL = 0mV) to (A) and SIG6 (VL variable) to (C). Raise the SIG6 amplitude (VL) from 0V and assume the voltage where the outputs at TP41, TP43 and TP45 go to black level as VTEXTB. Then raise the amplitude further and assume the voltage where these outputs go to white level as VTEXTW.		0.8	1.0	1.2	V
	VTEXTW			1.8	2.0	2.2	V
Propagation delay time between external RGB input and output	TD1EXT	Input SIG5 (VL = 0mV) to (A) and SIG6 (VL = 3V) to (C). Measure the rise delay time TD1EXT and the fall delay time TD2EXT of the outputs at TP41, TP43 and TP45. (See Fig. 2.)		50	100	150	ns
	TD2EXT			50	100	150	ns
Output blanking level during external RGB input	EXTBK	Input SIG5 (VL = 0mV) to (A) and SIG6 (VL = 1.7V) to (C). Measure the difference from the black level of the outputs at TP41, TP43 and TP45.				0	V
Output white level during external RGB input	EXTWT	Input SIG5 (VL = 0mV) to (A) and SIG6 (VL = 2.7V) to (C). Measure the difference from the black level of the outputs at TP41, TP43 and TP45.		3.5			V

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Serial transfer block						
Data setup time	ts0	LOAD setup time, activated by the rising edge of SCLK. (See Fig. 6.)	150			ns
	ts1	DATA setup time, activated by the rising edge of SCLK. (See Fig. 6.)	150			ns
Data hold time	th0	LOAD hold time, activated by the rising edge of SCLK. (See Fig. 6.)	150			ns
	th1	DATA hold time, activated by the rising edge of SCLK. (See Fig. 6.)	150			ns
Minimum pulse width	tw1L	SCLK pulse width. (See Fig. 6.)		160		ns
	tw1H	SCLK pulse width. (See Fig. 6.)		160		ns
	tw2	LOAD pulse width. (See Fig. 6.)	1			µs
Other						
AFC adjustment voltage output range	VPLLMN	Measure the DC voltage of the output at TP11 when serial bus register PLL ADJ = 0H, 80H and 0FFH as VPLLMN, VPLLTP and VPLLMX, respectively.	5.65	5.8	5.95	V
	VPLLTP		7.4	7.5	7.6	
	VPLLMX		9.15	9.3	9.45	

Description of Electrical Characteristics Measurement Methods

Serial Bus Register Initial Values

Item		Symbol	Serial bus													
			Mode settings						DAC settings							
			Input	System	Panel	S/H	H-POSI	HD-POSI	HUE	COLOR	BRIGHT	CONTRAST	R-BRT	B-BRT	γ1	γ2
Setting 2	Horizontal AFC adjustment		COMP	NTSC	—	SHS1	10H	0H	80H	80H	80H	80H	80H	80H	0H	0H
Power supply characteristics	Current consumption $V_{CC}1$	$I_{CC}11$	COMP	NTSC	—	SHS1	10H	0H	80H	80H	80H	80H	80H	80H	0H	0H
		$I_{CC}12$	Y/C	NTSC	—	SHS1	10H	0H	80H	80H	80H	80H	80H	80H	0H	0H
		$I_{CC}13$	Y/color difference	NTSC	—	SHS1	10H	0H	80H	80H	80H	80H	80H	80H	0H	0H
	Current consumption $V_{CC}2$	$I_{CC}2$	COMP	NTSC	—	SHS1	10H	0H	80H	80H	80H	80H	80H	80H	0H	0H
	Current consumption V_{DD}	$I_{DD}1$	COMP	NTSC	LCX009	SHS1	10H	0H	80H	80H	80H	80H	80H	80H	0H	0H
		$I_{DD}2$	COMP	NTSC	LCX005	SHS1	10H	0H	80H	80H	80H	80H	80H	80H	0H	0H
Digital block I/O characteristics	Input current	II1	COMP	NTSC	—	SHS1	10H	0H	80H	80H	80H	80H	80H	80H	0H	0H
	Input current	II2	COMP	NTSC	—	SHS1	10H	0H	80H	80H	80H	80H	80H	80H	0H	0H
	High level input voltage	VIH	COMP	NTSC	—	SHS1	10H	0H	80H	80H	80H	80H	80H	80H	0H	0H
	Low level input voltage	VIL	COMP	NTSC	—	SHS1	10H	0H	80H	80H	80H	80H	80H	80H	0H	0H
	High level output voltage	VOH1	COMP	NTSC	—	SHS1	10H	0H	80H	80H	80H	80H	80H	80H	0H	0H
	Low level output voltage	VOL1	COMP	NTSC	—	SHS1	10H	0H	80H	80H	80H	80H	80H	80H	0H	0H
	High level output voltage	VOH2	COMP	NTSC	—	SHS1	10H	0H	80H	80H	80H	80H	80H	80H	0H	0H
	Low level output voltage	VOL2	COMP	NTSC	—	SHS1	10H	0H	80H	80H	80H	80H	80H	80H	0H	0H
	High level output voltage	VOH3	COMP	NTSC	—	SHS1	10H	0H	80H	80H	80H	80H	80H	80H	0H	0H
	Low level output voltage	VOL3	COMP	NTSC	—	SHS1	10H	0H	80H	80H	80H	80H	80H	80H	0H	0H
	Output off leak current	IOFF	COMP	NTSC	—	SHS1	10H	0H	80H	80H	80H	80H	80H	80H	0H	0H

(—: don't care, ADJ: adjustment, SET: setting)

Item		Symbol	Serial bus													
			Mode settings						DAC settings							
			Input	System	Panel	S/H	H-POSI	HD-POSI	HUE	COLOR	BRIGHT	CONTRAST	R-BRT	B-BRT	γ1	γ2
Y signal block	Video maximum gain	GV	COMP	NTSC	—	Through	10H	0H	80H	80H	80H	0FFH	80H	80H	0H	0H
	Contrast characteristics TYP	GCNTTP	COMP	NTSC	—	Through	10H	0H	80H	80H	80H	80H	80H	80H	0H	0H
	Contrast characteristics MIN	GCNTMN	COMP	NTSC	—	Through	10H	0H	80H	80H	80H	0H	80H	80H	0H	0H
	Y signal frequency response	FCYYC	Y/C	NTSC	LCX009	Through	10H	0H	80H	80H	80H	80H	80H	80H	0H	0H
		FCYCMN	COMP	NTSC	LCX005	Through	10H	0H	80H	80H	80H	80H	80H	80H	0H	0H
		FCYCMP	COMP	PAL	LCX005	Through	10H	0H	80H	80H	80H	80H	80H	80H	0H	0H
	Picture quality adjustment variable amount 1	GSHP1X	COMP	NTSC	LCX005	Through	10H	0H	80H	80H	80H	80H	80H	80H	0H	0H
		GSHP1N	COMP	NTSC	LCX005	Through	10H	0H	80H	80H	80H	80H	80H	80H	0H	0H
	Picture quality adjustment variable amount 2	GSHP2X	COMP	NTSC	LCX009	Through	10H	0H	80H	80H	80H	80H	80H	80H	0H	0H
		GSHP2N	COMP	NTSC	LCX009	Through	10H	0H	80H	80H	80H	80H	80H	80H	0H	0H
	Picture quality adjustment variable amount 3	GSHP3X	Y/C	NTSC	LCX005	Through	10H	0H	80H	80H	80H	80H	80H	80H	0H	0H
		GSHP3N	Y/C	NTSC	LCX005	Through	10H	0H	80H	80H	80H	80H	80H	80H	0H	0H
	Picture quality adjustment variable amount 4	GSHP4X	Y/C	NTSC	LCX009	Through	10H	0H	80H	80H	80H	80H	80H	80H	0H	0H
		GSHP4N	Y/C	NTSC	LCX009	Through	10H	0H	80H	80H	80H	80H	80H	80H	0H	0H
	Carrier leak	CRLEKY	COMP	—	—	Through	10H	0H	80H	80H	80H	80H	80H	80H	0H	0H
	Y signal I/O delay time	TDYYC	Y/C	—	—	Through	10H	0H	80H	80H	80H	80H	80H	80H	0H	0H
		TDYCMN	COMP	NTSC	—	Through	10H	0H	80H	80H	80H	80H	80H	80H	0H	0H
		TDYCMP	COMP	PAL	—	Through	10H	0H	80H	80H	80H	80H	80H	80H	0H	0H

(—: don't care, ADJ: adjustment, SET: setting)

	Item	Symbol	Serial bus													
			Mode settings						DAC settings							
			Input	System	Panel	S/H	H-POSI	HD-POSI	HUE	COLOR	BRIGHT	CONTRAST	R-BRT	B-BRT	γ1	γ2
Chroma signal block	ACC amplitude characteristics 1	ACC1	COMP	NTSC	—	Through	10H	0H	80H	80H	80H	80H	80H	80H	0H	0H
		ACC1	COMP	PAL	—	Through	10H	0H	80H	80H	80H	80H	80H	80H	0H	0H
	ACC amplitude characteristics 2	ACC2	COMP	NTSC	—	Through	10H	0H	80H	80H	80H	80H	80H	80H	0H	0H
		ACC2	COMP	PAL	—	Through	10H	0H	80H	80H	80H	80H	80H	80H	0H	0H
	APC pull-in range	FAPCN	COMP	NTSC	—	Through	10H	0H	80H	80H	80H	80H	80H	80H	0H	0H
		FAPCP	COMP	PAL	—	Through	10H	0H	80H	80H	80H	80H	80H	80H	0H	0H
	Color adjustment characteristics MAX	GCOLMX	COMP	NTSC	—	Through	10H	0H	80H	0FFH	80H	80H	80H	80H	0H	0H
	Color adjustment characteristics MIN	GCOLMN	COMP	NTSC	—	Through	10H	0H	80H	0H	80H	80H	80H	80H	0H	0H
	HUE adjustment characteristics MAX	HUEMX	COMP	NTSC	—	Through	10H	0H	0FFH	80H	96H	80H	80H	80H	0H	0H
	HUE adjustment characteristics MIN	HUEMN	COMP	NTSC	—	Through	10H	0H	0H	80H	96H	80H	80H	80H	0H	0H
	Killer operation input level	ACKN	COMP	NTSC	—	Through	10H	0H	80H	80H	96H	80H	80H	80H	0H	0H
		ACKP	COMP	PAL	—	Through	10H	0H	80H	80H	96H	80H	80H	80H	0H	0H
	Demodulation output amplitude ratio NTSC	VRBN	COMP	NTSC	—	Through	10H	0H	80H	80H	96H	80H	80H	80H	0H	0H
		VGBN	COMP	NTSC	—	Through	10H	0H	80H	80H	96H	80H	80H	80H	0H	0H
	Demodulation output phase difference NTSC	θRBN	COMP	NTSC	—	Through	10H	0H	80H	80H	96H	80H	80H	80H	0H	0H
		θGBN	COMP	NTSC	—	Through	10H	0H	80H	80H	96H	80H	80H	80H	0H	0H
	Demodulation output amplitude ratio PAL	VRBP	COMP	PAL	—	Through	10H	0H	80H	80H	96H	80H	80H	80H	0H	0H
		VGBP	COMP	PAL	—	Through	10H	0H	80H	80H	96H	80H	80H	80H	0H	0H
	Demodulation output phase difference PAL	θRBP	COMP	PAL	—	Through	10H	0H	80H	80H	96H	80H	80H	80H	0H	0H
		θGBP	COMP	PAL	—	Through	10H	0H	80H	80H	96H	80H	80H	80H	0H	0H

(—: don't care, ADJ: adjustment, SET: setting)

Item		Symbol	Serial bus													
			Mode settings						DAC settings							
			Input	System	Panel	S/H	H-POSI	HD-POSI	HUE	COLOR	BRIGHT	CONTRAST	R-BRT	B-BRT	γ1	γ2
Chroma signal block	Color difference input color adjustment characteristics MAX	GEXCMX	Y/color difference	—	—	Through	10H	0H	80H	0FFH	80H	80H	80H	80H	0H	0H
	Color difference input color adjustment characteristics MIN	GEXCMN	Y/color difference	—	—	Through	10H	0H	80H	0H	80H	80H	80H	80H	0H	0H
	Color difference balance	VEXCBL	Y/color difference	—	—	Through	10H	0H	80H	80H	80H	80H	80H	80H	0H	0H
	Color difference input balance adjustment R	GEXRMX	Y/color difference	—	—	Through	10H	0H	0FFH	80H	80H	80H	80H	80H	0H	0H
		GEXRMN	Y/color difference	—	—	Through	10H	0H	0H	80H	80H	80H	80H	80H	0H	0H
	Color difference input balance adjustment B	GEXBMX	Y/color difference	—	—	Through	10H	0H	0FFH	80H	80H	80H	80H	80H	0H	0H
		GEXBMN	Y/color difference	—	—	Through	10H	0H	0H	80H	80H	80H	80H	80H	0H	0H
	G-Y matrix characteristics	VEXGB	Y/color difference	NTSC	—	Through	10H	0H	80H	80H	80H	80H	80H	80H	0H	0H
			Y/color difference	PAL	—	Through	10H	0H	80H	80H	80H	80H	80H	80H	0H	0H
		VEXGR	Y/color difference	—	—	Through	10H	0H	80H	80H	80H	80H	80H	80H	0H	0H
RGB signal output block	RGB signal output DC voltage	VOUT	—	—	—	Through	10H	0H	80H	80H	ADJ	80H	80H	80H	0H	0H
	RGB signal output DC voltage difference	ΔVOUT	—	—	—	Through	10H	0H	80H	80H	ADJ	80H	80H	80H	0H	0H
	RGB output limiter operation voltage	VLIMMX	—	—	—	Through	10H	0H	80H	80H	ADJ	80H	80H	80H	0H	0H
		VLIMMN	—	—	—	Through	10H	0H	80H	80H	ADJ	80H	80H	80H	0H	0H
	Amount of change in brightness	BRTMX	—	—	—	Through	10H	0H	80H	80H	0H	80H	80H	80H	0H	0H
		BRTMN	—	—	—	Through	10H	0H	80H	80H	0FFH	80H	80H	80H	0H	0H
	Amount of change in sub-brightness	SBBRT	—	—	—	Through	10H	0H	80H	80H	0B4H	80H	SET	SET	0H	0H
	Difference in gain between RGB output signals	ΔGRGB	—	—	—	Through	10H	0H	80H	80H	80H	80H	80H	80H	0H	0H

(—: don't care, ADJ: adjustment, SET: setting)

Item		Symbol	Serial bus													
			Mode settings						DAC settings							
			Input	System	Panel	S/H	H-POSI	HD-POSI	HUE	COLOR	BRIGHT	CONTRAST	R-BRT	B-BRT	γ1	γ2
RGB signal output block	Difference in RGB output inverted/ non-inverted gain	ΔGINV	—	—	—	Through	10H	0H	80H	80H	80H	80H	80H	80H	0H	0H
	Difference in black level potential between RGB output signals	ΔVBL	—	—	—	Through	10H	0H	80H	80H	80H	80H	80H	80H	0H	0H
	γ gain	Gγ1	—	—	—	Through	10H	0H	80H	80H	ADJ	ADJ	80H	80H	78H	0D7H
		Gγ2	—	—	—	Through	10H	0H	80H	80H	ADJ	ADJ	80H	80H	78H	0D7H
		Gγ3	—	—	—	Through	10H	0H	80H	80H	ADJ	ADJ	80H	80H	78H	0D7H
	γ1 adjustment variable range	Vγ1MN	—	—	—	Through	10H	0H	80H	80H	ADJ	46H	80H	80H	0H	0H
		Vγ1MX	—	—	—	Through	10H	0H	80H	80H	ADJ	46H	80H	80H	0FFH	0H
	γ2 adjustment variable range	Vγ2MN	—	—	—	Through	10H	0H	80H	80H	ADJ	46H	80H	80H	0H	0H
		Vγ2MX	—	—	—	Through	10H	0H	80H	80H	ADJ	46H	80H	80H	0H	0FFH
Filter characteristics	Amount of BPF attenuation	ATBPF	COMP	SET	—	Through	10H	0H	80H	80H	96H	80H	80H	80H	0H	0H
	Amount of TRAP attenuation	ATRAPN	SET	NTSC	—	Through	10H	0H	80H	80H	96H	80H	80H	80H	0H	0H
		ATRAPP	SET	PAL	—	Through	10H	0H	80H	80H	96H	80H	80H	80H	0H	0H
	R-Y, B-Y and LPF characteristics	DEMLPF	Y/C	NTSC	—	Through	10H	0H	80H	80H	96H	80H	80H	80H	0H	0H

(—: don't care, ADJ: adjustment, SET: setting)

Item		Symbol	Serial bus													
			Mode settings						DAC settings							
			Input	System	Panel	S/H	H-POSI	HD-POSI	HUE	COLOR	BRIGHT	CONTRAST	R-BRT	B-BRT	γ1	γ2
Sync separation, TG block	Input sync signal width sensitivity	WSSEP	—	—	—	Through	10H	0H	80H	80H	80H	80H	80H	80H	0H	0H
	Sync separation input sensitivity	VSSEP	—	—	—	Through	10H	0H	80H	80H	80H	80H	80H	80H	0H	0H
	Sync separation output delay time	TDSYL	—	—	—	Through	10H	0H	80H	80H	80H	80H	80H	80H	0H	0H
		TDSYH	—	—	—	Through	10H	0H	80H	80H	80H	80H	80H	80H	0H	0H
	Horizontal pull-in range	HPLLN	—	NTSC	—	Through	10H	0H	80H	80H	80H	80H	80H	80H	0H	0H
		HPLLP	—	PAL	—	Through	10H	0H	80H	80H	80H	80H	80H	80H	0H	0H
	Output transition time	tTLH	—	—	—	SHS1	10H	0H	80H	80H	80H	80H	80H	80H	0H	0H
		tTHL	—	—	—	SHS1	10H	0H	80H	80H	80H	80H	80H	80H	0H	0H
	Cross-point time difference	ΔT	—	—	—	SHS1	10H	0H	80H	80H	80H	80H	80H	80H	0H	0H
	HCK duty	DTYHC	—	—	—	SHS1	10H	0H	80H	80H	80H	80H	80H	80H	0H	0H
External I/O characteristics	External RGB input threshold voltage	VTEXTB	—	—	—	Through	10H	0H	80H	80H	80H	80H	80H	80H	0H	0H
		VTEXTW	—	—	—	Through	10H	0H	80H	80H	80H	80H	80H	80H	0H	0H
	Propagation delay time between external RGB input and output	TD1EXT	—	—	—	Through	10H	0H	80H	80H	80H	80H	80H	80H	0H	0H
		TD2EXT	—	—	—	Through	10H	0H	80H	80H	80H	80H	80H	80H	0H	0H
	Output blanking level during external RGB input	EXTBK	—	—	—	Through	10H	0H	80H	80H	80H	80H	80H	80H	0H	0H
	Output white level during external RGB input	EXTWT	—	—	—	Through	10H	0H	80H	80H	64H	80H	80H	80H	0H	0H
Other	AFC adjustment voltage output range	VPPLMN	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		VPPLTP	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		VPPLMX	—	—	—	—	—	—	—	—	—	—	—	—	—	—

(—: don't care, ADJ: adjustment, SET: setting)

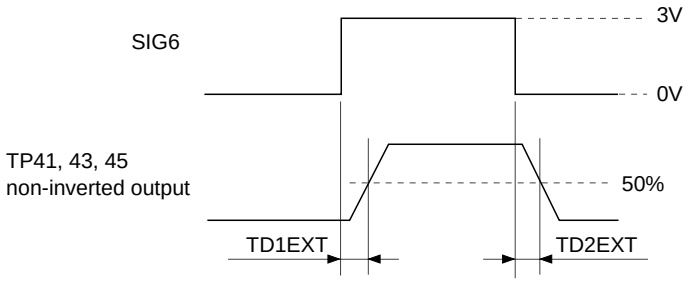


Fig. 2. Conditions for measuring the delay between external RGB input and output

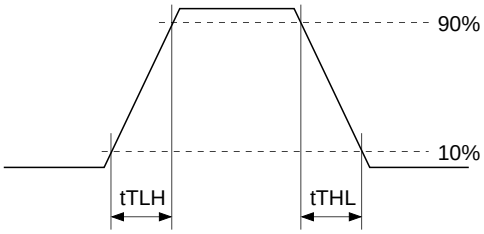


Fig. 3. Output transition time measurement conditions

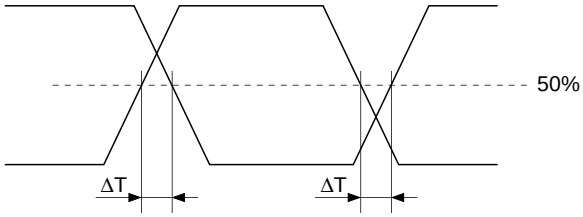


Fig. 4. Cross-point time difference measurement conditions

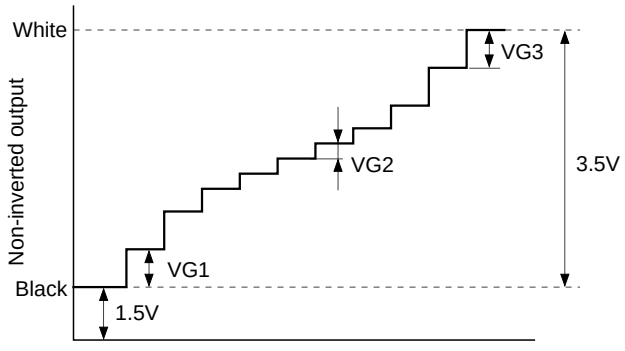


Fig. 5. γ characteristics measurement conditions

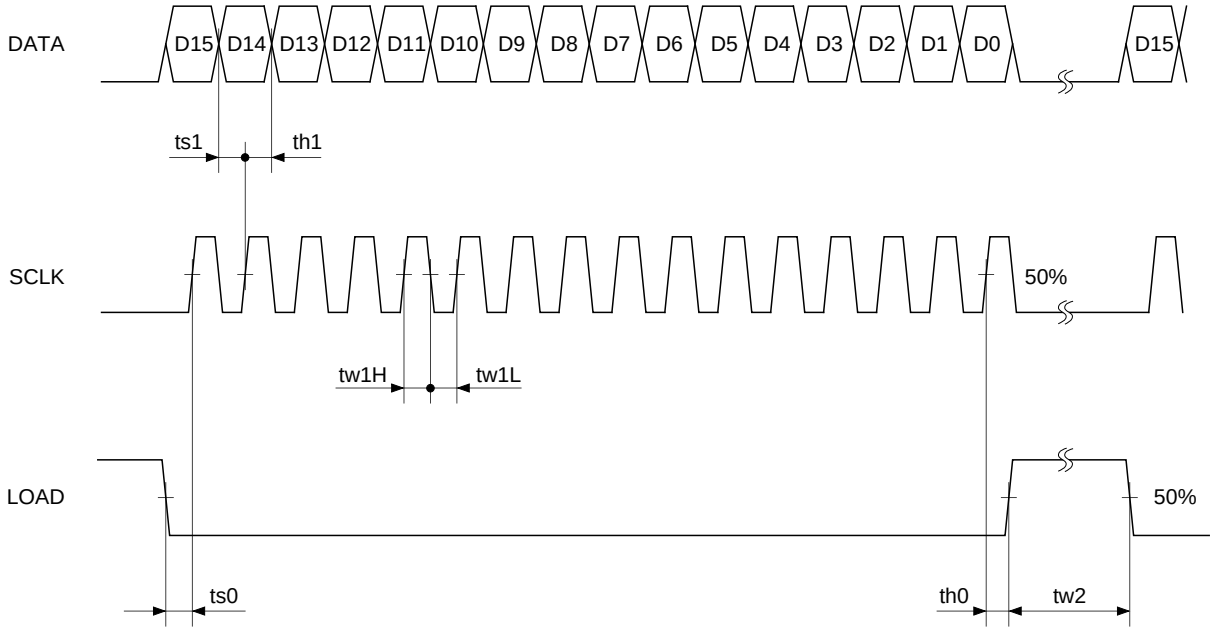
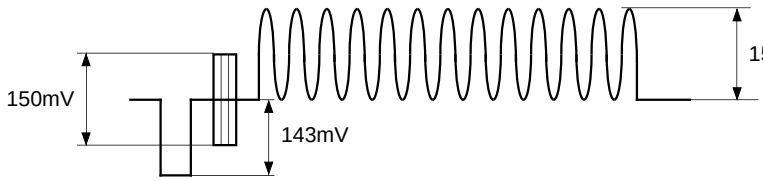
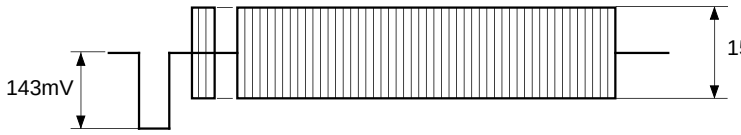
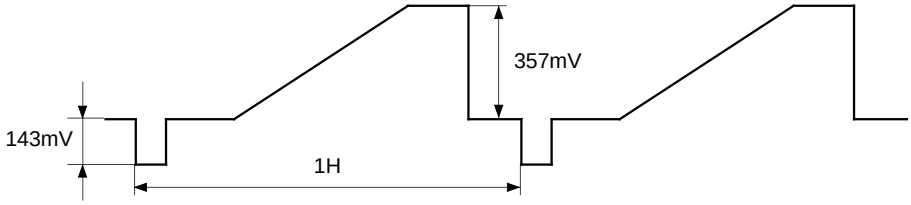
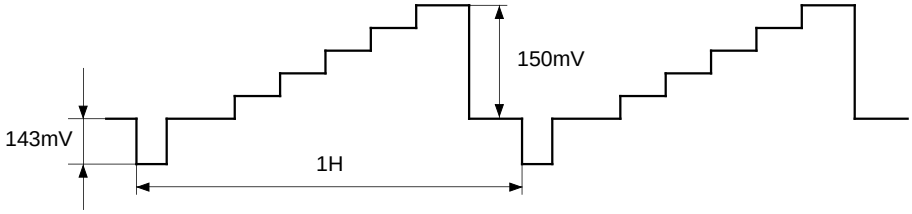
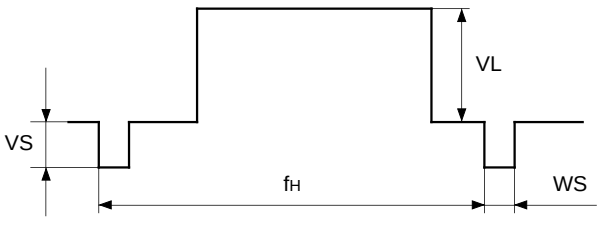
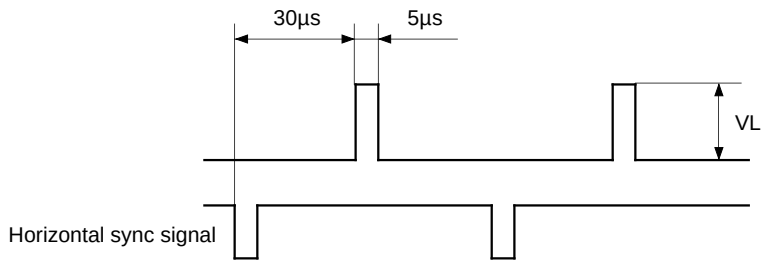
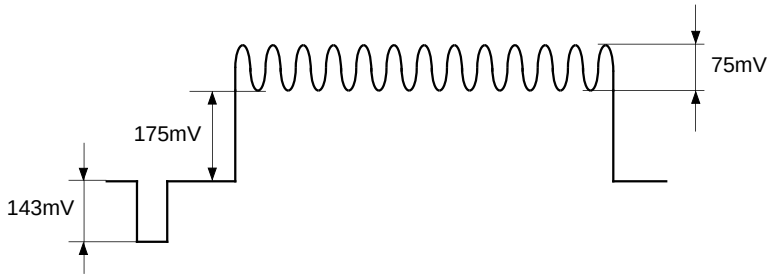
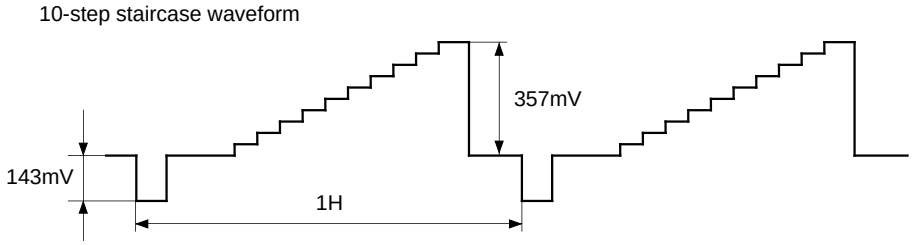
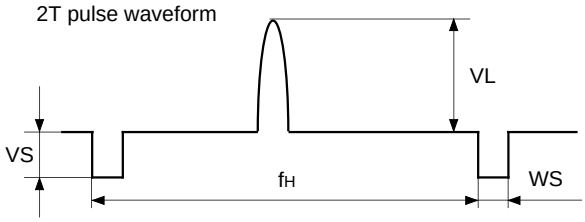


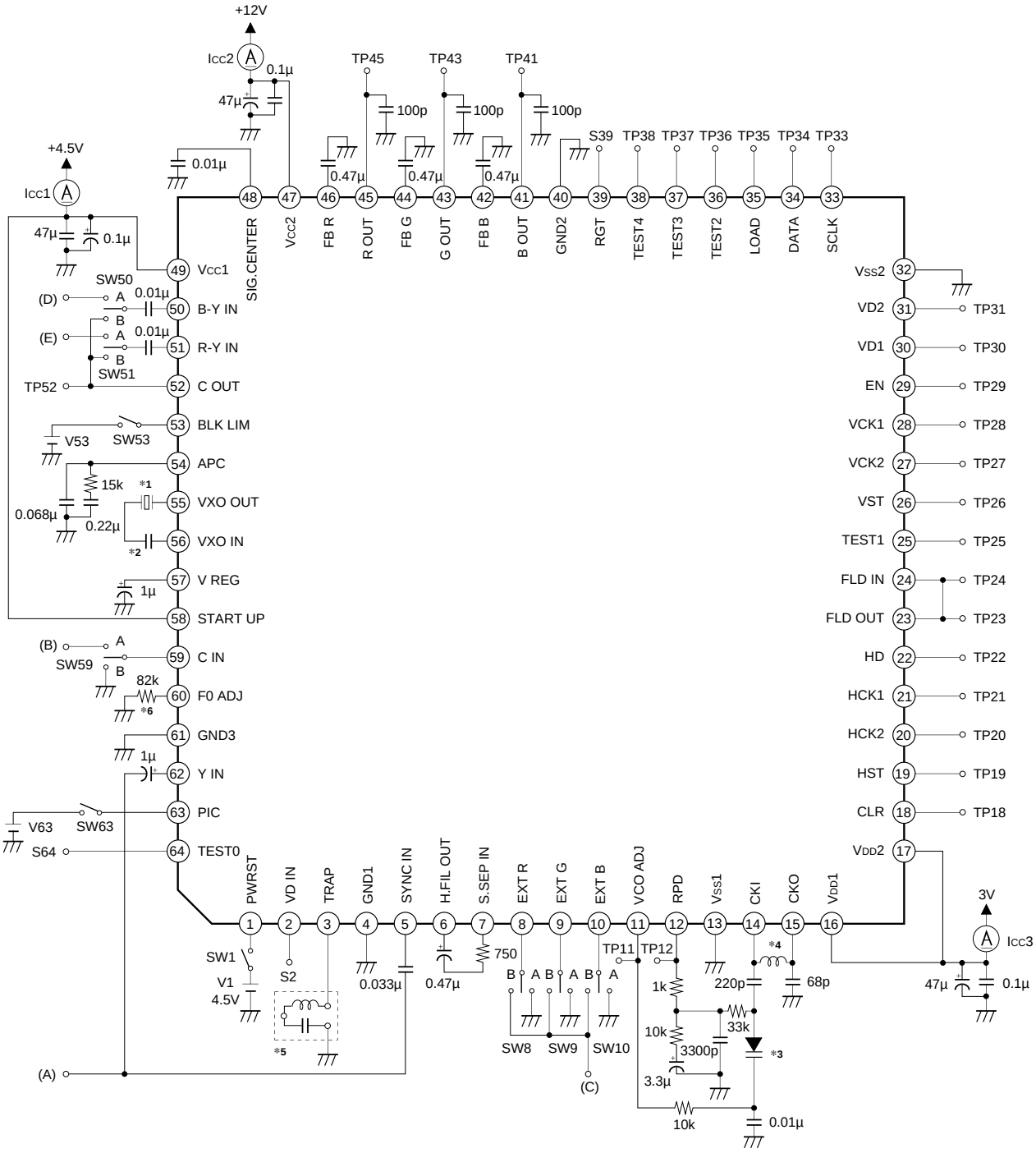
Fig. 6. Serial transfer block measurement conditions

Input Waveforms

SG No.	Waveform
SIG1	Sine wave video signal: With/without burst Amplitude and frequency variable  ← Value noted on left: 0dB
SIG2	Chroma signal: Burst, chroma frequency (3.579545MHz, 4.433619MHz) Chroma phase and burst frequency variable  ← Value noted on left: 0dB
SIG3	Ramp waveform 
SIG4	5-step staircase waveform 
SIG5	 VL amplitude variable VS variable: 143mV unless otherwise specified WS variable: 4.7µs unless otherwise specified fH variable: 15.734kHz (NTSC) or 15.625kHz (PAL) unless otherwise specified

SG No.	Waveform
SIG6	 VL amplitude variable
SIG7	 Frequency variable
SIG8	
SIG9	 VL amplitude variable VS variable: 143mV unless otherwise specified WS variable: 4.7µs unless otherwise specified fH variable: 15.734kHz (NTSC) or 15.625kHz (PAL) unless otherwise specified

Electrical Characteristics Measurement Circuit



*1 Used crystal: KINSEKI CX-5F
Frequency deviation: within ±30ppm, frequency temperature characteristics: within ±30ppm, load capacity: 16pF
NTSC: 3.579545MHz
PAL: 4.433619MHz

*2 NTSC: none, PAL: 18pF

*3 Varicap diode: 1T369 (SONY)

*4 L value: 8.2µH during LCX005 mode
3.9µH during LCX009 mode

*5 Trap (TDK)
NTSC: NLT4532-S3R6B
PAL: NLT4532-S4R4

*6 Resistance value tolerance: ±2%, temperature coefficient: ±200ppm or less

Description of Operation

The CXA2503AR incorporates the three functions of an RGB decoder block, an RGB driver block and a timing generator (TG) block onto a single chip using BiCMOS technology.

1) RGB decoder block

- Input mode switching
  The input mode can be switched between composite input, Y/C input and Y/color difference input by the serial bus settings.
  During composite input: The composite signal is input to Pins 5, 59 and 62.
  During Y/C input: The Y signal is input to Pins 5 and 62, and the C signal to Pin 59.
  During Y/color difference input: The Y signal is input to Pins 5 and 62, the B-Y signal to Pin 50, and the R-Y signal to Pin 51.

- System switching
  The input system can be switched between NTSC and PAL (DPAL using external delay line and SPAL) by the serial bus settings.

- Trap, BPF
  The center frequency of the built-in trap and BPF can be switched to 3.58MHz during NTSC and 4.43MHz during PAL.
  During composite input, the Y signal enters the trap circuit and the C signal enters the BPF. These signals do not pass through the trap or BPF during Y/C input and Y/color difference input.

- ACC detection, ACC amplifier
  The amplitude of the burst signal output from the ACC amplifier is detected and the ACC amplifier is controlled to maintain the burst signal amplitude at a constant level.

- VXO, APC detection
  The VXO local oscillation circuit is a crystal oscillation circuit. The phases of the input burst signal and the VXO oscillator output are compared in the APC detection block, and the detective output is used to form a PLL loop that controls the VXO oscillation frequency, which means that the need for adjustments is eliminated.

- External inputs
  These are digital inputs with two thresholds. When one of the RGB inputs is higher than the lower threshold Vth1 (≈ 1.0V), all RGB outputs go to black level. When the higher threshold Vth2 (≈ 2.0V) is exceeded, the output for only the signal in question goes to white level, while the other outputs remain at black level.

2) RGB driver block

• γ correction

In order to support the characteristics of LCD panels, the I/O characteristics are as shown in Fig. 1. The characteristics change as shown in Fig. 2 by adjusting the serial bus register γ1, and as shown in Fig. 3 by adjusting γ2.

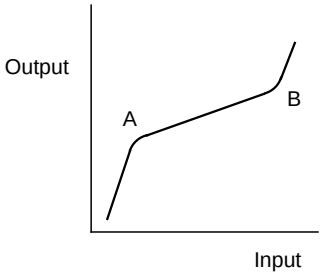


Fig. 1

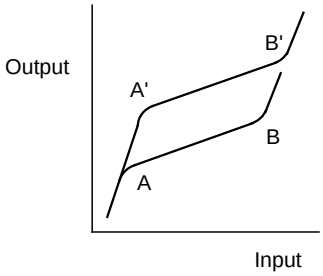


Fig. 2

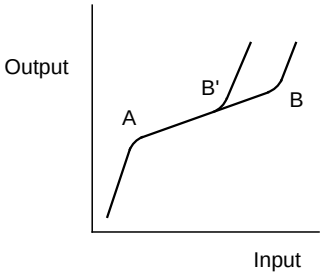
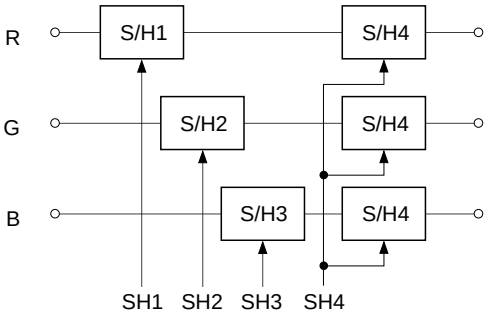
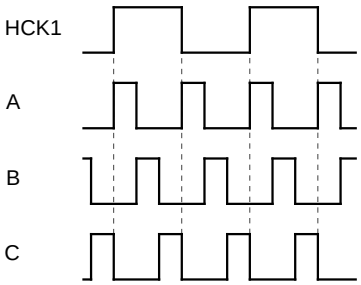


Fig. 3

• Sample-and-hold circuit

As LCD panels sample RGB signals simultaneously, RGB signals output from the CXA2503AR must be sampled-and-held in sync with the LCD panel drive pulses.





RGT = H (normal)

	SHS1	SHS2	SHS3
SH1	B	A	C
SH2	Through	Through	Through
SH3	A	C	B
SH4	C	B	A

RGT = L (inverted)

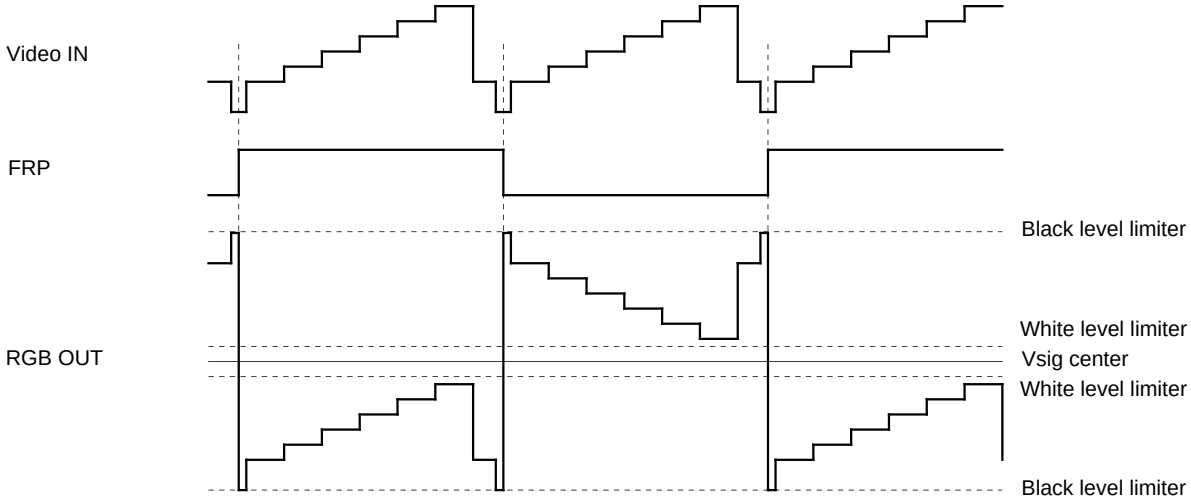
	SHS1	SHS2	SHS3
SH1	B	A	C
SH2	A	C	B
SH3	Through	Through	Through
SH4	C	B	A

SH1: R signal SH pulse
SH2: G signal SH pulse
SH3: B signal SH pulse
SH4: RGB signal SH pulse

The sample-and-hold circuit performs sample and hold by receiving the SH1 to SH4 pulses from the TG block. Since LCD panels perform color coding using an RGB delta arrangement, each horizontal line must be compensated by 1.5 dots. This relationship is reversed during right/left inversion. This compensation timing is also generated by the TG block. The sample-and-hold timing changes according to the phase relationship with the HCK1 pulse, so the timing should be set to SHS1, 2 or 3 in accordance with the actual board.

• RGB output

RGB outputs (Pins 41, 43, and 45) are inverted each horizontal line by the FRP pulse supplied from the TG block as shown in the figure below. Feedback is applied so that the center voltage (Vsig center) of the output signal matches the reference voltage ($V_{CC}2$ + GND2)/2 (or the voltage input to SIG CENTER (Pin 48)). In addition, the white level output is clipped by the Vsig center ±0.7V, and the black level output is clipped by the limiter operation point that is adjusted at the BLKLIM (Pin 53).

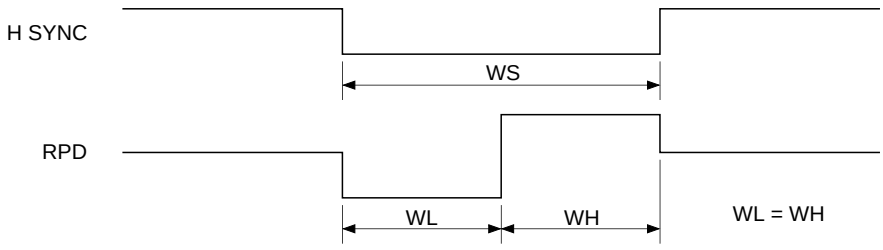


3) TG block

• PLL and AFC circuits

The TG block contains a PLL circuit phase comparator and frequency division counter, and a PLL circuit can be comprised by connecting an external VCO circuit.

The PLL error detection signal is generated at the following timing. The phase comparison output of the entire bottom of HSYNC and the internal frequency division counter becomes RPD. RPD output is converted to DC error with the lag-lead filter, and then it changes the varicap capacitance to stabilize the oscillation frequency at 702f_H in the LCX005BK/BKB and 1050f_H in the LCX009AK/AKB. The PLL of this system is adjusted by setting the serial bus register PLL ADJ so that RPD changes in the center of the window as shown in the figure below.



• H position

The horizontal display position can be set at 2f_H intervals in 32 different ways by the serial bus settings.

The picture center is set at the internal default value, but because there is a difference between the RGB signal and the drive pulse delays on the actual board, the picture center may not match the design center. In this case, adjust with the serial bus.

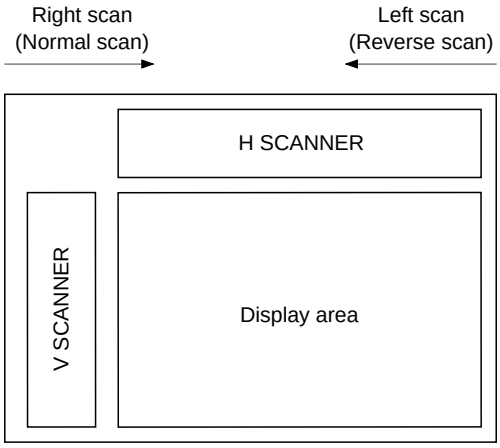
• Right/left inversion

The LCD panel is arranged in a delta pattern, where identical signal lines are offset by 1.5 dots from adjoining lines. For this reason, a 1.5-bit offset is attached to the horizontal start pulse (HST) between odd lines and even lines. HCK and S/H are also 1.5-bit offset in a similar manner.

When the panel is driven by left scan (Reverse scan), this offset relationship is inverted for even and odd lines. Moreover, since the dot arrangement is asymmetrical, the HST position is also changed.

RGT = H: Right scan mode

RGT = L: Left scan mode



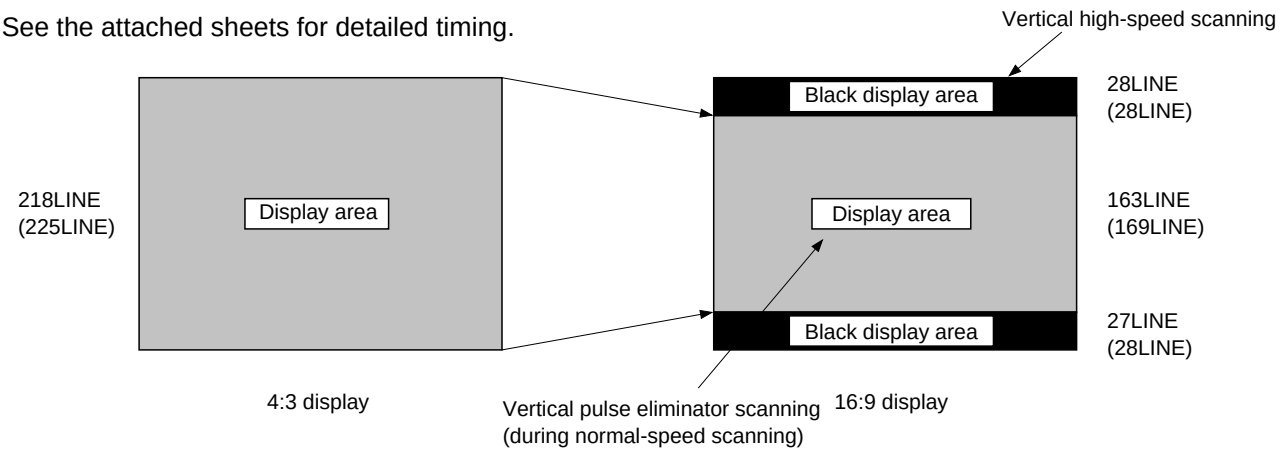
• WIDE mode

Setting the WIDE mode by switching the aspect ratio with the serial bus shifts the unit to WIDE mode. In this mode, the aspect ratio is converted through pulse eliminator processing, allowing 16:9 quasi-WIDE display.

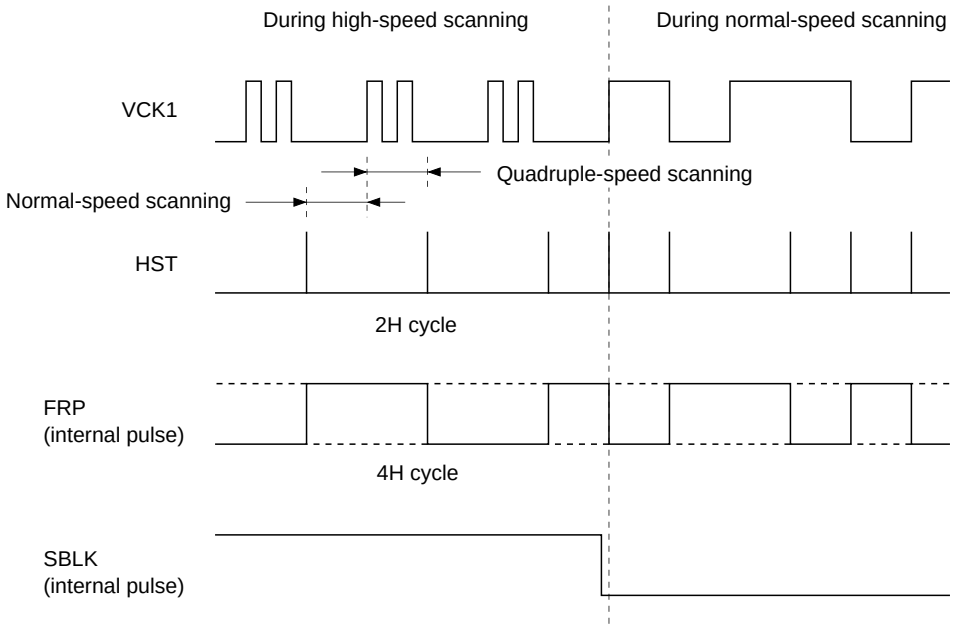
During WIDE mode, vertical pulse eliminator scanning of 1/4 for NTSC or 1/2 and 1/4 for PAL are performed, and the video signal is compressed to achieve a 16:9 aspect ratio. In addition, in areas outside the display area, black is displayed by performing high-speed scanning.

The timing during high-speed scanning is a 2H cycle pulse consisting of normal drive (1H) and quadruple-speed drive (1H) and black signals are written in the 28 and 27 lines, respectively at the top and bottom of this display area. During this time, FRP is changed to a 4H cycle, HST to a 2H cycle, and EN and CLR are not output.

See the attached sheets for detailed timing.



Numbers in parentheses are for the LCX009AK/AKB.
All other numbers are for the LCX005BK/BKB.



• AC driving of LCD panels during no signal

HST, HCK1, HCK2, VST, VCK1, VCK2, HD, VD1, VD2 and FRP are made to run free so that the LCD panel is AC driven even when there is no composite sync from the SYNC IN pin.

During this time, the HSYNC separation circuit stops and the PLL counter is made to run free. In addition, the VSYNC separation circuit is also stopped, so the auxiliary V counter is used to create the reference pulse for generating VD1 and VST.

The cycle of this V counter is designed to be 269H for NTSC and 321H for PAL. However, when there is no vertical sync signal for 5 frames, the no signal state is assumed and the free running VD1 and VST pulses are generated from the next field.

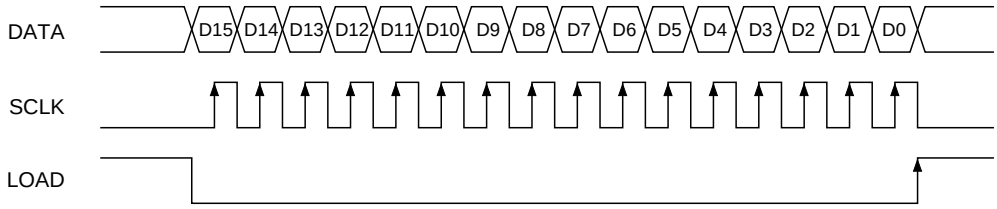
In addition, RPD is kept at high impedance when there is no signal in order to prevent the AFC circuit from causing errors due to phase comparison.

Description of Serial Control Operation

1) Control method

Control data consists of 16 bits of data which is loaded one bit at a time at the rising edge of SCLK. This loading operation starts from the falling edge of LOAD and is completed at the next rising edge. (D13 to D15 are dummy data.)

Digital block control data is established by the vertical sync signal, so if data is transferred multiple times for the same item, the data immediately before the vertical sync signal is valid.
Analog (electronic attenuator) block control data becomes valid each time the LOAD signal is input.



Serial transfer timing

2) Serial data map

The serial data map is as follows.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
*	*	*	0	0	0	0	S/H phase		VD polarity	HD polarity	Supported panel	System		Input switching	
*	*	*	0	0	1	0	0	0	External VSYNC	FRP polarity	SYNC GEN	FRP256 1F inversion	Mode	Aspect	Y/color difference clamp
*	*	*	0	1	0	HD-POSITION					H-POSITION				
*	*	*	1	0	0	0	0	HUE							
*	*	*	1	0	0	0	1	COLOR							
*	*	*	1	0	0	1	0	BRIGHT							
*	*	*	1	0	0	1	1	CONTRAST							
*	*	*	1	0	1	0	0	R-BRT							
*	*	*	1	0	1	0	1	B-BRT							
*	*	*	1	0	1	1	0	$\gamma 1$							
*	*	*	1	0	1	1	1	$\gamma 2$							
*	*	*	1	1	0	0	0	PLL ADJ							

3) Serial data mode settings

- Input switching

D1	D0	
0	X	Composite input (default)
1	0	Y/C input
1	1	Y/color difference input

- System switching

D3	D2	
0	X	NTSC (default)
1	0	D-PAL
1	1	S-PAL

- Supported panel switching

D4	
0	LCX005 (default)
1	LCX009

- HD output polarity switching

D5	
0	Negative polarity (default)
1	Positive polarity

- VD1 output polarity switching

D6	
0	Negative polarity (default)
1	Positive polarity

- Sample-and-hold timing switching

D8	D7	
0	0	SHS1 (default)
0	1	SHS2
1	0	SHS3
1	1	Through (sample-and-hold not performed)

- Y/color difference clamp position switching

  This switches the position at which the R-Y and B-Y input signals are clamped during Y/color difference input mode.

D0	
0	Pedestal position (default)
1	SYNC position

- Aspect switching

D1	
0	4:3 (normal) (default)
1	16:9 (pulse eliminator WIDE)

- Mode switching

  This is the test mode. Set to normal mode.

D2	
0	Normal mode (default)
1	Test mode

• FRP256 field inversion
This further inverts the polarity of the RGB output that is inverted every 1H for 256 fields.

D3	
0	OFF (default)
1	ON

• Sync generator function
This stops the HST, VST and FRP outputs of the TG block.

D4	
0	OFF (default)
1	ON

• FRP polarity inversion function

D5	
0	ON (1H inversion) (default)
1	OFF (polarity not inverted)

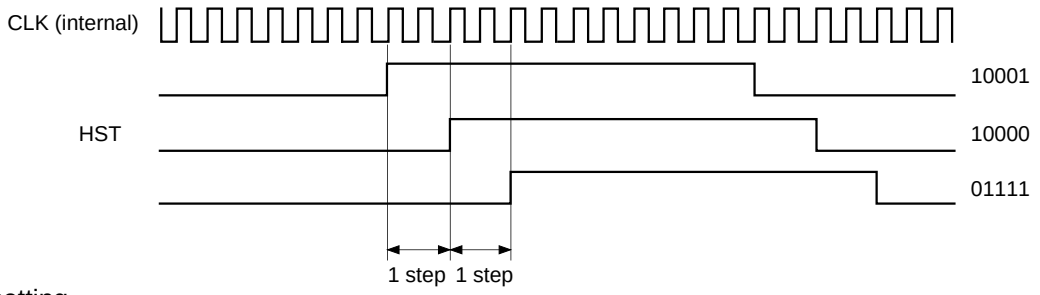
• External VSYNC input switching
Internal VSYNC separation is not performed and an externally input VSYNC is used.

D6	
0	OFF (default)
1	ON

• H position setting

D4	D3	D2	D1	D0	
0	0	0	0	0	
to	to	to	to	to	
1	0	0	0	0	(default)
to	to	to	to	to	
1	1	1	1	1	

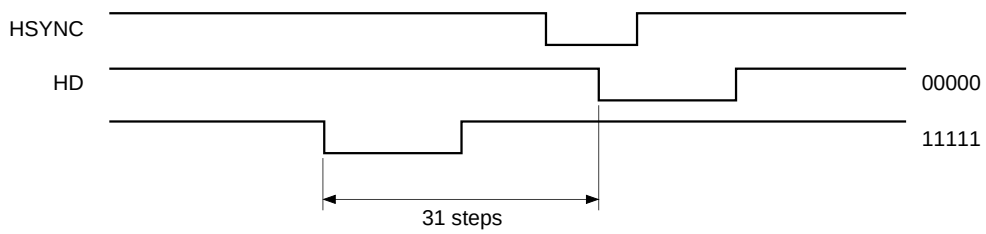
Variable in $2f_H$ (= 1 bit) increments



• HD phase setting

D9	D8	D7	D6	D5	
0	0	0	0	0	(default)
to	to	to	to	to	
1	1	1	1	1	

Variable in $4f_H$ (= 1 bit) increments



4) Serial data electronic attenuator (D/A converter) settings

• HUE

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	0	0 (default)

• COLOR

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	0	0 (default)

• BRIGHT

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	0	0 (default)

• CONTRAST

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	0	0 (default)

• R-BRT

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	0	0 (default)

• B-BRT

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	0	0 (default)

• γ-1

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0 (default)

• γ-2

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0 (default)

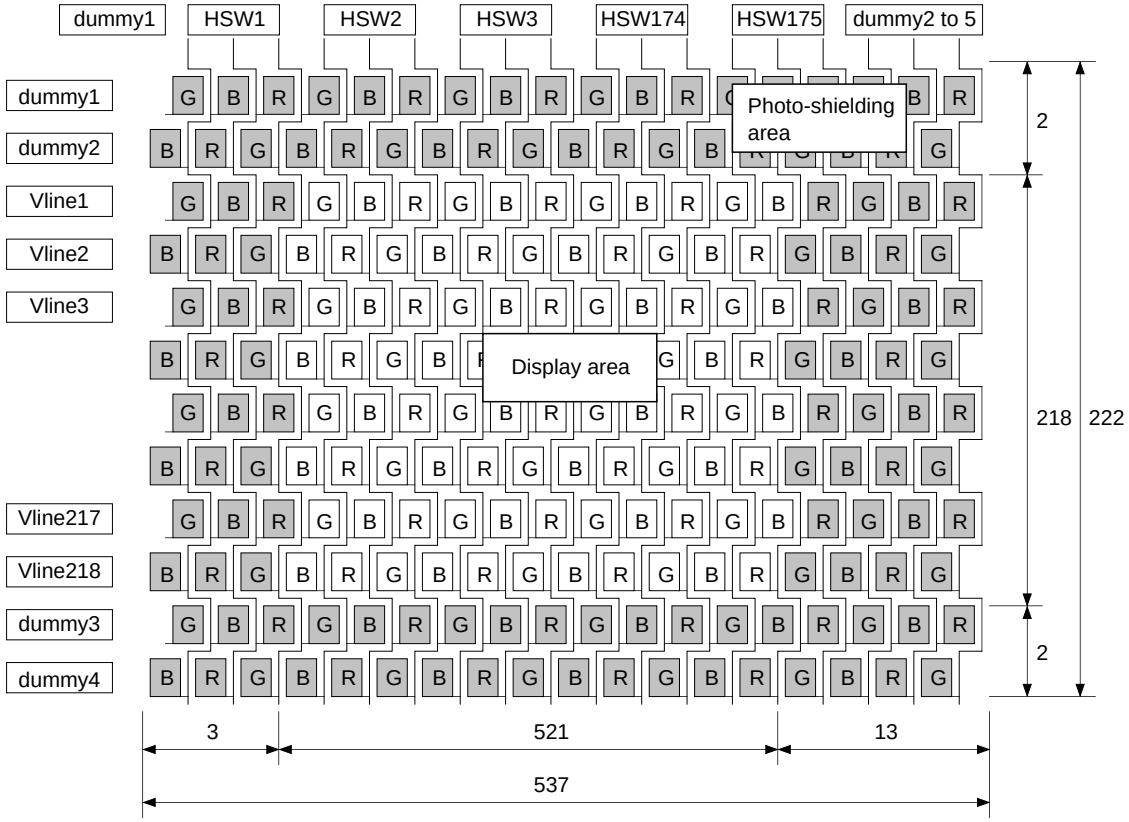
• PLL-ADJ

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	0	0	0	0 (default)

LCX005BK/BKB and LCX009AK/AKB Color Coding Diagram

The delta arrangement is used for the color coding in the LCD panels with which this IC is compatible. Note that the shaded region within the diagram is not displayed.

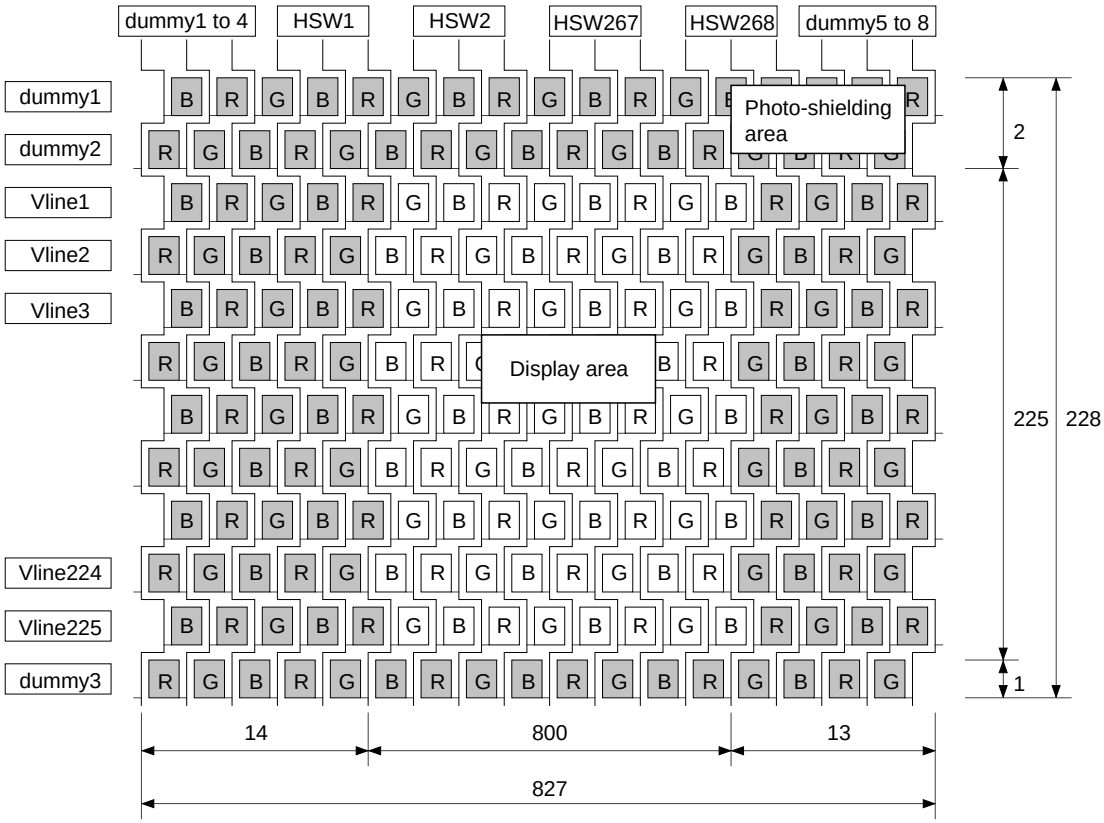
LCX005BK/BKB pixel arrangement



Basic specifications

Total horizontal dots:	537H
Horizontal display dots:	521H
Total vertical dots:	222H
Vertical display dots:	218H
Total dots:	119,214H
Display dots:	113,578H

LCX009AK/AKB pixel arrangement



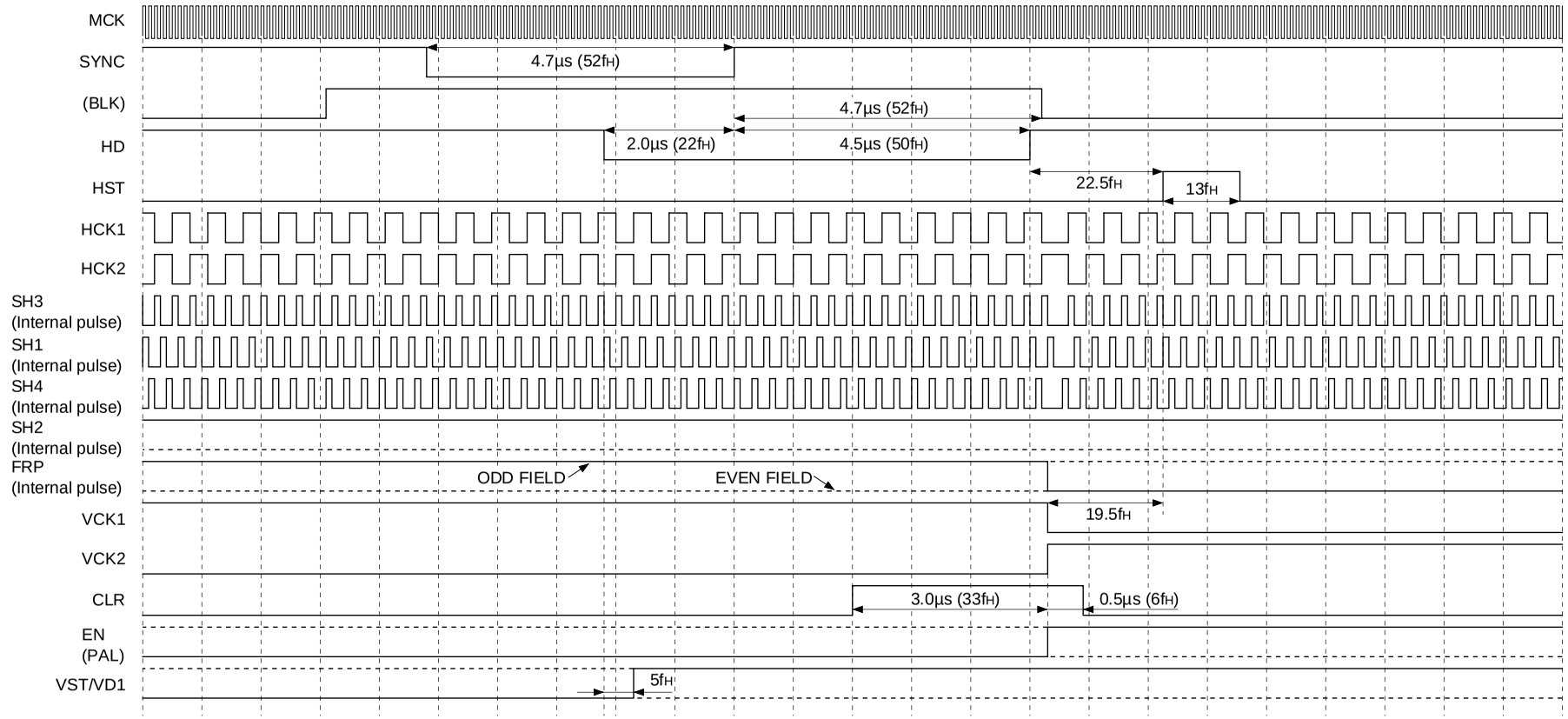
Basic specifications

Total horizontal dots:	827H
Horizontal display dots:	800H
Total vertical dots:	228H
Vertical display dots:	225H
Total dots:	188,556H
Display dots:	180,000H

LCX005BK/BKB Horizontal Direction Timing Chart

NTSC/PAL

Unless otherwise specified, serial settings are the default values.
RGT: H (Normal scan)
702f_H

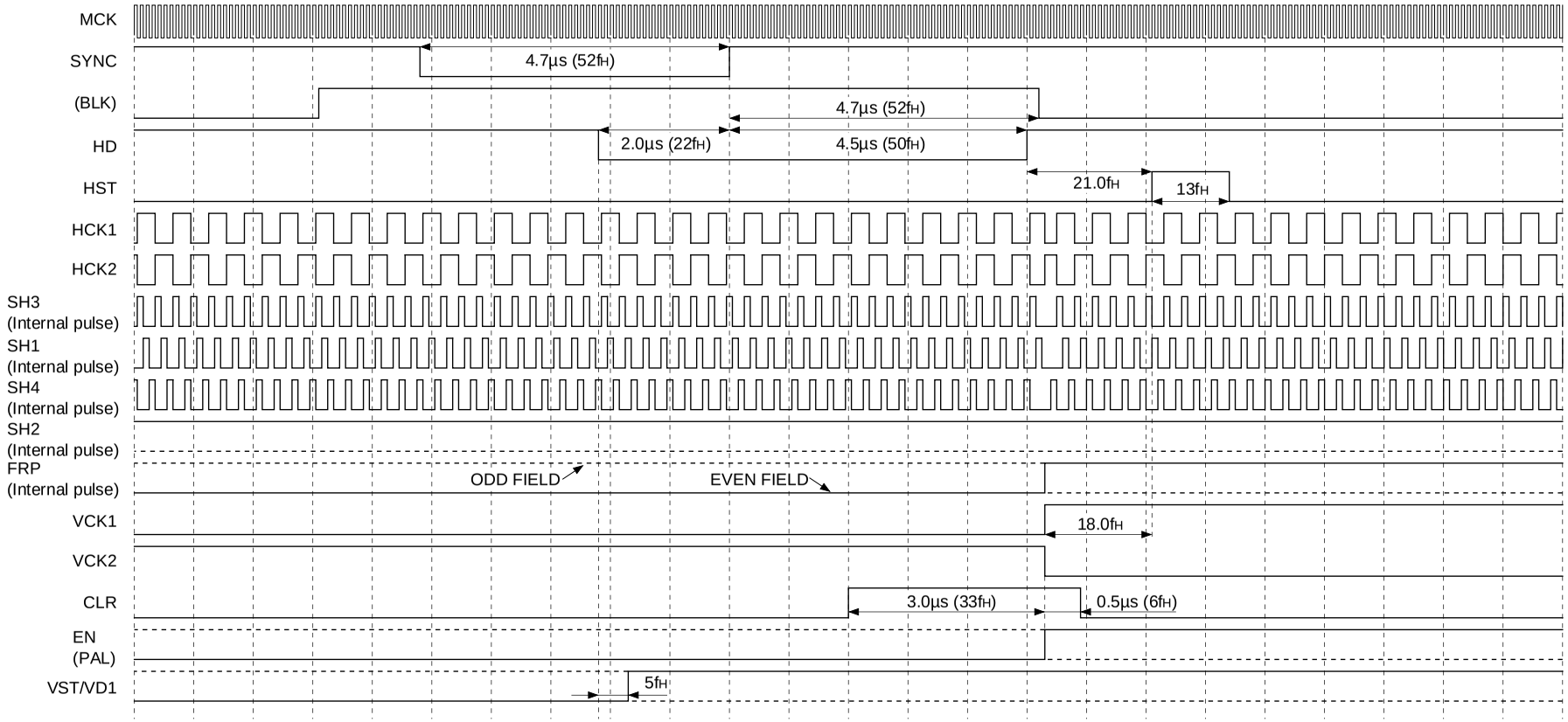


Note) The third row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

LCX005BK/BKB Horizontal Direction Timing Chart

NTSC/PAL

Unless otherwise specified, serial settings are the default values.
RGT: H (Normal scan)
702fH



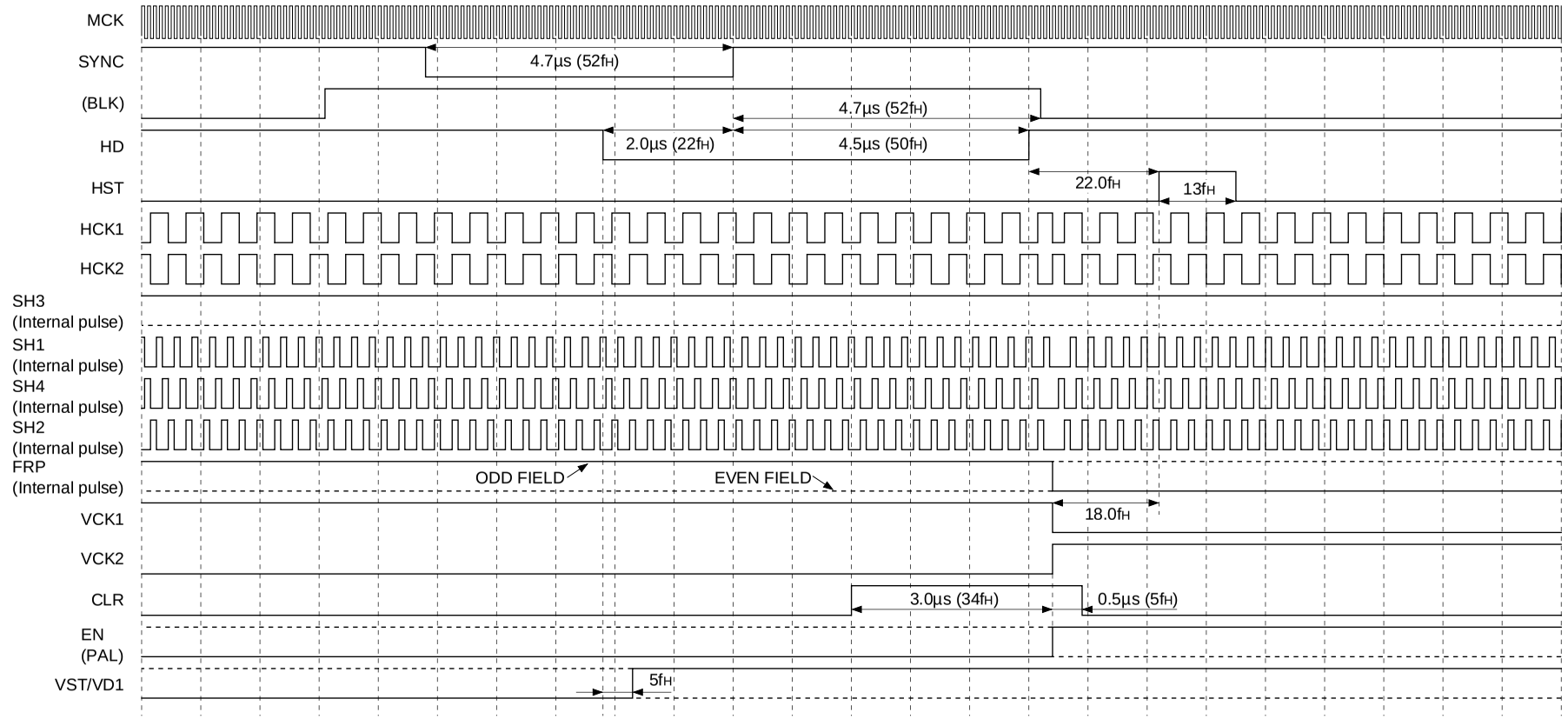
EVEN LINE

Note) The third row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

LCX005BK/BKB Horizontal Direction Timing Chart

NTSC/PAL

Unless otherwise specified, serial settings are the default values.
RGT: L (Reverse scan)
702f_H



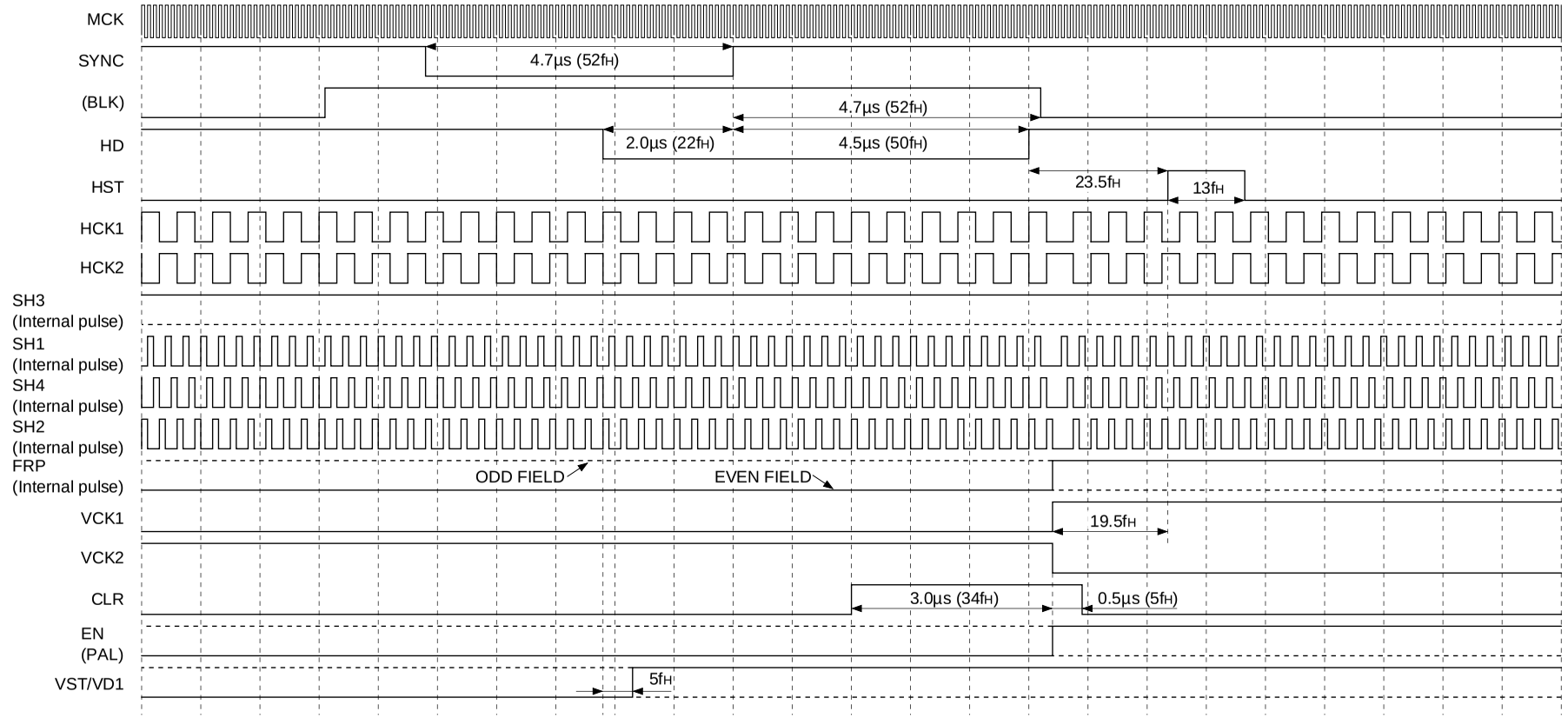
ODD LINE

Note) The third row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

LCX005BK/BKB Horizontal Direction Timing Chart

NTSC/PAL

Unless otherwise specified, serial settings are the default values.
RGT: L (Reverse scan)
702fH



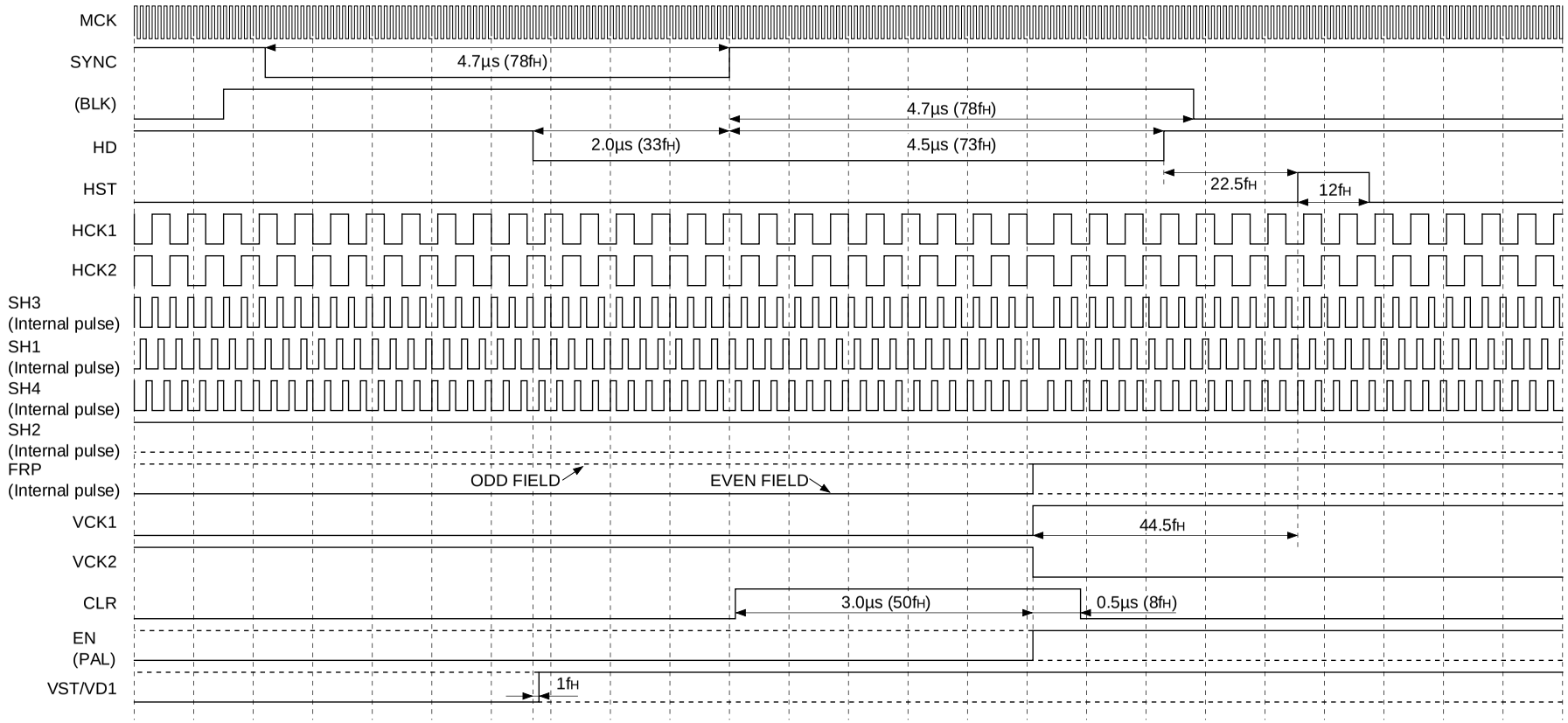
EVEN LINE

Note) The third row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

LCX009AK/AKB Horizontal Direction Timing Chart

NTSC/PAL

Unless otherwise specified, serial settings are the default values.
RGT: H (Normal scan)
1050f_H



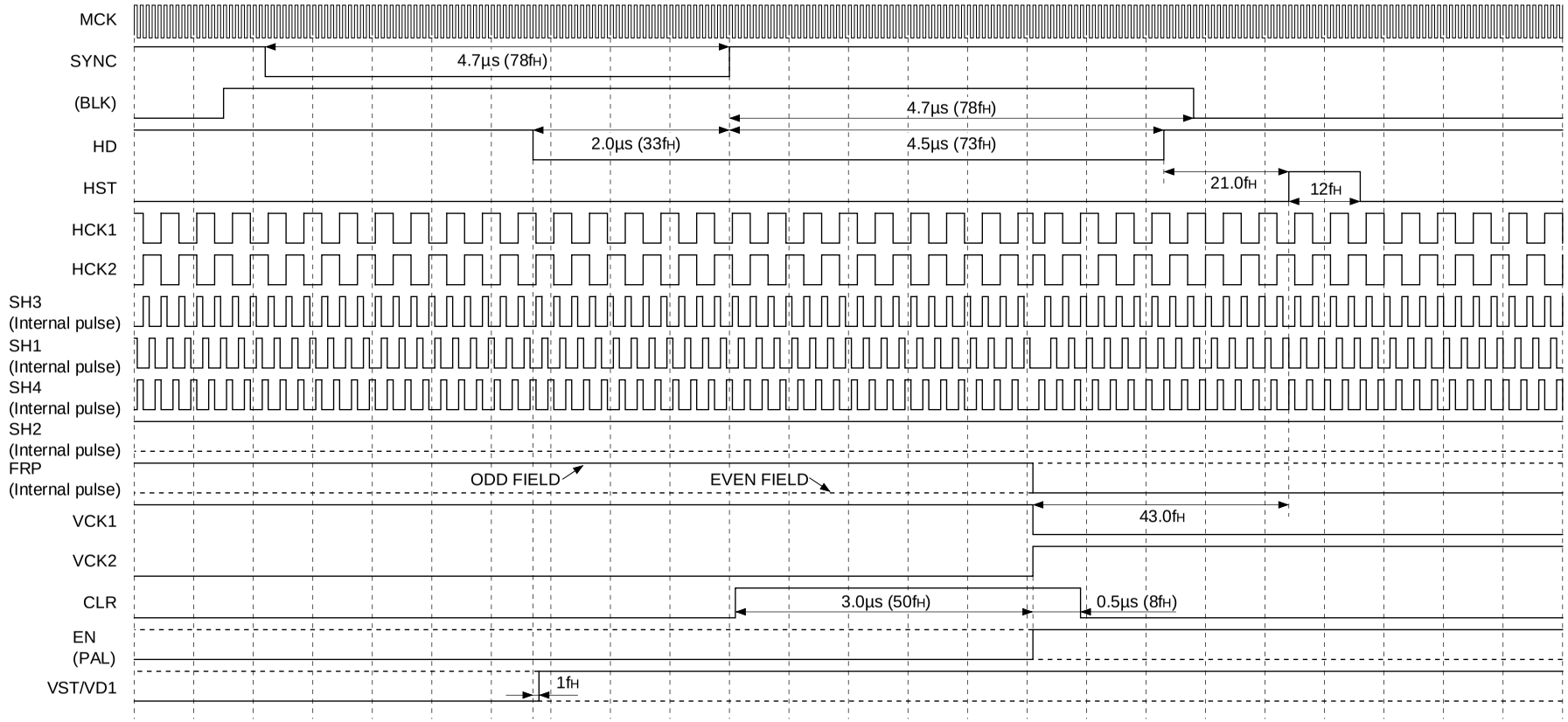
ODD LINE

Note) The third row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

LCX009AK/AKB Horizontal Direction Timing Chart

NTSC/PAL

Unless otherwise specified, serial settings are the default values.
RGT: H (Normal scan)
1050f_H



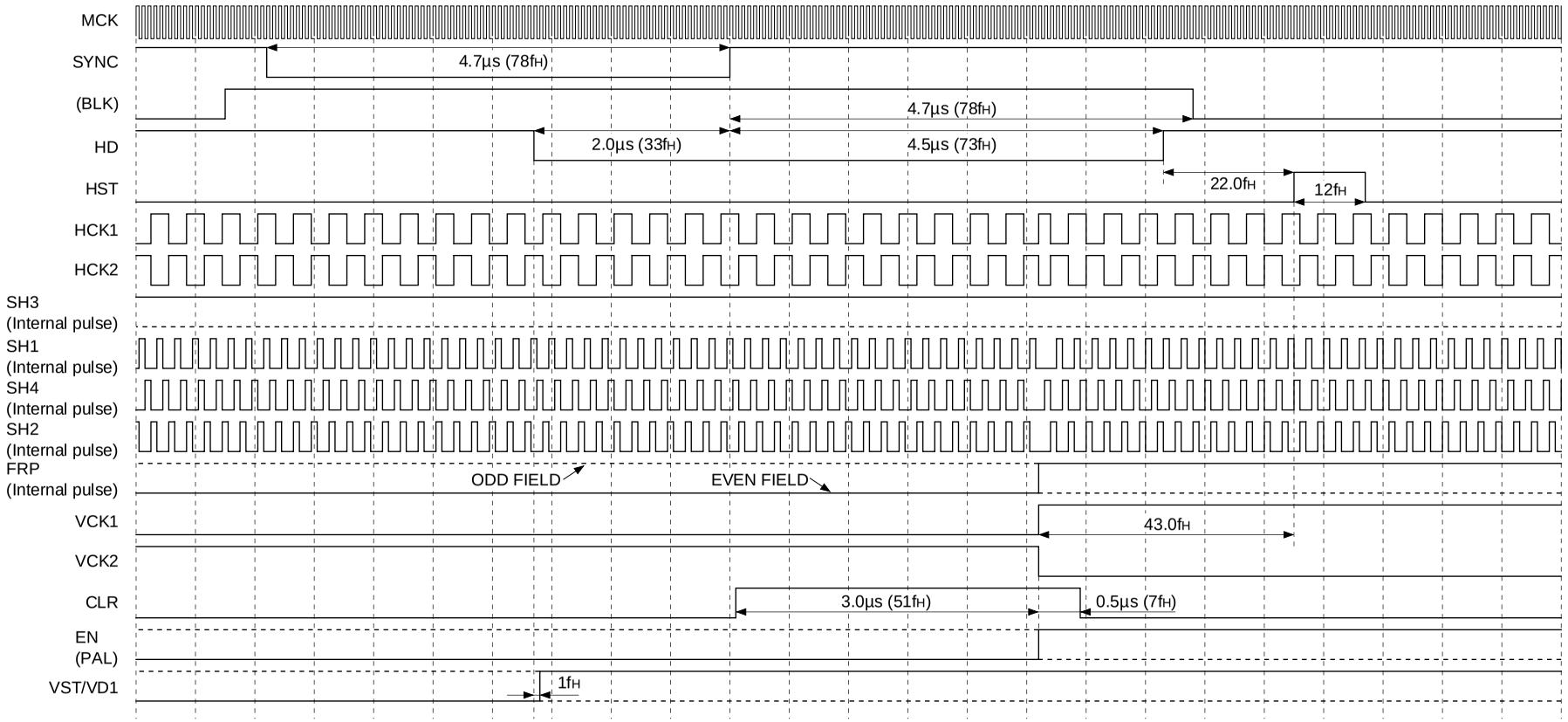
EVEN LINE

Note) The third row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

LCX009AK/AKB Horizontal Direction Timing Chart

NTSC/PAL

Unless otherwise specified, serial settings are the default values.
RGT: L (Reverse scan)
1050f_H

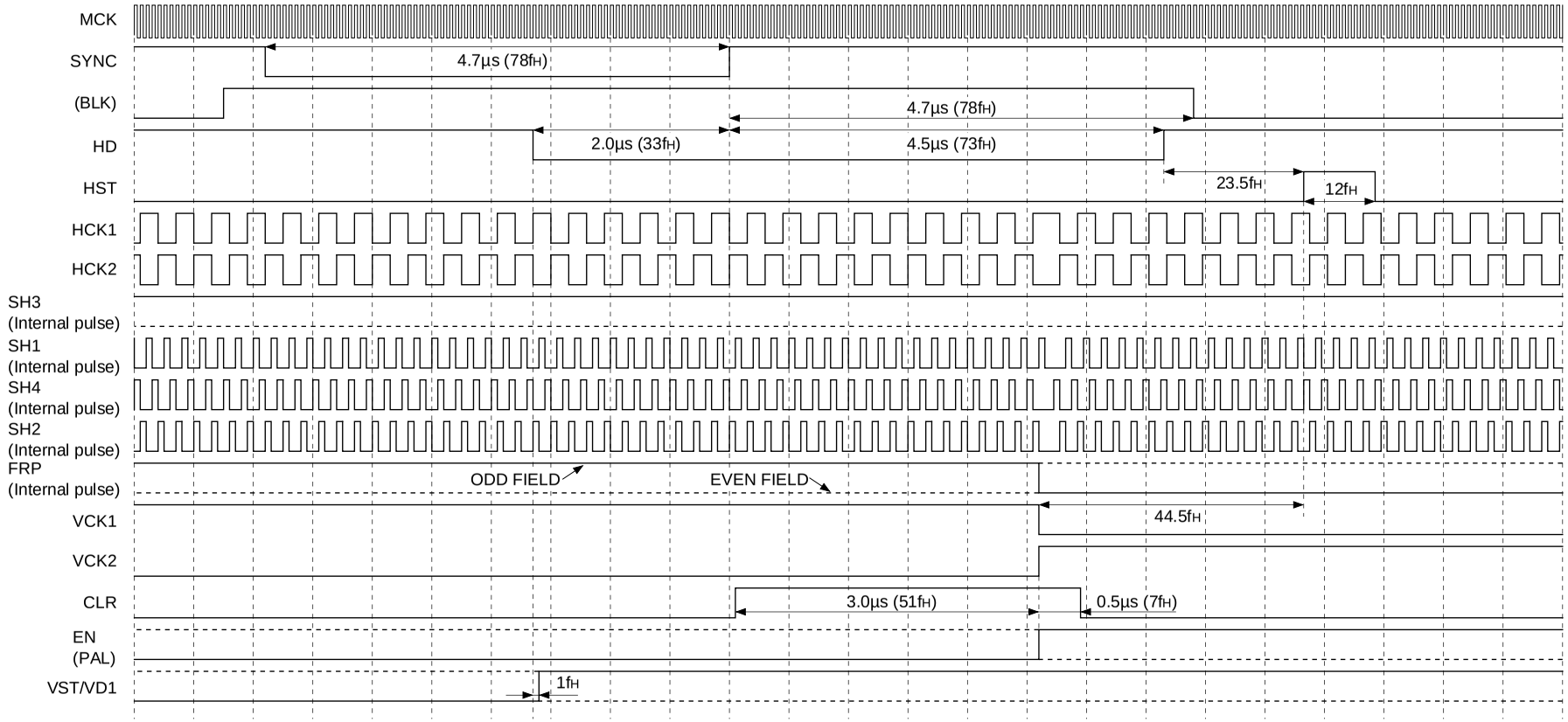


Note) The third row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

LCX009AK/AKB Horizontal Direction Timing Chart

NTSC/PAL

Unless otherwise specified, serial settings are the default values.
RGT: L (Reverse scan)
1050f_H

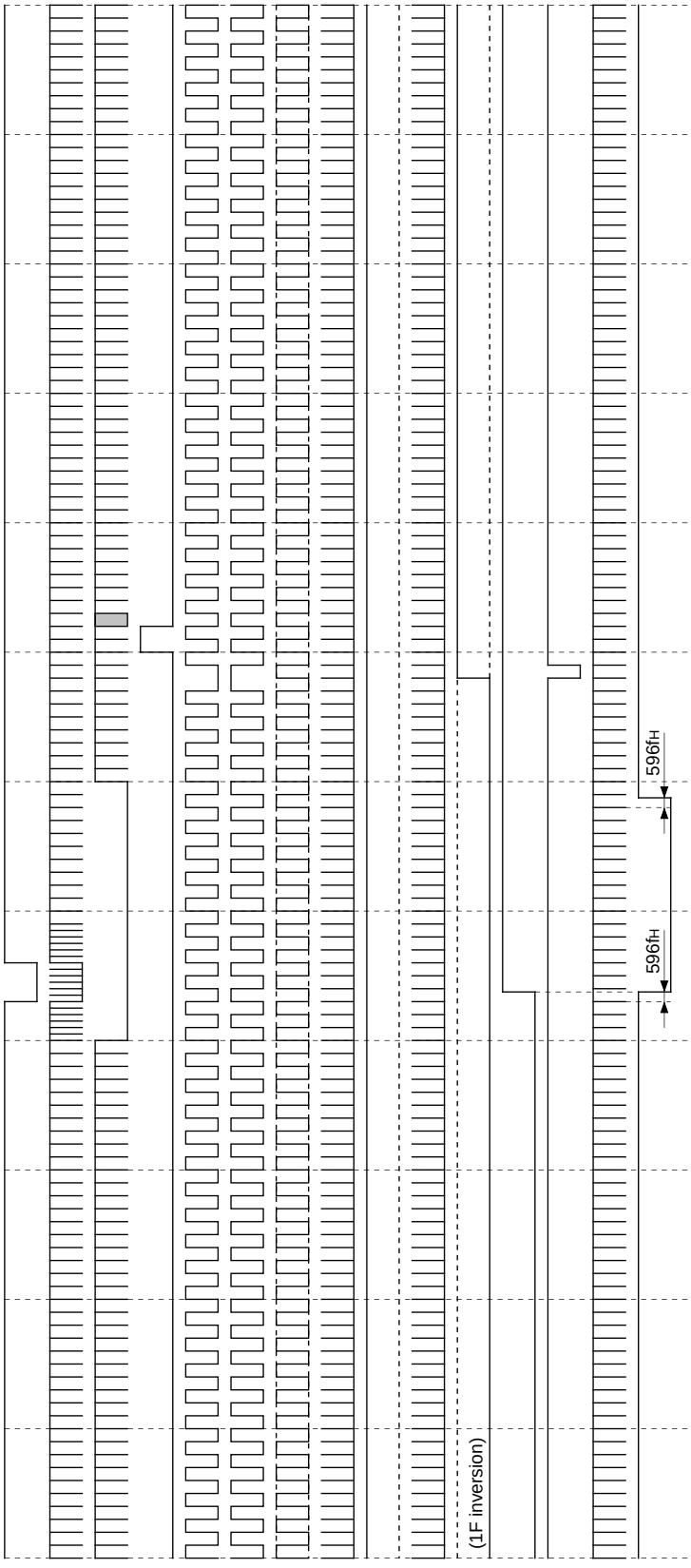


EVEN LINE

Note) The third row of the timing chart "BLK" is a pulse indicated as a reference and is not a pulse output from pins.
FRP polarity is not specified for each line and field.

LCX005BK/BKB Vertical Direction Timing Chart

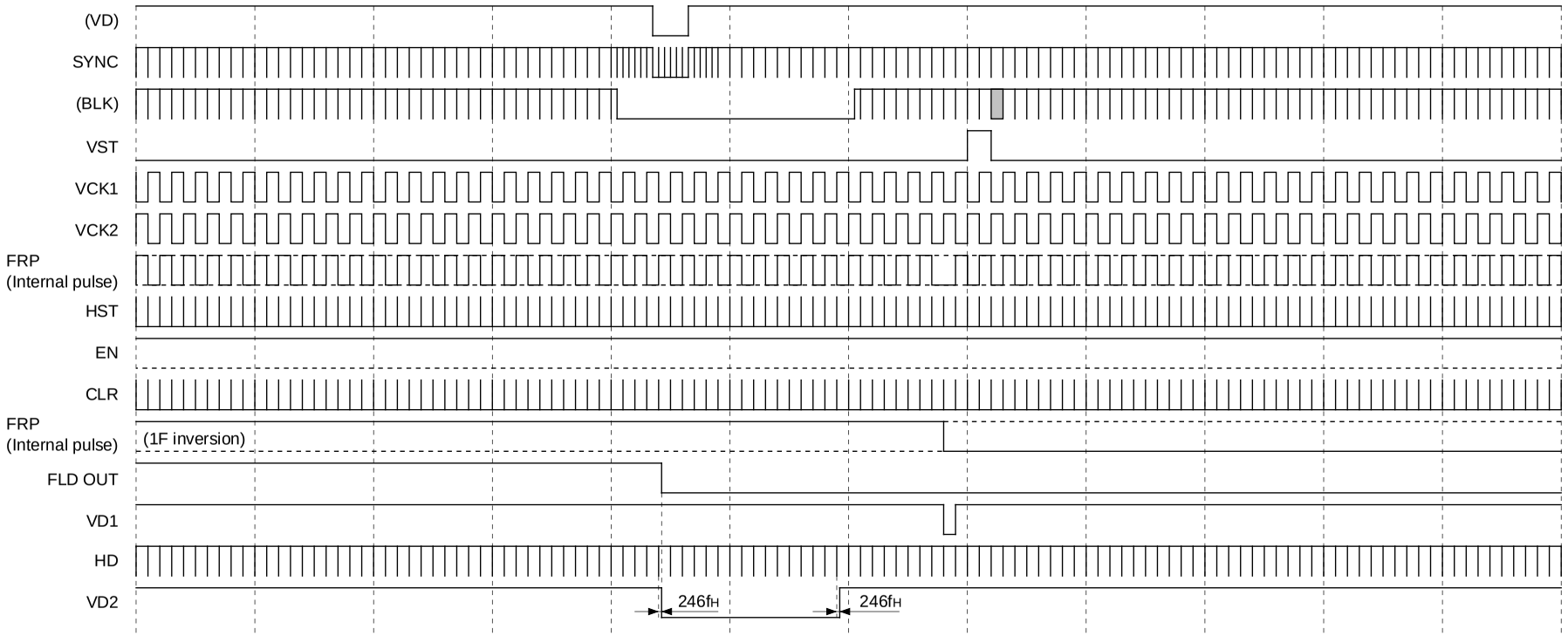
NTSC



Note) The first and third rows of the timing chart "VD" and "BLK", respectively, are pulses indicated as a reference and are not pulses output from pins.
FRP polarity is not specified for each line and field.

LCX005BK/BKB Vertical Direction Timing Chart

NTSC

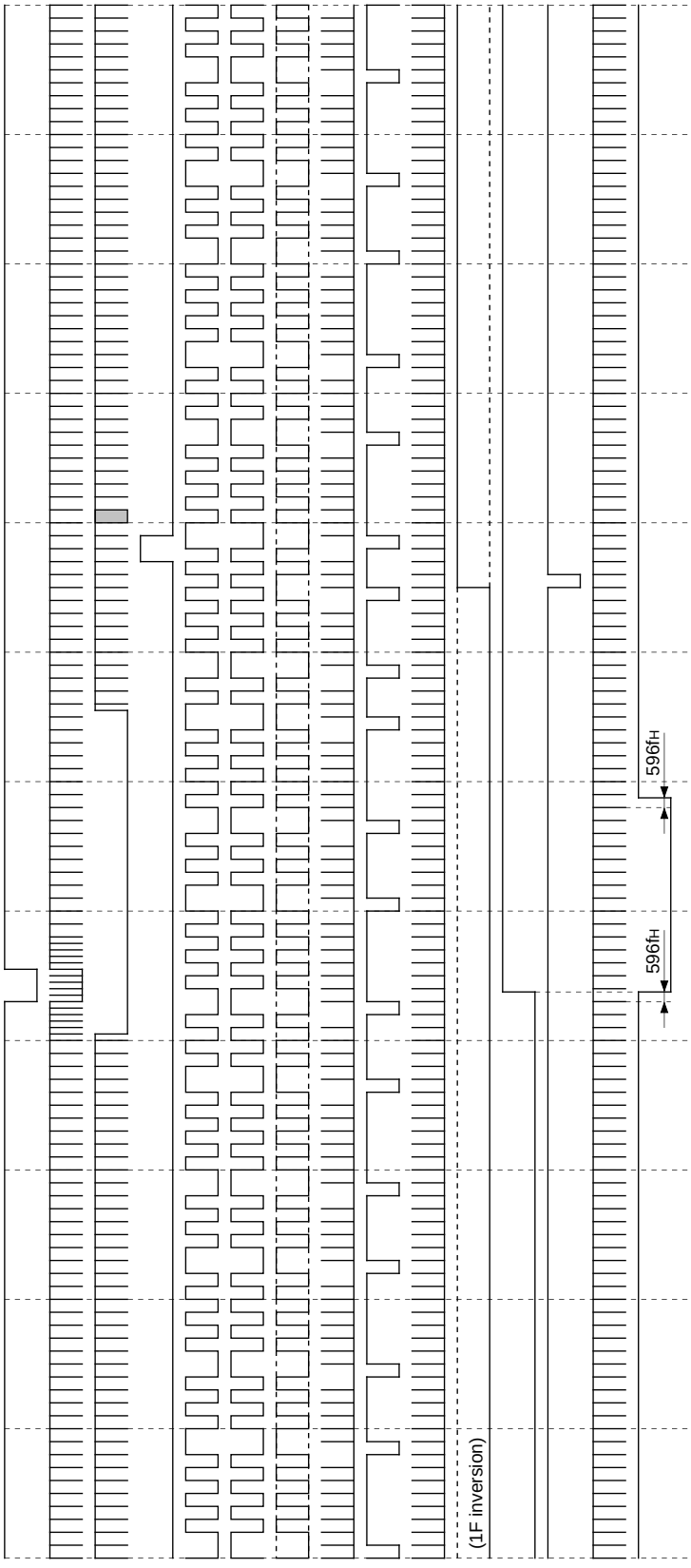


EVEN FIELD

Note) The first and third rows of the timing chart "VD" and "BLK", respectively, are pulses indicated as a reference and are not pulses output from pins.
FRP polarity is not specified for each line and field.

LCX005BK/BKB Vertical Direction Timing Chart

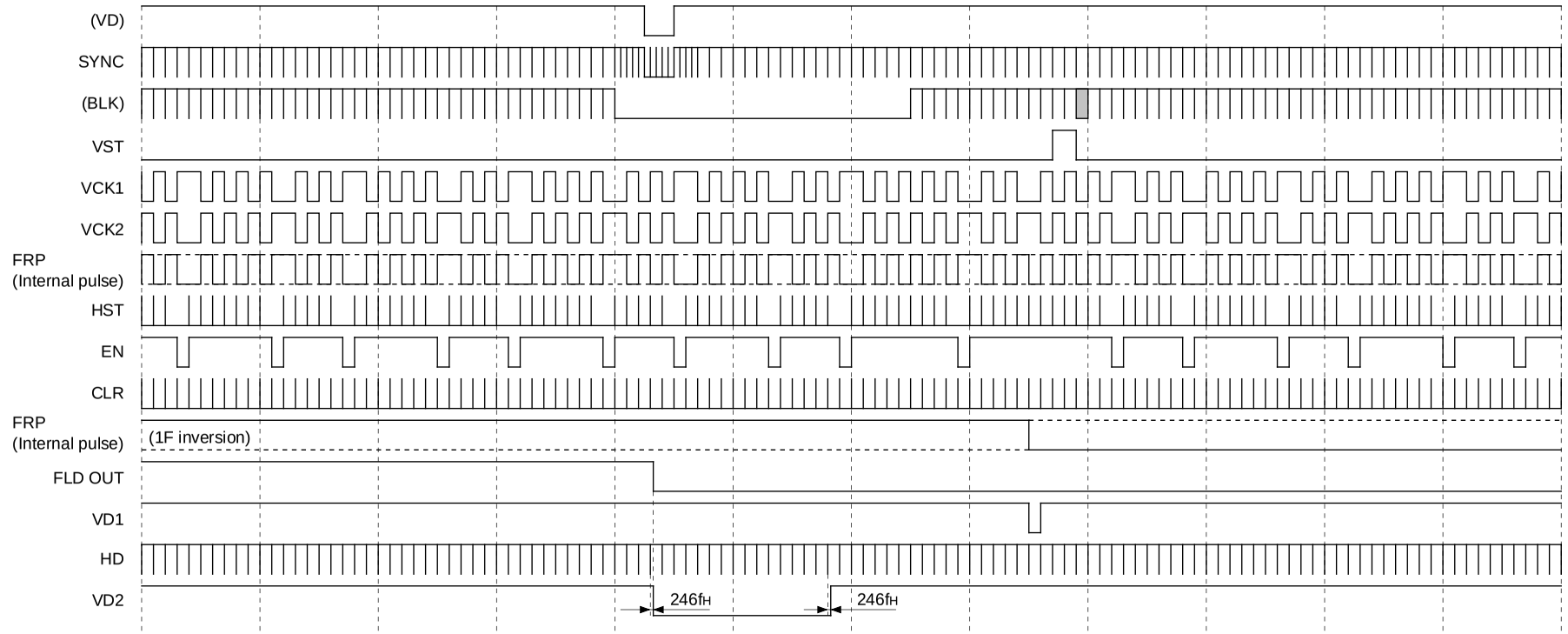
PAL



Note) The first and third rows of the timing chart "VD" and "BLK", respectively, are pulses indicated as a reference and are not pulses output from pins.
FRP polarity is not specified for each line and field.

LCX005BK/BKB Vertical Direction Timing Chart

PAL

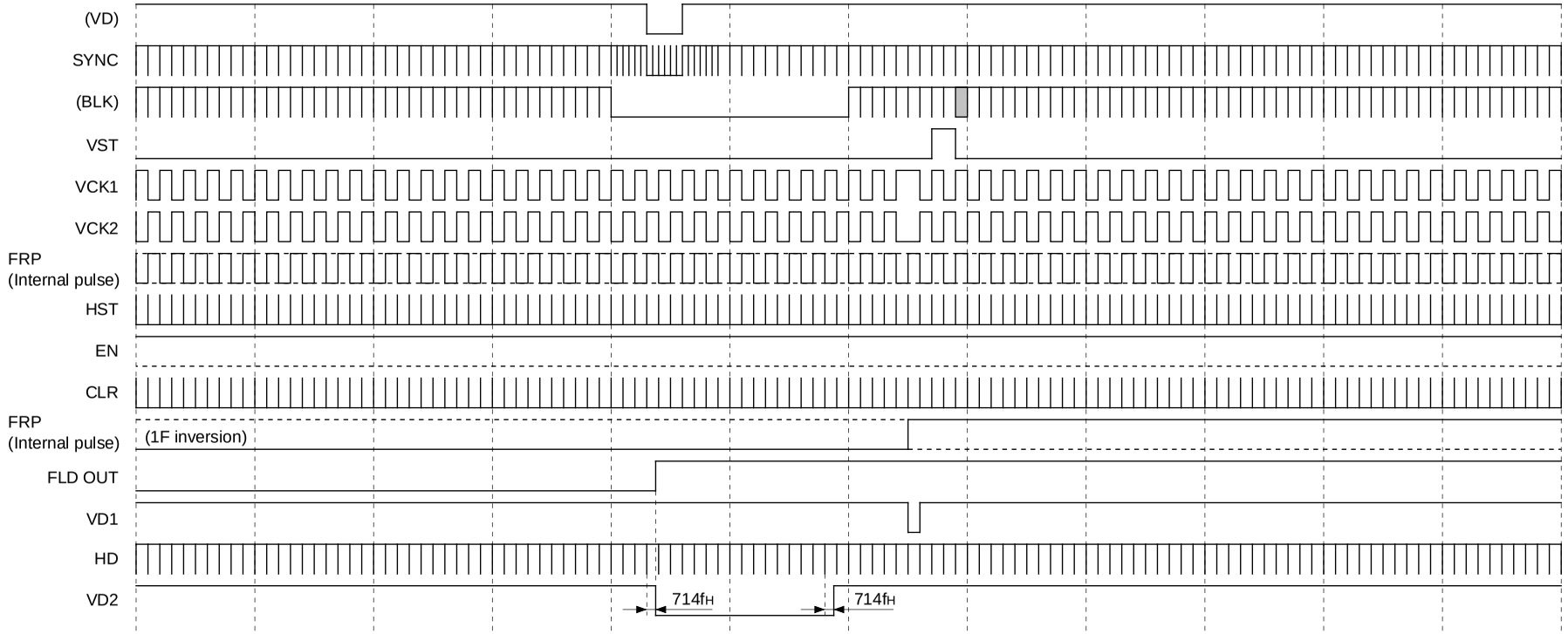


EVEN FIELD

Note) The first and third rows of the timing chart "VD" and "BLK", respectively, are pulses indicated as a reference and are not pulses output from pins.
FRP polarity is not specified for each line and field.

LCX009AK/AKB Vertical Direction Timing Chart

NTSC

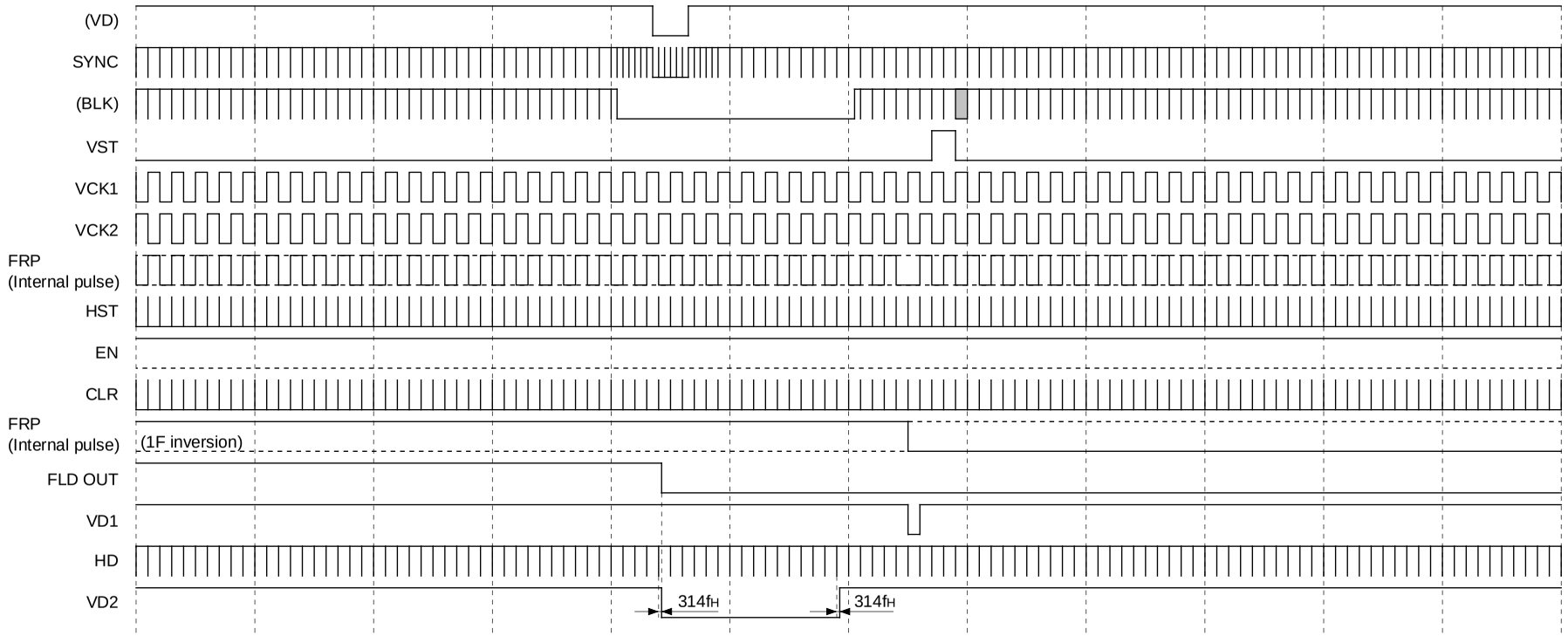


ODD FIELD

Note) The first and third rows of the timing chart "VD" and "BLK", respectively, are pulses indicated as a reference and are not pulses output from pins.
FRP polarity is not specified for each line and field.

LCX009AK/AKB Vertical Direction Timing Chart

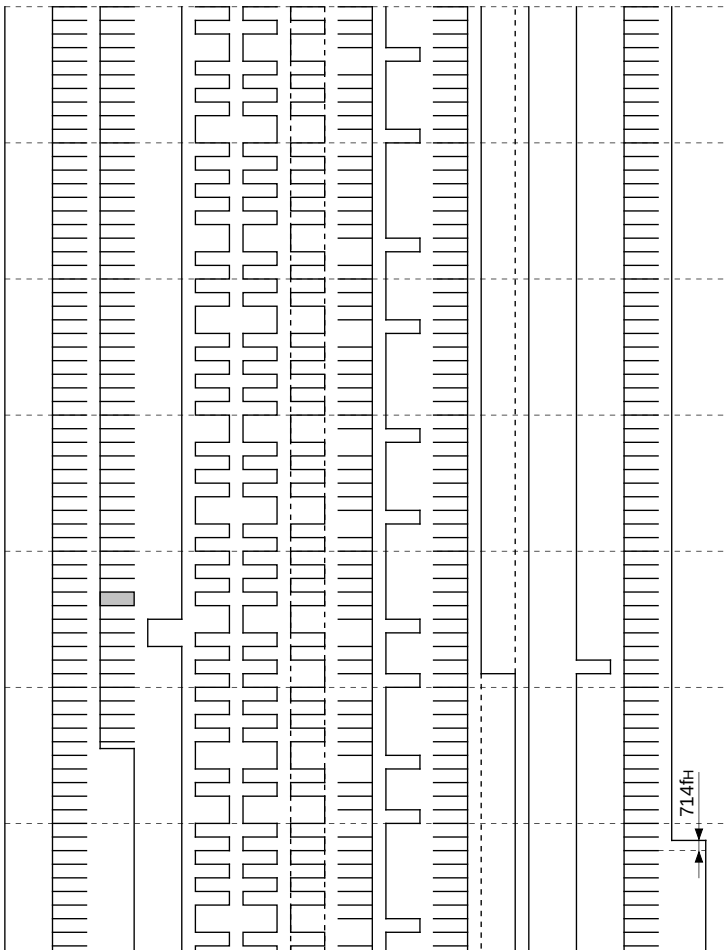
NTSC



EVEN FIELD

Note) The first and third rows of the timing chart "VD" and "BLK", respectively, are pulses indicated as a reference and are not pulses output from pins.
FRP polarity is not specified for each line and field.

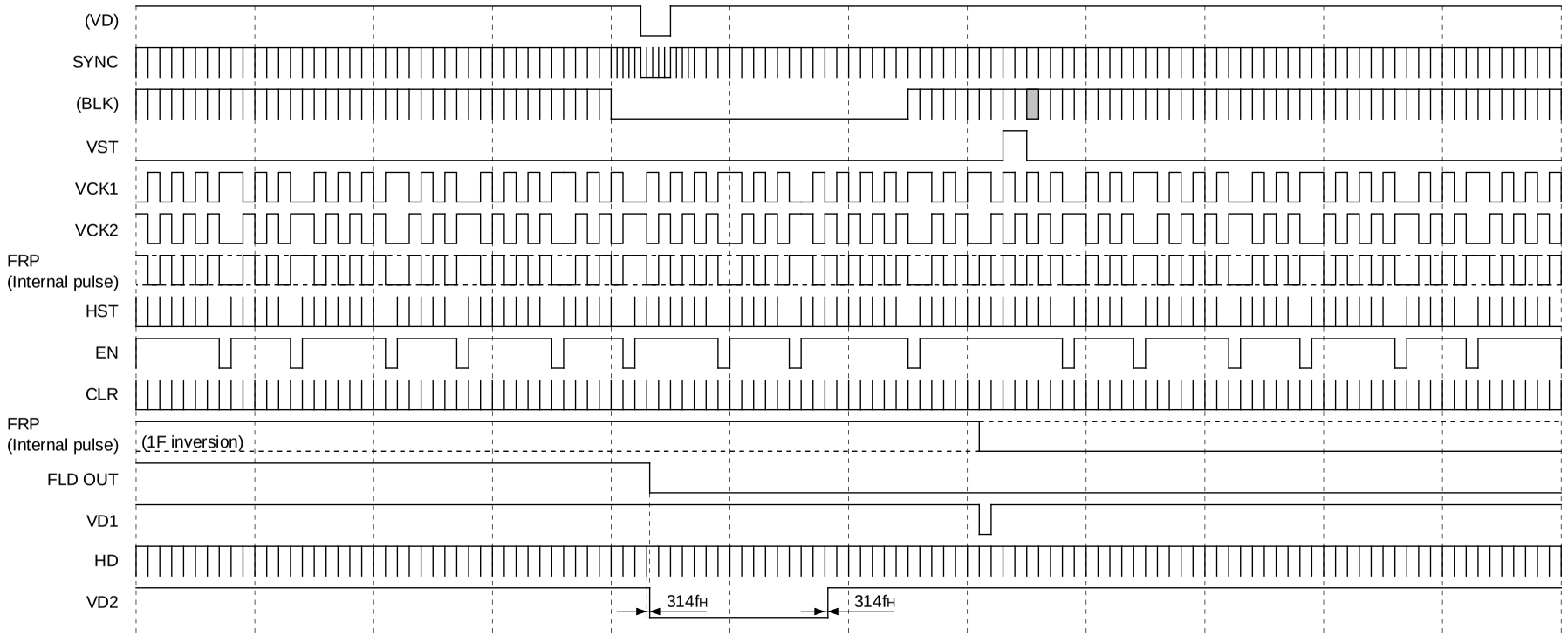
LCX009AK/AKB Vertical Direction Timing Chart
PAL



Note) The first and third rows of the timing chart "VD" and "BLK", respectively, are pulses indicated as a reference and are not pulses output from pins.
FRP polarity is not specified for each line and field.

LCX009AK/AKB Vertical Direction Timing Chart

PAL



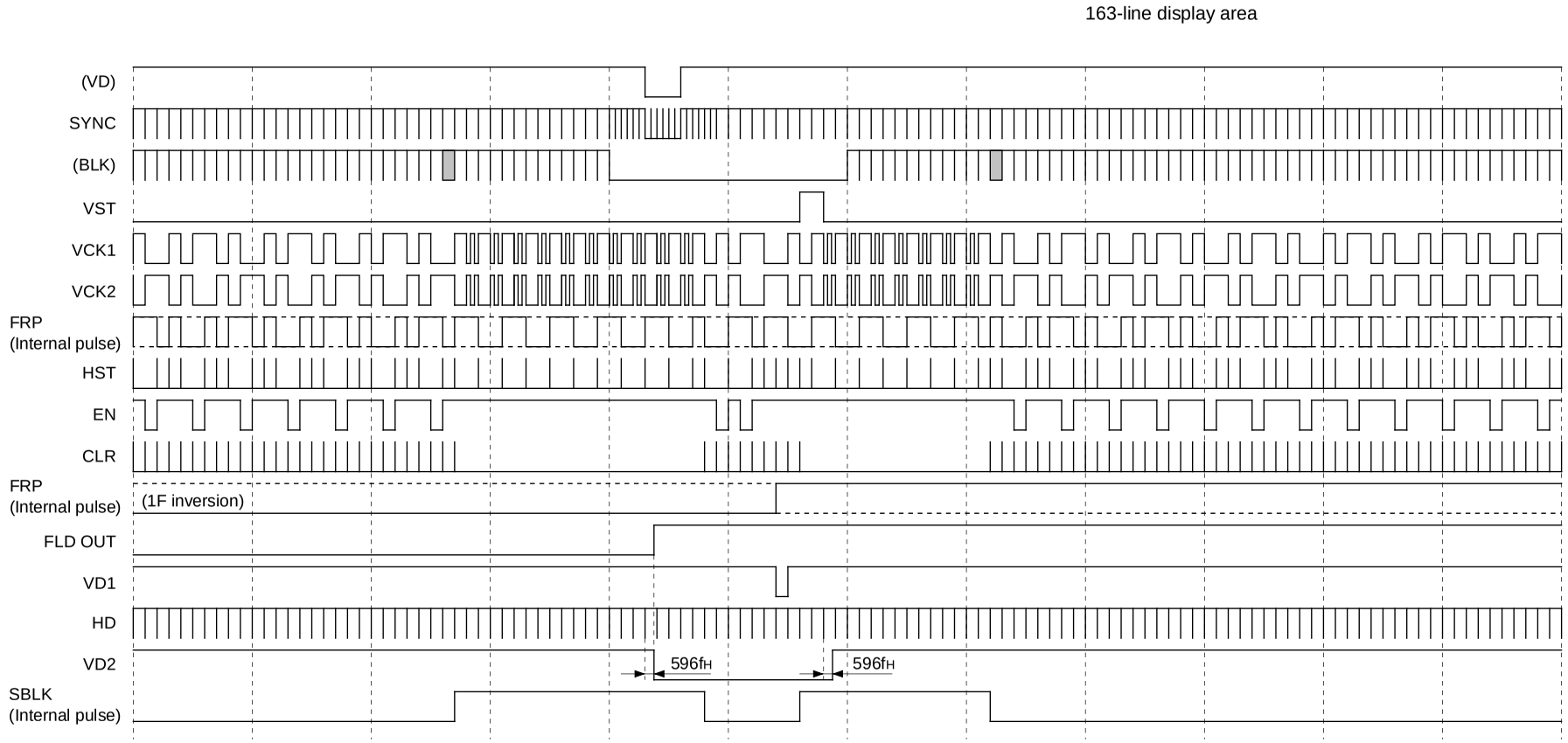
EVEN FIELD

Note) The first and third rows of the timing chart "VD" and "BLK", respectively, are pulses indicated as a reference and are not pulses output from pins.
FRP polarity is not specified for each line and field.

LCX005BK/BKB Vertical Direction Timing Chart

NTSC WIDE

1/4 pulse elimination



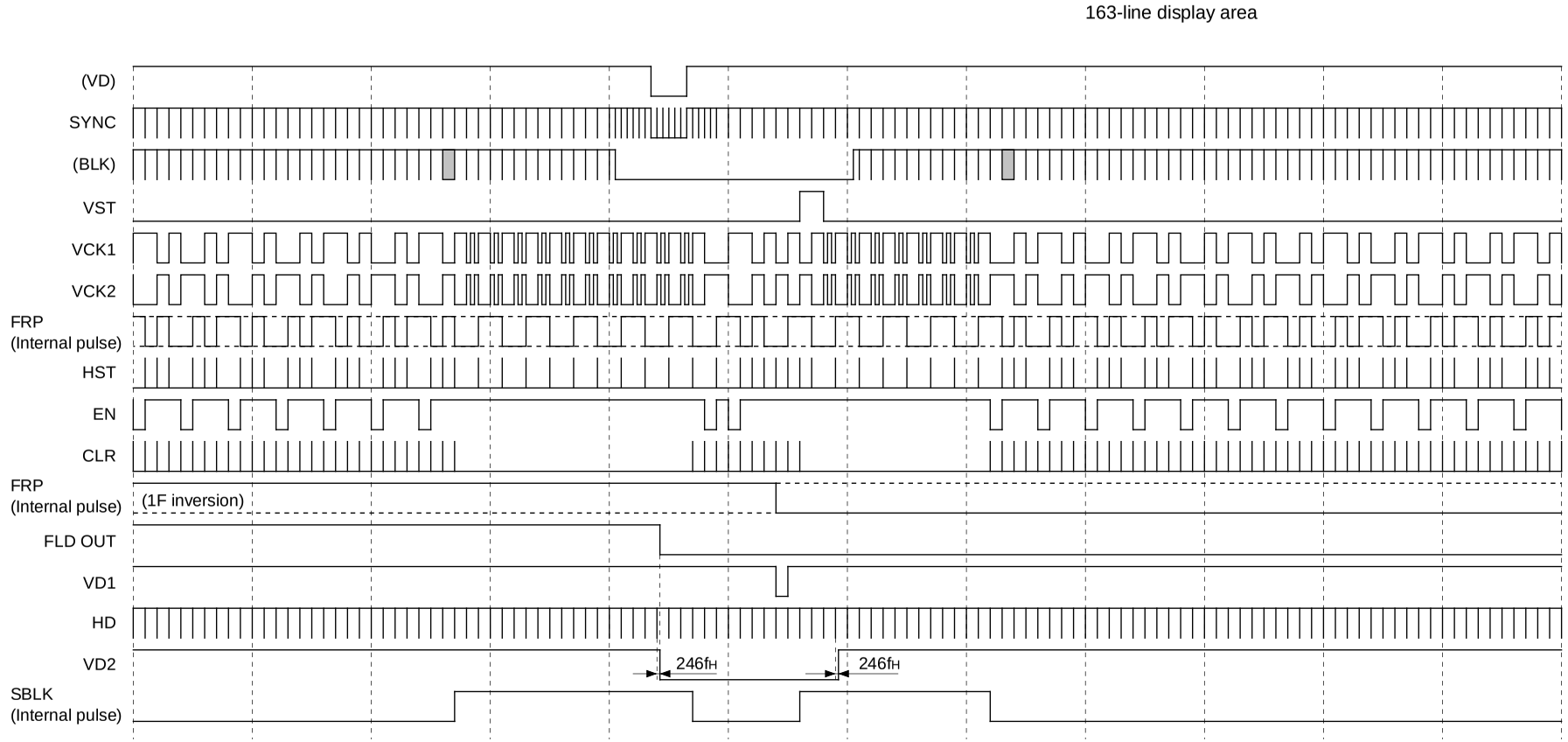
ODD FIELD

Note) The first and third rows of the timing chart "VD" and "BLK", respectively, are pulses indicated as a reference and are not pulses output from pins.
FRP polarity is not specified for each line and field.

LCX005BK/BKB Vertical Direction Timing Chart

NTSC WIDE

1/4 pulse elimination

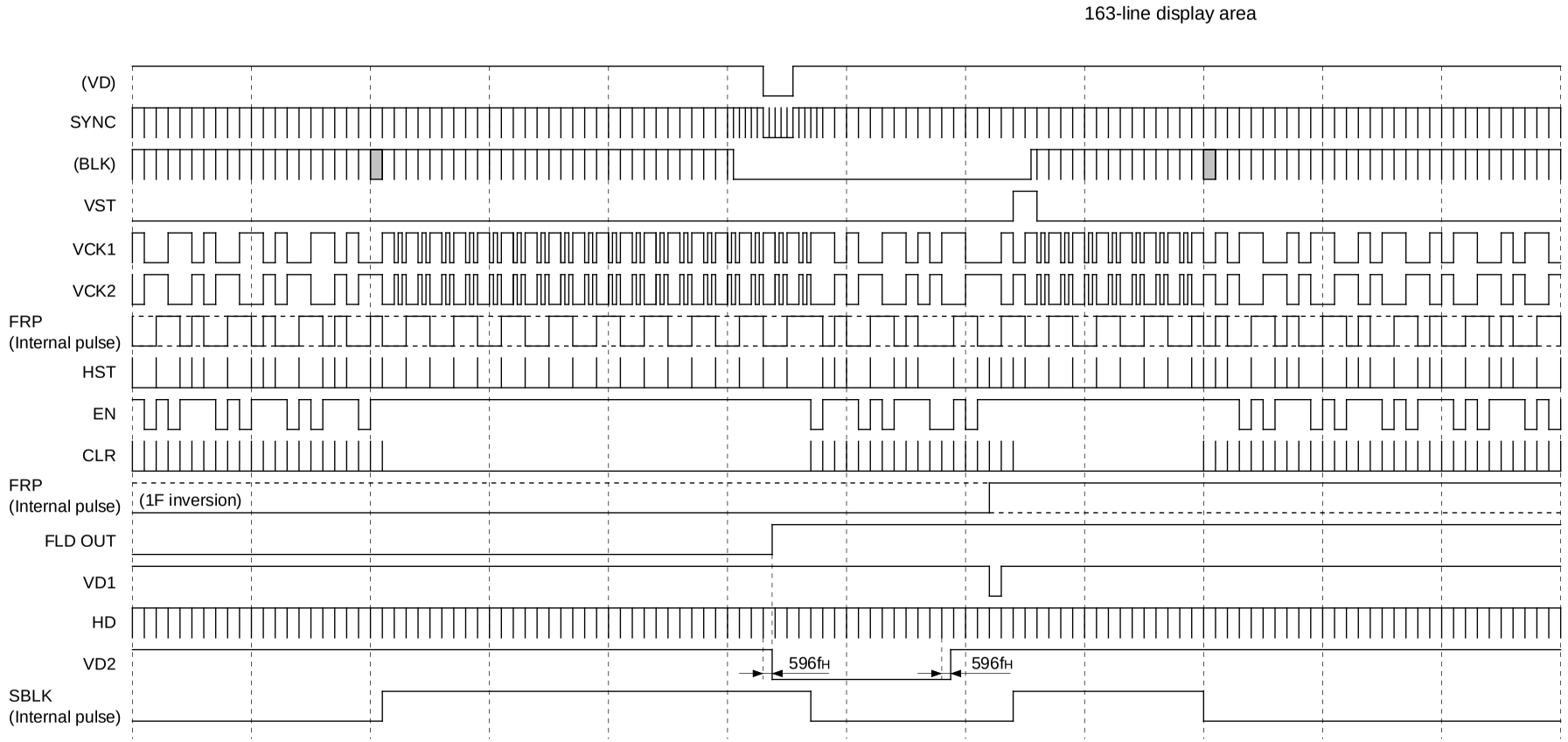


EVEN FIELD

Note) The first and third rows of the timing chart "VD" and "BLK", respectively, are pulses indicated as a reference and are not pulses output from pins.
FRP polarity is not specified for each line and field.

LCX005BK/BKB Vertical Direction Timing Chart

PAL WIDE

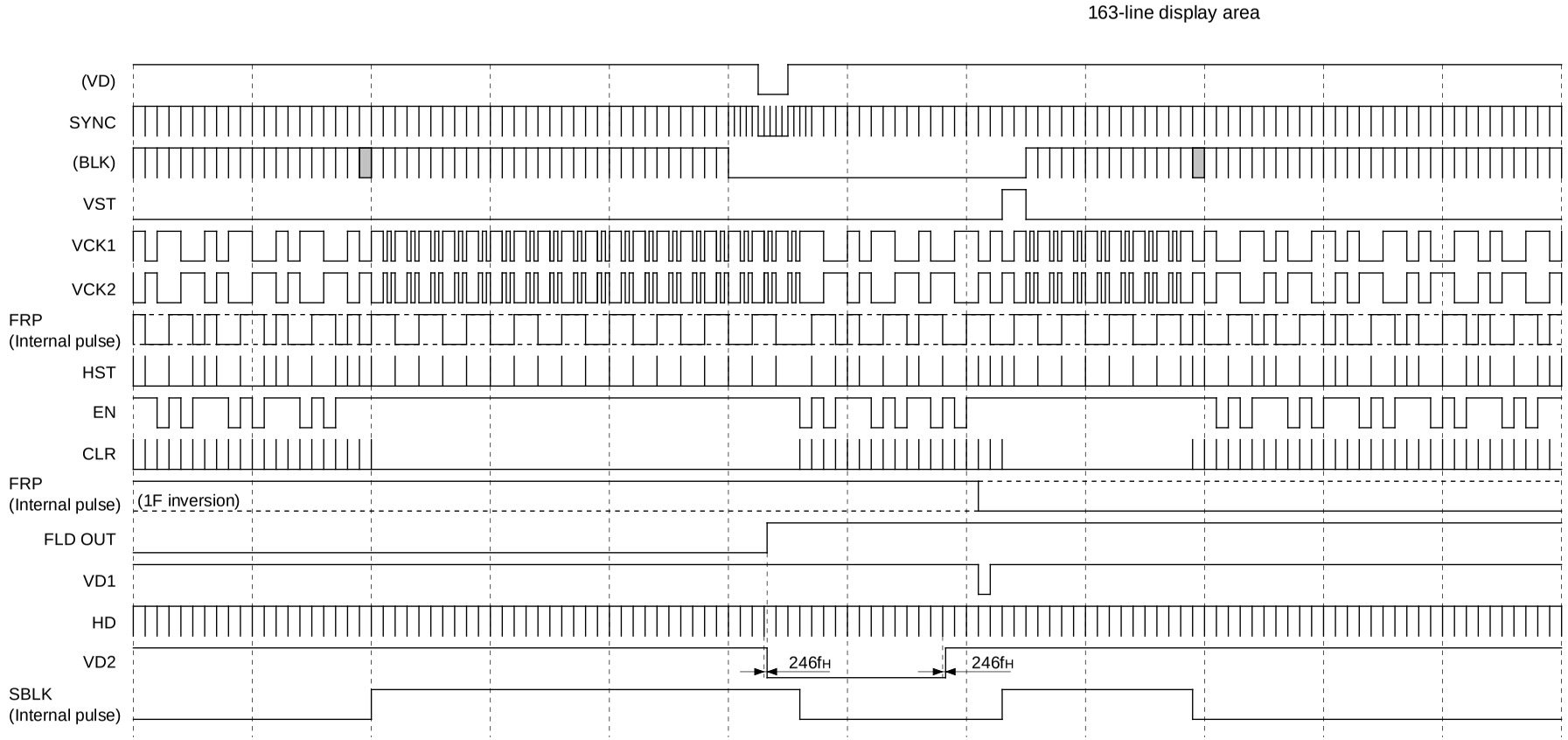


ODD FIELD

Note) The first and third rows of the timing chart "VD" and "BLK", respectively, are pulses indicated as a reference and are not pulses output from pins.
FRP polarity is not specified for each line and field.

LCX005BK/BKB Vertical Direction Timing Chart

PAL WIDE



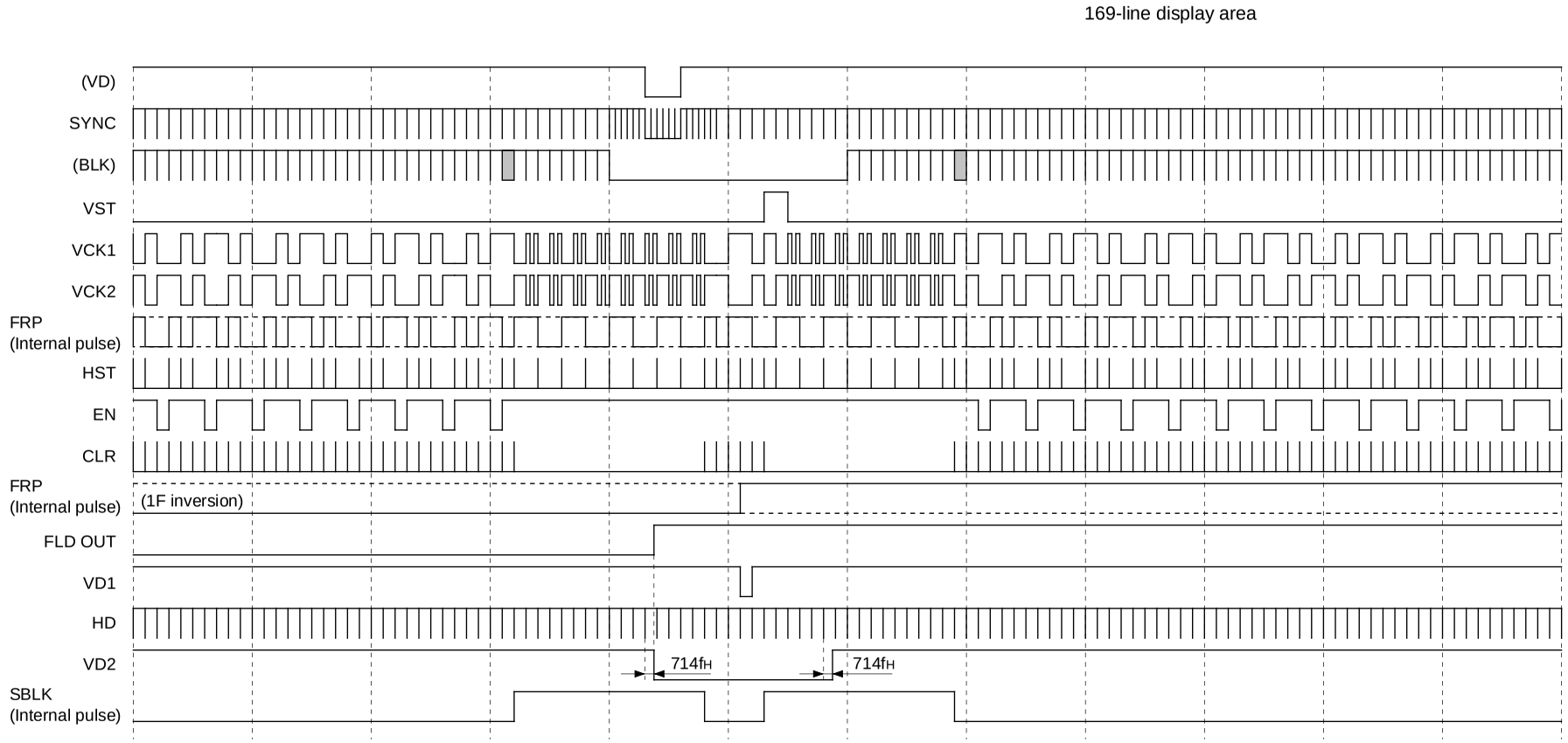
EVEN FIELD

Note) The first and third rows of the timing chart "VD" and "BLK", respectively, are pulses indicated as a reference and are not pulses output from pins.
FRP polarity is not specified for each line and field.

LCX009AK/AKB Vertical Direction Timing Chart

1/4 pulse elimination

NTSC WIDE



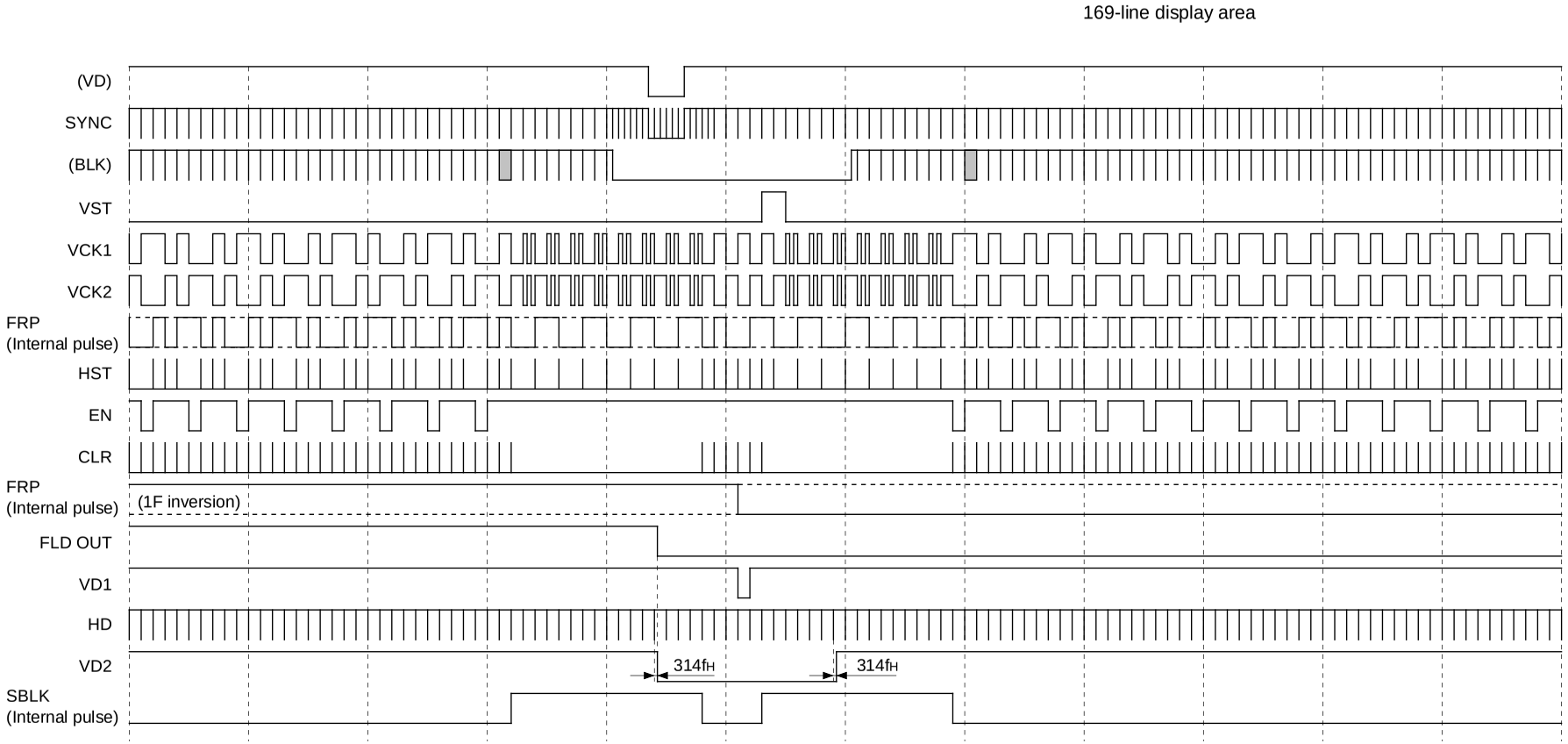
ODD FIELD

Note) The first and third rows of the timing chart "VD" and "BLK", respectively, are pulses indicated as a reference and are not pulses output from pins.
FRP polarity is not specified for each line and field.

LCX009AK/AKB Vertical Direction Timing Chart

1/4 pulse elimination

NTSC WIDE

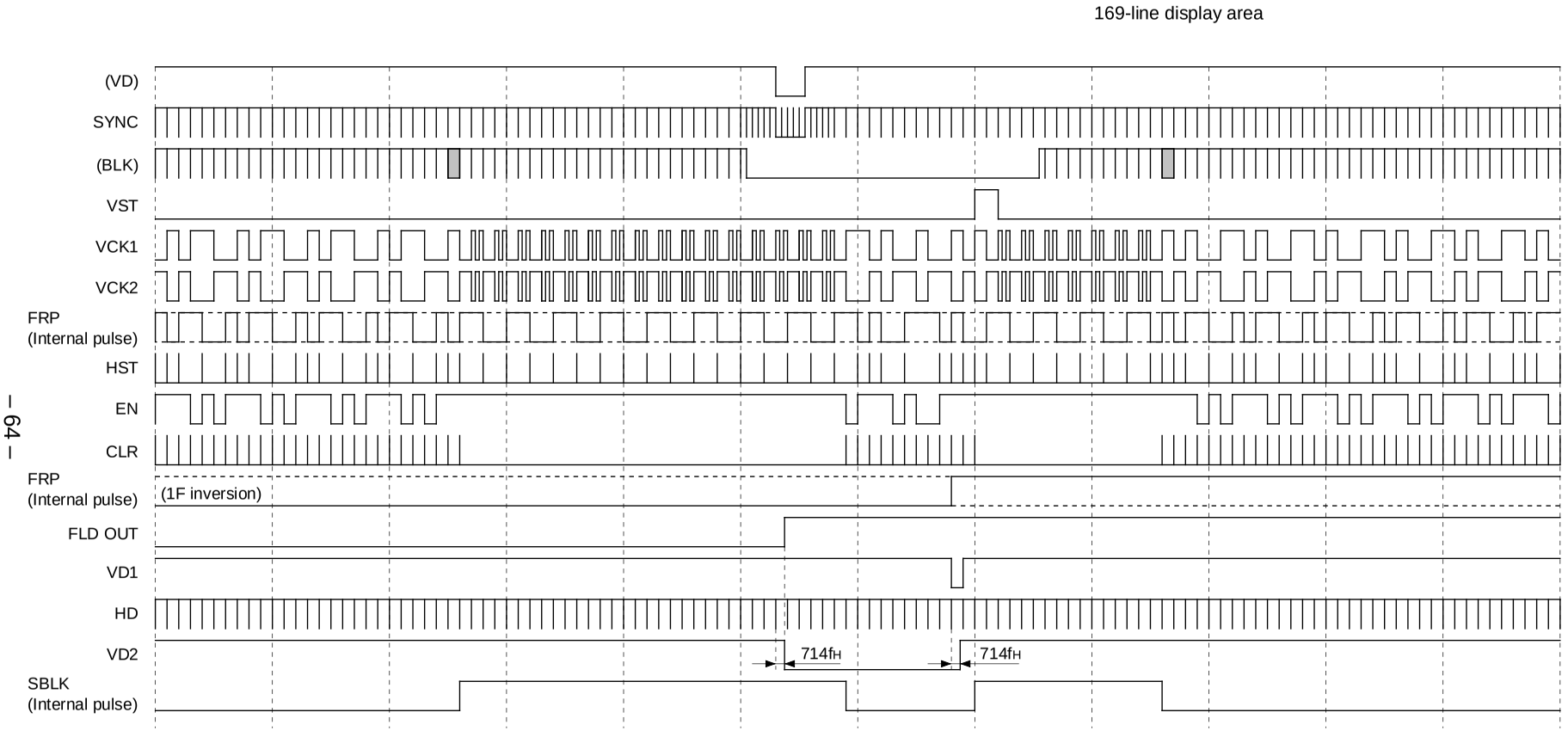


EVEN FIELD

Note) The first and third rows of the timing chart "VD" and "BLK", respectively, are pulses indicated as a reference and are not pulses output from pins.
FRP polarity is not specified for each line and field.

LCX009AK/AKB Vertical Direction Timing Chart

PAL WIDE

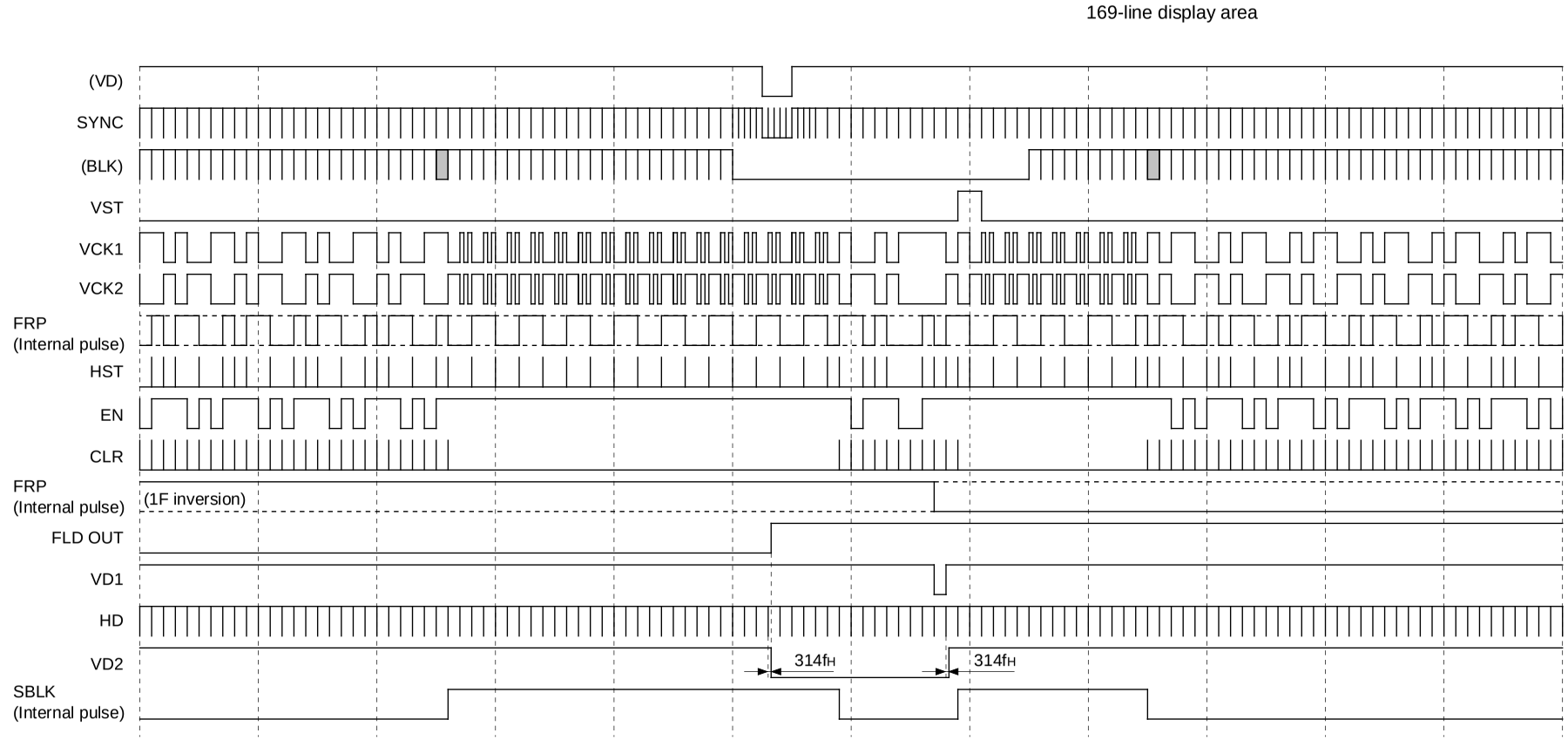


ODD FIELD

Note) The first and third rows of the timing chart "VD" and "BLK", respectively, are pulses indicated as a reference and are not pulses output from pins.
FRP polarity is not specified for each line and field.

LCX009AK/AKB Vertical Direction Timing Chart

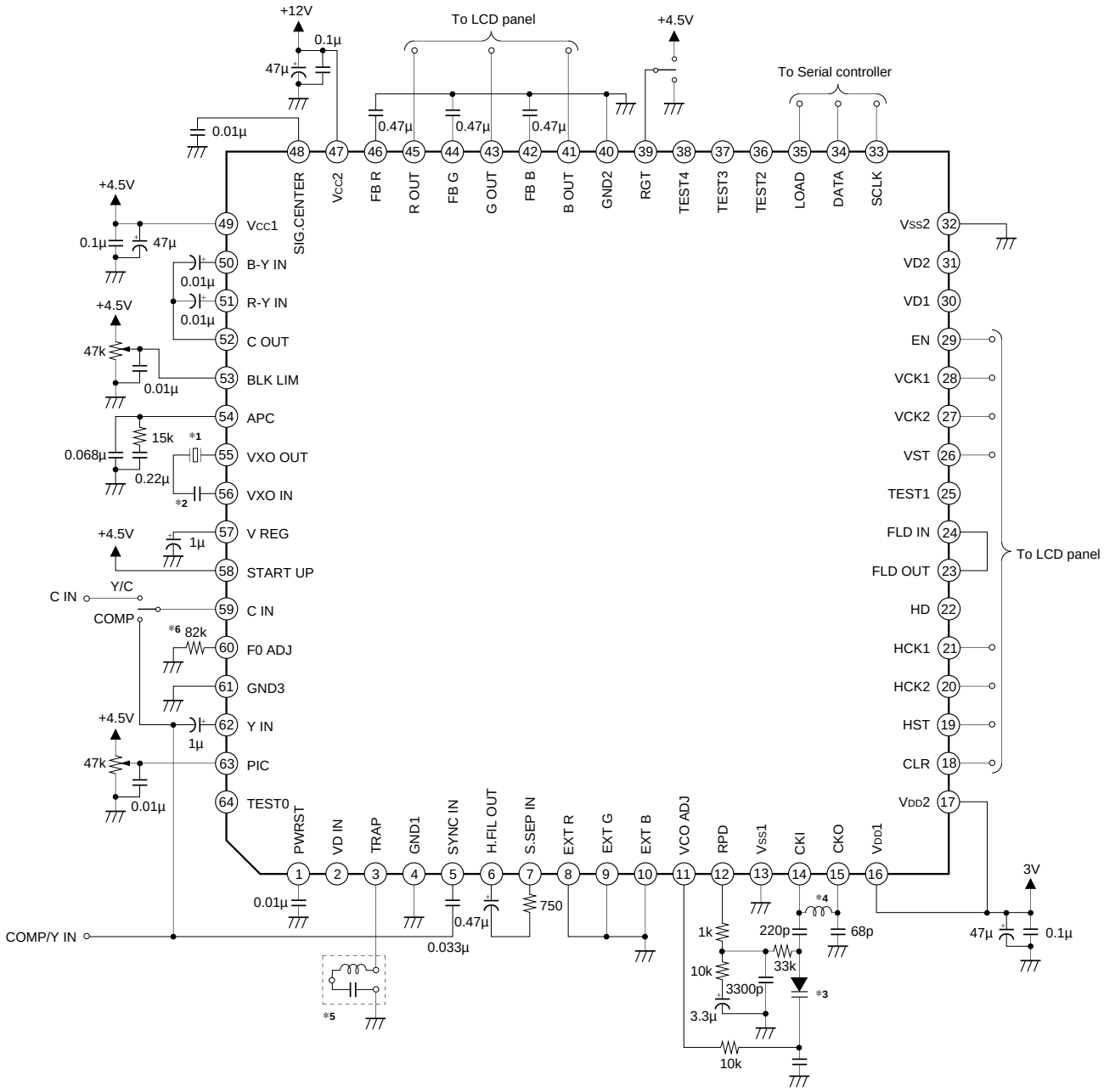
PAL WIDE



EVEN FIELD

Note) The first and third rows of the timing chart "VD" and "BLK", respectively, are pulses indicated as a reference and are not pulses output from pins.
FRP polarity is not specified for each line and field.

Application Circuit (NTSC/PAL, COMP and Y/C input)



*1 Used crystal: KINSEKI CX-5F
Frequency deviation: within ±30ppm, frequency temperature characteristics: within ±30ppm, load capacity: 16pF
NTSC: 3.579545MHz
PAL: 4.433619MHz

*2 NTSC: none, PAL: 18pF

*3 Varicap diode: 1T369 (SONY)

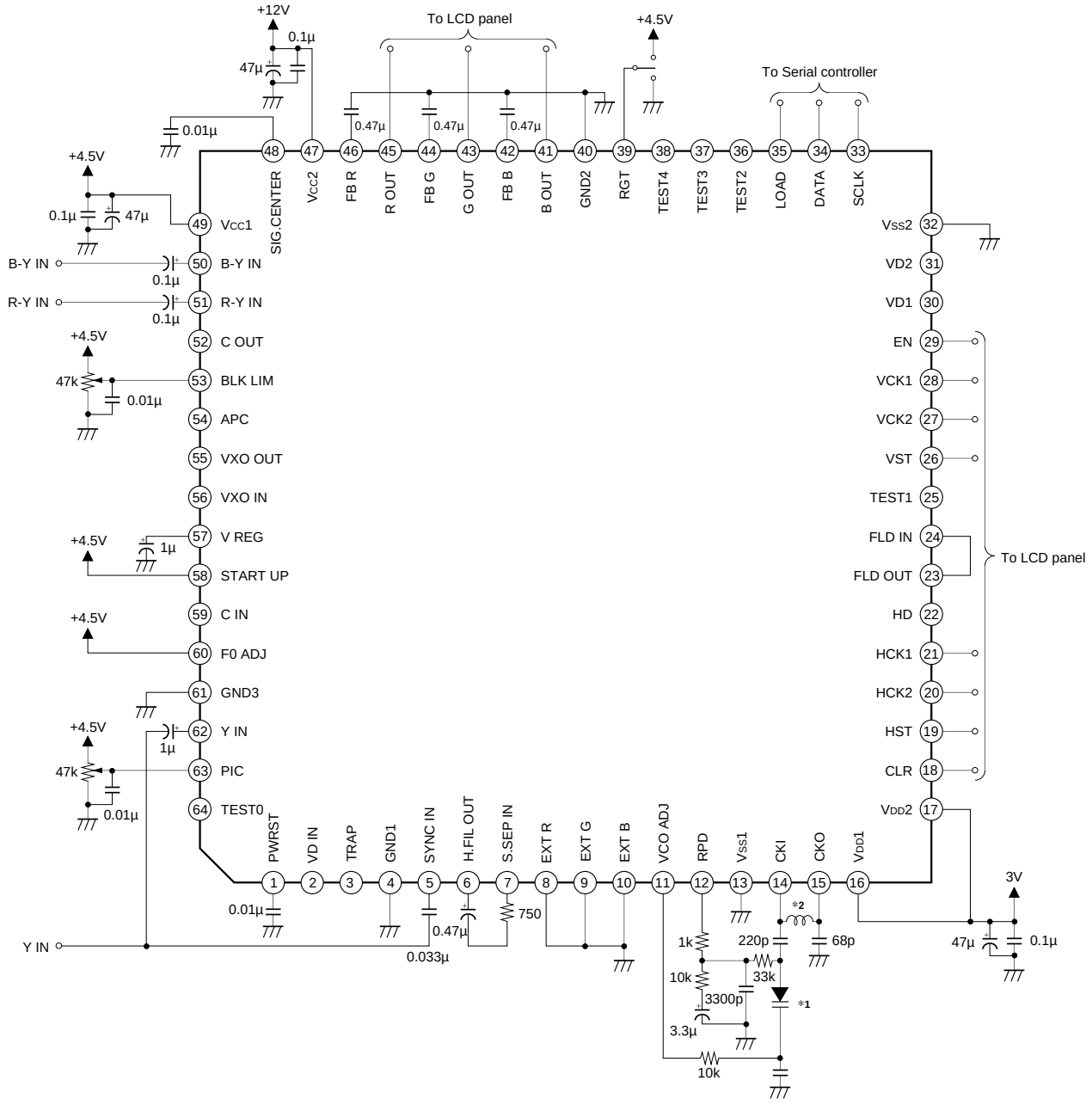
*4 L value: 8.2µH during LCX005 mode
3.9µH during LCX009 mode

*5 Trap (TDK), open during Y/C input
NTSC: NLT4532-S3R6B
PAL: NLT4532-S4R4

*6 Resistance value variation: ±2%,
temperature coefficient: ±200ppm or less
Connect to +4.5V during Y/C input

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Application Circuit (NTSC/PAL, Y/color difference input)



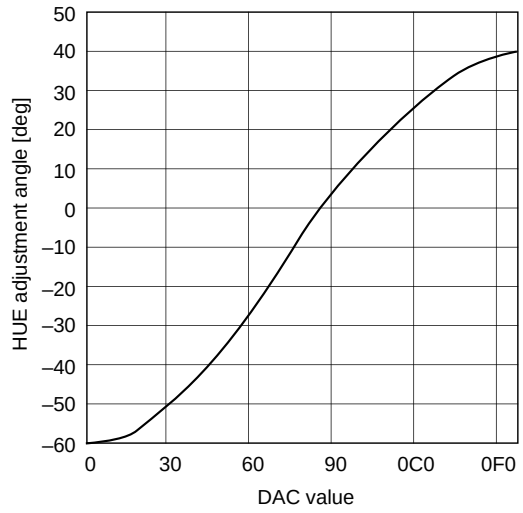
*1 Varicap diode: 1T369 (SONY)

*2 L value: 8.2µH during LCX005 mode
3.9µH during LCX009 mode

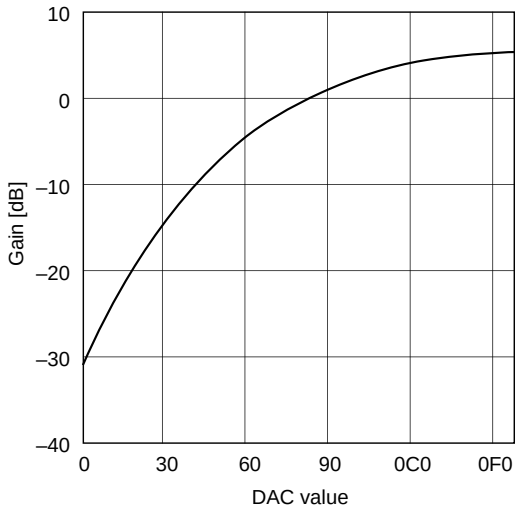
Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Example of Representative Characteristics

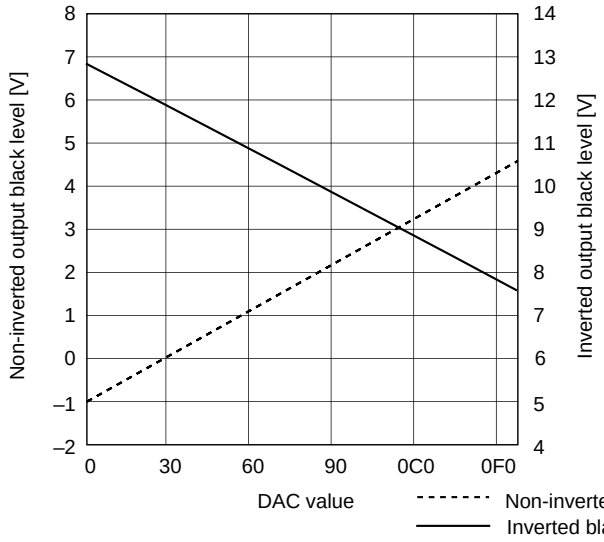
HUE adjustment characteristics



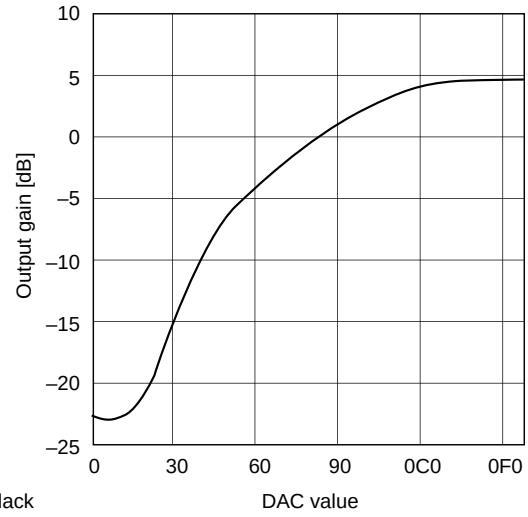
COLOR adjustment characteristics



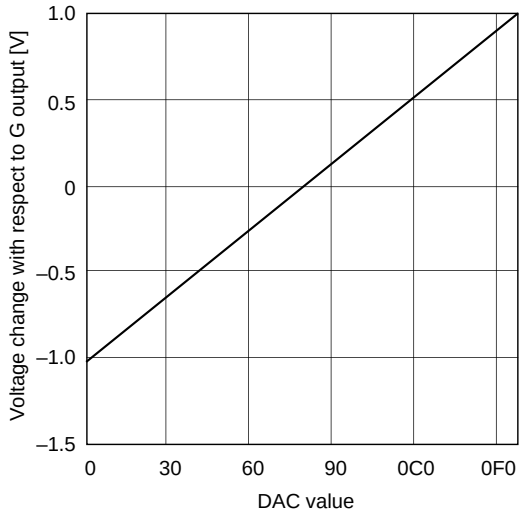
BRIGHT adjustment characteristics



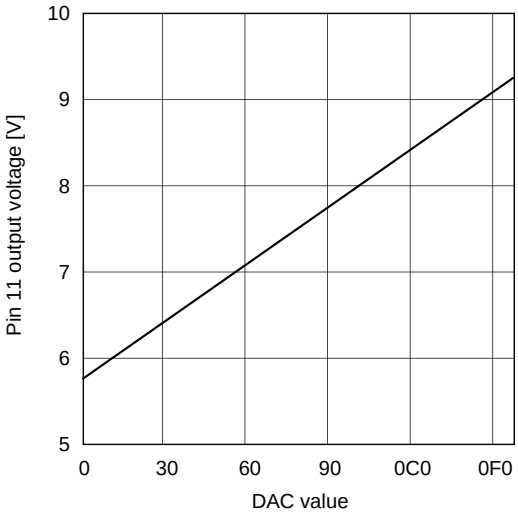
CONTRAST adjustment characteristics



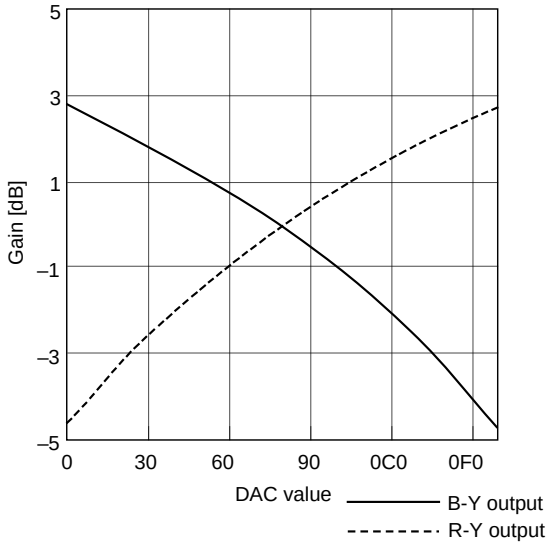
SUB-BRIGHT adjustment characteristics



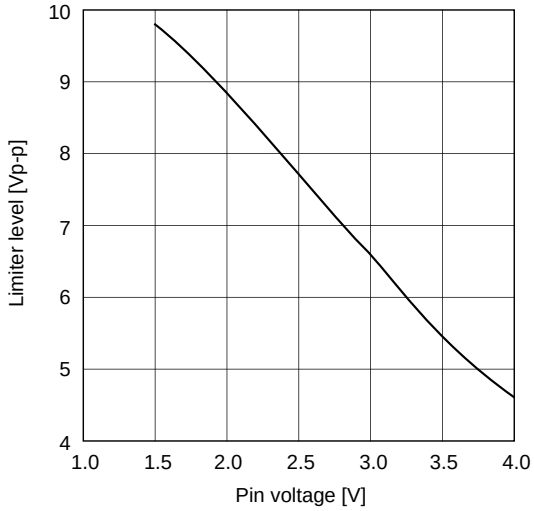
PLL adjustment voltage



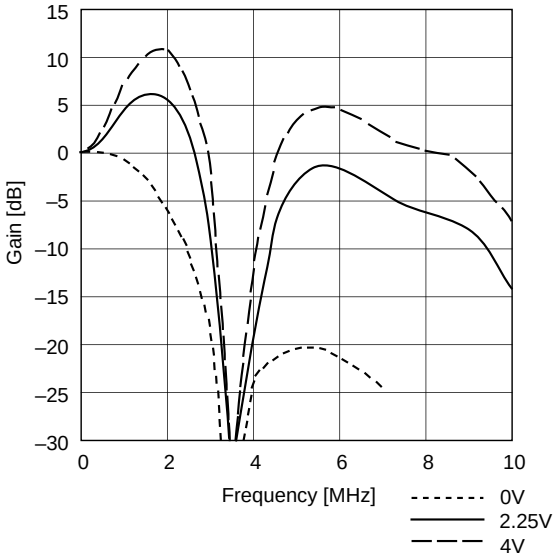
Color difference balance adjustment



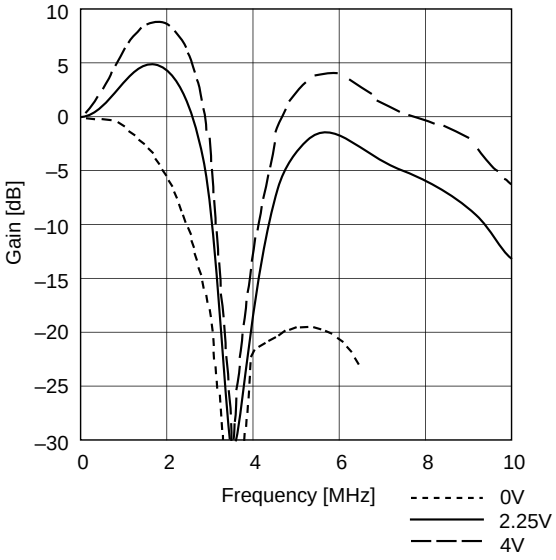
Black level limiter adjustment characteristics



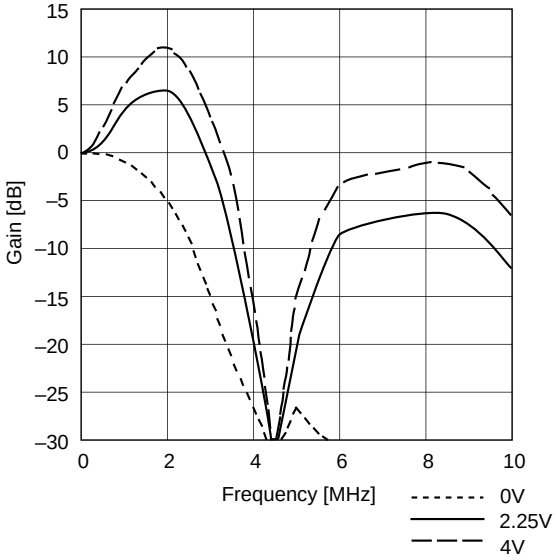
Sharpness characteristics (COMP, NTSC, 005)



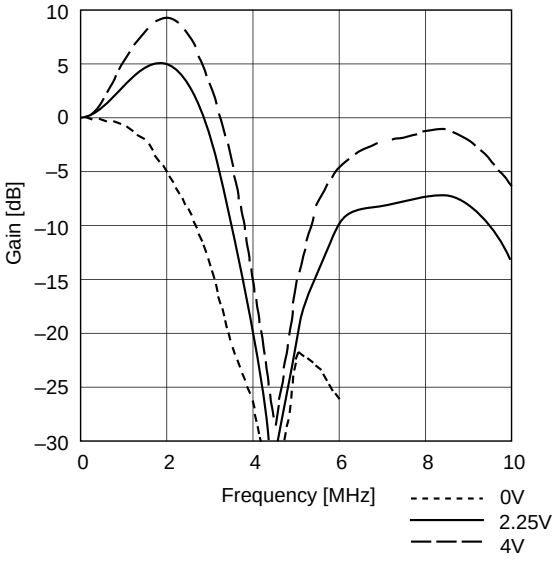
Sharpness characteristics (COMP, NTSC, 009)



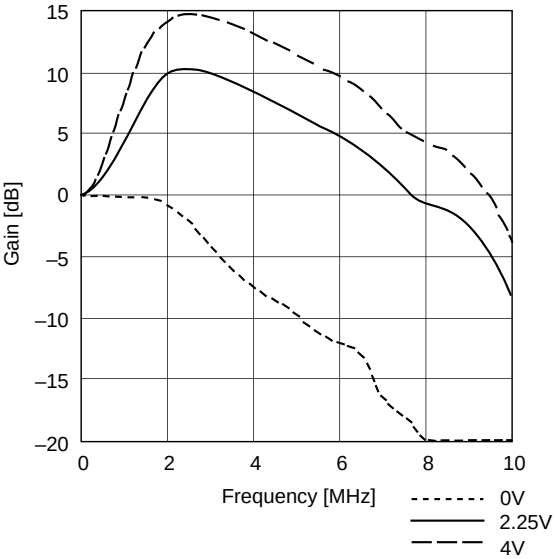
Sharpness characteristics (COMP, PAL, 005)



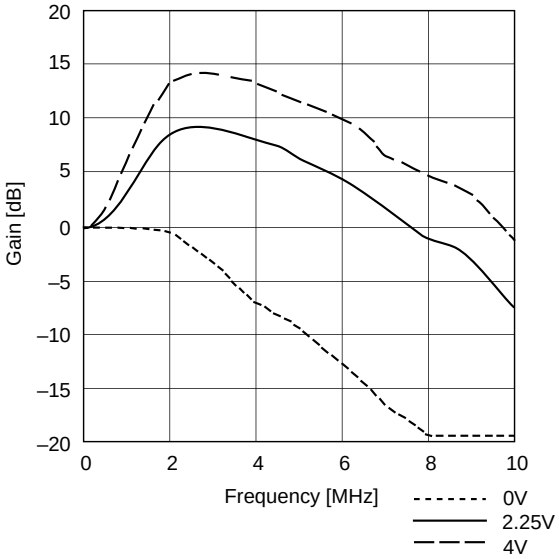
Sharpness characteristics (COMP, PAL, 009)



Sharpness characteristics (Y/C, 005)



Sharpness characteristics (Y/C, 009)



Notes on Operation

The CXA2503AR contains digital circuits, so the set board pattern must be designed in consideration of undesired radiation, interference to analog circuits, etc. Care should also be taken for the following items when designing the pattern.

- Make the IC power supply and GND patterns as plain as possible. In particular, GND and V_{SS} should not be separated and should be connected to the same GND pattern as close to the pins as possible.

- Connect the by-pass capacitors between the power supplies and GND as close to the pins as possible.

- The trap connected to Pin 3 should be located as close to the pin as possible. Also, take care not to pass other signal lines close to this pin or the connected trap.

- The wiring for the crystal and capacitor connected to Pins 55 and 56 should be as short as possible in order to prevent floating capacitance. Take care not to pass other signal lines close to these pins in order to prevent interference such as color unevenness. In addition, the APC pull-in characteristics vary significantly according to the characteristics of the used crystal and the wiring pattern, so be sure to thoroughly investigate these items before using the set.

- The resistor connected to Pin 60 should be located as close to the pin as possible. Also, take care not to pass other signal lines close to this pin.

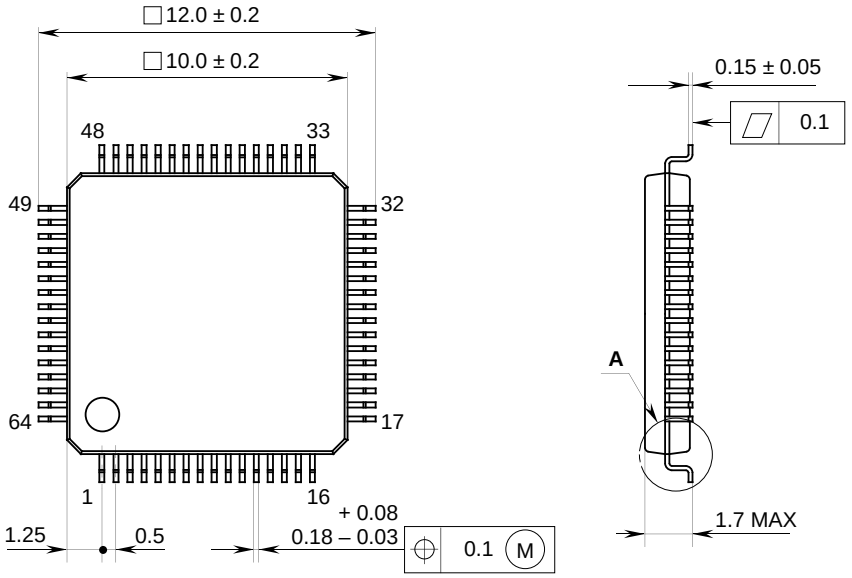
The composite/Y signal and the external R-Y and B-Y signals are clamped at the inputs using the capacitors connected to the input pins, so these signals should be input at sufficiently low impedance. The C signal is received by the internal capacitor, so an appropriate DC bias should be applied to this signal from an external source and this signal should be input at low impedance.

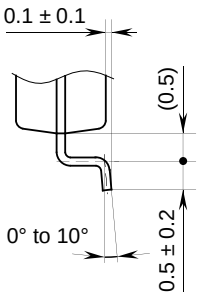
The smoothing capacitor of the DC level control feedback circuit in the output block should have a leak current with a small absolute value and variance.

This IC has a MOS structure which is easily damaged by static electricity, so thorough measures should be taken to prevent electrostatic discharge.

Package Outline Unit: mm

64PIN LQFP (PLASTIC)





DETAIL **A**

SONY CODE	LQFP-64P-L061
EIAJ CODE	LQFP064-P-1010-AY
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	0.3g