ML610Q419/ML610Q419C

8-bit Microcontroller with a Built-in LCD driver

GENERAL DESCRIPTION

This LSI is a high-performance 8-bit CMOS microcontroller into which rich peripheral circuits, such as synchronous serial port, UART, I2C bus interface (master), melody driver, battery level detect circuit, RC oscillation type A/D converter, and LCD driver, are incorporated around 8-bit CPU nX-U8/100.
The CPU nX-U8/100 is capable of efficient instruction execution in 1-instruction 1-clock mode by 3-stage pipe line architecture parallel procesing. The Flash ROM that is installed as program memory achieves low-voltage low-power consumption operation (read operation) equivalent to mask ROM and is most suitable for battery-driven applications.
The on-chip debug function that is installed enables program debugging and programming.

FEATURES

- CPU
  - 8-bit RISC CPU (CPU name: nX-U8/100)
  - Instruction system: 16-bit instructions
  - Instruction set: Transfer, arithmetic operations, comparison, logic operations, multiplication/division, bit manipulations, bit logic operations, jump, conditional jump, call return stack manipulations, arithmetic shift, and so on
  - On-Chip debug function
  - Minimum instruction execution time
    30.5 μs (@32.768 kHz system clock)
    0.24 4μs (@4.096 MHz system clock)

- Internal memory
  - Internal 64KByte Flash ROM (32K×16 bits) (including unusable 1KByte TEST area)
  - Internal 4KByte Data Flash (2K×16 bits)
  - Internal 2KByte Data RAM (2048×8 bits), 240×9bit Display Allocation RAM

- Interrupt controller
  - 1 non-maskable interrupt sources (Internal source: 1)
  - 21 maskable interrupt sources (Internal sources: 16, External sources: 5)

- Time base counter
  - Low-speed time base counter ×1 channel
    Frequency compensation (Compensation range: Approx. −488ppm to +488ppm. Compensation accuracy: Approx. 0.48ppm)
  - High-speed time base counter ×1 channel

- Watchdog timer
  - Non-maskable interrupt and reset
  - Free running
  - Overflow period: 4 types selectable (125ms, 500ms, 2s, and 8s)

- Timers
  - 8 bits × 4 channels (Timer0-3: 16-bit x 2 configuration available by using Timer0-1 or Timer2-3)
  - Clock frequency measurement mode (in one channel of 16-bit configuration using Timer2-3)

- Capture
  - Time base capture × 2 channels (4096 Hz to 32 Hz)

- PWM
  - Resolution 16 bits × 1 channel

- Synchronous serial port
  - Master/slave selectable × 2 channel
  - LSB first/MSB first selectable
  - 8-bit length/16-bit length selectable

- UART
  - TXD/RXD × 1 channel
  - Bit length, parity/no parity, odd parity/even parity, 1 stop bit/2 stop bits
  - Positive logic/negative logic selectable
  - Built-in baud rate generator

- I^2C bus interface
  - Master function only
  - Fast mode (400 kbps@4MHz), standard mode (100 kbps@4MHz, 50kbps@500kHz)

- Melody driver
  - Scale: 29 types (Melody sound frequency: 508 Hz to 32.768 kHz)
  - Tone length: 63 types
  - Tempo: 15 types
  - Buzzer output mode (4 output modes, 8 frequencies, 16 duty levels)

- RC oscillation type A/D converter
  - 24-bit counter
  - Time division × 2 channels

- Successive approximation type A/D converter (SA-ADC)
  - 12-bit A/D converter
  - Input × 4 channels

- General-purpose ports
  - Input-only port × 6 channels (including secondary functions)
  - Output-only port × 3 channels (including secondary functions)
  - Input/output port
    ML610Q419 : 18 channels (including secondary functions)
    ML610Q419C : 26 channels (including secondary functions)

- LCD driver
  - Dot matrix can be supported.
    ML610Q419 : 192 dots max. (48 seg × 4 com)
    ML610Q419C : 160 dots max. (40 seg × 4 com)
  - 1/1 to 1/4 duty
  - 1/2, 1/3 bias (built-in bias generation circuit)
  - Frame frequency selecable: approx. 64Hz, 73Hz, 85Hz, and 102Hz
  - Bias voltage multiplying clock selectable (8 types)
  - LCD drive stop mode, LCD display mode, all LCDs on mode, and all LCDs off mode selectable
  - Programmable display allocation function

- Reset
  - Reset by the RESET_N pin
  - Reset by power-on detection
  - Reset when oscillation stop of the low-speed clock is detected
  - Reset by low level detection (LLD)
    The voltage which is released from reset is selectable by the code-option: 1.1V, 1.8V (Max.)
  - Reset by the watchdog timer (WDT) 2nd overflow

- Power supply voltage detect function
  - Judgment voltages: One of 16 levels
  - Judgment accuracy: ±2% (Typ.)

- Clock
  - Low-speed clock: (This LSI can not guarantee the operation withoug low-speed clock)
    Crystal oscillation (32.768 kHz)
  - High-speed clock:
    Built-in RC oscillation (500kHz)
    Built-in PLL oscillation (8.192 MHz ±2.5%), crystal/ceramic oscillation (4.096 MHz), external clock
  - Selection of high-speed clock mode by software:
    Built-in RC oscillation, built-in PLL oscillation, crystal/ceramic oscillation, external clock

- Power management
  - HALT mode: Instruction execution by CPU is suspended (peripheral circuits are in operating states).
  - STOP mode: Stop of low-speed oscillation and high-speed oscillation (Operations of CPU and peripheral circuits are stopped.)
  - Clock gear: The frequency of high-speed system clock can be changed by software (1/1, 1/2, 1/4, or 1/8 of the oscillation clock)
  - Block Control Function: Power down (reset registers and stop clock supply) the circuits of unused peripherals.

- Guaranteed operating range
  - Operating temperature: –20°C to 70°C
  - Operating voltage: V_{DD} = 1.1V to 3.6V

• Product name – Supported Function
The line-up of the ML610Q419 is below.

- Chip (Die) -	ROM type	Operating temperature	LCD driver	Product availability
ML610Q419-xxxWA	Flash ROM	-20°C to +70°C	192 dots max. (48 seg x 4 com)	Yes
ML610Q419C -xxxWA	Flash ROM	-20°C to +70°C	160 dots max. (40 seg x 4 com)	Yes

-100-pin plastic TQFP -	ROM type	Operating temperature	LCD driver	Product availability
ML610Q419-xxxTB	Flash ROM	-20°C to +70°C	192 dots max. (48 seg x 4 com)	Yes
ML610Q419C -xxxTB	Flash ROM	-20°C to +70°C	160 dots max. (40 seg x 4 com)	Yes

xxx: ROM code number (xxx of the blank product is NNN)
Q:Flash ROM version
WA: Chip
TB: TQFP

BLOCK DIAGRAM

ML610Q419 Block Diagram

Figure 1 show the block diagram of the ML610Q419.
"*" indicates the secondary function of each port.

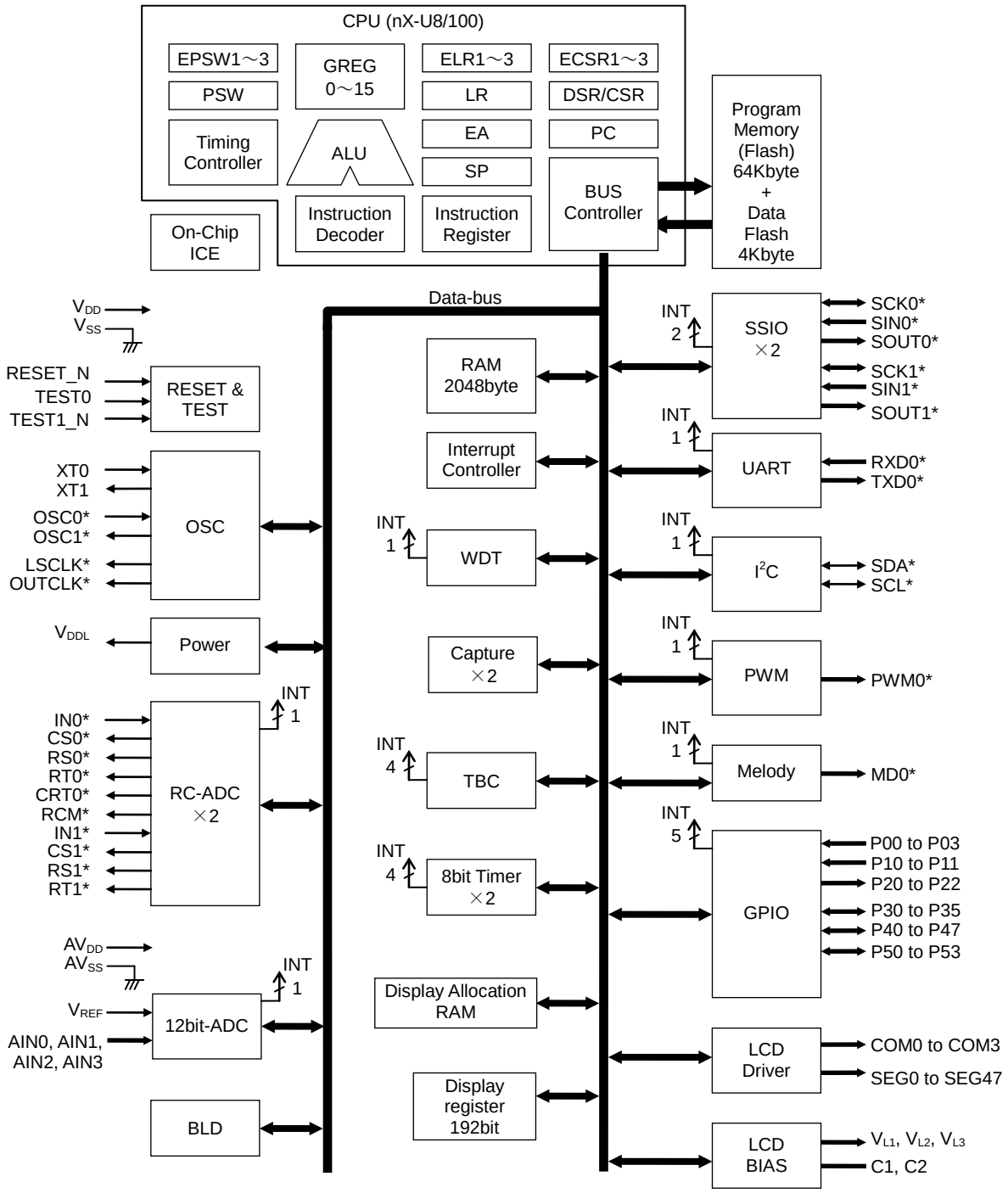


Figure 1 ML610Q419 Block Diagram

ML610Q419C Block Diagram

Figure 2 show the block diagram of the ML610Q419C.
"*" indicates the secondary function of each port.

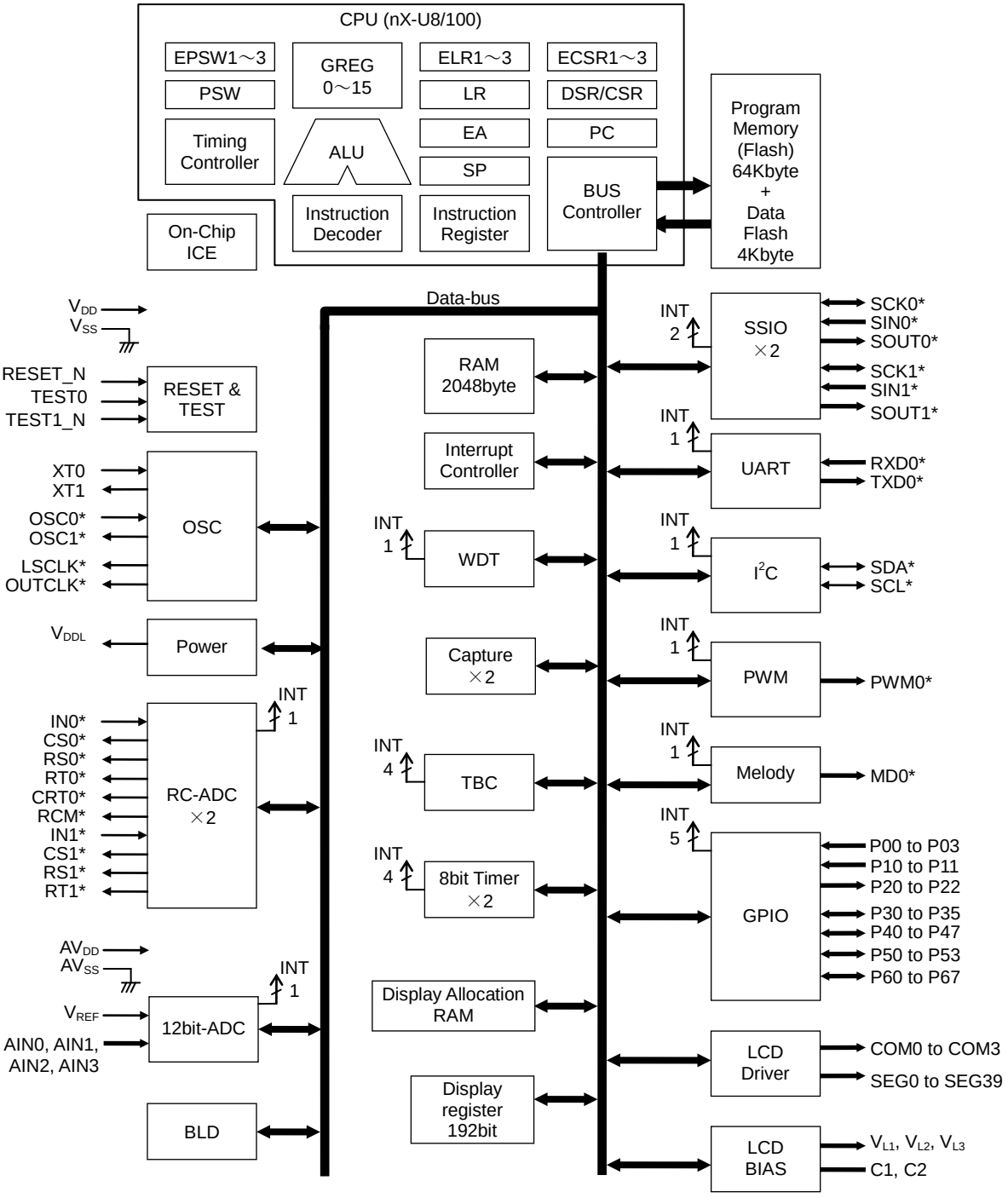
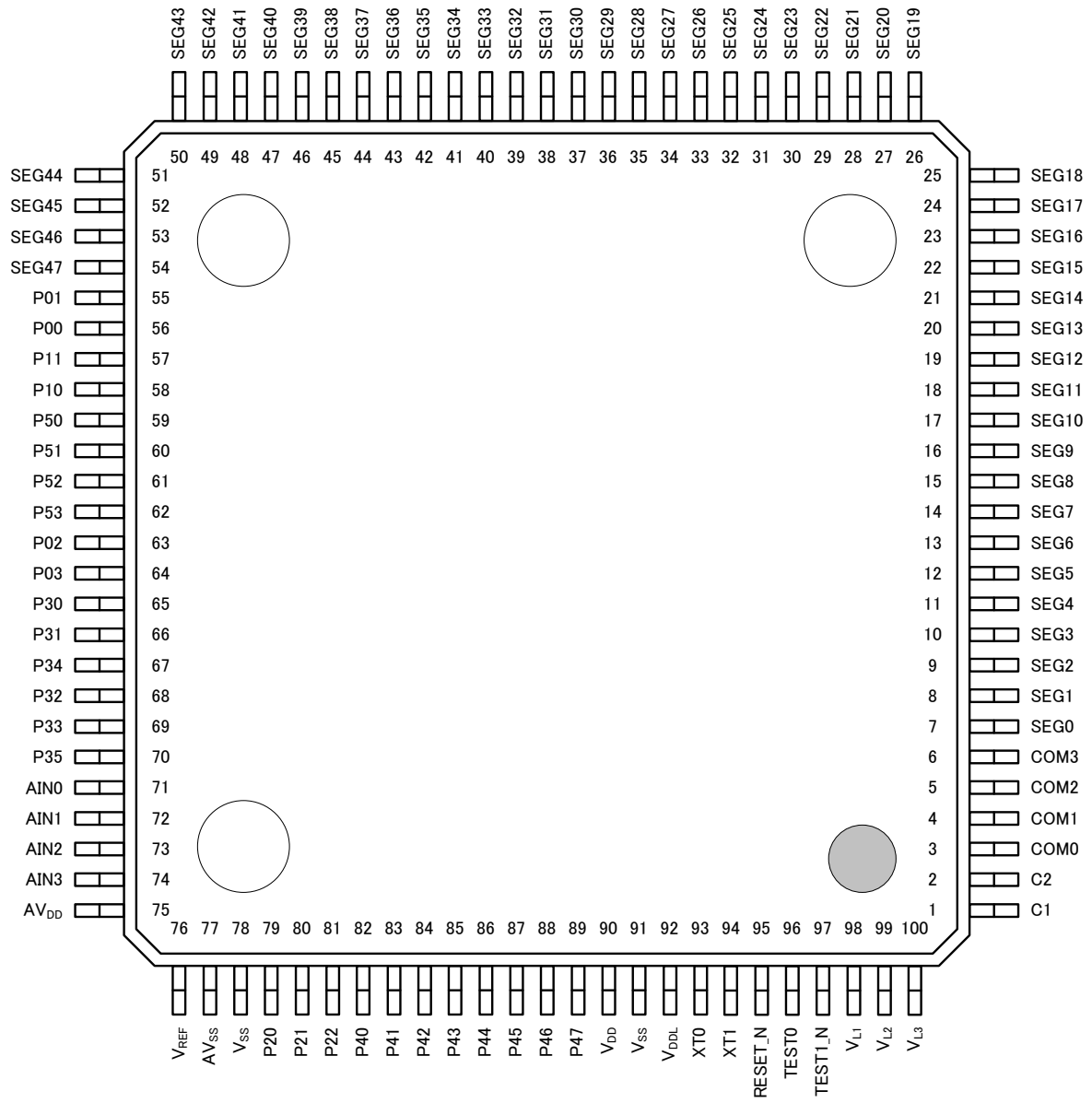


Figure 2 ML610Q419C Block Diagram

PIN CONFIGURATION

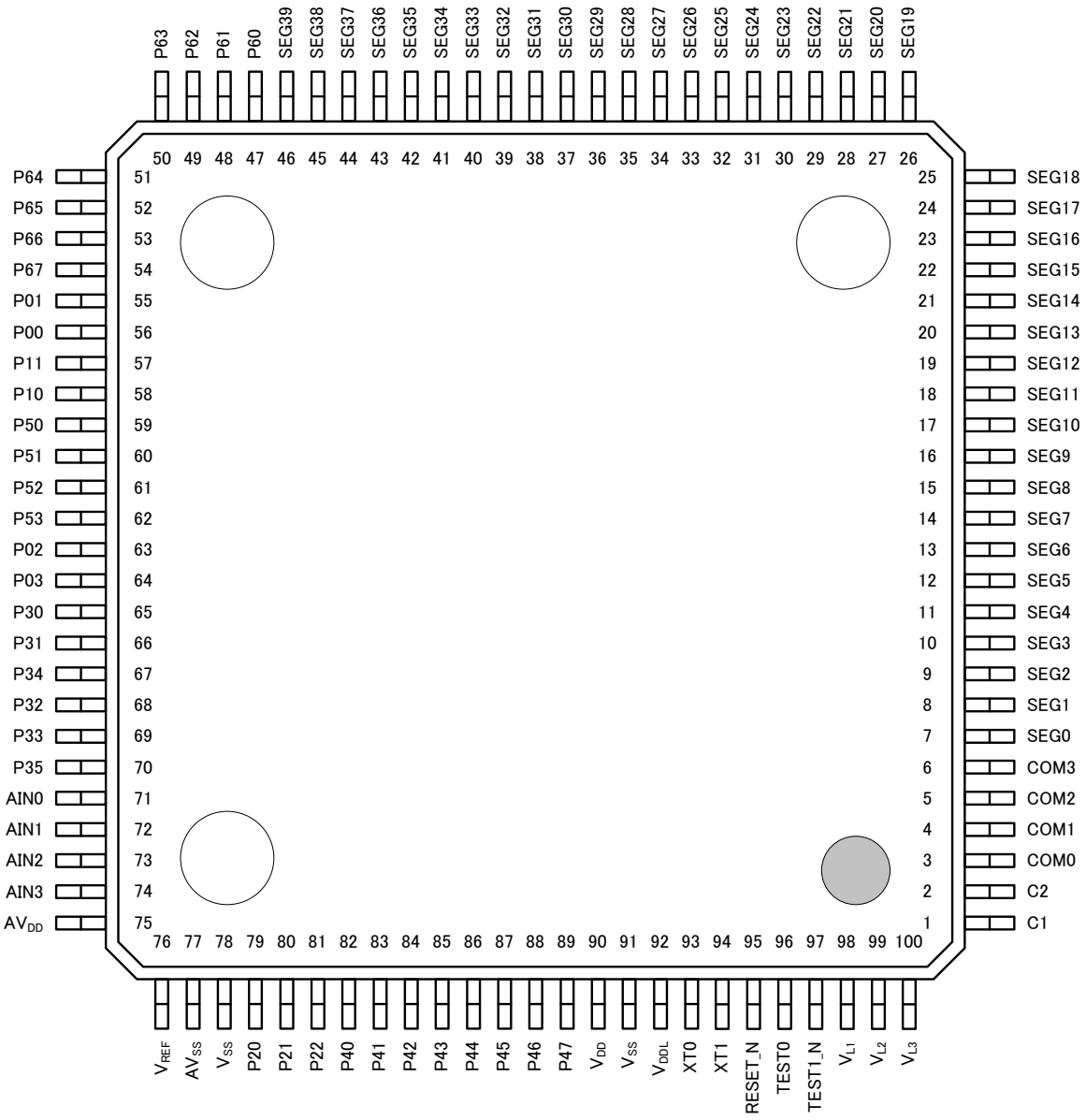
ML610Q419 TQFP100 Pin Layout



(NC): No Connection

Figure 3 ML610Q419 TQFP100 Pin Configuration

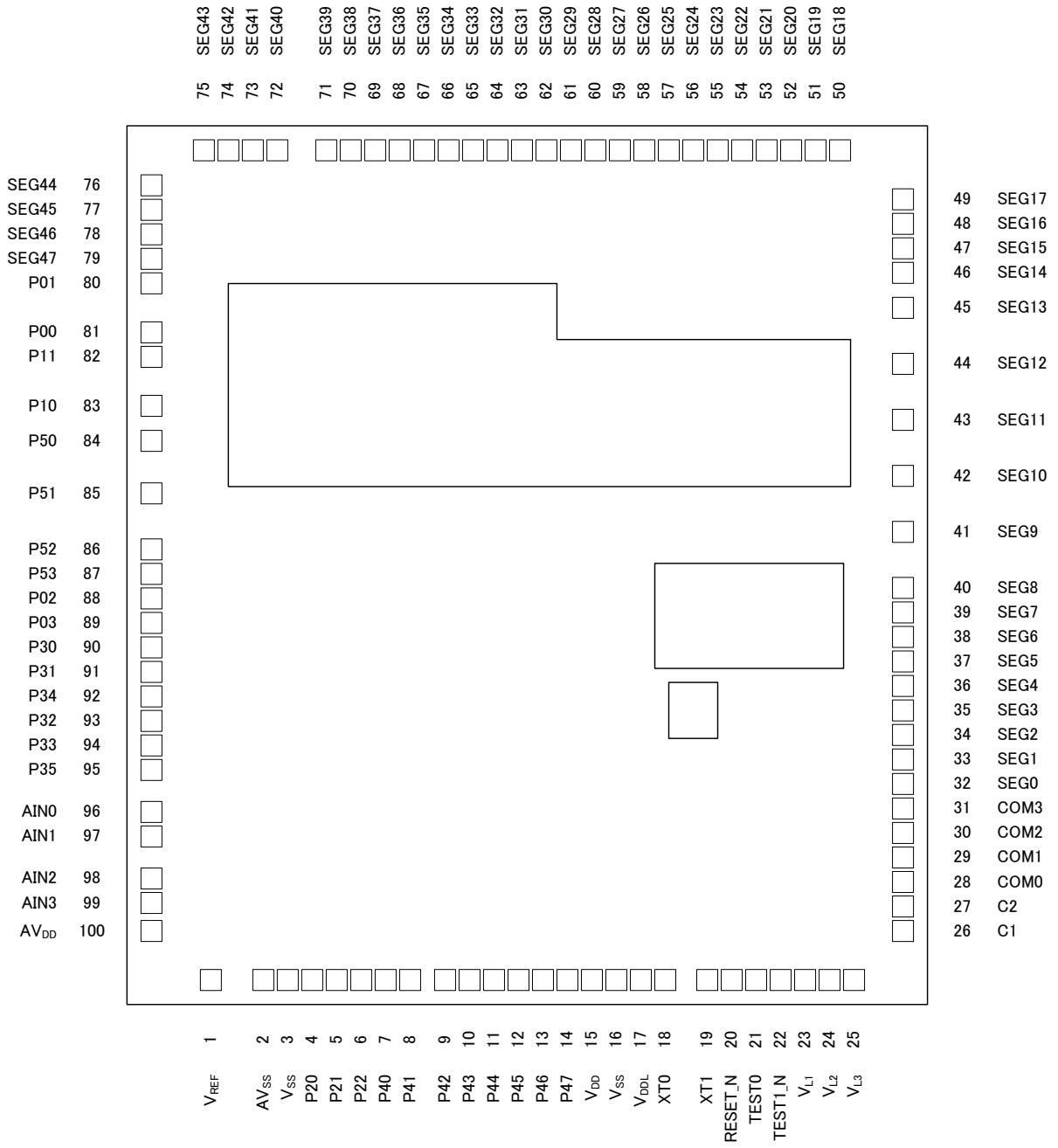
ML610Q419C TQFP100 Pin Layout



(NC): No Connection

Figure 4 ML610Q419C TQFP100 Pin Configuration

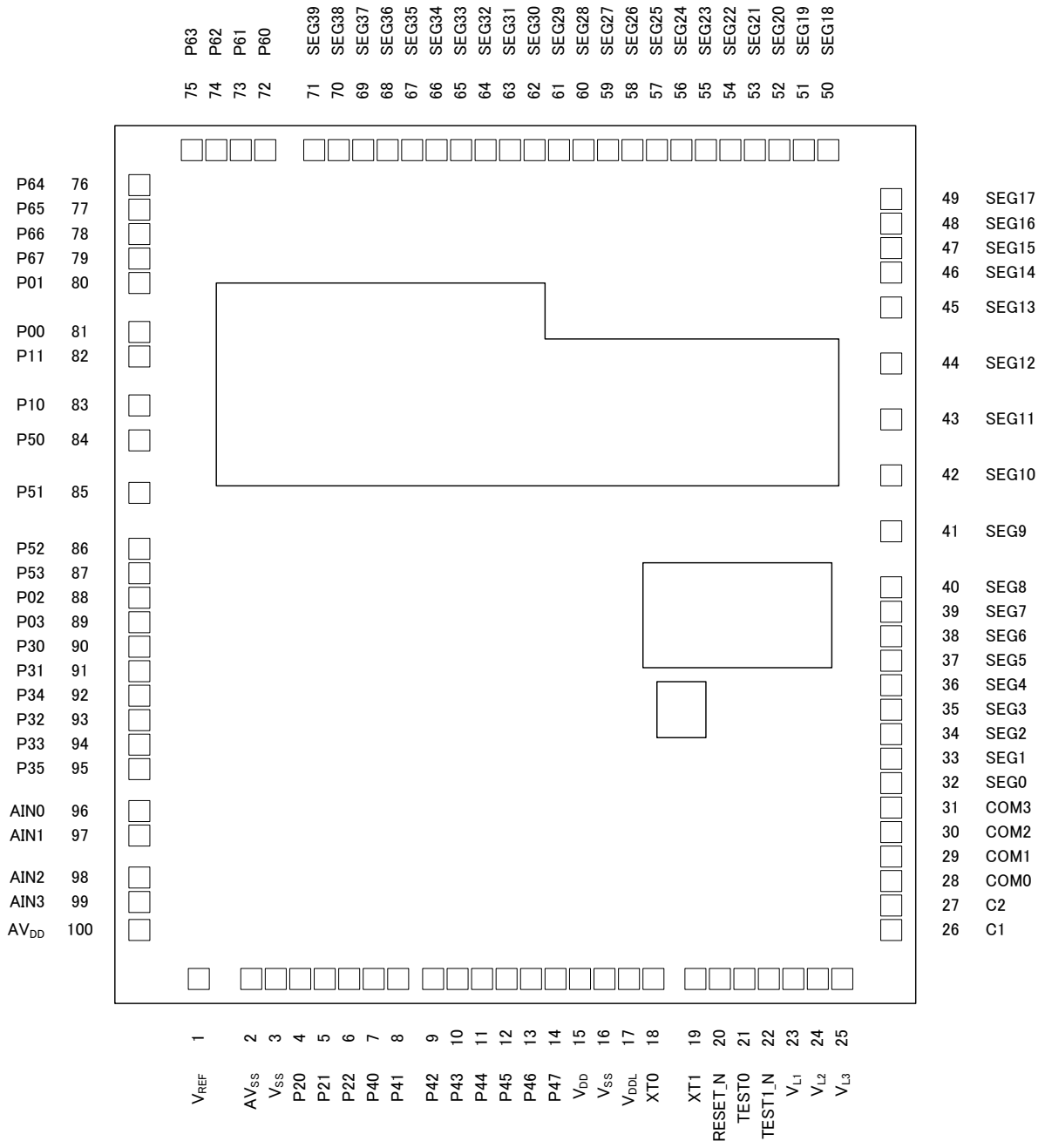
ML610Q419 Chip Dimension



Chip size:	2.64 mm × 3.20 mm
PAD count:	100 pins
Minimum PAD pitch:	80 μm
PAD aperture:	70 μm × 70 μm
Chip thickness:	350 μm
Voltage of the rear side of chip:	V_{SS} level

Figure 5 ML610Q419 Chip Dimension

ML610Q419C Chip Dimension



Chip size:	2.64 mm × 3.20 mm
PAD count:	100 pins
Minimum PAD pitch:	80 μm
PAD aperture:	70 μm × 70 μm
Chip thickness:	350 μm
Voltage of the rear side of chip:	V_{SS} level

Figure 6 ML610Q419C Chip Dimension

ML610Q419 Pad Coordinates

Table 1 ML610Q419 Pad Coordinates

Chip Center: X=0,Y=0

PAD No.	Pad Name	X (µm)	Y (µm)	PAD No.	Pad Name	X (µm)	Y (µm)	PAD No.	Pad Name	X (µm)	Y (µm)
1	V_{ref}	-1020.0	-1494.0	36	SEG4	1214.0	-525.0	71	SEG39	-620.0	1494.0
2	AV_{SS}	-860.0	-1494.0	37	SEG5	1214.0	-445.0	72	SEG40	-730.0	1494.0
3	V_{SS}	-780.0	-1494.0	38	SEG6	1214.0	-365.0	73	SEG41	-810.0	1494.0
4	P20	-700.0	-1494.0	39	SEG7	1214.0	-285.0	74	SEG42	-890.0	1494.0
5	P21	-620.0	-1494.0	40	SEG8	1214.0	-205.0	75	SEG43	-970.0	1494.0
6	P22	-540.0	-1494.0	41	SEG9	1214.0	52.0	76	SEG44	-1214.0	1380.0
7	P40	-460.0	-1494.0	42	SEG10	1214.0	258.0	77	SEG45	-1214.0	1300.0
8	P41	-380.0	-1494.0	43	SEG11	1214.0	464.0	78	SEG46	-1214.0	1220.0
9	P42	-280.0	-1494.0	44	SEG12	1214.0	670.0	79	SEG47	-1214.0	1140.0
10	P43	-200.0	-1494.0	45	SEG13	1214.0	876.0	80	P01	-1214.0	1040.0
11	P44	-120.0	-1494.0	46	SEG14	1214.0	1015.0	81	P00	-1214.0	850.0
12	P45	-40.0	-1494.0	47	SEG15	1214.0	1095.0	82	P11	-1214.0	760.0
13	P46	40.0	-1494.0	48	SEG16	1214.0	1175.0	83	P10	-1214.0	600.0
14	P47	120.0	-1494.0	49	SEG17	1214.0	1255.0	84	P50	-1214.0	476.0
15	V_{DD}	204.0	-1494.0	50	SEG18	1060.0	1494.0	85	P51	-1214.0	270.0
16	V_{SS}	284.0	-1494.0	51	SEG19	980.0	1494.0	86	P52	-1214.0	28.0
17	V_{DDL}	364.0	-1494.0	52	SEG20	900.0	1494.0	87	P53	-1214.0	-52.0
18	XT0	452.0	-1494.0	53	SEG21	820.0	1494.0	88	P02	-1214.0	-132.0
19	XT1	612.0	-1494.0	54	SEG22	740.0	1494.0	89	P03	-1214.0	-212.0
20	RESET_N	692.0	-1494.0	55	SEG23	660.0	1494.0	90	P30	-1214.0	-292.0
21	TEST0	772.0	-1494.0	56	SEG24	580.0	1494.0	91	P31	-1214.0	-372.0
22	TEST1_N	852.0	-1494.0	57	SEG25	500.0	1494.0	92	P34	-1214.0	-452.0
23	V_{L1}	932.0	-1494.0	58	SEG26	420.0	1494.0	93	P32	-1214.0	-532.0
24	V_{L2}	1012.0	-1494.0	59	SEG27	340.0	1494.0	94	P33	-1214.0	-612.0
25	V_{L3}	1092.0	-1494.0	60	SEG28	260.0	1494.0	95	P35	-1214.0	-692.0
26	C1	1214.0	-1325.0	61	SEG29	180.0	1494.0	96	AIN0	-1214.0	-833.0
27	C2	1214.0	-1245.0	62	SEG30	100.0	1494.0	97	AIN1	-1214.0	-913.0
28	COM0	1214.0	-1165.0	63	SEG31	20.0	1494.0	98	AIN02	-1214.0	-1085.0
29	COM1	1214.0	-1085.0	64	SEG32	-60.0	1494.0	99	AIN03	-1214.0	-1165.0
30	COM2	1214.0	-1005.0	65	SEG33	-140.0	1494.0	100	AV_{DD}	-1214.0	-1291.0
31	COM3	1214.0	-925.0	66	SEG34	-220.0	1494.0				
32	SEG0	1214.0	-845.0	67	SEG35	-300.0	1494.0				
33	SEG1	1214.0	-765.0	68	SEG36	-380.0	1494.0				
34	SEG2	1214.0	-685.0	69	SEG37	-460.0	1494.0				
35	SEG3	1214.0	-605.0	70	SEG38	-540.0	1494.0				

ML610Q419C Pad Coordinates

Table 2 ML610Q419C Pad Coordinates

Chip Center: X=0,Y=0

PAD No.	Pad Name	X (µm)	Y (µm)	PAD No.	Pad Name	X (µm)	Y (µm)	PAD No.	Pad Name	X (µm)	Y (µm)
1	V_{ref}	-1020.0	-1494.0	36	SEG4	1214.0	-525.0	71	SEG39	-620.0	1494.0
2	AV_{SS}	-860.0	-1494.0	37	SEG5	1214.0	-445.0	72	P60	-730.0	1494.0
3	V_{SS}	-780.0	-1494.0	38	SEG6	1214.0	-365.0	73	P61	-810.0	1494.0
4	P20	-700.0	-1494.0	39	SEG7	1214.0	-285.0	74	P62	-890.0	1494.0
5	P21	-620.0	-1494.0	40	SEG8	1214.0	-205.0	75	P63	-970.0	1494.0
6	P22	-540.0	-1494.0	41	SEG9	1214.0	52.0	76	P64	-1214.0	1380.0
7	P40	-460.0	-1494.0	42	SEG10	1214.0	258.0	77	P65	-1214.0	1300.0
8	P41	-380.0	-1494.0	43	SEG11	1214.0	464.0	78	P66	-1214.0	1220.0
9	P42	-280.0	-1494.0	44	SEG12	1214.0	670.0	79	P67	-1214.0	1140.0
10	P43	-200.0	-1494.0	45	SEG13	1214.0	876.0	80	P01	-1214.0	1040.0
11	P44	-120.0	-1494.0	46	SEG14	1214.0	1015.0	81	P00	-1214.0	850.0
12	P45	-40.0	-1494.0	47	SEG15	1214.0	1095.0	82	P11	-1214.0	760.0
13	P46	40.0	-1494.0	48	SEG16	1214.0	1175.0	83	P10	-1214.0	600.0
14	P47	120.0	-1494.0	49	SEG17	1214.0	1255.0	84	P50	-1214.0	476.0
15	V_{DD}	204.0	-1494.0	50	SEG18	1060.0	1494.0	85	P51	-1214.0	270.0
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23	V_{L1}	932.0	-1494.0	58	SEG26	420.0	1494.0	93	P32	-1214.0	-532.0
24	V_{L2}	1012.0	-1494.0	59	SEG27	340.0	1494.0	94	P33	-1214.0	-612.0
25	V_{L3}	1092.0	-1494.0	60	SEG28	260.0	1494.0	95	P35	-1214.0	-692.0
26	C1	1214.0	-1325.0	61	SEG29	180.0	1494.0	96	AIN0	-1214.0	-833.0
27	C2	1214.0	-1245.0	62	SEG30	100.0	1494.0	97	AIN1	-1214.0	-913.0
28	COM0	1214.0	-1165.0	63	SEG31	20.0	1494.0	98	AIN02	-1214.0	-1085.0
29	COM1	1214.0	-1085.0	64	SEG32	-60.0	1494.0	99	AIN03	-1214.0	-1165.0
30	COM2	1214.0	-1005.0	65	SEG33	-140.0	1494.0	100	AV_{DD}	-1214.0	-1291.0
31	COM3	1214.0	-925.0	66	SEG34	-220.0	1494.0				
32	SEG0	1214.0	-845.0	67	SEG35	-300.0	1494.0				
33	SEG1	1214.0	-765.0	68	SEG36	-380.0	1494.0				
34	SEG2	1214.0	-685.0	69	SEG37	-460.0	1494.0				
35	SEG3	1214.0	-605.0	70	SEG38	-540.0	1494.0				

PIN LIST

PAD No.		Primary function			Secondary function			Tertiary function		
Q419	Q419C	Pin name	I/O	Function	Pin name	I/O	Function	Pin name	I/O	Function
3, 16	3. 16	Vss	—	Negative power supply pin	—	—	—	—	—	—
15	15	V_{DD}	—	Positive power supply pin	—	—	—	—	—	—
17	17	V_{DDL}	—	Power supply pin for internal logic (internally generated)	—	—	—	—	—	—
2	2	AV_{SS}	—	Negative power supply pin for successive approximation type ADC	—	—	—	—	—	—
100	100	AV_{DD}	—	Positive power supply pin for successive approximation type ADC	—	—	—	—	—	—
1	1	V_{REF}	—	Reference power supply pin for successive approximation type ADC	—	—	—	—	—	—
96	96	AIN0	—	Successive approximation type ADC input	—	—	—	—	—	—
97	97	AIN1	—	Successive approximation type ADC input	—	—	—	—	—	—
98	98	AIN2	—	Successive approximation type ADC input	—	—	—	—	—	—
99	99	AIN3	—	Successive approximation type ADC input	—	—	—	—	—	—
23	23	V_{L1}	—	Power supply pin for LCD bias (internally generated)	—	—	—	—	—	—
24	24	V_{L2}	—	Power supply pin for LCD bias (internally generated)	—	—	—	—	—	—
25	25	V_{L3}	—	Power supply pin for LCD bias (internally generated)	—	—	—	—	—	—
26	26	C1	—	Capacitor connection pin for LCD bias generation	—	—	—	—	—	—
27	27	C2	—	Capacitor connection pin for LCD bias generation	—	—	—	—	—	—
21	21	TEST0	I/O	Test pin	—	—	—	—	—	—
22	22	TEST1_N	I	Test pin	—	—	—	—	—	—
20	20	RESET_N	I	Reset input pin	—	—	—	—	—	—
18	18	XT0	I	Low-speed clock oscillation pin	—	—	—	—	—	—
19	19	XT1	O	Low-speed clock oscillation pin	—	—	—	—	—	—
81	81	P00/EXI0/ CAP0	I	Input port, External interrupt, Capture 0 input	—	—	—	—	—	—
80	80	P01/EXI1/ CAP1	I	Input port, External interrupt, Capture 1 input	—	—	—	—	—	—
88	88	P02/EXI2 /RXD0	I	Input port, External interrupt, UART0 received data	—	—	—	—	—	—

PAD No.		Primary function			Secondary function			Tertiary function		
Q419	Q419C	Pin name	I/O	Function	Pin name	I/O	Function	Pin name	I/O	Function
89	89	P03/EXI3	I	Input port, External interrupt	—	—	—	—	—	—
83	83	P10	I	Input port	OSC0	I	High-speed oscillation	—	—	—
82	82	P11	I	Input port	OSC1	O	High-speed oscillation	—	—	—
4	4	P20/LED0	O	Output port	LSCLK	O	Low-speed clock output	—	—	—
5	5	P21/LED1	O	Output port	OUTCLK	O	High-speed clock output	—	—	—
6	6	P22/LED2	O	Output port	MD0	O	Melody 0 output	—	—	—
90	90	P30	I/O	Input/output port	IN0	I	RC type ADC0 oscillation input pin	—	—	—
91	91	P31	I/O	Input/output port	CS0	O	RC type ADC0 reference capacitor connection pin	—	—	—
93	93	P32	I/O	Input/output port	RS0	O	RC type ADC0 reference resistor connection pin	—	—	—
94	94	P33	I/O	Input/output port	RT0	O	RC type ADC0 measurement resistor sensor connection pin	—	—	—
92	92	P34	I/O	Input/output port	RCT0	O	RC type ADC0 resistor/capacitor sensor connection pin	PWM0	O	PWM output
95	95	P35	I/O	Input/output port	RCM	O	RC type ADC oscillation monitor	—	—	—
7	7	P40	I/O	Input/output port	SDA	I/O	I2C data input/output	SIN0	I	SSIO0 data input
8	8	P41	I/O	Input/output port	SCL	I/O	I2C clock input/output	SCK0	I/O	SSIO0 synchronous clock
9	9	P42	I/O	Input/output port	RXD0	I	UART data input	SOUT0	O	SSIO0 data output
10	10	P43	I/O	Input/output port	TXD0	O	UART data output	PWM0	O	PWM output
11	11	P44/T02P0CK	I/O	Input/output port, Timer 0/Timer 2/PWM0 external clock input	IN1	I	RC type ADC1 oscillation input pin	SIN0	I	SSIO0 data input
12	12	P45/T13CK	I/O	Input/output port, Timer 1/Timer 3 external clock input	CS1	O	RC type ADC1 reference capacitor connection pin	SCK0	I/O	SSIO0 synchronous clock
13	13	P46	I/O	Input/output port	RS1	O	RC type ADC1 reference resistor connection pin	SOUT0	O	SSIO0 data output
14	14	P47	I/O	Input/output port	RT1	O	RC type ADC1 resistor sensor connection pin	—	—	—
84	84	P50/EXI8	I/O	Input/output port, External interrupt	MD0	O	Melody 0 output	SIN1	I	SSIO1 data input
85	85	P51/EXI8	I/O	Input/output port, External interrupt	—	—	—	SCK1	I/O	SSIO1 synchronous clock input/output
86	86	P52/EXI8	I/O	Input/output port, External interrupt	—	—	—	SOUT1	O	SSIO1 data output
87	87	P53/EXI8	I/O	Input/output port, External interrupt	—	—	—	—	—	—
28	28	COM0	O	LCD common pin	—	—	—	—	—	—
29	29	COM1	O	LCD common pin	—	—	—	—	—	—
30	30	COM2	O	LCD common pin	—	—	—	—	—	—
31	31	COM3	O	LCD common pin	—	—	—	—	—	—

PAD No.		Primary function			Secondary function			Tertiary function		
Q419	Q419C	Pin name	I/O	Function	Pin name	I/O	Function	Pin name	I/O	Function
32	32	SEG0	O	LCD segment pin	—	—	—	—	—	—
33	33	SEG1	O	LCD segment pin	—	—	—	—	—	—
34	34	SEG2	O	LCD segment pin	—	—	—	—	—	—
35	35	SEG3	O	LCD segment pin	—	—	—	—	—	—
36	36	SEG4	O	LCD segment pin	—	—	—	—	—	—
37	37	SEG5	O	LCD segment pin	—	—	—	—	—	—
38	38	SEG6	O	LCD segment pin	—	—	—	—	—	—
39	39	SEG7	O	LCD segment pin	—	—	—	—	—	—
40	40	SEG8	O	LCD segment pin	—	—	—	—	—	—
41	41	SEG9	O	LCD segment pin	—	—	—	—	—	—
42	42	SEG10	O	LCD segment pin	—	—	—	—	—	—
43	43	SEG11	O	LCD segment pin	—	—	—	—	—	—
44	44	SEG12	O	LCD segment pin	—	—	—	—	—	—
45	45	SEG13	O	LCD segment pin	—	—	—	—	—	—
46	46	SEG14	O	LCD segment pin	—	—	—	—	—	—
47	47	SEG15	O	LCD segment pin	—	—	—	—	—	—
48	48	SEG16	O	LCD segment pin	—	—	—	—	—	—
49	49	SEG17	O	LCD segment pin	—	—	—	—	—	—
50	50	SEG18	O	LCD segment pin	—	—	—	—	—	—
51	51	SEG19	O	LCD segment pin	—	—	—	—	—	—
52	52	SEG20	O	LCD segment pin	—	—	—	—	—	—
53	53	SEG21	O	LCD segment pin	—	—	—	—	—	—
54	54	SEG22	O	LCD segment pin	—	—	—	—	—	—
55	55	SEG23	O	LCD segment pin	—	—	—	—	—	—
56	56	SEG24	O	LCD segment pin	—	—	—	—	—	—
57	57	SEG25	O	LCD segment pin	—	—	—	—	—	—
58	58	SEG26	O	LCD segment pin	—	—	—	—	—	—
59	59	SEG27	O	LCD segment pin	—	—	—	—	—	—
60	60	SEG28	O	LCD segment pin	—	—	—	—	—	—
61	61	SEG29	O	LCD segment pin	—	—	—	—	—	—
62	62	SEG30	O	LCD segment pin	—	—	—	—	—	—
63	63	SEG31	O	LCD segment pin	—	—	—	—	—	—
64	64	SEG32	O	LCD segment pin	—	—	—	—	—	—
65	65	SEG33	O	LCD segment pin	—	—	—	—	—	—
66	66	SEG34	O	LCD segment pin	—	—	—	—	—	—
67	67	SEG35	O	LCD segment pin	—	—	—	—	—	—
68	68	SEG36	O	LCD segment pin	—	—	—	—	—	—
69	69	SEG37	O	LCD segment pin	—	—	—	—	—	—
70	70	SEG38	O	LCD segment pin	—	—	—	—	—	—
71	71	SEG39	O	LCD segment pin	—	—	—	—	—	—
72	—	SEG40	O	LCD segment pin	—	—	—	—	—	—
73	—	SEG41	O	LCD segment pin	—	—	—	—	—	—
74	—	SEG42	O	LCD segment pin	—	—	—	—	—	—
75	—	SEG43	O	LCD segment pin	—	—	—	—	—	—
76	—	SEG44	O	LCD segment pin	—	—	—	—	—	—
77	—	SEG45	O	LCD segment pin	—	—	—	—	—	—
78	—	SEG46	O	LCD segment pin	—	—	—	—	—	—
79	—	SEG47	O	LCD segment pin	—	—	—	—	—	—
—	72	P60	I/O	Input/output port	—	—	—	—	—	—
—	73	P61	I/O	Input/output port	—	—	—	—	—	—
—	74	P62	I/O	Input/output port	—	—	—	—	—	—
—	75	P63	I/O	Input/output port	—	—	—	—	—	—
—	76	P64	I/O	Input/output port	—	—	—	—	—	—

PAD No.		Primary function			Secondary function			Tertiary function		
Q419	Q419C	Pin name	I/O	Function	Pin name	I/O	Function	Pin name	I/O	Function
—	77	P65	I/O	Input/output port	—	—	—	—	—	—
—	78	P66	I/O	Input/output port	—	—	—	—	—	—
—	79	P67	I/O	Input/output port	—	—	—	—	—	—

PIN DESCRIPTION

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
System				
RESET_N	I	Reset input pin. When this pin is set to a “L” level, system reset mode is set and the internal section is initialized. When this pin is set to a “H” level subsequently, program execution starts. A pull-up resistor is internally connected.	—	Negative
XT0	I	Crystal connection pin for low-speed clock.	—	—
XT1	O	A 32.768 kHz crystal oscillator (see measuring circuit 1) is connected to this pin. Capacitors CDL and CGL are connected across this pin and V_{SS} as required.	—	—
OSC0	I	Crystal/ceramic connection pin for high-speed clock.	Secondary	—
OSC1	O	A crystal or ceramic is connected to this pin (4.1 MHz max.). Capacitors CDH and CGH (see measuring circuit 1) are connected across this pin and V_{SS}. This pin is used as the secondary function of the P10 pin(OSC0) and P11 pin(OSC1).	Secondary	—
LSCLK	O	Low-speed clock output pin. This pin is used as the secondary function of the P20 pin.	Secondary	—
OUTCLK	O	High-speed clock output pin. This pin is used as the secondary function of the P21 pin.	Secondary	—
General-purpose input port				
P00-P03	I	General-purpose input port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
P10-P11	I	General-purpose input port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
General-purpose output port				
P20-P22	O	General-purpose output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
General-purpose input/output port				
P30-P35	I/O	General-purpose input/output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
P40-P47	I/O	General-purpose input/output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
P50-P53	I/O	General-purpose input/output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
P60-P67	I/O	General-purpose input/output port. These pins are for the ML610Q419C, but are not provided in the ML610Q419.	Primary	Positive

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
UART				
TXD0	O	UART data output pin. This pin is used as the secondary function of the P43 pin.	Secondary	Positive
RXD0	I	UART data input pin. This pin is used as the secondary function of the P42 or the primary function of the P02 pin.	Primary/Secondary	Positive
I^2C bus interface				
SDA	I/O	I^2C data input/output pin. This pin is used as the secondary function of the P40 pin. This pin has an NMOS open drain output. When using this pin as a function of the I^2C, externally connect a pull-up resistor.	Secondary	Positive
SCL	O	I^2C clock output pin. This pin is used as the secondary function of the P41 pin. This pin has an NMOS open drain output. When using this pin as a function of the I^2C, externally connect a pull-up resistor.	Secondary	Positive
Synchronous serial (SSIO)				
SCK0	I/O	Synchronous serial clock input/output pin. This pin is used as the tertiary function of the P41 or P45 pin.	Tertiary	—
SIN0	I	Synchronous serial data input pin. This pin is used as the tertiary function of the P40 or P44 pin.	Tertiary	Positive
SOUT0	O	Synchronous serial data output pin. This pin is used as the tertiary function of the P42 or P46 pin.	Tertiary	Positive
SCK1	I/O	Synchronous serial clock input/output pin. This pin is used as the tertiary function of the P51 pin.	Tertiary	—
SIN1	I	Synchronous serial data input pin. This pin is used as the tertiary function of the P50 pin.	Tertiary	Positive
SOUT1	O	Synchronous serial data output pin. This pin is used as the tertiary function of the P52 pin.	Tertiary	Positive
PWM				
PWM0	O	PWM0 output pin. This pin is used as the tertiary function of the P43 or P34 pin.	Tertiary	Positive
T0P0CK	I	PWM0 external clock input pin. This pin is used as the primary function of the P44 pin.	Primary	—
External interrupt				
EXI0-3	I	External maskable interrupt input pins. Interrupt enable and edge selection can be performed for each bit by software. These pins are used as the primary functions of the P00-P03 pins.	Primary	Positive/ negative
EXI8	I	External maskable interrupt input pins. Interrupt enable and edge selection can be performed for each bit by software. These pins are used as the primary functions of the P50-P53 pins.	Primary	Positive/ negative
Capture				
CAP0	I	Capture trigger input pins. The value of the time base counter is captured in the register synchronously with the interrupt edge selected by software. These pins are used as the primary functions of the P00 pin(CAP0) and P01 pin(CAP1).	Primary	—
CAP1	I		Primary	—
Timer				
T0P0CK	I	External clock input pin used for Timer 0. This pin is used as the primary function of the P44 pin.	Primary	—
T1P1CK	I	External clock input pin used for Timer 1. This pin is used as the primary function of the P45 pin.	Primary	—
Melody				
MD0	O	Melody/buzzer signal output pin. This pin is used as the secondary function of the P22 pin.	Secondary	Positive/ negative
LED drive				
LED0-2	O	Nch open drain output pins to drive LED.	Primary	Positive/ negative

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
RC oscillation type A/D converter				
IN0	I	Channel 0 oscillation input pin. This pin is used as the secondary function of the P30 pin.	Secondary	—
CS0	O	Channel 0 reference capacitor connection pin. This pin is used as the secondary function of the P31 pin.	Secondary	—
RS0	O	This pin is used as the secondary function of the P32 pin which is the reference resistor connection pin of Channel 0.	Secondary	—
RT0	O	Resistor sensor connection pin of Channel 0 for measurement. This pin is used as the secondary function of the P34 pin.	Secondary	—
CRT0	O	Resistor/capacitor sensor connection pin of Channel 0 for measurement. This pin is used as the secondary function of the P33 pin.	Secondary	—
RCM	O	RC oscillation monitor pin. This pin is used as the secondary function of the P35 pin.	Secondary	—
IN1	I	Oscillation input pin of Channel 1. This pin is used as the secondary function of the P44 pin.	Secondary	—
CS1	O	Reference capacitor connection pin of Channel 1. This pin is used as the secondary function of the P45 pin.	Secondary	—
RS1	O	Reference resistor connection pin of Channel 1. This pin is used as the secondary function of the P46 pin.	Secondary	—
RT1	O	Resistor sensor connection pin for measurement of Channel 1. This pin is used as the secondary function of the P47 pin.	Secondary	—
Successive approximation type A/D converter				
AV_{SS}	—	Negative power supply pin for successive approximation type A/D converter.	—	—
AV_{DD}	—	Positive power supply pin for successive approximation type A/D converter.	—	—
V_{REF}	—	Reference power supply pin for successive approximation type A/D converter.	—	—
AIN0	I	Channel 0 analog input for successive approximation type A/D converter.	—	—
AIN1	I	Channel 1 analog input for successive approximation type A/D converter.	—	—
AIN2	I	Channel 2 analog input for successive approximation type A/D converter.	—	—
AIN3	I	Channel 3 analog input for successive approximation type A/D converter.	—	—
LCD drive signal				
COM0-3	O	Common output pins.	—	—
SEG0-39	O	Segment output pins.	—	—
SEG40-47	O	Segment output pins. These pins are for the ML610Q419, but are not provided in the ML610Q419C.	—	—
LCD driver power supply				
V_{L1}	—	Power supply pins for LCD bias (internally generated). Capacitors Ca, Cb, and Cc (see measuring circuit 1) are connected between V_{SS} and V_{L1}, V_{L2}, and V_{L3} respectively.	—	—
V_{L2}	—		—	—
V_{L3}	—		—	—
C1	—	Power supply pins for LCD bias (internally generated). Capacitors C12 is connected between C1 and C2.	—	—
C2	—		—	—
For testing				
TEST0	I/O	Input/output pin for testing. A pull-down resistor is internally connected.	—	—
TEST1_N	I	Input/output pin for testing. A pull-up resistor is internally connected.	—	—
Power supply				
V_{SS}	—	Negative power supply pin.	—	—
V_{DD}	—	Positive power supply pin.	—	—
V_{DDL}	—	Positive power supply pin (internally generated) for internal logic. Capacitors CL0 and CL1 (see measuring circuit 1) are connected between this pin and V_{SS}.	—	—

TERMINATION OF UNUSED PINS

Table 3 shows methods of terminating the unused pins.

Table 3 Termination of Unused Pins

Pin	Recommended pin termination
AV_{DD}	V_{SS}
AV_{SS}	V_{SS}
V_{REF}	V_{SS}
AIN0, AIN1, AIN2, AIN3	Open
V_{L1}, V_{L2}, V_{L3}	Open
C1, C2	Open
RESET_N	Open
TEST0	Open
TEST1_N	Open
P00 to P03	V_{DD} or V_{SS}
P10 to P11	V_{DD}
P20 to P22	Open
P30 to P35	Open
P40 to P47	Open
P50 to P53	Open
P60 to P67	Open
COM0 to 3	Open
SEG0 to 47	Open

Note:
It is recommended to set the unused input ports and input/output ports to the inputs with pull-down resistors/pull-up resistors or the output mode since the supply current may become excessively large if the pins are left open in the high impedance input setting.

The main difference points of ML610Q419 and ML610Q419C

Table 4 The main difference points of ML610Q419 and ML610Q419C

Function	ML610Q419	ML610Q419C
LCD SEG	SEG47 to SEG0	SEG39 to SEG0

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

(V_{SS} = 0V)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage 1	V_{DD}	Ta = 25°C	–0.3 to +4.6	V
Power supply voltage 2	AV_{DD}	Ta = 25°C	–0.3 to +4.6	V
Power supply voltage 3	V_{DDL}	Ta = 25°C	–0.3 to +3.6	V
Power supply voltage 4	V_{L1}	Ta = 25°C	–0.3 to +1.75	V
Power supply voltage 5	V_{L2}	Ta = 25°C	–0.3 to +3.5	V
Power supply voltage 6	V_{L3}	Ta = 25°C	–0.3 to +5.25	V
Input voltage	V_{IN}	Ta = 25°C	–0.3 to V_{DD}+0.3	V
Output voltage	V_{OUT}	Ta = 25°C	–0.3 to V_{DD}+0.3	V
Output current 1	I_{OUT1}	Port3–5, Ta = 25°C	–12 to +11	mA
Output current 2	I_{OUT2}	Port2, Ta = 25°C	–12 to +20	mA
Power dissipation	PD	Ta = 25°C	0.9	W
Storage temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(V_{SS} = 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T_{OP}	—	-20～+70	°C
Operating voltage	V_{DD}	f_{OP} = 30k to 625kHz	1.1～3.6	V
		f_{OP} = 30k to 4.2MHz	1.8～3.6	V
Operating frequency (CPU)	f_{OP}	VDD = 1.1～3.6V	30k～36k	Hz
		VDD = 1.3～3.6V	30k～650k	
		VDD = 1.8～3.6V	30k～4.2M	
Capacitor externally connected to V_{DD} pin	C_V	—	More than 2.2±30%	µF
Capacitor externally connected to V_{DDL} pin	C_{L0}	—	2.2±30%	µF
	C_{L1}	—	0.1±30%	
Capacitors externally connected to $V_{L1, 2, 3}$ pins	$C_{a, b, c}$	—	0.1±30%	µF
Capacitors externally connected across C1 and C2 pins	C_{12}	—	0.47±30%	µF

CLOCK GENERATION CIRCUIT OPERATING CONDITIONS

(V_{SS} = 0V)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Low-speed crystal oscillation frequency	f_{XTL}	—	—	32.768k	—	Hz
Recommended equivalent series resistance value of low-speed crystal oscillation	R_L	—	—	—	40k	Ω
Low-speed crystal oscillation external capacitor *1	C_{DL}/C_{GL}	C_L=6pF of crystal oscillation *2	—	3	—	pF
		C_L=9pF of crystal oscillation	—	9	—	
		C_L=12pF of crystal oscillation	—	15	—	
High-speed crystal/ceramic oscillation frequency	f_{XTH}	—	—	4.0M / 4.096M	—	Hz
High-speed crystal oscillation external capacitor	C_{DH}	—	—	24	—	pF
	C_{GH}	—	—	24	—	

*1: The external C_{DL} and C_{GL} need to be adjusted in consideration of variation of internal loading capacitance C_D and C_G, and other additional capacitance such as PCB layout.

*2: When using a crystal oscillator C_L = 6pF, there is a possibility that can not be adjusted by external C_{DL} and C_{GL}.

OPERATING CONDITIONS OF FLASH ROM

(V_{SS} = 0V)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Operating temperature	T_{OP}	Flash ROM, At write/erase	0	—	+40	°C
		Data flash memory, At write/erase	-40	—	+85	°C
Operating voltage	V_{DD}	At write/erase	1.8	—	3.6	V
Rewrite counts	C_{EP}	Flash ROM	—	—	100	cycles
		Data flash memory	—	—	10k	
Data retention	Y_{DR}	Flash ROM	10	—		years
		Data flash memory, 1000 cycles	10	—		
Chip-erase time	t_{CERASE}	—		85	100	ms
Block-erase time	t_{BERASE}	—		85	100	ms
Sector-erase time	t_{SERASE}	—		85	100	ms
1-word (16 bits) write time	t_{WRITE}	—		18	40	μs

DC CHARACTERISTICS (1/5)

(V_{DD} = 1.1 to 3.6V, AV_{DD} =2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = -20 to +70°C, unless otherwise specified)

Parameter	Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Measuring circuit
500kHz RC oscillation frequency	f_{RC}	V_{DD} = 1.3 to 3.6V	Ta = 25°C	Typ. −10%	500	Typ. +10%	kHz	1
			Ta = -20 to +70°C	Typ. −25%	500	Typ. +25%	kHz	
PLL oscillation frequency*4	f_{PLL}	LSCLK = 32.768kHz V_{DD} = 1.8 to 3.6V		-2.5%	8.192	+2.5%	MHz	
Low-speed crystal oscillation start time*2	T_{XTL}	—		—	0.3	2	s	
500kHz RC oscillation start time	T_{RC}	—		—	50	500	µs	
High-speed crystal oscillation start time*3	T_{XTH}	V_{DD} = 1.8 to 3.6V		—	2	20	ms	
PLL oscillation start time	T_{PLL}	V_{DD} = 1.8 to 3.6V		—	1	10		
Low-speed oscillation stop detect time*1	T_{STOP}	—		0.2	3	20		
Reset pulse width	P_{RST}	—		200	—	—	µs	
Reset noise elimination pulse width	P_{NRST}	—		—	—	0.3		
Power-on reset activation power rise time	T_{POR}	—		—	—	10	ms	
Low level reset detection voltage	V_{LLR}	COLD0=0*5		—	—	1.1	V	
		COLD0=1*5		—	—	1.8		
Low level reset detection time	T_{LLR}	—		200	—	—	µs	
Release reset voltage	V_{RER}	COLD0=0*5		—	—	1.1	V	
		COLD0=1*5		—	—	1.8		

*1: When low-speed crystal oscillation stops for a duration more than the low-speed oscillation stop detect time, the system is reset to shift to system reset mode.

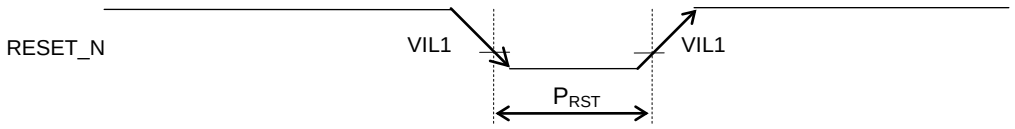
*2 : Use 32.768kHz crystal resonator DT-26 (Load capacitance 6pF) (made by KDS:DAISHINKU CORP.) is used (C_{GL}=C_{DL}=1pF).

*3 : Use 4.096MHz Crystal Oscillator CHC49SFWB (Kyocera).

*4 : 1024 clock average.

*5 : The COLD0 bit is the code-option which is set up into the Flash memory.

Reset pulse width (P_{RST})



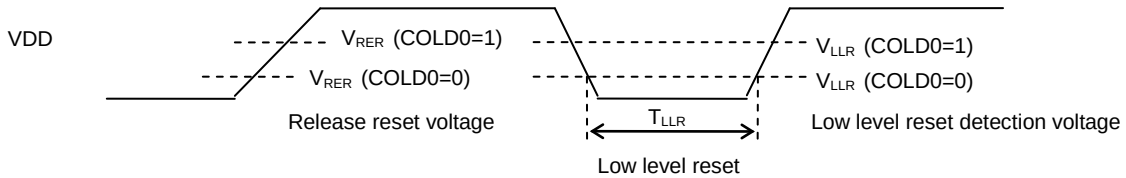
Reset pulse width (P_{RST})

Power-on reset activation power rise time (T_{POR})



Power-on reset activation power rise time (T_{POR})

Low level reset detection time(T_{LLR})



Low level reset detection time(T_{LLR})

DC CHARACTERISTICS (2/5)

(V_{DD} = 1.1 to 3.6V, AV_{DD} =2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = -20 to +70°C, unless otherwise specified)

Parameter	Symbol	Condition		Rating Min.	Rating Min.	Rating Min.	Unit	Measuring circuit
V_{L1} voltage	V_{L1}	V_{DD} = 3.0V, Tj = 25°C	CN4-0 = 00H	0.89	0.94	0.99	V	1
			CN4-0 = 01H	0.91	0.96	1.01		
			CN4-0 = 02H	0.93	0.98	1.03		
			CN4-0 = 03H	0.95	1.00	1.05		
			CN4-0 = 04H	0.97	1.02	1.07		
			CN4-0 = 05H	0.99	1.04	1.09		
			CN4-0 = 06H	1.01	1.06	1.11		
			CN4-0 = 07H	1.03	1.08	1.13		
			CN4-0 = 08H	1.05	1.10	1.15		
			CN4-0 = 09H	1.07	1.12	1.17		
			CN4-0 = 0AH	1.09	1.14	1.19		
			CN4-0 = 0BH	1.11	1.16	1.21		
			CN4-0 = 0CH	1.13	1.18	1.23		
			CN4-0 = 0DH	1.15	1.20	1.25		
			CN4-0 = 0EH	1.17	1.22	1.27		
			CN4-0 = 0FH	1.19	1.24	1.29		
			CN4-0 = 10H	1.21	1.26	1.31		
			CN4-0 = 11H	1.23	1.28	1.33		
			CN4-0 = 12H	1.25	1.30	1.35		
			CN4-0 = 13H	1.27	1.32	1.37		
			CN4-0 = 14H*[1]	1.29	1.34	1.39		
			CN4-0 = 15H*[1]	1.31	1.36	1.41		
			CN4-0 = 16H*[1]	1.33	1.38	1.43		
			CN4-0 = 17H*[1]	1.35	1.40	1.45		
			CN4-0 = 18H*[1]	1.37	1.42	1.47		
			CN4-0 = 19H*[1]	1.39	1.44	1.49		
			CN4-0 = 1AH*[1]	1.41	1.46	1.51		
			CN4-0 = 1BH*[1]	1.43	1.48	1.53		
			CN4-0 = 1CH*[1]	1.45	1.50	1.55		
			CN4-0 = 1DH*[1]	1.47	1.52	1.57		
			CN4-0 = 1EH*[1]	1.49	1.54	1.59		
			CN4-0 = 1FH*[1]	1.51	1.56	1.61		
V_{L1} temperature deviation	ΔV_{L1}	V_{DD} = 3.0V		—	-1.5	—	mV/°C	
V_{L1} voltage dependency	ΔV_{L1}	V_{DD} = 1.3 to 3.6V		—	5	20	mV/V	
V_{L2} voltage	V_{L2}	VDD = 3.0V, Tj = 25°C, 300kΩ load (V_{L3}–V_{SS})	1/2bias	—	V_{L1}×1	—	V	
			1/3bias	Typ. ×09	V_{L1}×2	—		
V_{L3} voltage	V_{L3}		1/2bias	Typ. ×09	V_{L1}×2	—		
			1/3bias	Typ. ×09	V_{L1}×3	—		
LCD bias voltage generation time	T_{BIAS}	—		—	—	100	ms	

DC CHARACTERISTICS (3/5)

(V_{DD} = 1.1 to 3.6V, AV_{DD} =2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = -20 to +70°C, unless otherwise specified)

Parameter	Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Measuring circuit
BLD threshold voltage	V_{BLD}	V_{DD} = 1.35 to 3.6V	LD2–0 = 0H	Typ. –2%	1.35	Typ. +2%	V	1
			LD2–0 = 1H		1.4			
			LD2–0 = 2H		1.45			
			LD2–0 = 3H		1.5			
			LD2–0 = 4H		1.6			
			LD2–0 = 5H		1.7			
			LD2–0 = 6H		1.8			
			LD2–0 = 7H		1.9			
			LD2–0 = 8H		2.0			
			LD2–0 = 9H		2.1			
			LD2–0 = 0AH		2.2			
			LD2–0 = 0BH		2.3			
			LD2–0 = 0CH		2.4			
			LD2–0 = 0DH		2.5			
			LD2–0 = 0EH		2.7			
			LD2–0 = 0FH		2.9			
BLD threshold voltage temperature deviation	ΔV_{BLD}	V_{DD} = 1.35 to 3.6V		—	0	—	%/°C	
Supply current 1	IDD1	CPU: In STOP state. Low-speed/high-speed oscillation: stopped.	Ta = 25°C	—	0.4	0.8	μA	
			Ta = -20 to +70°C	—	—	8		
Supply current 2	IDD2	CPU: In HALT state (LTBC, RTC: Operating*3*5). High-speed oscillation: Stopped. LCD/BIAS circuits: Stopped.	Ta = 25°C	—	0.9	1.8	μA	
			Ta = -20 to +70°C	—	—	9		
Supply current 3	IDD3	CPU: In 32.768kHz operating state.*1*3 High-speed oscillation: Stopped. LCD/BIAS circuits: Operating.*2	Ta = 25°C	—	5	8	μA	
			Ta = -20 to +70°C	—	—	15		
Supply current 4	IDD4	CPU: In 500kHz CR operating state. LCD/BIAS circuits: Operating.*2*3	Ta = 25°C	—	80	100	μA	
			Ta = -20 to +70°C	—	—	120		
Supply current 5	IDD5	CPU: In 4.096MHz operating state.*2*3 PLL: In oscillating state. LCD/BIAS circuits: Operating. *2 V_{DD} = 1.8 to 3.6V	Ta = 25°C	—	0.9	1.0	mA	
			Ta = -20 to +70°C	—	—	1.2		
Supply current 6	IDD6	CPU: In 4.096MHz operating state.*2 PLL: In oscillating state. *3*4 A/D: In operating state. LCD/BIAS circuits: Operating. *2 V_{DD} = AV_{DD} = 3.0V	Ta = 25°C	—	1.5	1.6	mA	
			Ta = -20 to +70°C	—	—	2.5		

*1 : CPU operating rate is 100% (No HALT state).
*2 : All SEGs: off waveform, No LCD panel load, 1/3 bias, 1/3 duty, Frame frequency: Approx. 64 Hz, Bias voltage multiplying clock: 1/128 LSCLK (256Hz)
*3 : Use 32.768kHz crystal resonator DT-26 (Load capacitance 6pF) (made by KDS:DAISHINKU CORP.) is used (C_{GL}=C_{DL}=1pF).
*4 : Use 4.096MHz Crystal Oscillator CHC49SFWB (Kyocera).
*5 : Significant bits of BLKCON0~BLKCON4 registers are all "1".

DC CHARACTERISTICS (4/5)

(V_{DD} = 1.1 to 3.6V, AV_{DD} =2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = -20 to +70°C, unless otherwise specified)

Parameter	Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Measuring circuit
Output voltage 1 (P20–P22/2nd function is selected) (P30–P36) (P40–P47) (P50–P53) (P60–P67)*1	VOH1	IOH1 = –0.5mA, V_{DD} = 1.8 to 3.6V		V_{DD}–0.5	—	—	V	2
		IOH1 = -0.1mA, V_{DD} = 1.3 to 3.6V		V_{DD}–0.3	—	—		
		IOH1 = -0.03mA, VDD = 1.1 to 3.6V		V_{DD}–0.3	—	—		
	VOL1	IOL1 = +0.5mA, V_{DD} = 1.8 to 3.6V		—	—	0.5		
		IOL1 = +0.1mA, V_{DD} = 1.3 to 3.6V		—	—	0.5		
		IOL1 = +0.03mA, V_{DD} = 1.1 to 3.6V		—	—	0.3		
Output voltage 2 (P20–P22/2nd function is Not selected)	VOH2	IOH1 = –0.5mA, V_{DD} = 1.8 to 3.6V		V_{DD}–0.5	—	—		
		IOH1 = -0.1mA, V_{DD} = 1.3 to 3.6V		V_{DD}–0.3	—	—		
		IOH1 = -0.03mA, V_{DD} = 1.1 to 3.6V		V_{DD}–0.3	—	—		
	VOL2	IOL2 = +5mA, V_{DD} = 1.8 to 3.6V		—	—	0.5		
Output voltage 3 (P40–P41)	VOL3	IOL3 = +3mA, V_{DD} = 2.0 to 3.6V (when I^2C mode is selected)		—	—	0.4		
Output voltage 4 (COM0–3) (SEG0–39) (SEG40–47)*2	VOH4	IOH4 = –0.05mA, VL1=1.2V		V_{L3}–0.2	—	—		
	VOML4	IOMH4 = +0.05mA, VL1=1.2V		—	—	V_{L2}+0.2		
	VOML4S	IOMH4S = –0.05mA, VL1=1.2V		V_{L2}–0.2	—	—		
	VOLM4	IOML4 = +0.05mA, VL1=1.2V		—	—	V_{L1}+0.2		
	VOLM4S	IOML4S = –0.05mA, VL1=1.2V		V_{L1}–0.2	—	—		
	VOL4	IOL4 = +0.05mA, VL1=1.2V		—	—	0.2		
Output leakage (P20–P22) (P30–P35) (P40–P47) (P50–P53) (P60–P67)*1	IOOH	VOH = V_{DD} (in high-impedance state)		—	—	1	µA	3
	IOOL	VOL = V_{SS} (in high-impedance state)		–1	—	—		
Input current 1 (RESET_N) (TEST1_N)	IIH1	VIH1 = V_{DD}		0	—	1	µA	4
	IIL1	VIL1 = V_{SS}	V_{DD} = 1.8 to 3.6V	–600	–300	–20		
			V_{DD} = 1.3 to 3.6V	–600	–300	-10		
			V_{DD} = 1.1 to 3.6V	–600	–300	-2		
Input current 1 (TEST0)	IIH1	VIH1 = V_{DD}	V_{DD} = 1.8 to 3.6V	20	300	600		
			V_{DD} = 1.3 to 3.6V	10	300	600		
			V_{DD} = 1.1 to 3.6V	2	300	600		
	IIL1	VIL1 = V_{ss}		-1	—	—		
Input current 2 (P00–P03) (P10–P11) (P30–P35) (P40–P47) (P50–P53) (P60–P67)*1	IIH2	VIH2 = V_{DD} (when pulled-down)	V_{DD} = 1.8 to 3.6V	2	30	200		
			V_{DD} = 1.3 to 3.6V	0.2	30	200		
			V_{DD} = 1.1 to 3.6V	0.01	30	200		
	IIL2	VIL2 = V_{SS} (when pulled-up)	V_{DD} = 1.8 to 3.6V	–200	–30	–2		
			V_{DD} = 1.3 to 3.6V	–200	–30	-0.2		
			V_{DD} = 1.1 to 3.6V	–200	–30	-0.01		
	IIH2Z	VIH2 = V_{DD} (in high-impedance state)		—	—	1		
	IIL2Z	VIL2 = V_{SS} (in high-impedance state)		–1	—	—		

*1: ML610Q419C only

*2: ML610Q419 only

DC CHARACTERISTICS (5/5)

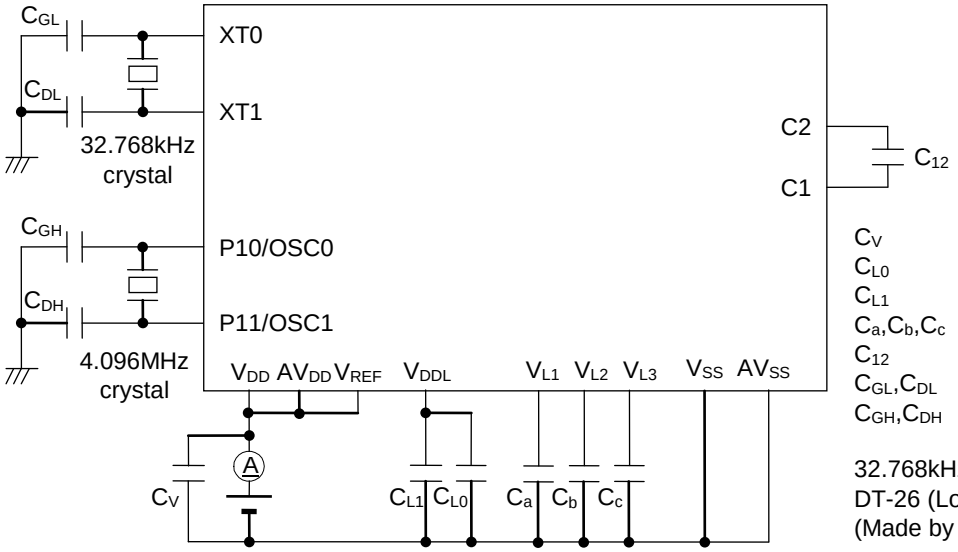
(V_{DD} = 1.1 to 3.6V, AV_{DD} =2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = -20 to +70°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Input voltage 1 (RESET_N) (TEST1_N) (TEST0) (P00–P03) (P10–P11) (P31–P35) (P40–P43) (P45–P47) (P50–P53) (P60–P67)*1	VIH1	V_{DD} = 1.3 to 3.6V	0.7 ×V_{DD}	—	V_{DD}	V	5
		V_{DD} = 1.1 to 3.6V	0.7 ×V_{DD}	—	V_{DD}		
	VIL1	V_{DD} = 1.3 to 3.6V	0	—	0.3 ×V_{DD}		
		V_{DD} = 1.1 to 3.6V	0	—	0.2 ×V_{DD}		
Input voltage 2 (P30, P44)	VIH2	—	0.7 ×V_{DD}	—	V_{DD}		
	VIL2	—	0	—	0.3 ×V_{DD}		
Input pin capacitance (P00–P03) (P10–P11) (P30–P35) (P40–P47) (P50–P53) (P60–P67)*1	CIN	f = 10kHz V_{rms} = 50mV Ta = 25°C	—	—	5	pF	—

*1: ML610Q419C only

MEASURING CIRCUITS

MEASURING CIRCUIT 1

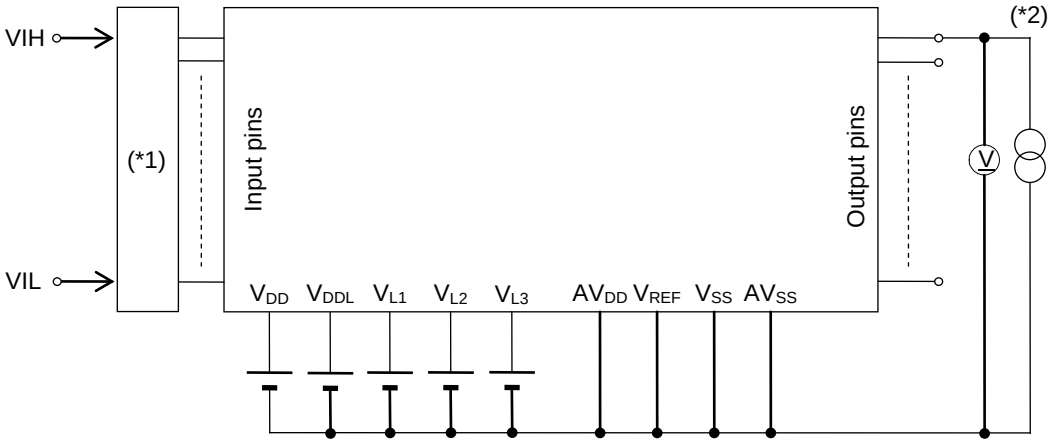


C_V	: >2.2µF
C_{L0}	: 2.2µF
C_{L1}	: 0.1µF
C_a,C_b,C_c	: 0.1µF
C_{12}	: 0.47µF
C_{GL},C_{DL}	: 1pF
C_{GH},C_{DH}	: 24pF

32.768kHz crystal resonator
DT-26 (Load capacitance 6pF)
(Made by KDS:DAISHINKU CORP.)

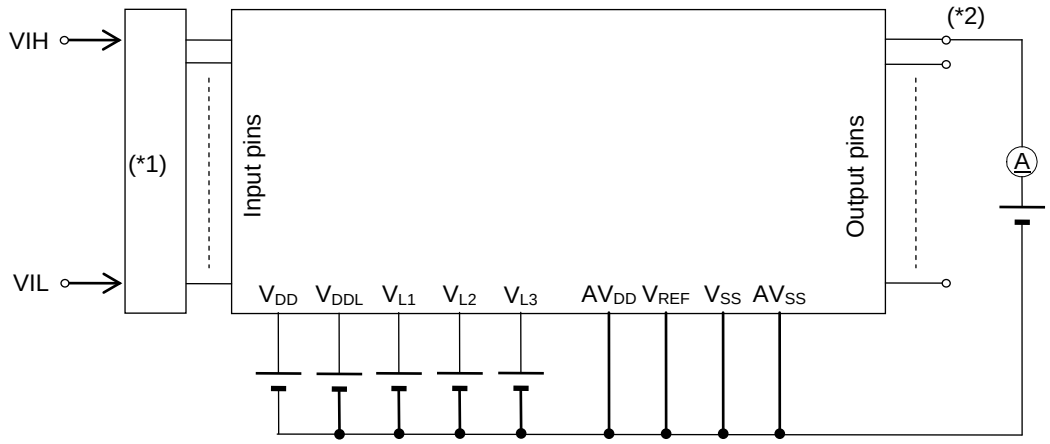
4.096MHz crystal:
HC49SFWB (Kyocera)

MEASURING CIRCUIT 2



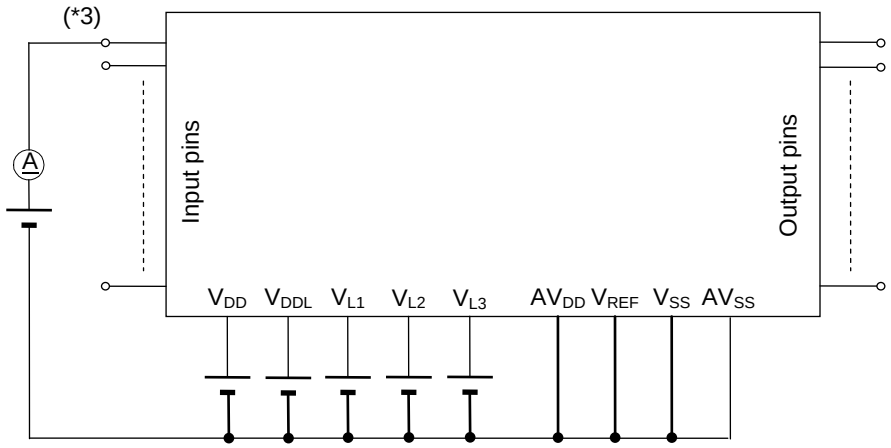
(*1) Input logic circuit to determine the specified measuring conditions.
(*2) Measured at the specified output pins.

MEASURING CIRCUIT 3



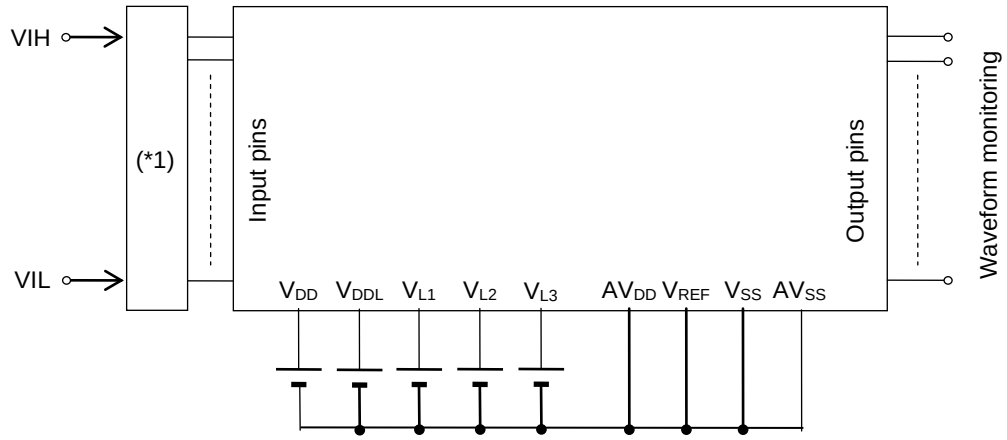
*1: Input logic circuit to determine the specified measuring conditions.
*2: Measured at the specified output pins.

MEASURING CIRCUIT 4



*3: Measured at the specified output pins.

MEASURING CIRCUIT 5

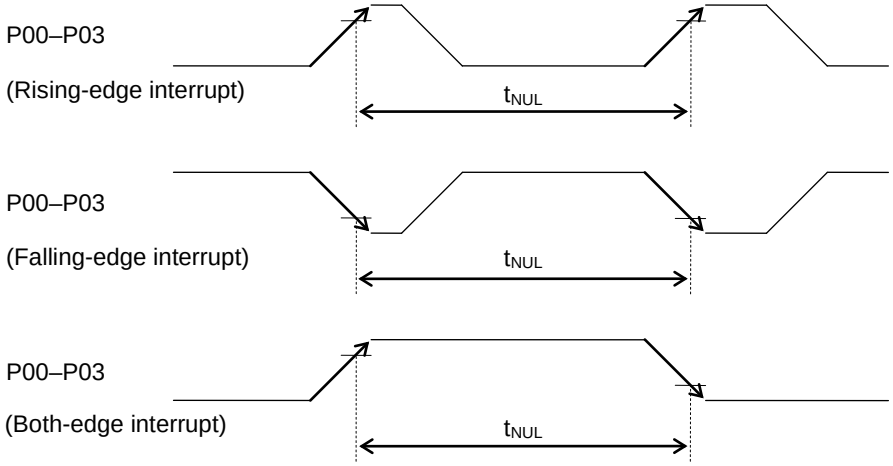


*1: Input logic circuit to determine the specified measuring conditions.

AC CHARACTERISTICS (External Interrupt)

(V_{DD} = 1.1 to 3.6V, AV_{DD} =2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = -20 to +70°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
External interrupt disable period	t_{NUL}	Interrupt: Enabled (MIE = 1), CPU: NOP operation System clock: 32.768kHz	76.8	—	106.8	μs

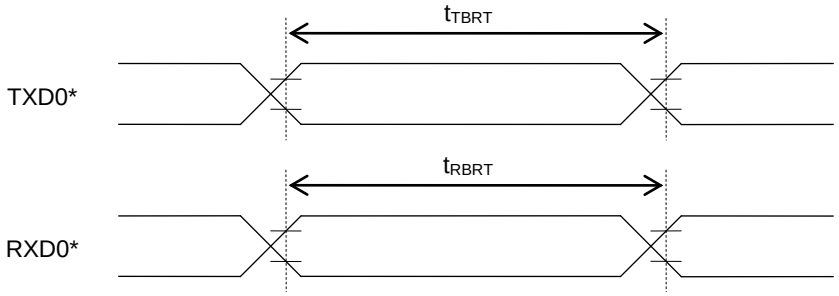


AC CHARACTERISTICS (UART)

(V_{DD} = 1.3 to 3.6V, AV_{DD} =2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = -20 to +70°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Transmit baud rate	t_{TBRT}	—	—	BRT*1	—	s
Receive baud rate	t_{RBRT}	—	BRT*1 −3%	BRT*1	BRT*1 +3%	s

*1: Baud rate period (including the error of the clock frequency selected) set with the UART baud rate register (UA0BRTL,H) and the UART mode register 0 (UA0MOD0).



*: Indicates the secondary function of the port.

AC CHARACTERISTICS (Synchronous Serial Port)

(V_{DD} = 1.3 to 3.6V, AV_{DD} =2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = -20 to +70°C, unless otherwise specified)

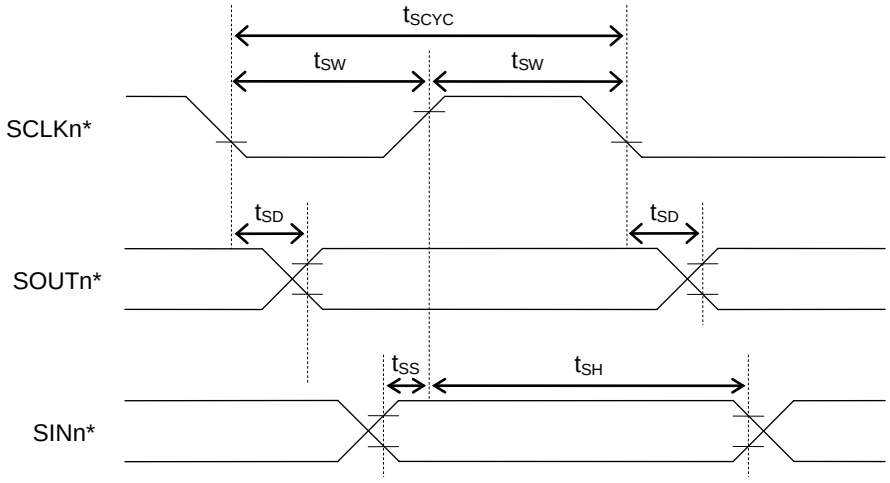
Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCLKn input cycle (slave mode)	t_{SCYC}	When high-speed oscillation is not active*2 (V_{DD} = 1.3 to 3.6V)	10	—	—	µs
		When high-speed oscillation is active*3 (V_{DD} = 1.8 to 3.6V)	1	—	—	µs
SCLKn output cycle (master mode)	t_{SCYC}	—	—	SCLKn*1	—	s
SCLKn input pulse width (slave mode)	t_{SW}	When high-speed oscillation is not active*2 (V_{DD} = 1.3 to 3.6V)	4	—	—	µs
		When high-speed oscillation is active*3 (V_{DD} = 1.8 to 3.6V)	0.4	—	—	µs
SCLKn output pulse width (master mode)	t_{SW}	—	SCLKn*1 ×0.4	SCLKn*1 ×0.5	SCLKn*1 ×0.6	s
SOUTn output delay time (slave mode)	t_{SD}	When high-speed oscillation is not active*2 (V_{DD} = 1.3 to 3.6V)	—	—	500	ns
		When high-speed oscillation is active*3 (V_{DD} = 1.8 to 3.6V)	—	—	240	
SOUTn output delay time (master mode)	t_{SD}	When high-speed oscillation is not active*2 (V_{DD} = 1.3 to 3.6V)	—	—	500	ns
		When high-speed oscillation is active*3 (V_{DD} = 1.8 to 3.6V)	—	—	240	
SINn input setup time (slave mode)	t_{SS}	—	80	—	—	ns
SINn input setup time (master mode)	t_{SS}	When high-speed oscillation is not active*2 (V_{DD} = 1.3 to 3.6V)	500	—	—	ns
		When high-speed oscillation is active*3 (V_{DD} = 1.8 to 3.6V)	240	—	—	
SINn input hold time	t_{SH}	When high-speed oscillation is not active*2 (V_{DD} = 1.3 to 3.6V)	300	—	—	ns
		When high-speed oscillation is active*3 (V_{DD} = 1.8 to 3.6V)	80	—	—	

n= 0,1

*1: Clock period selected with SnCK3–0 of the serial port n mode register (SIOnMOD1)

*2: When RC oscillation is selected with OSCM1–0 of the frequency control register (FCON0)

*3: When Crystal/ceramic oscillation, built-in PLL oscillation, or external clock input is selected with OSCM1–0 of the frequency control register (FCON0)



*: Indicates the secondary function of the port.

AC CHARACTERISTICS (I2C Bus Interface: Standard Mode 100kHz)

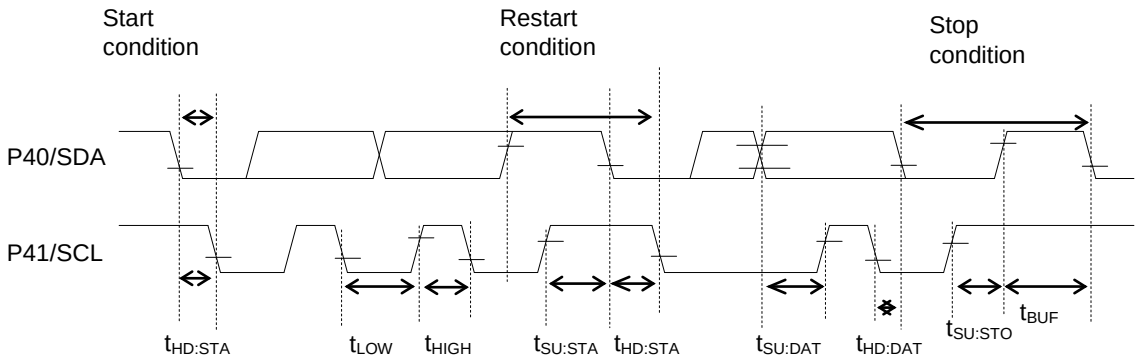
(V_{DD} = 1.8 to 3.6V, AV_{DD} =2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = -20 to +70°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	—	0	—	100	kHz
SCL hold time (start/restart condition)	$t_{HD:STA}$	—	4.0	—	—	µs
SCL "L" level time	t_{LOW}	—	4.7	—	—	µs
SCL "H" level time	t_{HIGH}	—	4.0	—	—	µs
SCL setup time (restart condition)	$t_{SU:STA}$	—	4.7	—	—	µs
SDA hold time	$t_{HD:DAT}$	—	0	—	3.45	µs
SDA setup time	$t_{SU:DAT}$	—	0.25	—	—	µs
SDA setup time (stop condition)	$t_{SU:STO}$	—	4.0	—	—	µs
Bus-free time	t_{BUF}	—	4.7	—	—	µs

AC CHARACTERISTICS (I^2C Bus Interface: Fast Mode 400kHz)

(V_{DD} = 1.8 to 3.6V, AV_{DD} =2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = -20 to +70°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	—	0	—	400	kHz
SCL hold time (start/restart condition)	$t_{HD:STA}$	—	0.6	—	—	µs
SCL "L" level time	t_{LOW}	—	1.3	—	—	µs
SCL "H" level time	t_{HIGH}	—	0.6	—	—	µs
SCL setup time (restart condition)	$t_{SU:STA}$	—	0.6	—	—	µs
SDA hold time	$t_{HD:DAT}$	—	0	—	0.9	µs
SDA setup time	$t_{SU:DAT}$	—	0.1	—	—	µs
SDA setup time (stop condition)	$t_{SU:STO}$	—	0.6	—	—	µs
Bus-free time	t_{BUF}	—	1.3	—	—	µs



AC CHARACTERISTICS (RC Oscillation A/D Converter)

Condition for VDD=1.8 to 3.6V

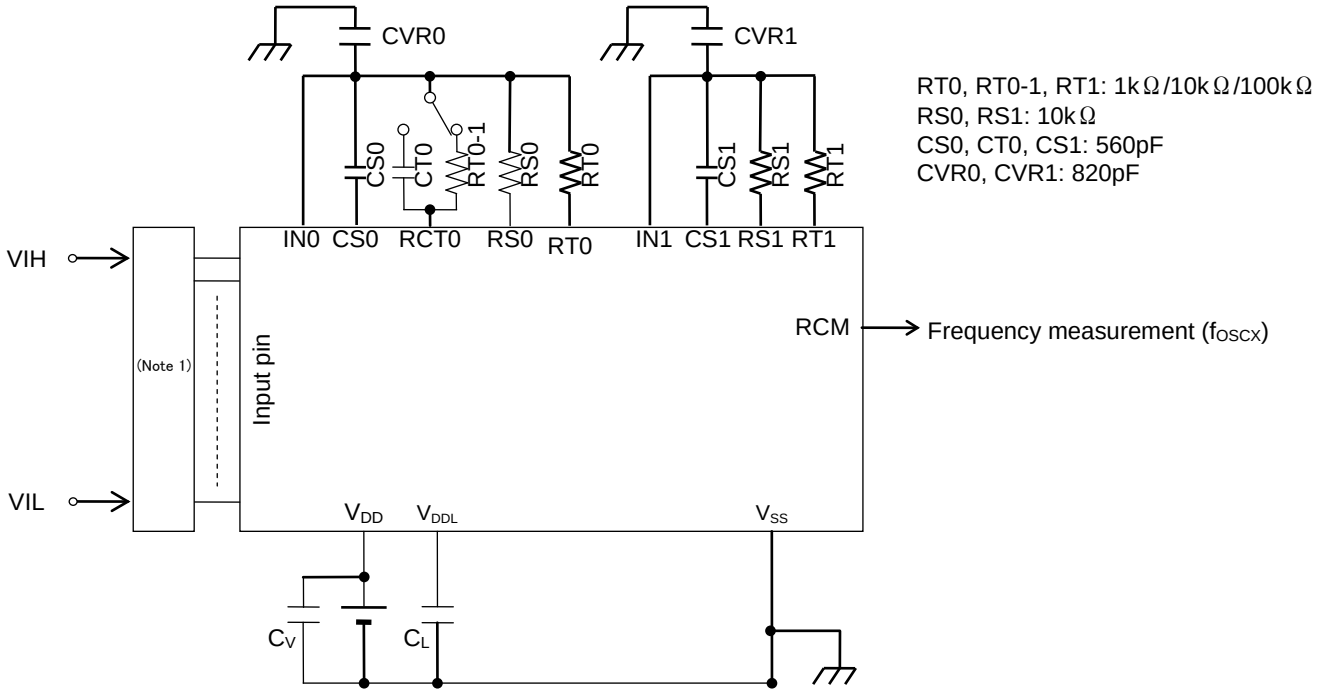
(V_{DD}=1.8 to 3.6V, AV_{DD} =2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = -20 to +70°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Oscillation resistor	RS0,RS1,RT0, RT0-1,RT1	CS0, CT0, CS1≥740pF	1	—	—	kΩ
Oscillation frequency V_{DD} = 3.0V	f_{OSC1}	Resistor for oscillation=1kΩ	457.3	525.2	575.1	kHz
	f_{OSC2}	Resistor for oscillation=10kΩ	53.48	58.18	62.43	kHz
	f_{OSC3}	Resistor for oscillation=100kΩ	5.43	5.89	6.32	kHz
RS to RT oscillation frequency ratio *1 V_{DD} = 3.0V	Kf1	RT0, RT0-1, RT1=1kΩ	7.972	9.028	9.782	—
	Kf2	RT0, RT0-1, RT1=10kΩ	0.981	1	1.019	—
	Kf3	RT0, RT0-1, RT1=100kΩ	0.099	0.101	0.104	—

*1: Kfx is the ratio of the oscillation frequency by the sensor resistor to the oscillation frequency by the reference resistor on the same conditions.

$$Kfx = \frac{f_{OSCx}(RT0\text{-}CS0\ oscillation)}{f_{OSCx}(RS0\text{-}CS0\ oscillation)}\ ,\ \frac{f_{OSCx}(RT0\text{-}1\text{-}CS0\ oscillation)}{f_{OSCx}(RS0\text{-}CS0\ oscillation)}\ ,\ \frac{f_{OSCx}(RT1\text{-}CS1\ oscillation)}{f_{OSCx}(RS1\text{-}CS1\ oscillation)}$$

(x = 1, 2, 3)



*1: Input logic circuit to determine the specified measuring conditions.

Condition for VDD=1.25 to 3.6V

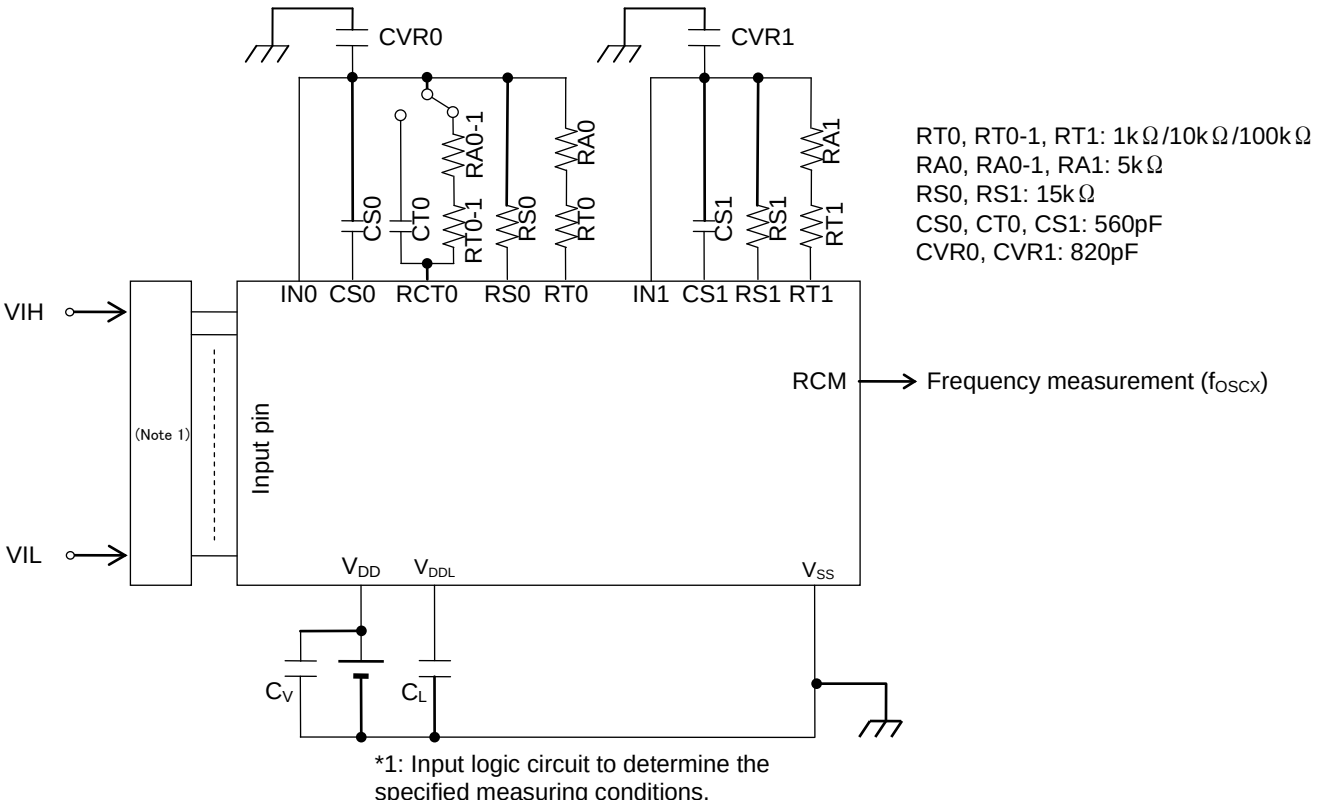
(V_{DD}=1.25 to 3.6V, AV_{DD} =2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = -20 to +70°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Oscillation resistor	RS0,RS1,RT0, RT0-1,RT1	CS0, CT0, CS1≥740pF	1	—	—	kΩ
Oscillation frequency V_{DD} = 1.5V	f_{OSC1}	Resistor for oscillation=6kΩ	81.93	93.16	101.2	kHz
	f_{OSC2}	Resistor for oscillation=15kΩ	35.32	38.75	41.48	kHz
	f_{OSC3}	Resistor for oscillation=105kΩ	5.22	5.65	6.03	kHz
RS to RT oscillation frequency ratio *1 V_{DD} = 1.5V	Kf1	RT0, RT0-1, RT1=1kΩ	2.139	2.381	2.632	—
	Kf2	RT0, RT0-1, RT1=10kΩ	0.973	1	1.028	—
	Kf3	RT0, RT0-1, RT1=100kΩ	0.142	0.147	0.152	—
Oscillation frequency V_{DD} = 3.0V	f_{OSC1}	Resistor for oscillation=6kΩ	85.28	94.58	103.3	kHz
	f_{OSC2}	Resistor for oscillation=15kΩ	35.72	38.87	41.78	kHz
	f_{OSC3}	Resistor for oscillation=105kΩ	5.189	5.622	6.012	kHz
RS to RT oscillation frequency ratio *1 V_{DD} = 3.0V	Kf1	RT0, RT0-1, RT1=1kΩ	2.227	2.432	2.626	—
	Kf2	RT0, RT0-1, RT1=10kΩ	0.982	1	1.018	—
	Kf3	RT0, RT0-1, RT1=100kΩ	0.141	0.145	0.149	—

*1: Kfx is the ratio of the oscillation frequency by the sensor resistor to the oscillation frequency by the reference resistor on the same conditions.

$$Kfx = \frac{f_{OSCX}(RT0\text{-}CS0\ oscillation)}{f_{OSCX}(RS0\text{-}CS0\ oscillation)}\ ,\ \frac{f_{OSCX}(RT0\text{-}1\text{-}CS0\ oscillation)}{f_{OSCX}(RS0\text{-}CS0\ oscillation)}\ ,\ \frac{f_{OSCX}(RT1\text{-}CS1\ oscillation)}{f_{OSCX}(RS1\text{-}CS1\ oscillation)}$$

(x = 1, 2, 3)



*1: Input logic circuit to determine the specified measuring conditions.

Note:

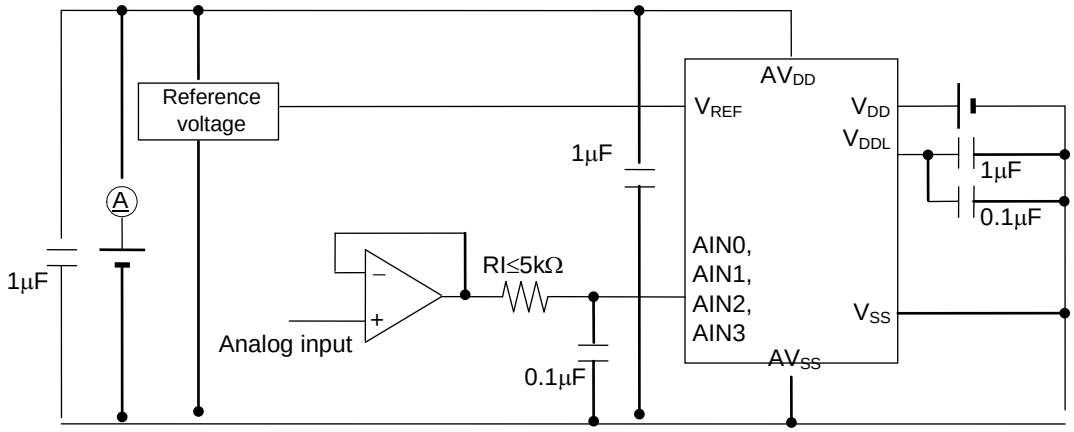
- Please have the shortest layout for the common node (wiring patterns which are connected to the external capacitors, resistors and IN0/IN1 pin), including CVR0/CVR1. Especially, do not have long wire between IN0/IN1 and RS0/RS1. The coupling capacitance on the wires may occur incorrect A/D conversion. Also, please do not have signals which may be a source of noise around the node.
- When RT0/RT1 (Thermistor and etc.) requires long wiring due to the restricted placement, please have VSS(GND) trace next to the signal.
- Please make wiring to components (capacitor, resisteor and etc.) necessory for objective measurement. Wiring to reserved components may affect to the A/D conversion operation by noise the components itself may have.

Electrical Characteristics of Successive Approximation Type A/D Converter

(V_{DD} = 1.8 to 3.6V, AV_{DD} =2.2 to 3.6V, V_{SS} = AV_{SS} = 0V, Ta = -20 to +70°C, unless otherwise specified)

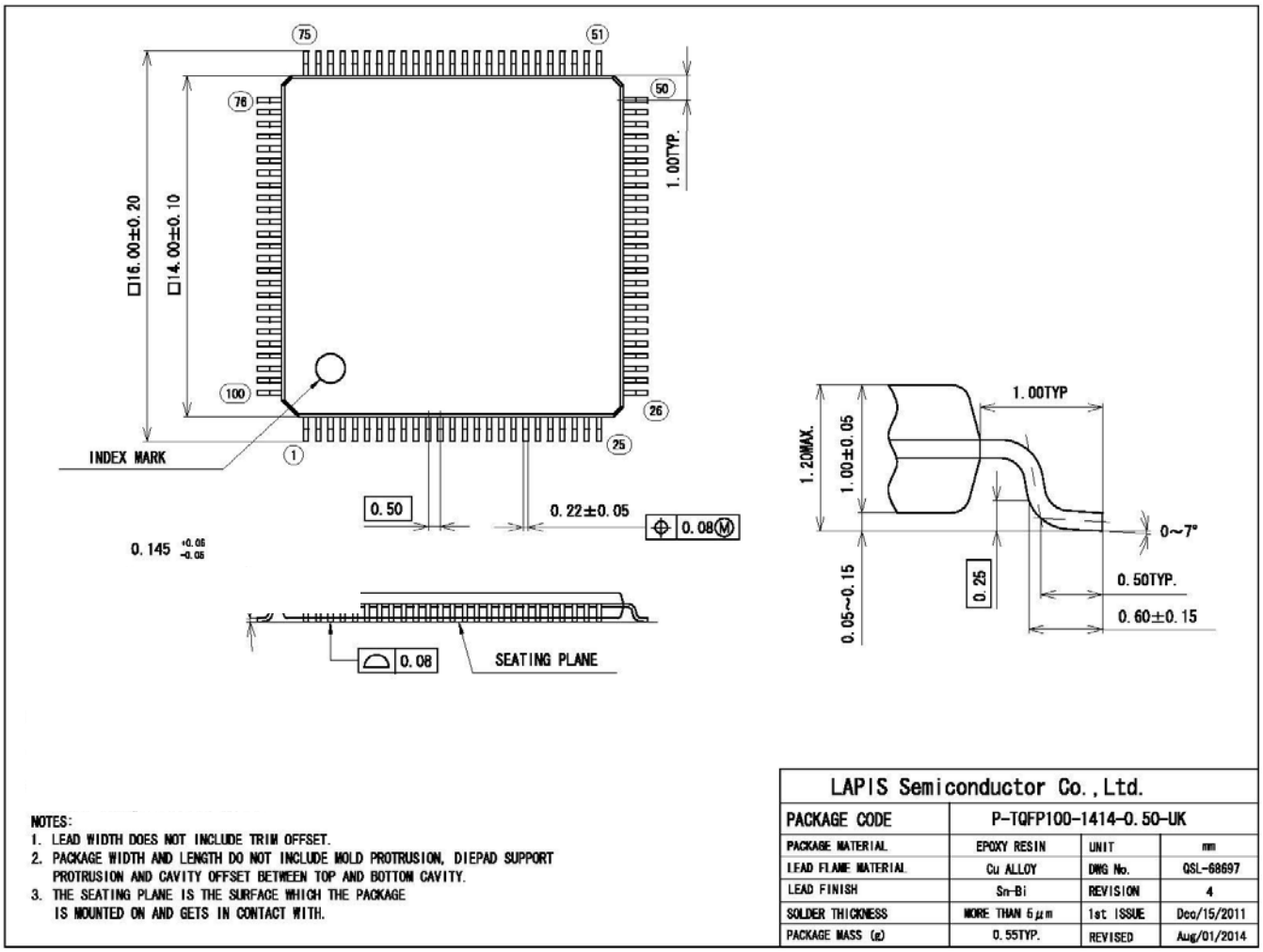
Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Resolution	n	—	—	—	12	bit
Integral non-linearity error	IDL	2.7V ≤ V_{REF} ≤ 3.6V	–4	—	+4	LSB
		2.2V ≤ V_{REF} ≤ 2.7V	–6	—	+6	
Differential non-linearity error	DNL	2.7V ≤ V_{REF} ≤ 3.6V	–3	—	+3	
		2.2V ≤ V_{REF} ≤ 2.7V	–5	—	+5	
Zero-scale error	V_{OFF}	—	–6	—	+6	
Full-scale error	FSE	—	–6	—	+6	
Reference voltage	V_{REF}	—	2.2	—	AV_{DD}	V
Conversion time	t_{CONV}	SACK = 0 (HSCLK = 375kHz to 625kHz)	—	25	—	ϕ/CH
		SACK = 1 (HSCLK = 1.5MHz to 4.2MHz)	—	112	—	

ϕ: Period of high-speed clock (HSCLK)



PACKAGE DIMENSIONS

(Unit: mm)



LAPIS Semiconductor Co.,Ltd.			
PACKAGE CODE	P-TQFP100-1414-0.50-UK		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu ALLOY	DWG No.	QSL-68697
LEAD FINISH	Sn-Bi	REVISION	4
SOLDER THICKNESS	MORE THAN 6μm	1st ISSUE	Dec/15/2011
PACKAGE MASS (g)	0.55TYP.	REVISED	Aug/01/2014

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL610Q419-1	Dec.26.2011	–	–	Formally edition 1.0
FEDL610Q419-2	Jan.11.2012	35	35	Changed figure of package dimensions.
FEDL610Q419-3	Jun.5.2012	3	3	Changed part number of TQFP.
FEDL610Q419-4	Sep.4.2012	21	21	Changed parameter of data retention. Changed parameter of 1-word (16 bits) write time
FEDL610Q419-05	July.25.2014	All	All	Change header and footer
		3	4	Change from "Shipment" to " Product name – Supported Function "
		-	22	Add CLOCK GENERATION CIRCUIT OPERATING CONDITIONS
		22	23	Change "RESET" to "Reset pulse width (P_{RST})" , " Power-on reset activation power rise time (T_{POR})" and “Low level reset detection time(T_{LLR})”.
		22	23	Correct the CGL’s value and the CDL’s value of DC CHARACTERISTICS (1/5)’s note No.2
		24	25	Correct the C_{GL}’s value and the C_{DL}’s value of DC CHARACTERISTICS (3/5)’s note No.3
		27	28	Correct the C_{GL}’s value and the C_{DL}’s value of MEASURING CIRCUIT 1
FEDL610Q419-06	May.13,2015	2	2	Corrected a typo. “100kbps@1MHz HSCLK” is corrected to 100kbps@4MHz HSCLK.
		30	30	Corrected a typo.
		36	36	Change PKG
		3,4,21 23 to 27 30 to 35	3,4,21 23 to 27 30 to 35	Delete wide range temperature version (P version)

Notes

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