4M-BIT SERIAL FLASH MEMORY WITH BOOT AND PARAMETER SECTORS



Formally NexFlash NX25B40

The Winbond W25B40 / W25B40A is fully compatible with the previous NexFlash NX25B40 Serial Flash memory.

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1. GENERAL DESCRIPTION

The W25B40 / W25B40A is a 4Mb (512KB) Serial Flash Memory with erasable sectors that allows for boot code and parameter storage. The W25B40 / W25B40A is packaged in an 8-pin SOIC 150-mil and is compatible with the standard W25P40 specification with the following exceptions.

- The W25B40 / W25B40A has twelve sectors instead of eight including: seven sectors of 64KB, one sector of 32KB, one sector of 16KB, one sector of 8KB and two sectors of 4KB. (see figure 2a and 2b)
- The W25B40 / W25B40A status register write protect bits (BP2, BP1, and BP0) can protect the boot and parameter sectors. Unlike other Serial Flash devices, that only protect large portions of the memory and typically from the top address down, the W25B40 / W25B40A can protect boot code stored in the small sectors for either bottom or top boot configurations. This feature makes the process of field updates more robust and reliable. (See Write Protection Operation table)
- The W25B40 / W25B40A Bottom Boot Device ID is 32h instead of 12h as with the 25P40. Optional Top Boot is 42h.

The Winbond W25B40 / W25B40A is fully compatible with the previous NexFlash NX25B40 Serial Flash memory.

2. FEATURES

- **W25B40 / W25B40A 4M-bit Serial Flash**
  – 4M-bit /512K-byte (524,288)
  – 256-bytes per programmable page
- **Compatible with W25P40 with special features**
  – Small Boot and Parameter Sectors
  – Write protection of Boot/Parameter area
- **Variable Sector Sizes for Boot Code and Parameter Storage**
  – Seven sectors of 64KB
  – One sector each of 32KB, 16Kb and 8KB
  – Two sectors of 4KB
  – Bottom Boot organization (standard)
  – Top Boot organization (special order)
- **4-pin SPI Serial Interface**
  – Clock, Chip Select, Data In, Data Out
  – Easily interfaces to popular microcontrollers
  – Compatible with SPI Modes 0 and 3
  – Optional Hold function for SPI flexibility
- **Low Power Consumption, Wide Temperature Range**
  – Single 2.7 to 3.6V supply
  – 5mA active current, <1µA Power-down
  – -40° to +85°C operating range
- **Fast and Flexible Serial Data Access**
  – Clock operation to 40MHz
  – Byte-addressable Read and Program
  – Auto-increment Read capability
  – Manufacturer and Device ID
- **Programming Features**
  – Page program up to 256 bytes 2mS
  – Sector Erase 120mS to 650mS
  – Chip erase 5.5 seconds
  – 100,000 erase/write cycles
  – Twenty-year data retention
- **Software and Hardware Write Protection**
  – Write-Protect all or portion of memory
  – Enable/Disable protection with /WP pin
- **SOIC Compatible Packaging**
  – Tiny 8-pin SOIC 150mil
- **Ideal for systems with limited pins, space, and power**
  – Controller-based serial code-download
  – µC systems storing data, text or voice
  – Battery-operated and portable product

3. PIN CONFIGURATION

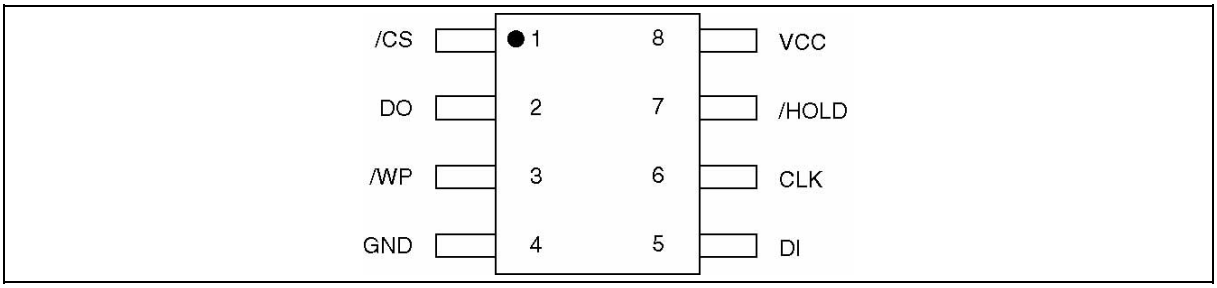


Figure 1. W25B40 / W25B40A Pin Assignments, 8-pin SOIC (Package Code SN)

4. PIN DESCRIPTION

PIN NO.	PIN NAME	I/O	FUNCTION
1	/CS	I	Chip Select Input
2	DO	O	Data Output
3	/WP	I	Write Protect Input
4	GND		Ground
5	DI	I	Data Input
6	CLK	I	Serial Clock Input
7	/HOLD	I	Hold Input
8	VCC		Power Supply

4.1 Package Types

The standard package for the W25B40 / W25B40A is an 8-pin plastic SOIC with 150-mil body (Winbond package code SN) (NexFlash package code N). The pinout for the package is shown in Figure 1. Package diagram and dimensions are illustrated at the end of this data sheet.

4.2 Chip Select (/CS)

The SPI Chip Select (/CS) pin enables and disables device operation. When /CS is high the device is deselected and the Serial Data Output (DO) pin is at high impedance. When deselected, the devices power consumption will be at standby levels unless an internal erase, program or status register cycle is in progress. When /CS is brought low the device will be selected, power consumption will increase to active levels and instructions can be written to and data read from the device. After power-up, /CS must transition from high to low before a new instruction will be accepted. The /CS input must track the VCC supply level at power-up (see “Write Protection” and figure 18). If needed a pull-up resister on /CS can be used to accomplish this.

4.3 Serial Data Output (DO)

The SPI Serial Data Output (DO) pin provides a means for data and status to be serially read from (shifted out of) the device. Data is shifted out on the falling edge of the Serial Clock (CLK) input pin.

4.4 Write Protect (/WP)

The Write Protect (/WP) pin can be used to prevent the Status Register from being written. Used in conjunction with the Status Register's Block Protect (BP2, BP1 and BP0) bits and Status Register Protect (SRP) bits, a portion or the entire memory array can be hardware protected. The /WP pin is active low.

4.5 Hold (/HOLD)

The /HOLD pin allows the device to be paused while it is actively selected. When /HOLD is brought low, while /CS is low, the DO pin will be at high impedance and signals on the DI and CLK pins will be ignored (don't care). When /HOLD is brought high, device operation can resume. The /HOLD function can be useful when multiple devices are sharing the same SPI signals. ("See Hold function")

4.6 Serial Clock (CLK)

The SPI Serial Clock Input (CLK) pin provides the timing for serial input and output operations. ("See SPI "Operations")

4.7 Serial Data Input (DI)

The SPI Serial Data Input (DI) pin provides a means for instructions, addresses and data to be serially written to (shifted into) the device. Data is latched on the rising edge of the Serial Clock (CLK) input pin.

5. BLOCK DIAGRAM (BOTTOM BOOT)

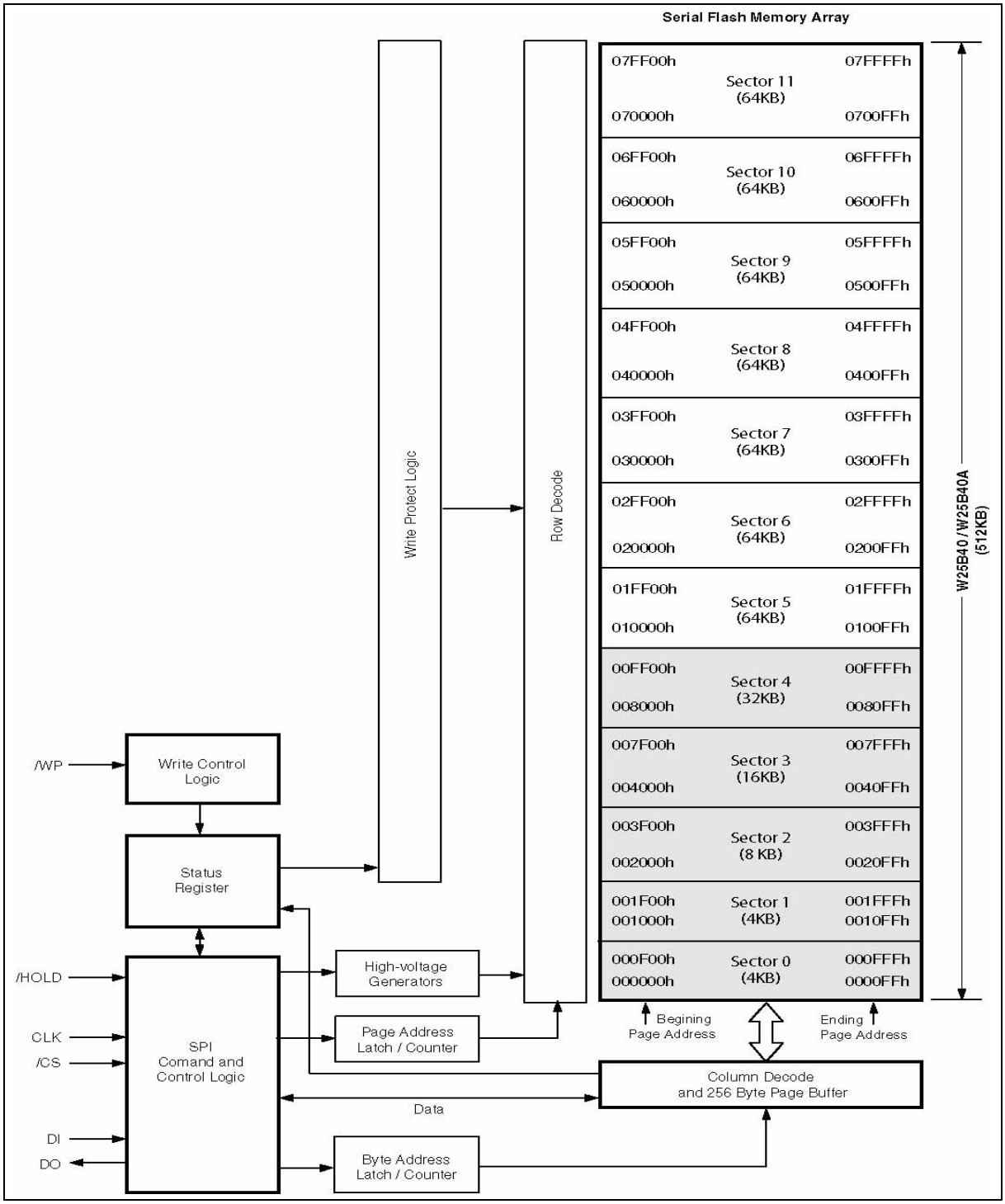


Figure 2a. W25B40 / W25B40A Block Diagram for Bottom Boot Sector Organization

6. BLOCK DIAGRAM (TOP BOOT-SPECIAL ORDER)

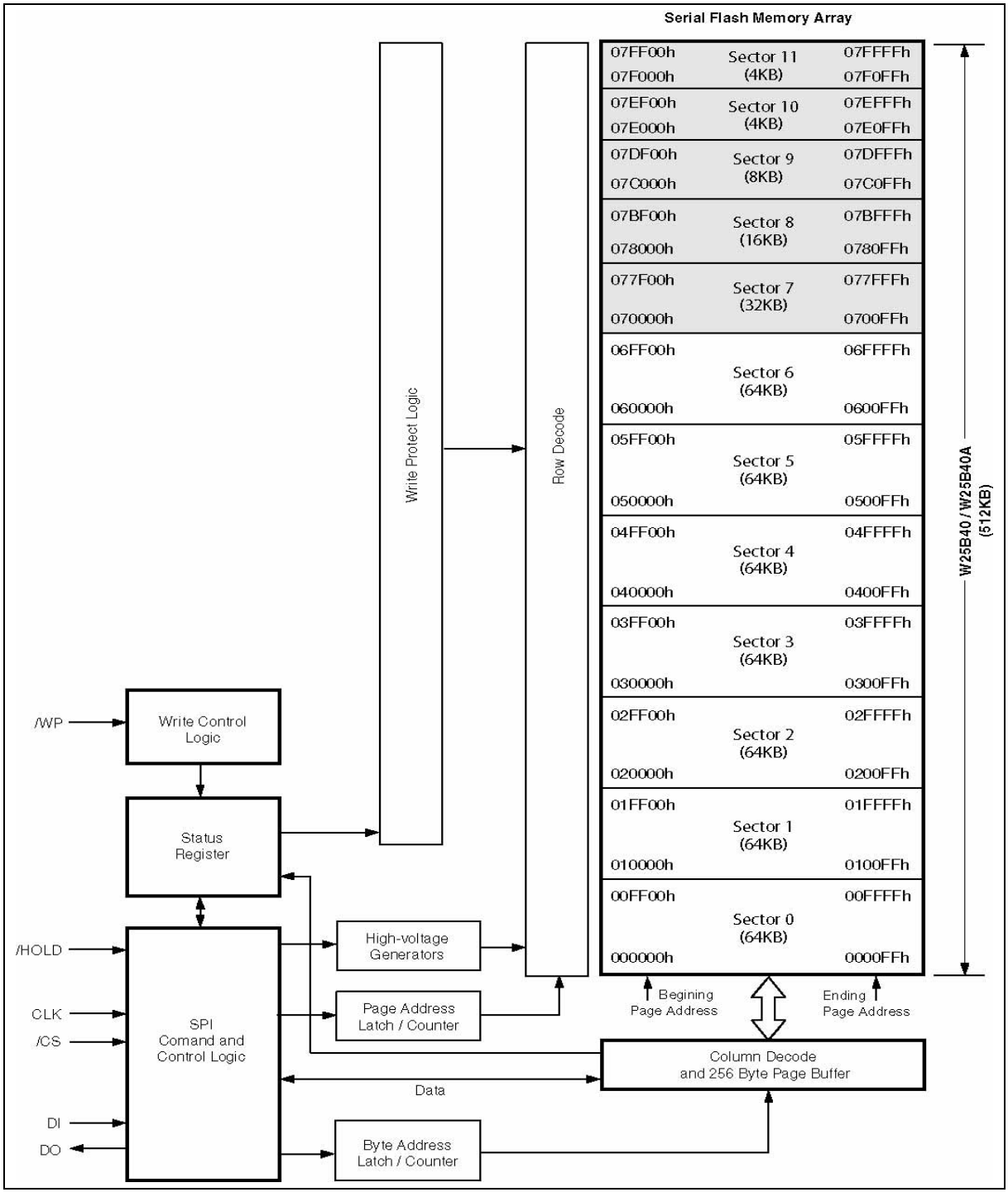


Figure 2b. W25B40 / W25B40A Block Diagram for Top Boot Sector Organization (Special Order)

7. FUNCTIONAL DESCRIPTION

7.1 SPI OPERATIONS

7.1.1 SPI Modes

The W25B40 / W25B40A is accessed through an SPI compatible bus consisting of four signals: Serial Clock (CLK), Chip Select (/CS), Serial Data Input (DI) and Serial Data Output (DO). Both SPI bus operation Modes 0 (0,0) and 3 (1,1) are supported. The primary difference between Mode 0 and Mode 3 concerns the normal state of the CLK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0 the CLK signal is normally low. For Mode 3 the CLK signal is normally high. In either case data input on the DI pin is sampled on the rising edge of the CLK. Data output on the DO pin is clocked out on the falling edge of CLK.

7.1.2 Hold Function

The /HOLD signal allows the W25B40 / W25B40A operation to be paused while it is actively selected (when /CS is low). The /HOLD function may be useful in cases where the SPI data and clock signals are shared with other devices. For example, consider if the page buffer was only partially written when a priority interrupt requires use of the SPI bus. In this case the /HOLD function can save the state of the instruction and the data in the buffer so programming can resume where it left off once the bus is available again.

To initiate a /HOLD condition, the device must be selected with /CS low. A /HOLD condition will activate on the falling edge of the /HOLD signal if the CLK signal is already low. If the CLK is not already low the /HOLD condition will activate after the next falling edge of CLK. The /HOLD condition will terminate on the rising edge of the /HOLD signal if the CLK signal is already low. If the CLK is not already low the /HOLD condition will terminate after the next falling edge of CLK.

During a /HOLD condition, the Serial Data Output (DO) is high impedance, and Serial Data Input (DI) and Serial Clock (CLK) are ignored. The Chip Select (/CS) signal should be kept active (low) for the full duration of the /HOLD operation to avoid resetting the internal logic state of the device.

7.2 WRITE PROTECTION

Applications that use non-volatile memory must take into consideration the possibility of noise and other adverse system conditions that may compromise data integrity. To address this concern the W25B40 / W25B40A provides several means to protect data from inadvertent writes.

7.2.1 Write Protect Features

- Device resets when VCC is below threshold.
- Time delay write disable after Power-up.
- Write enable/disable instructions.
- Automatic write disable after program and erase.
- Software write protection using Status Register.
- Hardware write protection using Status Register and /WP pin.

7.2.2 Write Protection using Power-down instruction.

Upon power-up or at power-down the W25B40 / W25B40A will maintain a reset condition while VCC is below the threshold value of V_{WI}, (See Power-up Timing and Voltage Levels and Figure 18). While reset, all operations are disabled and no instructions are recognized. During power-up and after the VCC voltage exceeds V_{WI}, all program and erase related instructions are further disabled for a time delay of t_{PUW}. This includes the Write Enable, Page Program, Sector Erase, Chip Erase and the Write Status Register instructions. Note that the chip select pin (/CS) must track the VCC supply level at power-up until the VCC-min level and t_{VSL} time delay is reached. If needed a pull-up resister on /CS can be used to accomplish this.

After power-up the device in automatically placed in a write-disabled state with the Status Register Write Enable Latch (WEL) set to a 0. A Write Enable instruction must be issued before a Page Program, Sector Erase, Chip Erase or Write Status Register instruction will be accepted. After completing a program, erase or write instruction the Write Enable Latch (WEL) is automatically cleared to a write-disabled state of 0.

Software controlled write protection is facilitated using the Write Status Register instruction and setting the Status Register Protect (SRP) and Block Protect (BP2, BP1, and BP0) bits. These Status Register bits allow a portion or all of the memory to be configured as read only. Used in conjunction with the Write Protect (/WP) pin, changes to the Status Register can be enabled or disabled under hardware control. See Status Register for further information.

Additionally, the Power-down instruction offers an extra level of write protection as all instructions are ignored except for the Release Power-down instruction.

8. CONTROL AND STATUS REGISTERS

The Read Status Register instruction can be used to provide status on the availability of the Flash memory array, if the device is write enabled or disabled, and the state of write protection. The Write Status Register instruction can be used to configure the devices write protection features. See Figure 3.

8.1 STATUS REGISTER

8.1.1 BUSY

BUSY is a read only bit in the status register (S0) that is set to a 1 state when the device is executing a Page Program, Sector Erase, Chip Erase or Write Status Register instruction. During this time the device will ignore further instructions except for the Read Status Register instruction (see t_W, t_{PP}, t_{SE} and t_{CE} in AC Characteristics). When the program, erase or write status register instruction has completed, the BUSY bit will be cleared to a 0 state indicating the device is ready for further instructions.

8.1.2 Write Enable Latch (WEL)

Write Enable Latch (WEL) is a read only bit in the status register (S1) that is set to a 1 after executing a Write Enable Instruction. The WEL status bit is cleared to a 0 when the device is write disabled. A

write disable state occurs upon power-up or after any of the following instructions: Write Disable, Page Program, Sector Erase, Chip Erase and Write Status Register.

8.1.3 Block Protect Bits (BP2, BP1, BP0)

The Block Protect Bits (BP2, BP1, BP0) are non-volatile read/write bits in the status register (S4, S3, S2) that provide Write Protection control and status. Block Protect bits can be set using the Write Status Register Instruction (see tW in AC characteristics). All, none or a portion of the memory array can be protected from Program and Erase instructions (see Status Register Memory Protection table). The factory default setting for the Block Protection Bits is 0, none of the array protected. The Block Protect bits can not be written to if the Status Register Protect (SRP) bit is set to 1 and the Write Protect (/WP) pin is low.

8.1.4 Reserved Bits

Status register bit locations 5 and 6 are reserved for future use. Current devices will read 0 for these bit locations. It is recommended to mask out the reserved bit when testing the Status Register. Doing this will ensure compatibility with future devices.

8.1.5 Status Register Protect (SRP)

The Status Register Protect (SRP) bit is a non-volatile read/write bit in the status register (S7) that can be used in conjunction with the Write Protect (/WP) pin to disable writes to the status register. When the SRP bit is set to a 0 state (factory default) the /WP pin has no control over the status register. When the SRP pin is set to a 1, the Write Status Register instruction is locked out while the /WP pin is low. When the /WP pin is high the Write Status Register instruction is allowed.

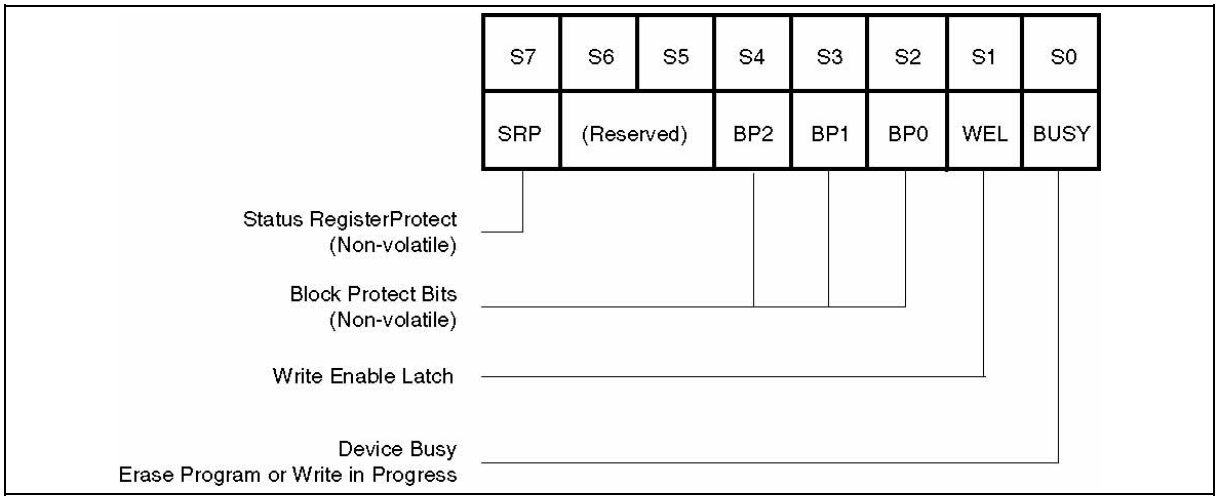


Figure 3. Status Register Bit Locations

8.1.6 Write Protection Operation - Bottom Boot Sector Organization

STATUS REGISTER			W25B40 / W25B40A (4M-BIT) MEMORY PROTECTION			
BP2	BP1	BP0	SECTOR(S)	ADDRESSES	DENSITY (KB)	PORTION
1	1	1	ALL	000000h - 07FFFFh	512KB	ALL
1	1	0	0 thru 7	000000h - 03FFFFh	256KB	Lower 1/2
1	0	1	0 thru 4	000000h - 00FFFFh	64KB	Lower 1/8
1	0	0	0 thru 3	000000h - 007FFFh	32KB	Lower 1/16
0	1	1	0 thru 2	000000h - 003FFFh	16KB	Lower 1/32
0	1	0	0 thru 1	000000h - 001FFFh	8KB	Lower 1/64
0	0	1	0	000000h - 000FFFh	4KB	Lower 1/128
0	0	0	NONE	NONE	NONE	NONE

8.1.7 Write Protection Operation - Top Boot Sector Organization (Special Order)

STATUS REGISTER			W25B40 / W25B40A (4M-BIT) MEMORY PROTECTION			
BP2	BP1	BP0	SECTOR(S)	ADDRESSES	DENSITY (KB)	PORTION
0	0	0	NONE	NONE	NONE	NONE
0	0	1	11	07F000h - 07FFFFh	4KB	Upper 1/128
0	1	0	10 thru 11	07E000h - 07FFFFh	8KB	Upper 1/64
0	1	1	9 thru 11	07C000h - 07FFFFh	16KB	Upper 1/32
1	0	0	8 thru 11	078000h - 07FFFFh	32KB	Upper 1/16
1	0	1	7 thru 11	070000h - 07FFFFh	64KB	Upper 1/8
1	1	0	4 thru 11	040000h - 07FFFFh	256KB	Upper 1/2
1	1	1	ALL	000000h - 07FFFFh	512KB	ALL

8.2 INSTRUCTIONS

The instruction set of the W25B40 / W25B40A consists of twelve basic instructions that are fully controlled through the SPI bus (see Instruction Set table). Instructions are initiated with the falling edge of Chip Select (/CS). The first byte of data clocked into the DI input provides the instruction code. Data on the DI input is sampled on the rising edge of clock with most significant bit (MSB) first.

Instructions vary in length from a single byte to several bytes and may be followed by address bytes, data bytes, dummy bytes (don't care), and in some cases, a combination. Instructions are completed with the rising edge of edge /CS. Clock relative timing diagrams for each instruction are included in figures 4 through 17. All read instructions can be completed after any clocked bit. However, all instructions that Write, Program or Erase must complete on a byte boundary (/CS) driven high after a full 8-bits have been clocked) otherwise the instruction will be terminated. This feature further protects the device from inadvertent writes. Additionally, while the memory is being programmed or erased, or when the Status Register is being written, all instructions except for Read Status Register will be ignored until the program or erase cycle has completed.

8.2.1 Manufacturer and Device Identification

MANUFACTURER ID	**(M7-M0)**
Winbond Serial Flash	EFH
Device ID	**(ID7-ID0)**
W25B40 / W25B40A (Bottom Boot)	32h
W25B40 / W25B40A (Top Boot)	42h

8.2.2 Instruction Set (1)

INSTRUCTION NAME	**BYTE 1 CODE**	**BYTE 2**	**BYTE 3**	**BYTE 4**	**BYTE 5**	**BYTE 6**	**N-BYTES**
Write Enable	06h						
Write Disable	04h						
Read Status Register	05h	(S7–S0)(1)					(2)
Write Status Register	01h	S7–S0					
Read Data	03h	A23–A16	A15–A8	A7–A0	(D7–D0)	(Next byte)	continuous
Fast Read	0Bh	A23–A16	A15–A8	A7–A0	dummy	(D7–D0)	(Next Byte) continuous
Page Program	02h	A23–A16	A15–A8	A7–A0	(D7–D0)	(Next byte)	up to 256 bytes
Sector Erase	D8h	A23–A16	A15–A8	A7–A0(5)			
Chip Erase	C7h						
Power-down	B9h						
Release Power-down / Device ID	ABh	dummy	dummy	dummy	(ID7-ID0)		(3)
Manufacturer/ Device ID	90h	dummy	dummy	00h	(M7-M0)	(ID7-ID0)	(4)

Notes:
1. Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis "( )" indicate data being read from the device on the DO pin.
2. The Status Register contents will repeat continuously until /CS terminates the instruction.
3. The Device ID will repeat continuously until /CS terminates the instruction.
4. The Manufacturer ID and Device ID bytes will repeat continuously until /CS terminates the instruction.
5. The W25B40 Bottom Boot version must use the last page address for sectors 2, 3, and 4 (003Fxx, 007Fxx and 00FFxx hex respectively). The W25B40 Top Boot version must use the first page address for sectors 7, 8 and 9 (0700xx, 0780xx and 07C0xx hex respectively). All other sectors may use any page address within the sector. The W25B40A may use any page address within the sector for sector erase.

8.2.3 Write Disable (04h)

The Write Disable instruction (Figure 4) resets the Write Enable Latch (WEL) bit in the Status Register to a 0. The Write Disable instruction is entered by driving /CS low, shifting the instruction code “04h” into the DI pin and then driving /CS high. Note that the WEL bit is automatically reset after Power-up and upon completion of the Write Status Register, Page Program, Sector Erase, and Chip Erase instructions.

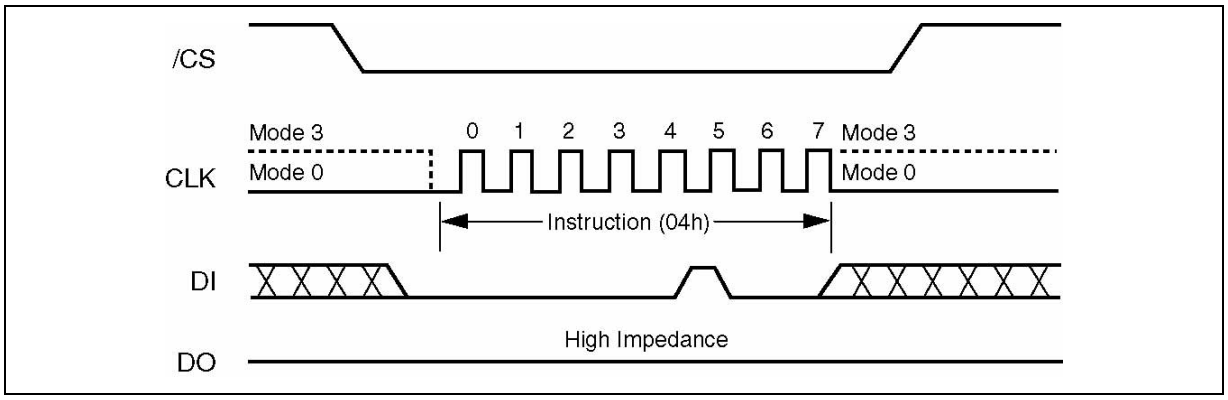


Figure 4. Write Disable Instruction Sequence Diagram

8.2.4 Write Enable (06h)

The Write Enable instruction (Figure 5) sets the Write Enable Latch (WEL) bit in the Status Register to a 1. The WEL bit must be set prior to every Page Program, Sector Erase, Chip Erase and Write Status Register instruction. The Write Enable instruction is entered by driving /CS low, shifting the instruction code “06h” into the Data Input (DI) pin on the rising edge of CLK, and then driving /CS high.

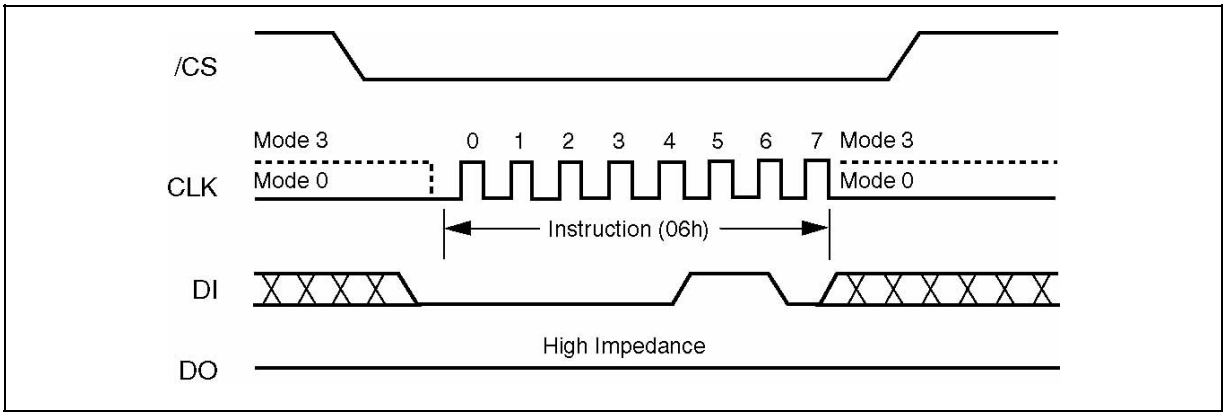


Figure 5. Write Enable Instruction Sequence Diagram

8.2.5 Read Status Register (05h)

The Read Status Register instruction allows the 8-bit Status Register to be read. The instruction is entered by driving /CS low and shifting the instruction code “05h” into the DI pin on the rising edge of CLK. The status register bits are then shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first as shown in figure 6. The Status Register bits are shown in figure 3 and include the BUSY, WEL, BP2-BP0, and SRP bits (see description of the Status Register earlier in this data sheet).

The Status Register instruction may be used at any time, even while a Program, Erase or Write Status Register cycle is in progress. This allows the BUSY status bit to be checked to determine when the cycle is complete and if the device can accept another instruction. The Status Register can be read continuously, as shown in Figure 7. The instruction is completed by driving /CS high.

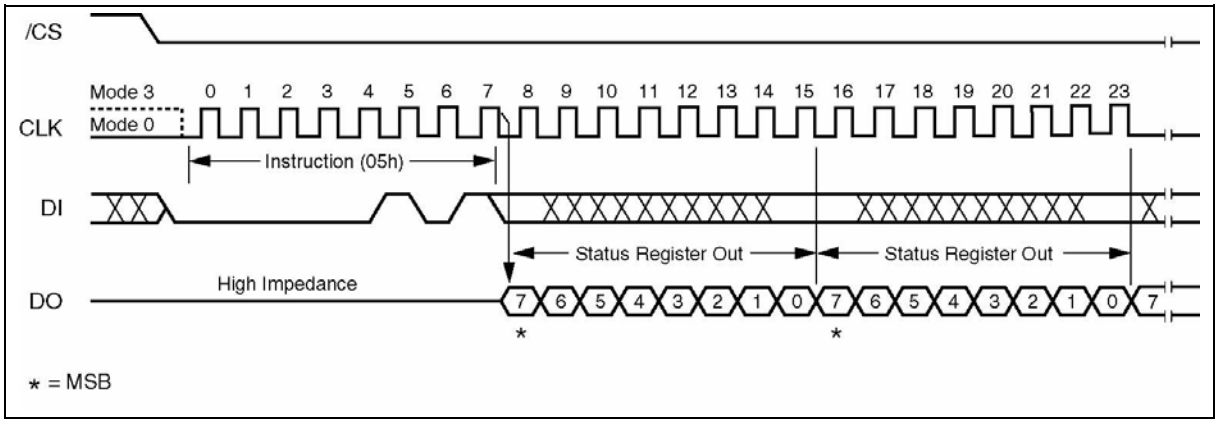


Figure 6. Read Status Register Instruction Sequence Diagram

8.2.6 Write Status Register (01h)

The Write Status Register instruction allows the Status Register to be written. A Write Enable instruction must previously have been executed for the device to accept the Write Status Register Instruction (Status Register bit WEL must equal 1). Once write enabled, the instruction is entered by driving /CS low, sending the instruction code “01h”, and then writing the status register data byte as illustrated in figure 7. The Status Register bits are shown in figure 3 and described earlier in this data sheet.

Only non-volatile Status Register bits SRP, BP2, BP1 and BP0 (bits 7, 4, 3 and 2) can be written to. All other Status Register bit locations are read-only and will not be affected by the Write Status Register instruction.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Write Status Register instruction will not be executed. After /CS is driven high, the self-timed Write Status Register cycle will commence for a time duration of tW (See AC Characteristics). While the Write Status Register cycle is in progress, the Read Status Register instruction may still accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Write Status Register cycle and a 0 when the cycle is finished and ready to accept other instructions again. After the Write Register cycle has finished the Write Enable Latch (WEL) bit in the Status Register will be cleared to 0.

The Write Status Register instruction allows the Block Protect bits (BP2, BP1 and BP0) to be set for protecting all, a portion, or none of the memory from erase and program instructions. Protected areas become read-only (see Status Register Memory Protection table). The Write Status Register instruction also allows the Status Register Protect bit (SRP) to be set. This bit is used in conjunction with the Write Protect (/WP) pin to disable writes to the status register. When the SRP bit is set to a 0 state (factory default) the /WP pin has no control over the status register. When the SRP pin is set to a 1, the Write Status Register instruction is locked out while the /WP pin is low. When the /WP pin is high the Write Status Register instruction is allowed.

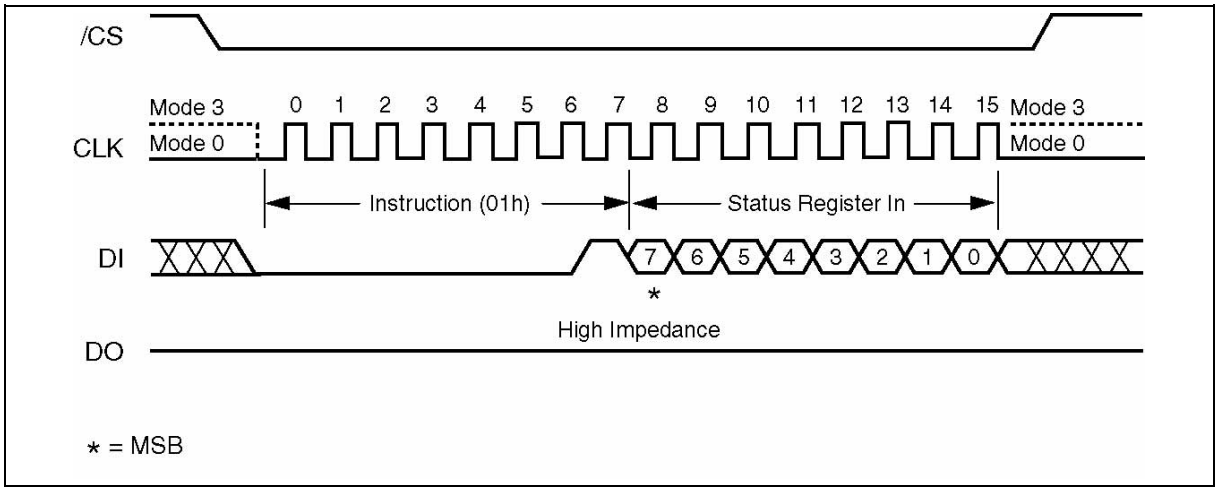


Figure 7. Write Status Register Instruction Sequence Diagram

8.2.7 Read Data (03h)

The Read Data instruction allows one or more data bytes to be sequentially read from the memory. The instruction is initiated by driving the /CS pin low and then shifting the instruction code “03h” followed by a 24-bit address (A23-A0) into the DI pin. The code and address bits are latched on the rising edge of the CLK pin. After the address is received, the data byte of the addressed memory location will be shifted out on the DO pin at the falling edge of CLK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. This means that the entire memory can be accessed with a single instruction as long as the clock continues. The instruction is completed by driving /CS high. The Read Data instruction sequence is shown in figure 8. If a Read Data instruction is issued while an Erase, Program or Write cycle is in process (BUSY=1) the instruction is ignored and will not have any effects on the current cycle. The Read Data instruction allows clock rates from D.C. to a maximum of f_R (see AC Electrical Characteristics).

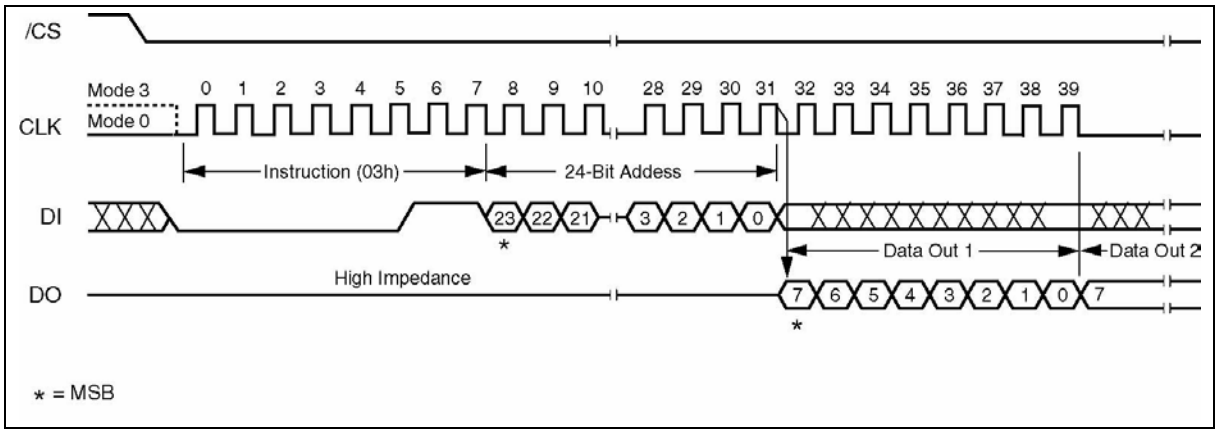


Figure 8. Read Data Instruction Sequence Diagram

8.2.8 Fast Read (0Bh)

The Fast Read instruction is similar to the Read Data instruction except that it can operate at the highest possible frequency of FR (see AC Electrical Characteristics). This is accomplished by adding a "dummy" byte after the 24-bit address as shown in figure 9. The dummy byte allows the devices internal circuits additional time for setting up the initial address. The dummy byte data value on the DI pin is a "don't care".

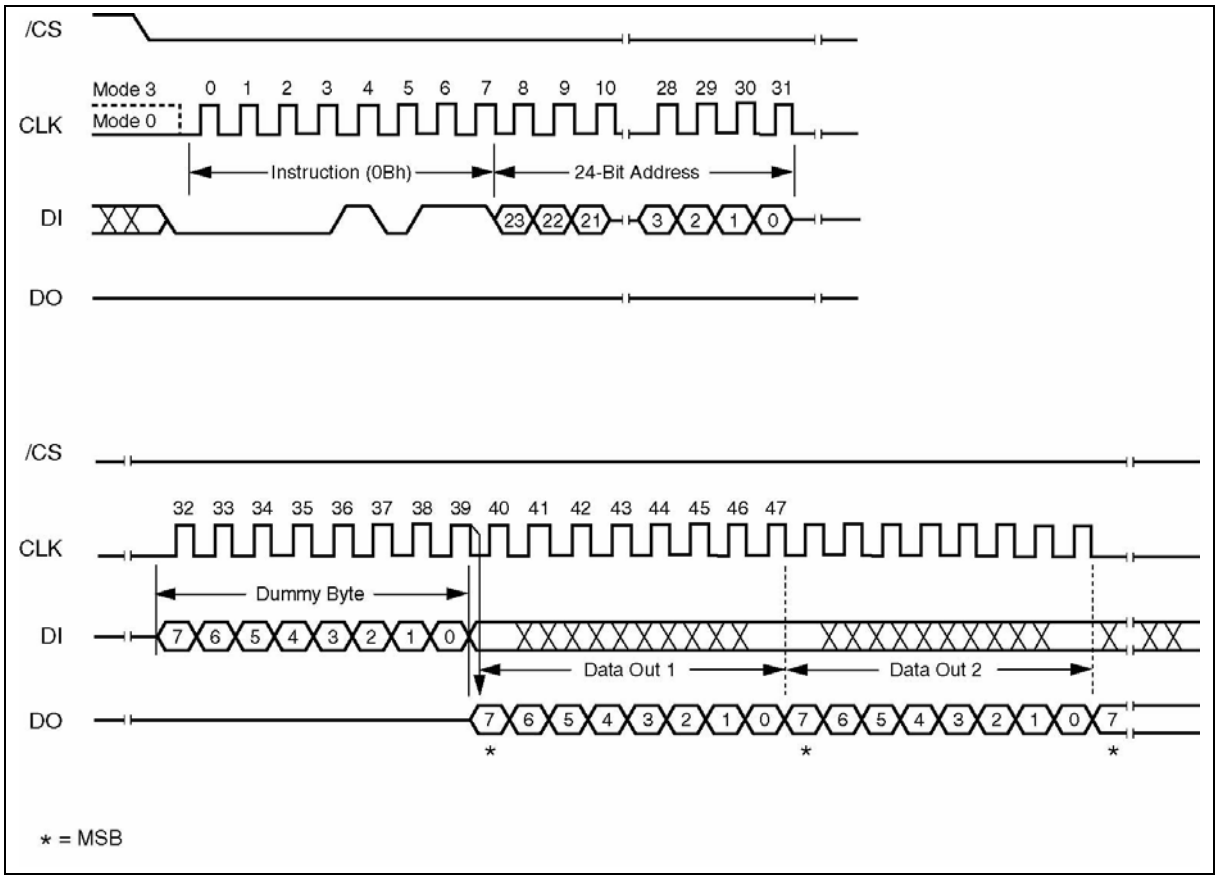


Figure 9. Fast Read Instruction Sequence Diagram

8.2.9 Page Program (02h)

The Page Program instruction allows from one byte to 256 bytes of data to be programmed at memory locations previously erased to all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Page Program Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low then shifting the instruction code “02h” followed by a 24-bit address (A23-A0) and at least one data byte, into the DI pin. The /CS pin must be driven low for the entire length of the instruction while data is being sent to the device. The Page Program instruction sequence is shown in figure 10.

If an entire 256 byte page is to be programmed, the last address byte (the 8 least significant address bits) should be set to 0. If the last address byte is not zero, and the number of clocks exceed the remaining page length, the addressing will wrap to the beginning of the page. Less than 256 bytes can be programmed without having any effect on other bytes within the same page. If more than 256 bytes are sent to the device the addressing will wrap to the beginning of the page and overwrite previously sent data.

As with the write and erase instructions, the /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Page Program instruction will not be executed. After /CS is driven high, the self-timed Page Program instruction will commence for a time duration of tpp (See AC Characteristics). While the Page Program cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Page Program cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Page Program cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Page Program instruction will not be executed if the addressed page is protected by the Block Protect (BP2, BP1, BP0) bits (see Write Protection Operation table).

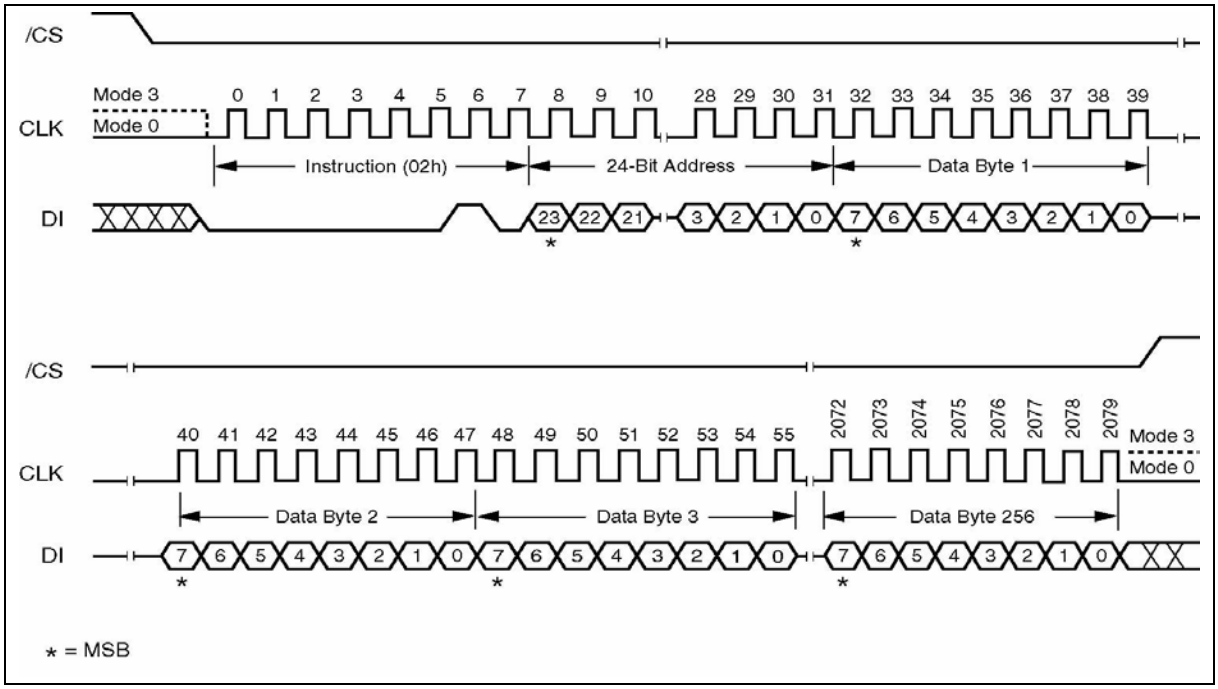


Figure 10. Page Program Instruction Sequence Diagram

8.2.10 Sector Erase (D8h)

The Sector Erase instruction sets all memory within a specified sector to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Erase Sector Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code "D8h" followed a 24-bit sector address (A23-A0) (see Figure 2a). **Please note that the W25B40 Bottom Boot version must use the last page address for sectors 2, 3, and 4 (003Fxx, 007Fxx and 00FFxx hex respectively).** The W25B40 Top Boot version must use the first page address for sectors 7, 8 and 9 (0700xx, 0780xx and 07C0xx hex respectively). All other sectors may use any page address within the sector.The W25B40A may use any page address within the sector for sector erase. The Sector Erase instruction sequence is shown in figure 11.

The /CS pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Sector Erase instruction will not be executed. After /CS is driven high, the self-timed Sector Erase instruction will commence for a time duration of t_{SE} (See AC Characteristics). While the Sector Erase cycle is in progress, the Read Status Register instruction may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Sector Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other instructions again. After the Sector Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0. The Sector Erase instruction will not be executed if the addressed page is protected by the Block Protect (BP2, BP1, BP0) bits ((see Write Protection Operation table).

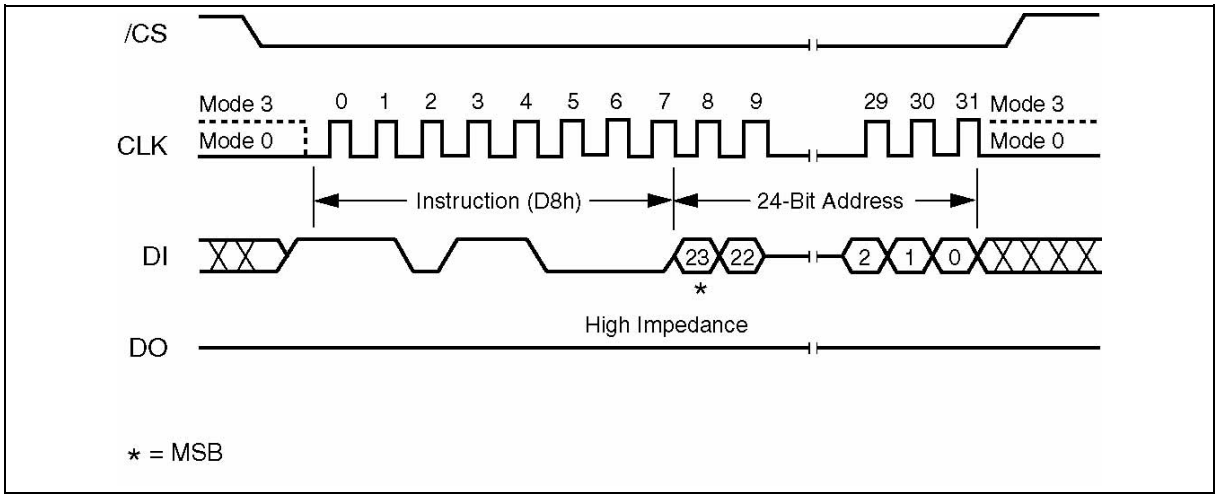


Figure 11. Sector Erase Instruction Sequence Diagram

8.2.11 Chip Erase (C7h)

The Chip Erase instruction sets all memory within the device to the erased state of all 1s (FFh). A Write Enable instruction must be executed before the device will accept the Chip Erase Instruction (Status Register bit WEL must equal 1). The instruction is initiated by driving the /CS pin low and shifting the instruction code “C7h”. The Chip Erase instruction sequence is shown in figure 12.

The /CS pin must be driven high after the eighth bit has been latched. If this is not done the Chip Erase instruction will not be executed. After /CS is driven high, the self-timed Chip Erase instruction will commence for a time duration of t_{CE} (See AC Characteristics). While the Chip Erase cycle is in progress, the Read Status Register instruction may still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Chip Erase cycle and becomes a 0 when finished and the device is ready to accept other instructions again. After the Chip Erase cycle has finished the Write Enable Latch (WEL) bit in the Status Register is cleared to 0.

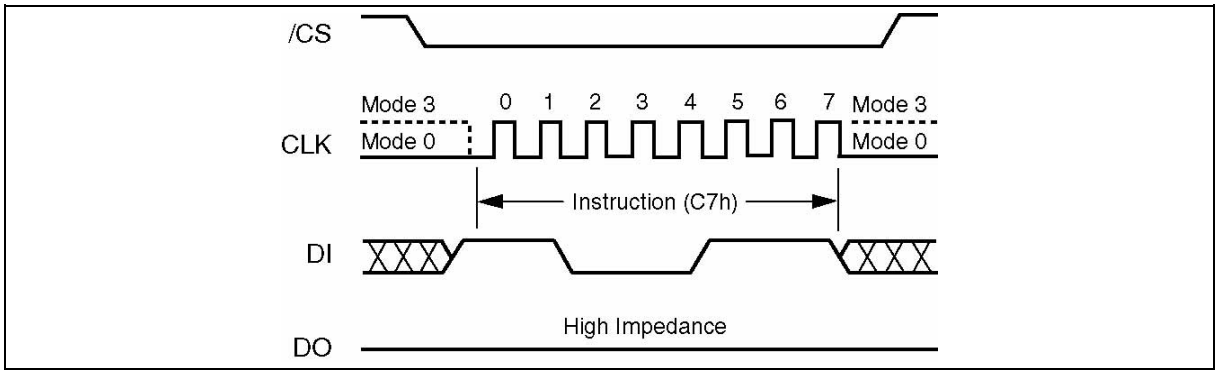


Figure 12. Chip Erase Instruction Sequence Diagram

8.2.12 Power-down (B9h)

Although the standby current during normal operation is relatively low, standby current can be further reduced with the Power-down instruction. The lower power consumption makes the Power-down instruction especially useful for battery powered applications (See ICC1 and ICC2 in AC Characteristics). The instruction is initiated by driving the /CS pin low and shifting the instruction code "B9h" as shown in figure 13.

The /CS pin must be driven high after the eighth bit has been latched. If this is not done the Power-down instruction will not be executed. After /CS is driven high, the power-down state will entered within the time duration of t_{DP} (See AC Characteristics). While in the power-down state only the Release from Power-down / Device ID instruction, which restores the device to normal operation, will be recognized. All other instructions are ignored. This includes the Read Status Register instruction, which is always available during normal operation. Ignoring all but one instruction makes the Power Down state a useful condition for securing maximum write protection. The device always powers-up in the normal operation with the standby current of ICC1.

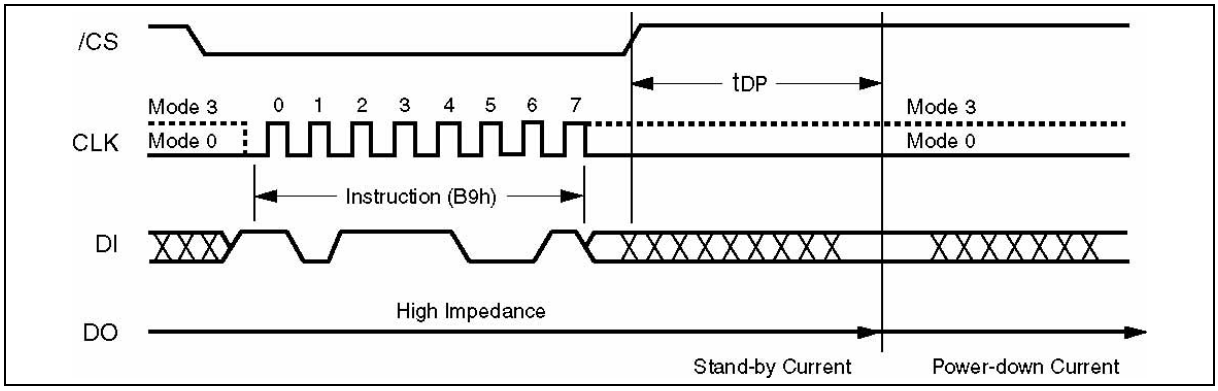


Figure 13. Deep Power-down Instruction Sequence Diagram

8.2.13 Release Power-down / Device ID (ABh)

The Release from Power-down / Device ID instruction is a multi-purpose instruction. It can be used to release the device from the power-down state, obtain the devices electronic identification (ID) number or do both.

When used only to release the device from the power-down state, the instruction is issued by driving the /CS pin low, shifting the instruction code “ABh” and driving /CS high as shown in figure 14. After the time duration of t_{RES1} (See AC Characteristics) the device will resume normal operation and other instructions will be accepted. The /CS pin must remain high during the t_{RES1} time duration.

When used only to obtain the Device ID while not in the power-down state, the instruction is initiated by driving the /CS pin low and shifting the instruction code “ABh” followed by 3-dummy bytes. The Device ID bits are then shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in figure 15. The Device ID value for the W25B40 / W25B40A are listed in Manufacturer and Device Identification table. The Device ID can be read continuously. The instruction is completed by driving /CS high.

When used to release the device from the power-down state and obtain the Device ID, the instruction is the same as previously described, and shown in figure 13, except that after /CS is driven high it must remain high for a time duration of t_{RES2} (See AC Characteristics). After this time duration the device will resume normal operation and other instructions will be accepted.

If the Release from Power-down / Device ID instruction is issued while an Erase, Program or Write cycle is in process (when BUSY equals 1) the instruction is ignored and will not have any effects on the current cycle.

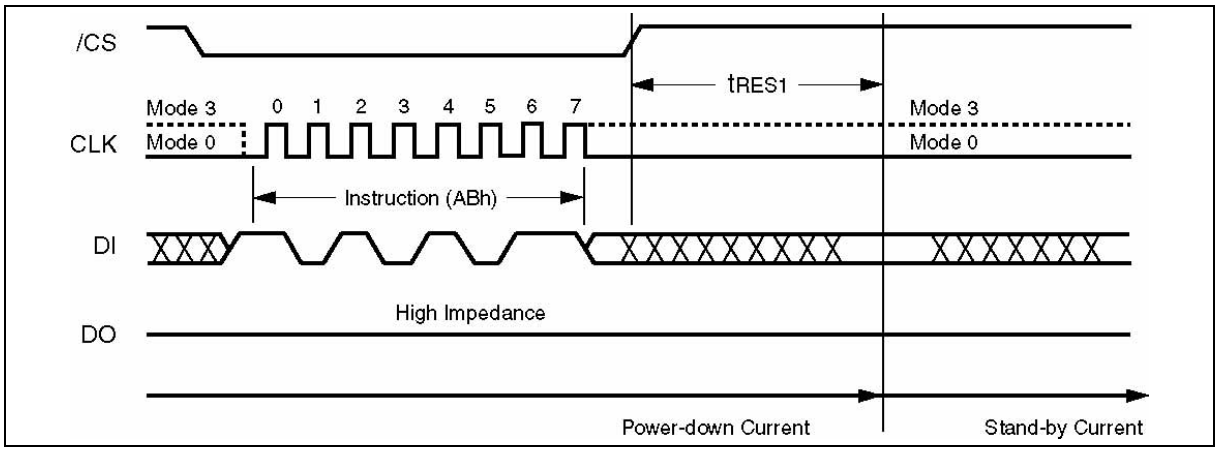


Figure 14. Release Power-down Instruction Sequence

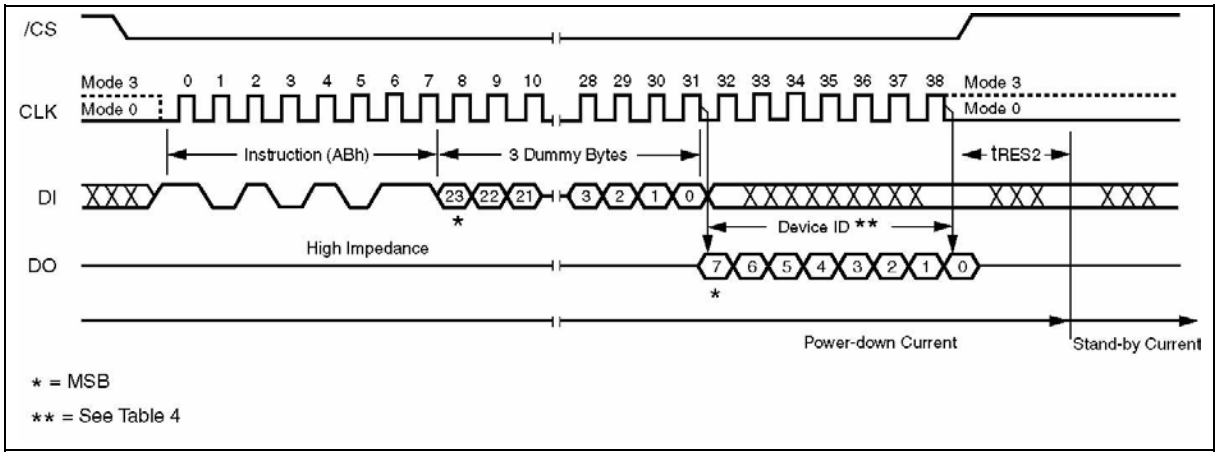


Figure 15. Release Power-down / Device ID Instruction Sequence Diagram

8.2.14 Read Manufacturer / Device ID (90h)

The Read Manufacturer/Device ID instruction is an alternative to the Release from Power-down / Device ID instruction that provides both the JEDEC assigned manufacturer ID and the specific device ID.

The Read Manufacturer/Device ID instruction is very similar to the Release from Power-down / Device ID instruction. The instruction is initiated by driving the /CS pin low and shifting the instruction code "90h" followed by a 24-bit address (A23-A0) of 000000h. After which, the Manufacturer ID for Winbond (EFh) and the Device ID are shifted out on the falling edge of CLK with most significant bit (MSB) first as shown in figure 16. The Device ID values for the W25B40 / W25B40A are listed in Manufacturer and Device Identification table. If the 24-bit address is initially set to 000001h the Device ID will be read first and then followed by the Manufacturer ID. The Manufacturer and Device IDs can be read continuously, alternating from one to the other. The instruction is completed by driving /CS high.

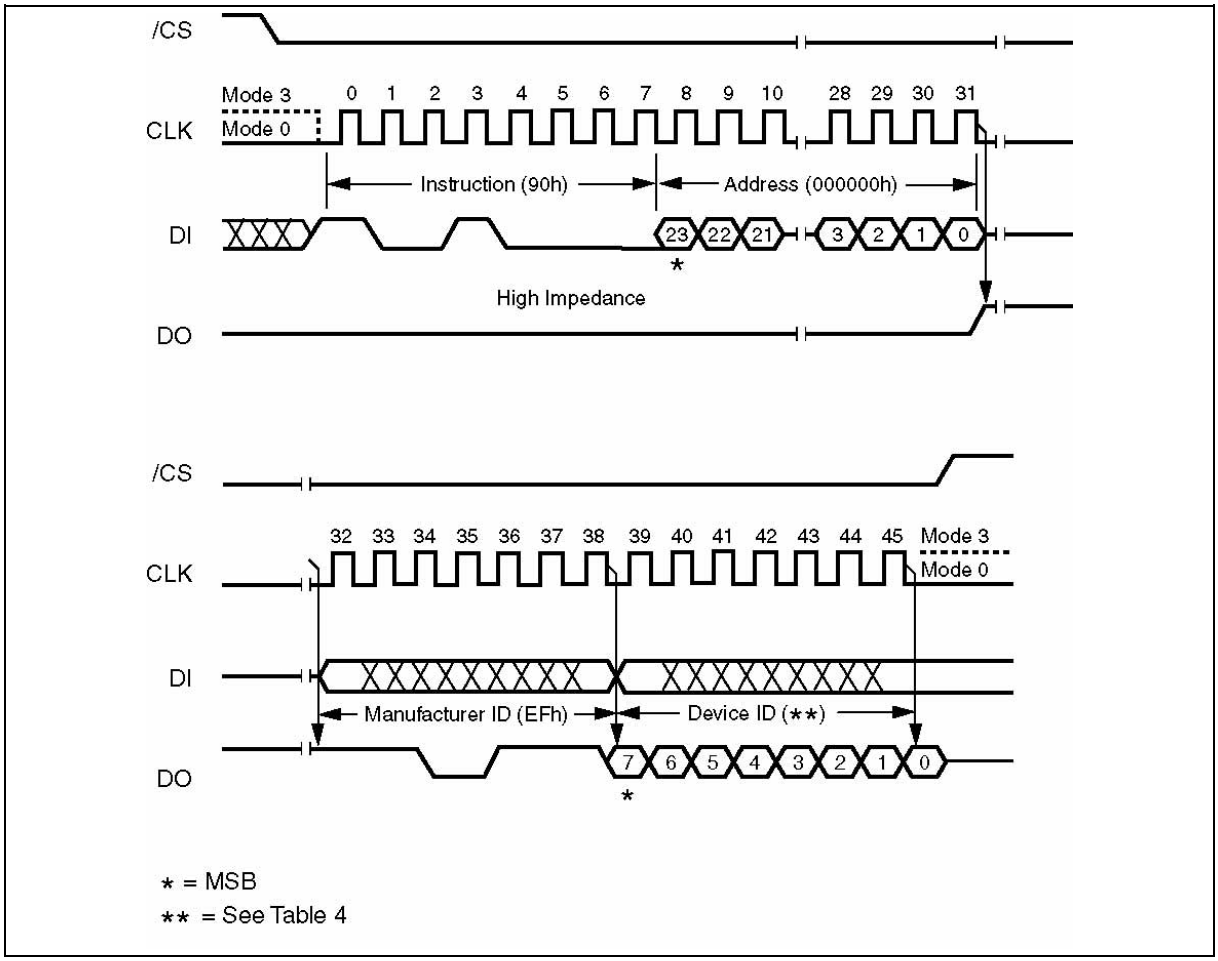


Figure 16. Read Manufacturer / Device ID Diagram

9. ELECTRICAL CHARACTERISTICS

9.1 Absolute Maximum Ratings (1)

PARAMETERS	SYMBOL	CONDITIONS	RANGE	UNIT
Supply Voltage	VCC		–0.6 to +4.0	V
Voltage Applied to Any Pin	VIO	Relative to Ground	–0.6 to VCC +0.4	V
Storage Temperature	TSTG		–65 to +150	°C
Lead Temperature	TLEAD		See Note 2	°C
Electrostatic Discharge Voltage	VESD	Human Body Model(3)	–2000 to +2000	V

Notes:

1 This device has been designed and tested for the specified operation ranges. Proper operation outside of these levels is not guaranteed. Exposure beyond absolute maximum ratings (listed above) may cause permanent damage.

2. Compliant with JEDEC Standard J-STD-20C for small body Sn-Pb or Pb-free (Green) assembly and the European directive on restrictions on hazardous substances (RoHS) 2002/95/EU..

3. JEDEC Std JESD22-A114A (C1=100 pF, R1=1500 ohms, R2=500 ohms).

9.2 Operating Ranges

PARAMETER	SYMBOL	CONDITIONS	SPEC		UNIT
			MIN	MAX	
Supply Voltage(1)	VCC	FR = 33MHz, fR = 25MHz	2.7	3.6	V
		FR = 40MHz, fR = 25MHz	3.0	3.6	V
Ambient Temperature, Operating	TA	Industrial	–40	+85	°C

Note:

1. VCC voltage during Read can operate across the min and max range but should not exceed ±10% of the programming (erase/write) voltage.

9.3 Power-up Timing and Write Inhibit Threshold

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
VCC (min) to /CS Low	t_{VSL}[1]	10		µs
Time Delay Before Write Instruction	t_{PUW}[1]	1	10	ms
Write Inhibit Threshold Voltage	V_{WI}[1]	1	2	V

Note:

1. These parameters are characterized only.

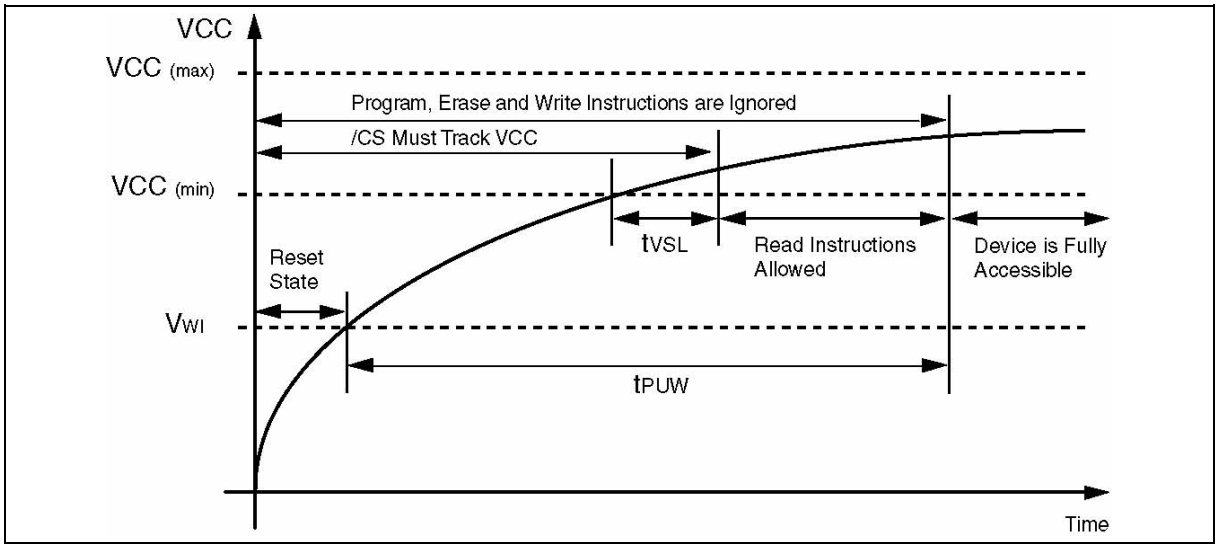


Figure 17. Power-up Timing and Voltage Levels

9.4 DC Electrical Characteristics (Preliminary) (1)

PARAMETER	SYMBOL	CONDITIONS	SPEC			UNIT
			MIN	TYP	MAX	
Input Capacitance	C_{IN}(2)	V_{IN} = 0V(2)			6	pf
Output Capacitance	Cout(2)	V_{OUT} = 0V(2)			8	pf
Input Leakage	I_{LI}				±2	µA
I/O Leakage	I_{LO}				±2	µA
Standby Current	I_{CC1}	/CS = VCC, VIN = GND or VCC		25	50	µA
Power-down Current	I_{CC2}	/CS = VCC, VIN = GND or VCC		<1	5	µA
Current Read Data 1MHz(3)	I_{CC3}	C = 0.1 VCC / 0.9 VCC DO = Open		5	7	mA
Current Read Data 20MHz(3)	I_{CC3}	C = 0.1 VCC / 0.9 VCC DO = Open		10	14	mA
Current Read Data 33MHz(3)	I_{CC3}	C = 0.1 VCC / 0.9 VCC DO = Open		14	18	mA
Current Page Program	I_{CC4}	/CS = VCC		15	20	mA
Current Write Status Register	I_{CC5}	/CS = VCC		6	20	mA
Current Sector Erase	I_{CC6}	/CS = VCC		15	25	mA
Current Chip Erase	I_{CC7}	/CS = VCC		17	25	mA
Input Low Voltage	V_{IL}		–0.5		VCC x0.3	V
Input High Voltage	V_{IH}		VCC x0.7		VCC +0.4	V
Output Low Voltage	V_{OL}	I_{OL} = 1.6 mA			0.4	V
Output High Voltage	V_{OH}	I_{OH} = –100 µA	VCC –0.2			V

Notes:

1 See Preliminary Designation.

2. Tested on sample basis and specified through design and characterization data. TA=25° C, VCC 3V.

3. Checker Board Pattern.

9.5 AC Measurement Conditions

PARAMETER	SYMBOL	SPEC		UNIT
		MIN	MAX	
Load Capacitance	C_L	30	30	pF
Input Rise and Fall Times	T_R, T_F		5	ns
Input Pulse Voltages	V_{IN}	0.2 VCC to	0.8 VCC	V
Output Timing Reference Voltages	OUT	0.3 VCC to	0.7 VCC	V

Note:

1. Output Hi-Z is defined as the point where data out is no longer driven.

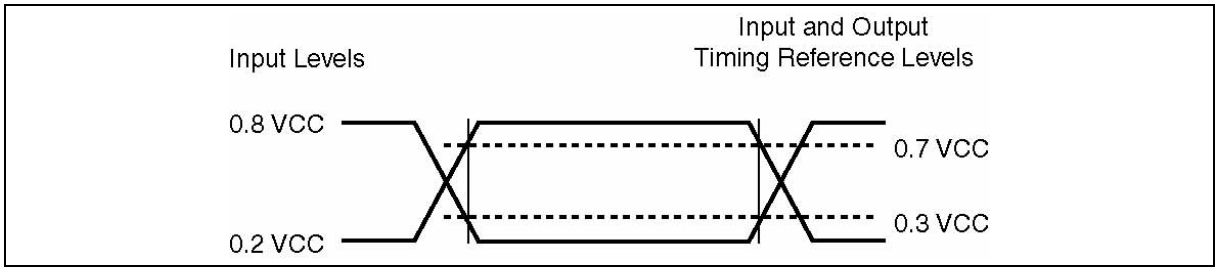


Figure 18. AC Measurement I/O Waveform

9.6 AC Electrical Characteristics (Preliminary)

DESCRIPTION	SYMBOL	ALT	SPEC			UNIT
			MIN	TYP	MAX	
Clock frequency, for Fast Read (0Bh) and all other instructions except Read Data (03h) 2.7V-3.6V VCC 3.0V-3.6V VCC	f_R	f_C	 D.C. D.C.		 33 40	 MHz MHz
Clock freq. Read Data instruction (03h) 2.7V-3.6V VCC 3.0V-3.6V VCC (for sequential read only) *	f_R		 D.C. D.C.		 25 33	 MHz MHz
Clock High, Low Time, for Fast Read (0Bh) and all other instructions except Read Data (03h)	t_{CLH}, t_{CLL}(1)		11			ns
Clock High, Low Time for Read Data instruction	t_{CRLH}, t_{CRLL}(1)		11			ns
Clock Rise Time peak to peak	t_{CLCH}(2)		0.1			V/ns
Clock Fall Time peak to peak	t_{CHCL}(2)		0.1			V/ns
/CS Active Setup Time relative to CLK	t_{SLCH}	t_{CSS}	5			ns
/CS Not Active Hold Time relative to CLK	t_{CHSL}		5			ns
Data In Setup Time	t_{DVCH}	t_{DSU}	2			ns
Data In Hold Time	t_{CHDX}	t_{DH}	5			ns
/CS Active Hold Time relative to CLK (2.7V-3.6V / 3.0V-3.6V)	t_{CHSH}		7/5			ns
/CS Not Active Setup Time relative to CLK	t_{SHCH}		5			ns
/CS Deselect Time	t_{SHSL}	t_{CSH}	100			ns
Output Disable Time	t_{SHQZ}(2)	t_{DIS}			9	ns
Clock Low to Output Valid (2.7V-3.6V / 3.0V-3.6V)	t_{CLQV}	t_V			12/9	ns
Output Hold Time	t_{CLQX}	t_{HO}	0			ns
/HOLD Active Setup Time relative to CLK (2.7V-3.6V / 3.0V-3.6V)	t_{HLCH}		6/5			ns

Continued – next page

* Sequential read uses autoincrement address, not random addressing.

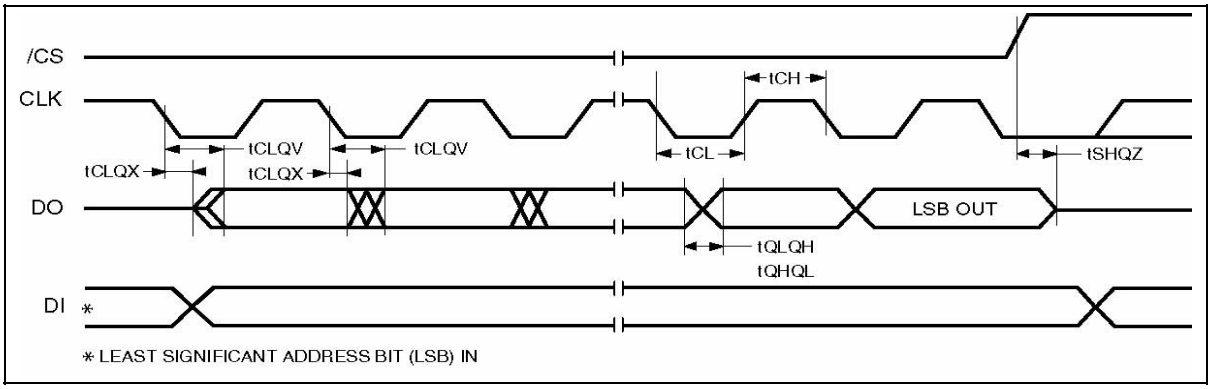
9.7 AC Electrical Characteristics (Preliminary) cont'd

DESCRIPTION	SYMBOL	ALT	SPEC			UNIT
			MIN	TYP	MAX	
/HOLD Active Hold Time relative to CLK	t_{CHHH}		5			ns
/HOLD Not Active Setup Time relative to CLK	t_{HHCH}		5			ns
/HOLD Not Active Hold Time relative to CLK	t_{CHHL}		5			ns
/HOLD to Output Low-Z	t_{HHQX}(2)	t_{LZ}			9	ns
/HOLD to Output High-Z	t_{HLQZ}(2)	t_{HZ}			9	ns
Write Protect Setup Time Before /CS Low	t_{WHSL}(4)		20			ns
Write Protect Hold Time After /CS High	t_{SHWL}(4)		100			ns
/CS High to Power-down Mode	t_{DP}(2)				3	µs
/CS High to Standby Mode without Electronic Signature Read	t_{RES1}(2)				3	µs
/CS High to Standby Mode with Electronic Signature Read	t_{RES2}(2)				1.8	µs
Write Status Register Cycle Time	t_W			10	15	ms
Page Program Cycle Time	t_{PP}			2	5	ms
Sector Erase Cycle Time 64KB sectors	t_{SE}			0.65	2	s
Sector Erase Cycle Time 32KB sectors				0.37	1	s
Sector Erase Cycle Time 16KB sectors				0.23	0.7	s
Sector Erase Cycle Time 8KB sectors				0.15	0.45	s
Sector Erase Cycle Time 4KB sectors				0.12	0.35	s
Chip Erase Cycle Time	t_{CE}			5.5	10	s

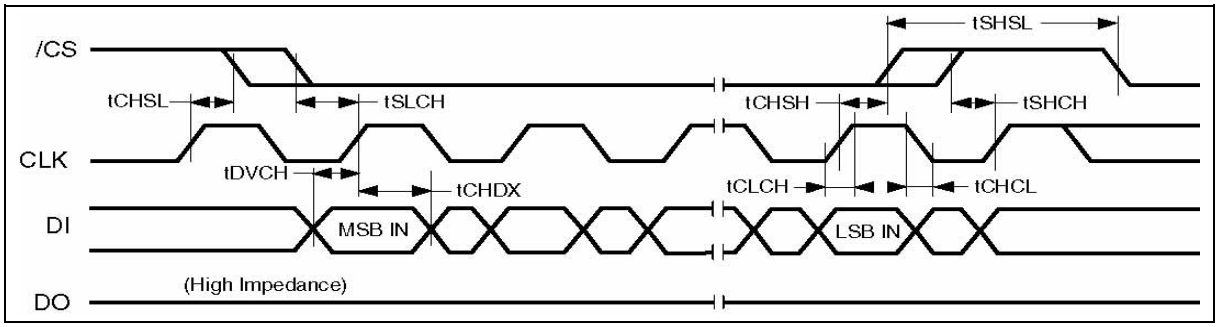
Notes:

1. Clock high + Clock low must be less than or equal to 1/fc.
2. Value guaranteed by design and/or characterization, not 100% tested in production.
3. Expressed as a slew-rate.
4. Only applicable as a constraint for a Write Status Register instruction when Sector Protect Bit is set at 1.

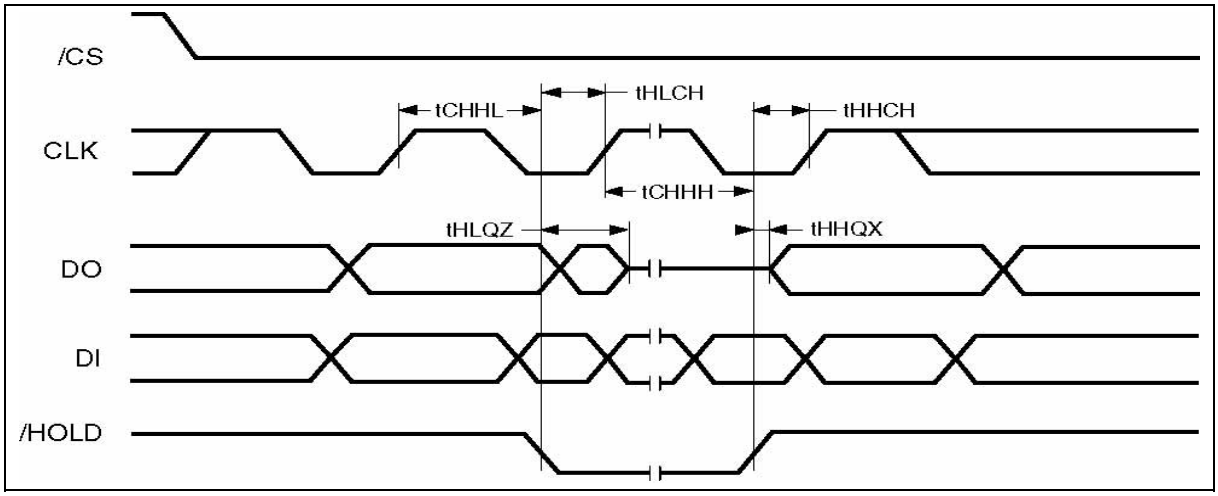
9.8 Serial Output Timing



9.9 Input Timing

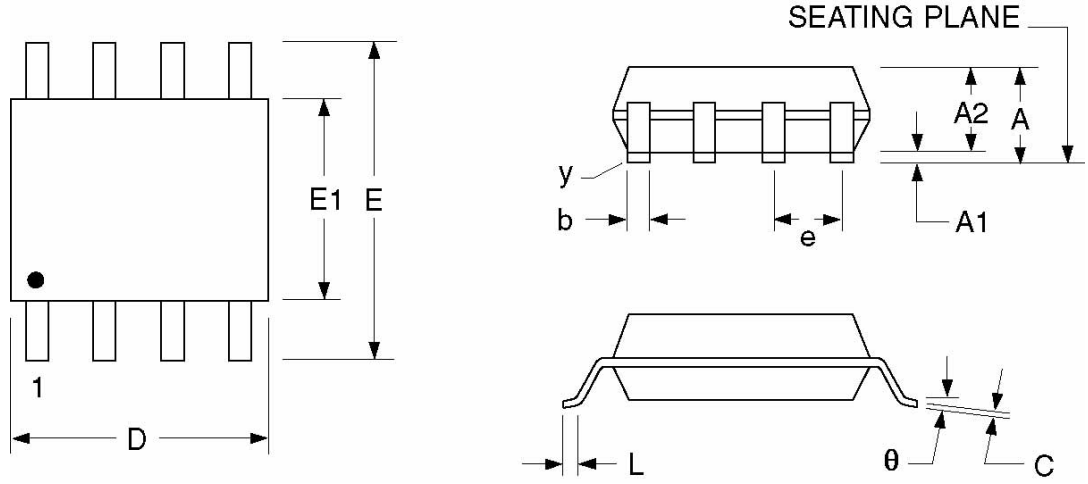


9.10 Hold Timing



10. PACKAGE SPECIFICATION

10.1 8-Pin SOIC 150-mil (Package Code SN)

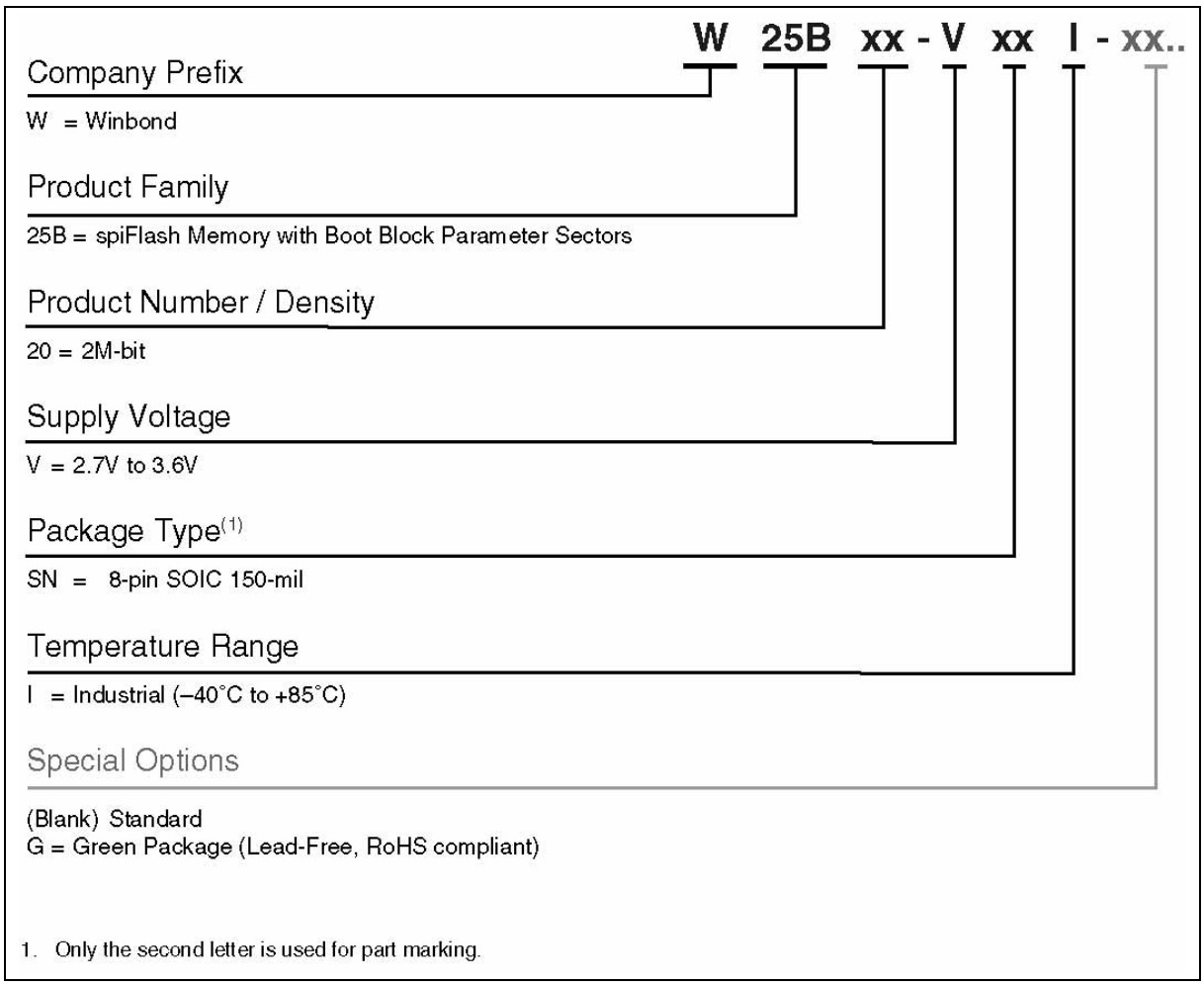


SYMBOL	MILLIMETERS			INCHES		
	MIN	TYP.	MAX	MIN	TYP.	MAX
A	1.47	1.60	1.72	0.058	0.063	0.068
A1	0.10	---	0.24	0.004	---	0.010
A2	---	1.45	---	---	0.057	---
b	0.33	0.41	0.50	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D(3)	4.80	4.85	4.95	0.189	0.191	0.195
E	5.80	6.00	6.19	0.228	0.236	0.244
E1(3)	3.80	3.90	4.00	0.150	0.154	0.157
e(2)	1.27 BSC			0.050 BSC		
L	0.40	0.71	1.27	0.015	0.028	0.050
θ	0°	---	8°	0°	---	8°
y	---	---	0.076	---	---	0.003

Notes:

1. Controlling dimensions: inches, unless otherwise specified.
2. BSC = Basic lead spacing between centers.
3. Dimensions D and E1 do not include mold flash protrusions and should be measured from the bottom of the package.

11. ORDERING INFORMATION



12. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A	06/09/04		New Create
B	08/13/04		Updated f_R and t_{CRLH}, t_{CRLL} data in AC Electrical Characteristics
C	09/25/04		Updated t_{SE} data in AC Electrical Characteristics
D	11/03/04		Modified t_{LEAD} in Absolute Maximum Ratings to reference JEDEC Standard information. Added F_R and f_R conditions to Operating Ranges. Updated I_{CC3} and I_{CC5} data in DC Electrical Characteristics. Added 20/33MHz call outs and updated min, max and typ data in AC Electrical Characteristics. Updated text for Chip Erase instruction.
E	12/05/04		Updated 8-pin SOIC 150-mil package information. Updated Green Package information under Special Options of Ordering Information. Removed 8-contact MLP 6x5mm package
F	01/19/05		Updated Sector Erase instruction and related notes in Instruction Set.
G	04/03/05		Updated package dimension symbols and values A1 and y for compliance.
H	05/09/05		Updated and improved AC Parameters in and changed t_{CHSH}, t_{CLQV} and t_{HLCH} to reference voltage (2.7V-3.6V / 3.0V-3.6V) for consistency with other spiFlash memory data sheets.
I	06/14/05		Updated Important Notice
J	06/28/05		Changed NexFlash part numbers to Winbond part numbers and updated ordering and contact information
K	12/22/05	ALL	Updated data sheet to comply with Winbond standard. Updated FR and f_R values in Operating Ranges Table and AC Characteristics Table Updated f_R = 25MHz and 33MHz in Operating Ranges Table and AC Characteristics Table for both 2.7V-3.6V and 3.0V-3.6V. Corrected Ordering Information chart from product family 25P to 25B.
L	12/26/05		Corrected Ordering Information
M	01/06/06	5	Corrected the pin assignment on table of pin description of page 5.

Preliminary Designation

The "Preliminary" designation on a *Winbond* data sheet indicates that the product is not fully characterized. The specifications are subject to change and are not guaranteed. *Winbond* or an authorized sales representative should be consulted for current information before using this product.

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Winbond products are not designed, intended, authorized or warranted for use as components in systems or equipment intended for surgical implantation, atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, or for other applications intended to support or sustain life. Further more, Winbond products are not intended for applications wherein failure of Winbond products could result or lead to a situation wherein personal injury, death or severe property or environmental damage could occur.

Winbond customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Winbond for any damages resulting from such improper use or sales.

NexFlash® Technologies, Inc.

The Winbond W25B40/40A is fully compatible with the previous NexFlash NX25B40 Serial Flash memory.

Headquarters
No. 4, Creation Rd. III,
Science-Based Industrial Park,
Hsinchu, Taiwan
TEL: 886-3-5770066
FAX: 886-3-5665577
http://www.winbond.com.tw/

Taipei Office
9F, No.480, Rueiguang Rd.,
Neihu District, Taipei, 114,
Taiwan, R.O.C.
TEL: 886-2-8177-7168
FAX: 886-2-8751-3579

Winbond Electronics Corporation America
2727 North First Street, San Jose,
CA 95134, U.S.A.
TEL: 1-408-9436666
FAX: 1-408-5441798

Winbond Electronics Corporation Japan
7F Daini-ueno BLDG, 3-7-18
Shinyokohama Kohoku-ku,
Yokohama, 222-0033
TEL: 81-45-4781881
FAX: 81-45-4781800

Winbond Electronics (Shanghai) Ltd.
27F, 2299 Yan An W. Rd. Shanghai,
200336 China
TEL: 86-21-62365999
FAX: 86-21-62365998

Winbond Electronics (H.K.) Ltd.
Unit 9-15, 22F, Millennium City,
No. 378 Kwun Tong Rd.,
Kowloon, Hong Kong
TEL: 852-27513100
FAX: 852-27552064

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