FAIRCHILD SEMICONDUCTOR™

April 2000

QFET™

FQAF13N50

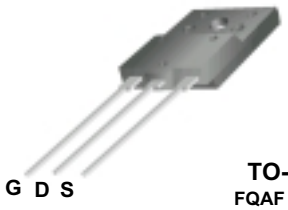
500V N-Channel MOSFET

General Description

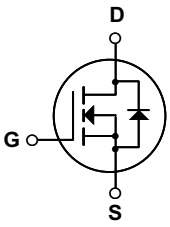
These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switch mode power supply, power factor correction, electronic lamp ballast based on half bridge.

Features

- 9.6A, 500V, $R_{DS(on)}$ = 0.43Ω @V_{GS} = 10 V
- Low gate charge (typical 45 nC)
- Low Crss (typical 25 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



TO-3PF
FQAF Series



Absolute Maximum Ratings

T_C = 25°C unless otherwise noted

Symbol	Parameter		FQAF13N50	Units
V_{DSS}	Drain-Source Voltage		500	V
I_D	Drain Current - Continuous (T_C = 25°C)		9.6	A
	Drain Current - Continuous (T_C = 100°C)		6.1	A
I_{DM}	Drain Current - Pulsed	(Note 1)	38.4	A
V_{GSS}	Gate-Source Voltage		± 30	V
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	810	mJ
I_{AR}	Avalanche Current	(Note 1)	9.6	A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	10	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	4.5	V/ns
P_D	Power Dissipation (T_C = 25°C)		100	W
	- Derate above 25°C		0.8	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		300	°C

Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	1.25	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	40	°C/W

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Electrical Characteristics

T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	500	--	--	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	--	0.48	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 500 V, V_{GS} = 0 V	--	--	1	μA
		V_{DS} = 400 V, T_C = 125°C	--	--	10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 30 V, V_{DS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -30 V, V_{DS} = 0 V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	3.0	--	5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 4.8 A	--	0.33	0.43	Ω
g_{FS}	Forward Transconductance	V_{DS} = 50 V, I_D = 4.8 A (Note 4)	--	8.5	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	--	1800	2300	pF
C_{oss}	Output Capacitance		--	245	320	pF
C_{rss}	Reverse Transfer Capacitance		--	25	35	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 250 V, I_D = 13.4 A, R_G = 25 Ω (Note 4, 5)	--	40	90	ns
t_r	Turn-On Rise Time		--	140	290	ns
$t_{d(off)}$	Turn-Off Delay Time		--	100	210	ns
t_f	Turn-Off Fall Time		--	85	180	ns
Q_g	Total Gate Charge	V_{DS} = 400 V, I_D = 13.4 A, V_{GS} = 10 V (Note 4, 5)	--	45	60	nC
Q_{gs}	Gate-Source Charge		--	11	--	nC
Q_{gd}	Gate-Drain Charge		--	22	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	9.6	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	38.4	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 9.6 A	--	--	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = 13.4 A, dI_F / dt = 100 A/μs (Note 4)	--	290	--	ns
Q_{rr}	Reverse Recovery Charge		--	2.6	--	μC

Notes:
1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 15.8mH, I_{AS} = 9.6A, V_{DD} = 50V, R_G = 25 Ω, Starting T_J = 25°C
3. I_{SD} ≤ 13.4A, di/dt ≤ 200A/μs, V_{DD} ≤ $BV_{DSS,}$ Starting T_J = 25°C
4. Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2%
5. Essentially independent of operating temperature

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Typical Characteristics

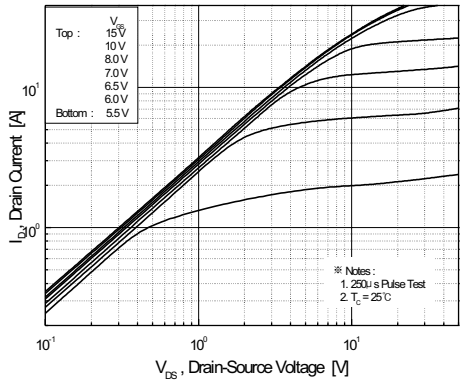


Figure 1. On-Region Characteristics

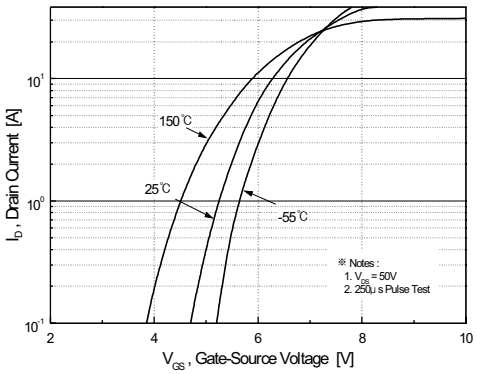


Figure 2. Transfer Characteristics

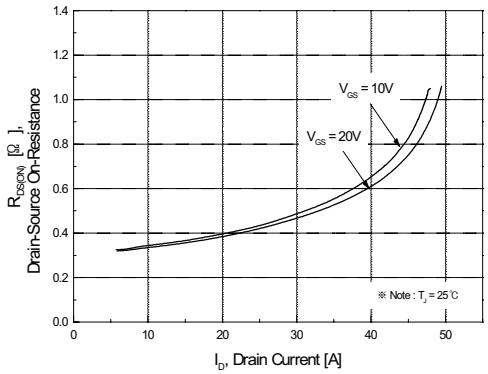


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

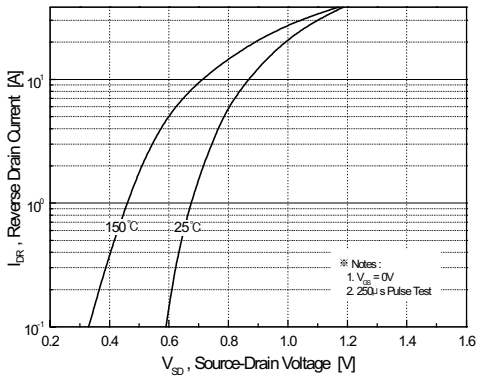


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

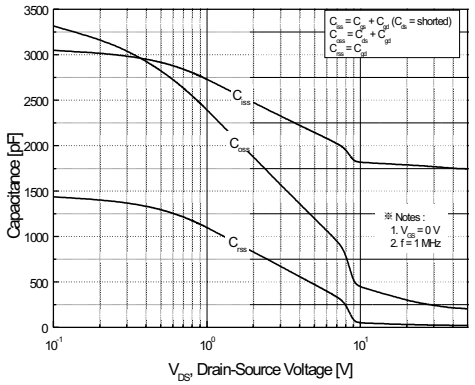


Figure 5. Capacitance Characteristics

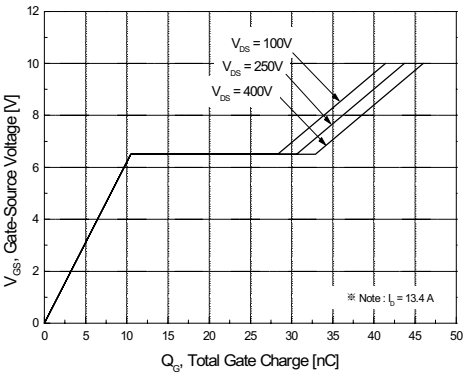


Figure 6. Gate Charge Characteristics

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Typical Characteristics (Continued)

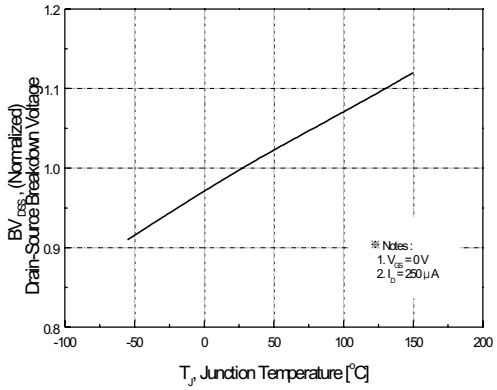


Figure 7. Breakdown Voltage Variation vs. Temperature

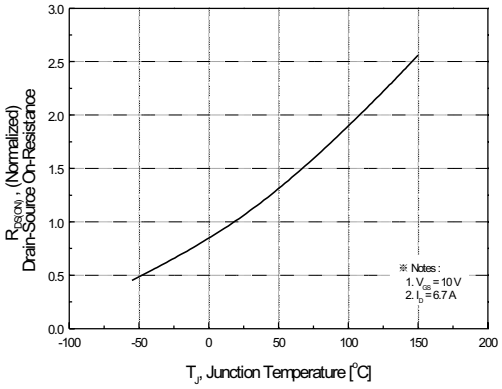


Figure 8. On-Resistance Variation vs. Temperature

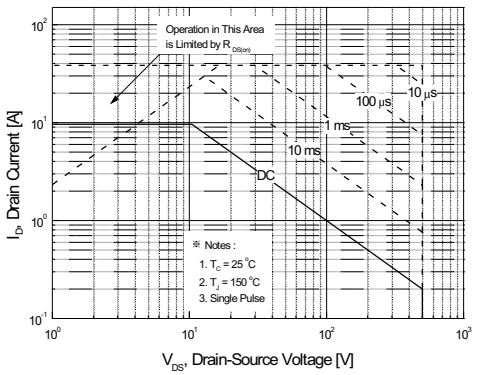


Figure 9. Maximum Safe Operating Area

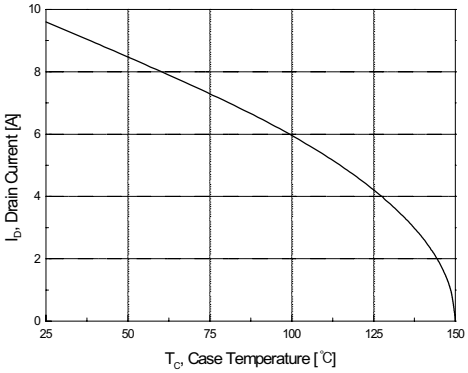


Figure 10. Maximum Drain Current vs. Case Temperature

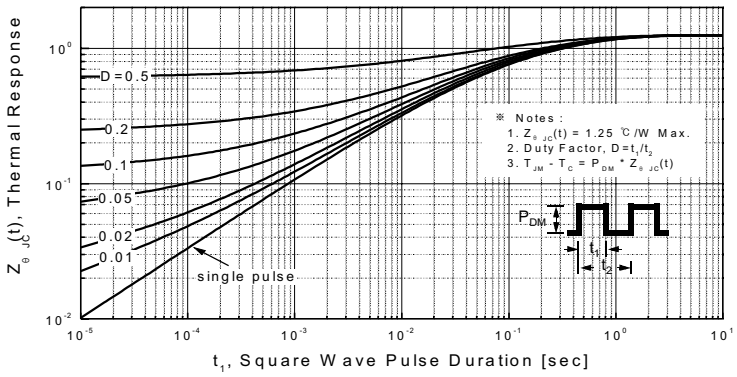
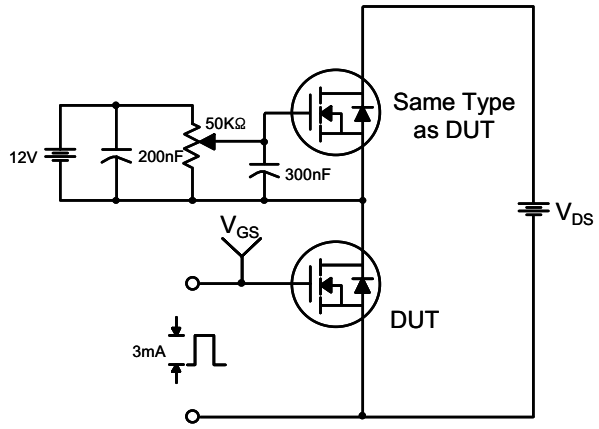
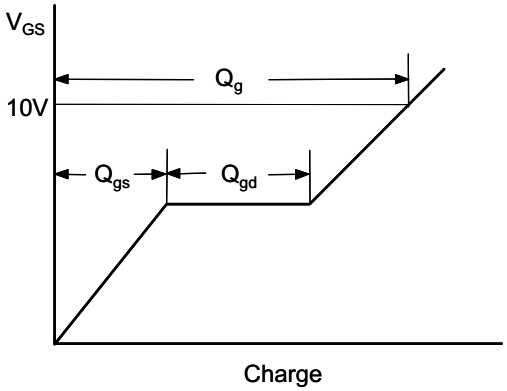


Figure 11. Transient Thermal Response Curve

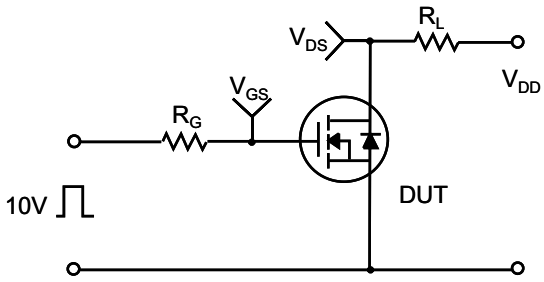
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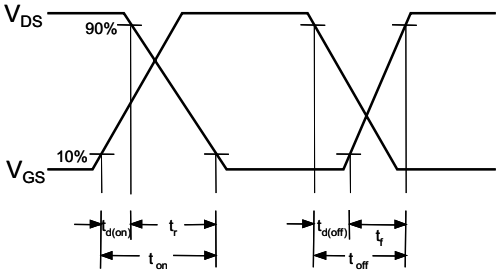
Gate Charge Test Circuit & Waveform



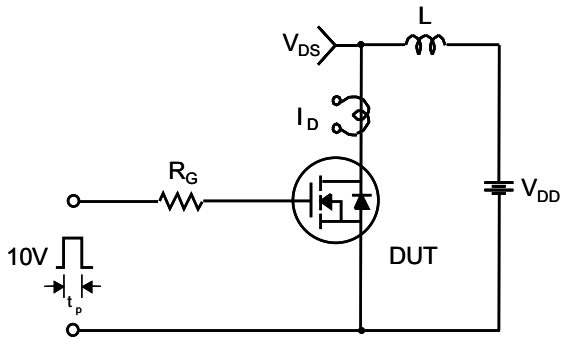


Resistive Switching Test Circuit & Waveforms

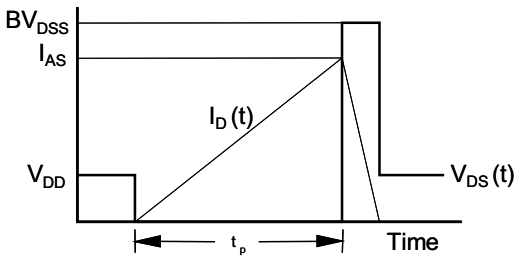




Unclamped Inductive Switching Test Circuit & Waveforms

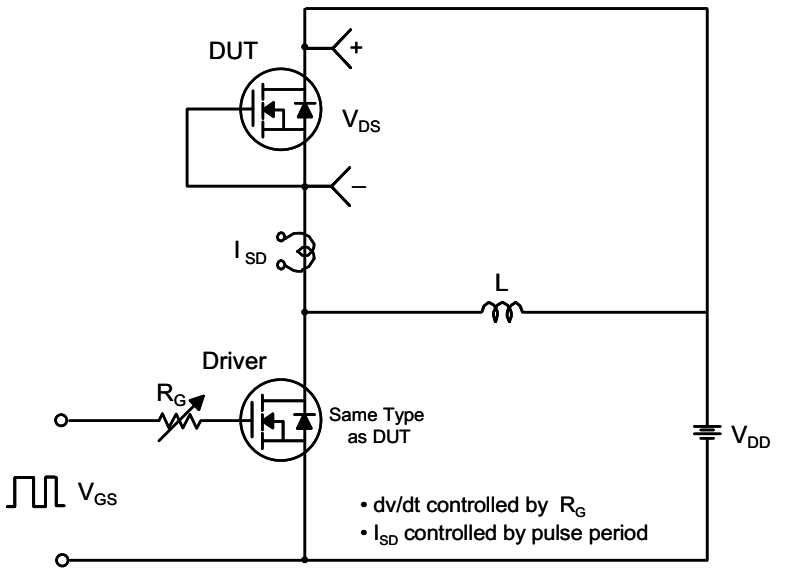


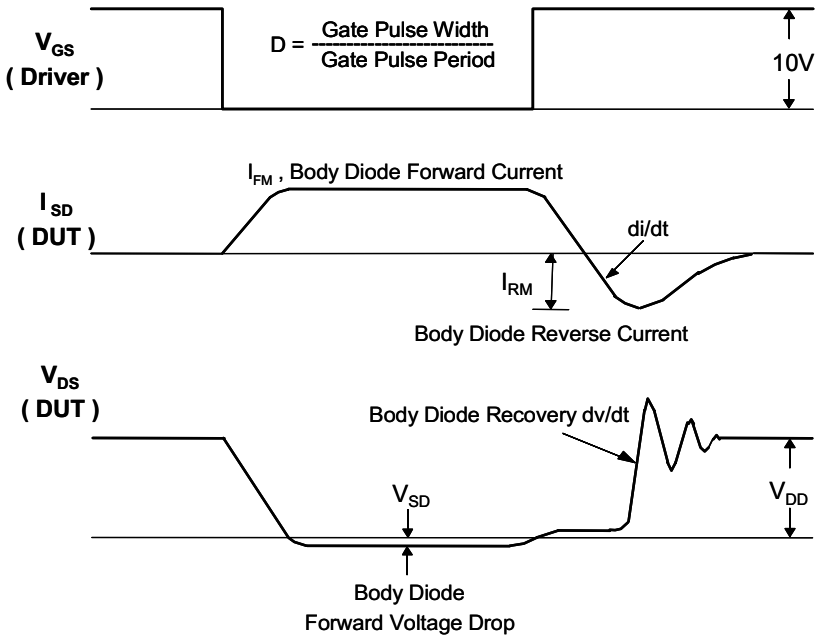
$$E_{AS} = \frac{1}{2} L I_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$



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Peak Diode Recovery dv/dt Test Circuit & Waveforms

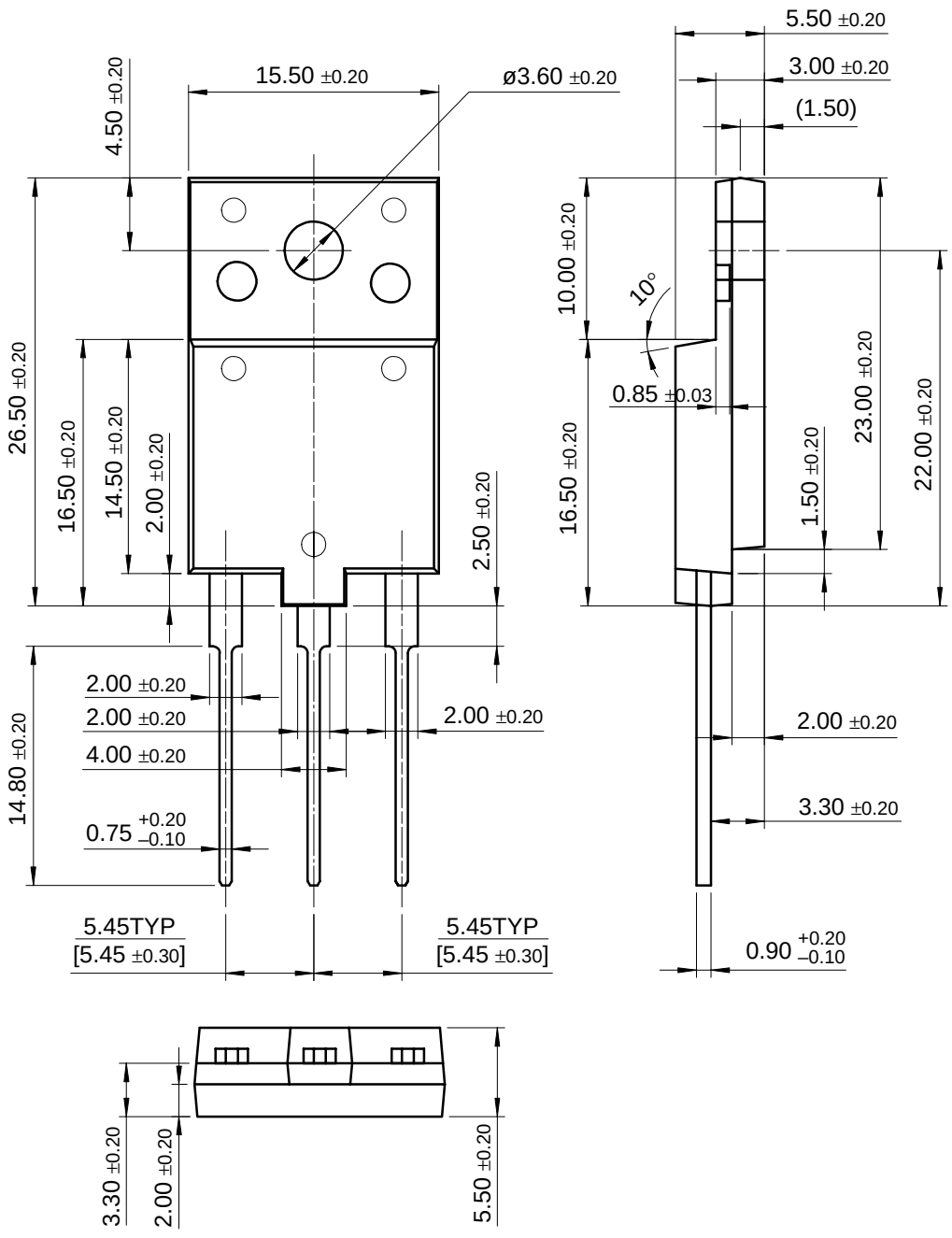




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Package Dimensions

TO-3PF



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