*Click **here** for production status of specific part numbers.*

MAX32660

Tiny, Ultra-Low-Power Arm Cortex-M4 Processor with FPU-Based Microcontroller (MCU) with 256KB Flash and 96KB SRAM

General Description

In the DARWIN family, the MAX32660 is an ultra-low-power, cost-effective, highly-integrated 32-bit microcontroller designed for battery-powered devices and wireless sensors. It combines a flexible and versatile power management unit with the powerful Arm® Cortex®-M4 processor with floating point unit (FPU) in the industry's smallest form factor: 1.6mm x 1.6mm, 16-bump WLP or 4mm x 4mm, 20-pin TQFN-EP, or 3mm x 3mm, 24-pin TQFN-EP.

The MAX32660 enables designs with complex sensor processing without compromising battery life. It also offers legacy designs an easy and cost optimal upgrade path from 8- or 16-bit microcontrollers.

The device supports SPI, UART, and I²C communication while also integrating up to 256KB of flash memory and 96KB of RAM to accommodate application and sensor code. An optional bootloader through I²C, UART, or SPI is available.

Applications

- Sports Watches
- Fitness Monitors
- Wearable Medical Patches
- Portable Medical Devices
- Industrial Sensors
- IoT
- Optical Modules: QSFP-DD, QSFP, 400G

Benefits and Features

- High-Efficiency Microcontroller for Wearable Devices
  - Internal Oscillator Operates Up to 96MHz
  - 256KB Flash Memory
  - 96KB SRAM, Optionally Preserved in Lowest Power Backup Mode
  - 16KB Instruction Cache
  - Memory Protection Unit (MPU)
  - Low 1.1V V_{CORE} Supply Voltage
  - 3.6V GPIO Operating Range
  - Internal LDO Provides Operation from Single Supply
  - Wide Operating Temperature: -40°C to +105°C
- Power Management Maximizes Uptime for Battery Applications
  - 85µA/MHz Active Executing from Flash
  - 2µA Full Memory Retention Power in Backup Mode at V_{DD} = 1.8V
  - 450nA Ultra-Low Power RTC at V_{DD} = 1.8V
  - Internal 80kHz Ring Oscillator
- Optimal Peripheral Mix Provides Platform Scalability
  - Up to 14 General-Purpose I/O Pins
  - Up to Two SPI Master/Slave
  - I²S Master/Slave
  - Up to Two UARTs
  - Up to Two I²C Master/Slave, 3.4Mbps High Speed
  - Four-Channel Standard DMA Controller
  - Three 32-Bit Timers
  - Watchdog Timer
  - CMOS-Level 32.768kHz RTC Output

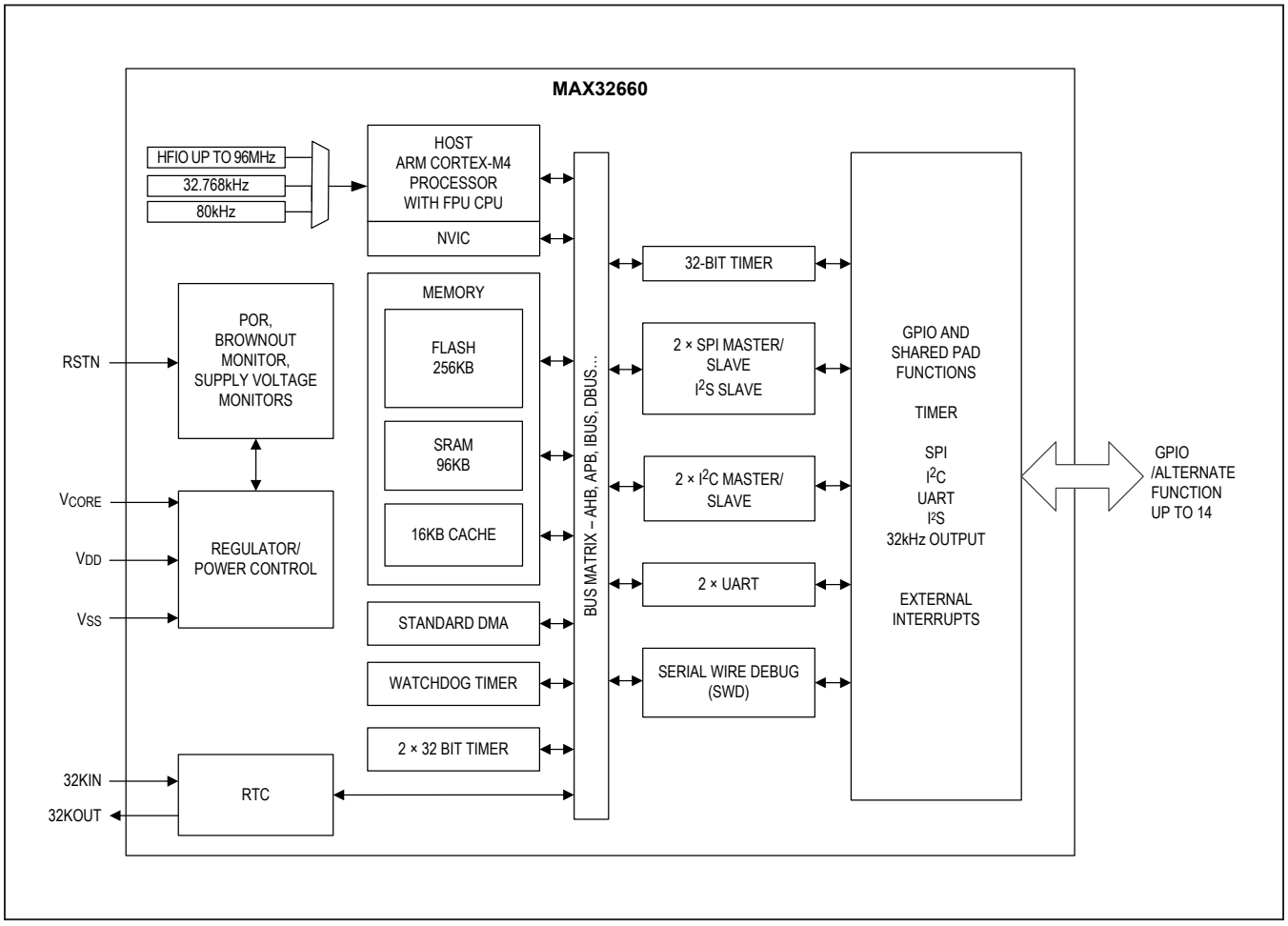
***Ordering Information** appears at end of data sheet.*

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19-100236; Rev 8; 9/19

maxim integrated™

Simplified Block Diagram



Absolute Maximum Ratings

(All voltages with respect to V_{SS}, unless otherwise noted.)

V_{CORE} .....-0.3V to +1.21V
V_{DD}.....-0.3V to +3.63V
32KIN, 32KOUT.....-0.3V to V_{DD} + 0.3V
RSTN, GPIO.....-0.3V to V_{DD} + 0.3V
Total Current into All GPIO Combined (sink).....100mA
V_{SS}.....100mA
Output Current (sink) by Any GPIO Pin 25mA
Output Current (source) by Any GPIO Pin.....-25mA

Continuous Package Power Dissipation
20 TQFN-EP (multilayer board) TA = +70°C
(derate 30.3mW/°C above +70°C) 2424.2mW
Continuous Package Power Dissipation
24 TQFN-EP (multilayer board) T_A = +70°C
(derate 16.3mW/°C above +70°C) 1305mW
Operating Temperature Range..... -40°C to +105°C
Storage Temperature Range..... -65°C to +150°C
Soldering Temperature (reflow).....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

16 WLP

Package Code	W161K1+1
Outline Number	**21-100241**
Land Pattern Number	Refer to **Application Note 1891**
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	66.34 °C/W
Junction to Case (θ_{JC})	N/A

20 TQFN-EP

Package Code	T2044+5C
Outline Number	**21-0139**
Land Pattern Number	**90-0429**
Thermal Resistance, Single-Layer Board:	
Junction to Ambient (θ_{JA})	48°C/W
Junction to Case (θ_{JC})	2°C/W
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	33°C/W
Junction to Case (θ_{JC})	2°C/W

24 TQFN-EP

Package Code	T2433+2C
Outline Number	**21-100264**
Land Pattern Number	**90-100089**
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	61.3°C/W
Junction to Case (θ_{JC})	2.2°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLIES/BOTH SINGLE SUPPLY OPERATION AND DUAL SUPPLY OPERATION							
Supply Voltage	V_{DD}			1.71	1.8	3.63	V
Supply Voltage, Core	V_{CORE}	Dual-supply operation	OVR = [00]	0.855	0.9	0.945	V
			OVR = [01]	0.95	1.0	1.05	
			Default OVR = [10]	1.045	1.1	1.155	
		Single-supply operation		Not used			
Power-Fail Reset Voltage	V_{RST}	Monitors V_{DD}		1.63		1.71	V
		Monitors V_{CORE} during dual-supply operation		0.80		0.845	
Power-On Reset Voltage	V_{POR}	Monitors V_{DD}			1.4		V
		Monitors V_{CORE} during dual supply operation			0.65		
Sleep Mode Resume Time	t_{SLP_ON}				0.57		µs
Deep Sleep Mode Resume Time	t_{DSL_ON}				150		µs
Backup Mode Resume Time	t_{BKU_ON}				150		µs
POWER SUPPLIES/SINGLE SUPPLY OPERATION (V_{DD} ONLY)							
V_{DD} Dynamic Current, Active Mode	I_{DD_DACT}	HFIO enabled, total current into V_{DD} pin, CPU in Active mode, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], Internal regulator set to 1.1V, $f_{SYS_CLK(MAX)}$ = 96MHz		85		µA/MHz
			OVR = [01], Internal regulator set to 1.0V, $f_{SYS_CLK(MAX)}$ = 48MHz		74		
			OVR = [00], Internal regulator set to 0.9V, $f_{SYS_CLK(MAX)}$ = 24MHz		50		
V_{DD} Fixed Current, Active Mode	I_{DD_FACT}	HFIO enabled, total current into V_{DD} pin, CPU in Active mode 0MHz execution, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], Internal regulator set to 1.1V, $f_{SYS_CLK(MAX)}$ = 96MHz		488		µA
			OVR = [01], Internal regulator set to 1.0V, $f_{SYS_CLK(MAX)}$ = 48MHz		394		
			OVR = [00], Internal regulator set to 0.9V, $f_{SYS_CLK(MAX)}$ = 24MHz		324		

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD} Dynamic Current, Sleep Mode	I_{DD_DSLP}	HFIO enabled, total current into V_{DD} pin, CPU in Sleep mode, standard DMA with two channels active	OVR = [10], Internal regulator set to 1.1V, $f_{SYS_CLK(MAX)}$ = 96MHz		30.3		µA/MHz
			OVR = [01], Internal regulator set to 1.0V, $f_{SYS_CLK(MAX)}$ = 48MHz		27		
			OVR = [00], Internal regulator set to 0.9V, $f_{SYS_CLK(MAX)}$ = 24MHz		24		
V_{DD} Fixed Current, Sleep Mode	I_{DD_FSLP}	HFIO enabled, total current into V_{DD} pin, CPU in Sleep mode, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA	OVR = [10], Internal regulator set to 1.1V, $f_{SYS_CLK(MAX)}$ = 96MHz		485		µA
			OVR = [01], Internal regulator set to 1.0V, $f_{SYS_CLK(MAX)}$ = 48MHz		391		
			OVR = [00], Internal regulator set to 0.9V, $f_{SYS_CLK(MAX)}$ = 24MHz		321		
V_{DD} Fixed Current, Deep Sleep Mode	I_{DD_FDSL}	Standby state with full data retention and 96kB SRAM retained			4.2		µA
V_{DD} Fixed Current, Backup Mode	I_{DD_FBKU}	0KB SRAM retained with RTC enabled; V_{DD}=1.8V			0.53		µA
		16KB SRAM retained with RTC enabled; V_{DD}=1.8V			0.99		
		32KB SRAM retained with RTC enabled; V_{DD}=1.8V			1.20		
		64KB SRAM retained with RTC enabled; V_{DD}=1.8V			1.64		
		96KB SRAM retained with RTC enabled; V_{DD}=1.8V			1.94		
POWER SUPPLIES / DUAL SUPPLY OPERATION (V_{DD} AND V_{CORE})							
V_{CORE} Dynamic Current, Active Mode	I_{CORE_DACT}	Total current into V_{CORE} pin, HFIO enabled, $f_{SYS_CLK(MAX)}$ = 96MHz, OVR = [10], executing code from cache memory, CPU in Active mode, inputs tied to V_{SS} or V_{DD},outputs source/sink 0mA			85		µA/MHz
V_{CORE} Fixed Current, Active Mode	I_{CORE_FACT}	HFIO enabled, OVR = [10], total current into V_{CORE} pin, CPU in Active mode 0MHz execution, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA			403		µA

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
V_{DD} Dynamic Current, Active Mode	I_{DD_DACT}	HFIO enabled, OVR = [10], $f_{SYS_CLK(MAX)}$ = 96MHz, total current into V_{DD} pin, executing code from cache memory, CPU in Active mode, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA		0.40		µA/MHz
V_{DD} Fixed Current, Active Mode	I_{DD_FACT}	HFIO enabled, OVR = [10], total current into V_{DD} pin, CPU in Active mode 0MHz execution, inputs tied to V_{SS} or V_{DD}, outputs source/sink 0mA		84.8		µA
V_{CORE} Dynamic Current, Sleep Mode	I_{CORE_DSLP}	HFIO enabled, OVR = [10], total current into V_{CORE} pin, CPU in Sleep mode, standard DMA with two channels active		27.7		µA/MHz
V_{CORE} Fixed Current, Sleep Mode	I_{CORE_FSLP}	HFIO enabled, OVR [10], total current into V_{CORE} pin, CPU in Sleep mode, standard DMA with two channels active		270.3		µA
V_{DD} Dynamic Current, Sleep Mode	I_{DD_DSLP}	HFIO enabled, OVR = [10], total current into V_{DD} pin, CPU in Sleep mode, standard DMA with two channels active		0.20		µA/MHz
V_{DD} Fixed Current, Sleep Mode	I_{DD_FSLP}	HFIO enabled, OVR = [10], total current into V_{DD} pin, CPU in Sleep mode, standard DMA with two channels active		65		µA
V_{CORE} Fixed Current, Deep-Sleep Mode	I_{CORE_FDSL}	V_{DD} = 1.8V; V_{CORE}=1.1V		5.7		µA
V_{DD} Fixed Current, Deep Sleep Mode	I_{DD_FDSL}	V_{DD} = 1.8V, V_{CORE}=1.1V		4.2		µA
V_{CORE} Fixed Current, Backup Mode	I_{CORE_FBKU}	V_{DD} = 1.8V; V_{CORE} = 1.1V, 96KB SRAM retained		5		µA
V_{DD} Fixed Current, Backup Mode	I_{DD_FBKU}	0KB SRAM retained with RTC enabled; V_{DD} = 1.8V; V_{CORE} = 0V or unbiased		0.53		µA
		16KB SRAM retained with RTC enabled; V_{DD} = 1.8V; V_{CORE} = 0V or unbiased		0.99		
		32KB SRAM retained with RTC enabled; V_{DD} = 1.8V; V_{CORE} = 0V or unbiased		1.20		
		64KB SRAM retained with RTC enabled; V_{DD} = 1.8V; V_{CORE} = 0V or unbiased		1.64		
		96KB SRAM retained with RTC enabled; V_{DD} = 1.8V; V_{CORE} = 0V or unbiased		1.94		

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GENERAL-PURPOSE I/O						
Input Low Voltage for All GPIO, RSTN	V_{IL_GPIO}	Pin configured as GPIO			0.3 × VDD	V
Input High Voltage for All GPIO, RSTN	V_{IH_GPIO}	Pin configured as GPIO	0.7 × V_{DD}			V
Output Low Voltage for All GPIO Except P0.2, P0.3, P0.8, and P0.9	V_{OL_GPIO}	V_{DD} = 1.71V, I_{OL} = 1mA, DS[1:0] = 00 (Note 1)		0.2	0.4	V
		V_{DD} = 1.71V, I_{OL} = 2mA, DS[1:0] = 10 (Note 1)		0.2	0.4	
		V_{DD} = 1.71V, I_{OL} = 4mA, DS[1:0] = 01 (Note 1)		0.2	0.4	
		V_{DD} = 1.71V, I_{OL} = 6mA, DS[1:0] = 11 (Note 1)		0.2	0.4	
Output Low Voltage for GPIO P0.2, P0.3, P0.8, P0.9	V_{OL_I2C}	V_{DD} = 1.71V, I_{OL} = 2mA, DS = 0 (Note 1)		0.2	0.4	V
		V_{DD} = 1.71V, I_{OL} = 10mA, DS = 1 (Note 1)		0.2	0.4	
Output High Voltage for All GPIO Except P0.2, P0.3, P0.8, and P0.9	V_{OH_GPIO}	V_{DD} = 1.71V, I_{OH} = 1mA, DS[1:0] = 00 (Note 1)	V_{DD} - 0.4			V
		V_{DD} = 1.71V, I_{OH} = 2mA, DS[1:0] = 10 (Note 1)	V_{DD} - 0.4			
		V_{DD} = 1.71V, I_{OH} = 4mA, DS[1:0] = 01 (Note 1)	V_{DD} - 0.4			
		V_{DD} = 1.71V, I_{OH} = 6mA, DS[1:0] = 11 (Note 1)	V_{DD} - 0.4			
Output High Voltage for GPIO P0.2, P0.3, P0.8, P0.9	V_{OH_I2C}	V_{DD} = 1.71V, I_{OH} = 2mA, DS = 0 (Note 1)	V_{DD} - 0.4			V
		V_{DD} = 1.71V, I_{OH} = 10mA, DS = 1 (Note 1)	V_{DD} - 0.4			
Combined I_{OL}, All GPIO	I_{OL_TOTAL}				32	mA
Combined I_{OH}, All GPIO	I_{OH_TOTAL}		-32			mA
Input Hysteresis (Schmitt)	V_{IHYS}			300		mV
Input/Output Pin Capacitance for All Pins	C_{IO}			4		pF
Input Leakage Current Low	I_{IL}	V_{IN} = 0V, internal pullup disabled	-500		+500	nA
Input Leakage Current High	I_{IH}	V_{IN} = 3.6V, internal pulldown disabled	-500		+500	nA
Input Pullup Resistor to RSTN	R_{PU_VDD}	Pullup to V_{DD} = 1.62V		22		kΩ
		Pullup to V_{DD} = 3.63V		10.5		

Electrical Characteristics (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Pullup Resistor for All GPIO	R_{PU}	Pin configured as GPIO, pullup to V_{DD} = 1.62V		22		kΩ
		Pin configured as GPIO, pullup to V_{DD} = 3.63V		10.5		
Input Pulldown Resistor for All GPIO	R_{PD}	Pin configured as GPIO, pulldown to V_{SS}, V_{DD} = 1.62V		20		kΩ
		Pin configured as GPIO, pulldown to V_{SS}, V_{DD} = 3.63V		8.8		
CLOCKS						
System Clock Frequency	f_{SYS_CLK}		24		96	MHz
System Clock Period	t_{SYS_CLK}			$1/f_{SYS_CLK}$		µs
High-Frequency Internal Oscillator (HFIO)	f_{HFIO}	Default OVR = [10]	93.5	96	98.5	MHz
Nanoring Oscillator Frequency	f_{NANO}			80		kHz
RTC Input Frequency	f_{32KIN}	32.768kHz watch crystal, C_L = 6pF, ESR < 90kΩ, C_0 < 2pF		32.768		kHz
RTC Operating Current	I_{RTC}	All power modes, RTC enabled		0.45		µA
RTC Power-Up Time	t_{RTC_ON}			250		ms
FLASH MEMORY						
Flash Erase Time	t_{M_ERASE}	Mass erase		30		ms
	t_{P_ERASE}	Page erase		30		
Flash Programming Time Per Word	t_{PROG}	32-bit programming mode, f_{FLC_CLK} = 1MHz		60		µs
Flash Endurance			10			kcycles
Data Retention	t_{RET}	T_A = +85°C	10			years

Note 1: When using a GPIO bias voltage of 2.97V, the drive current capability of the GPIO is 2x that of its drive strength when using a GPIO bias voltage of 1.62V.

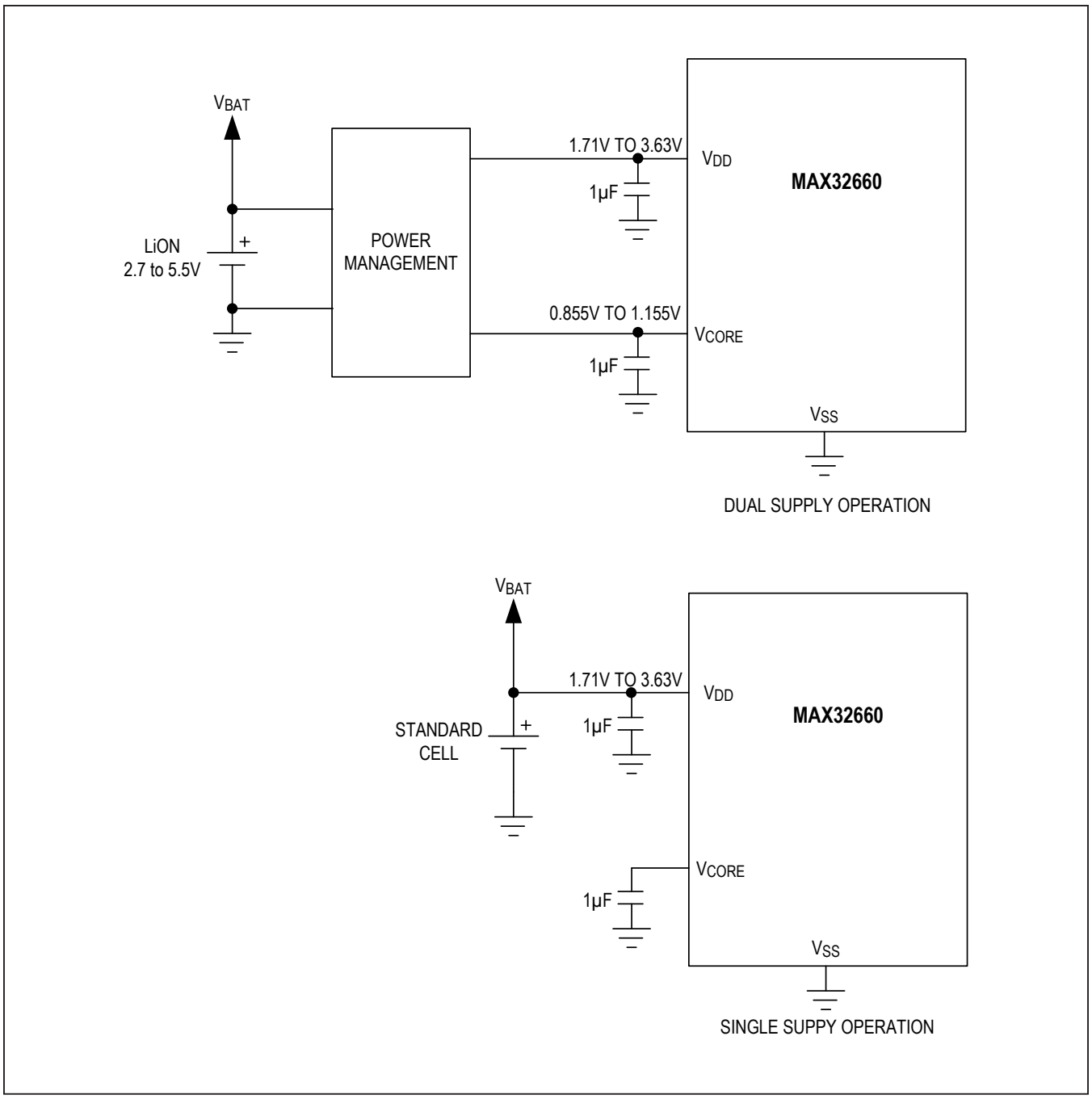


Figure 1. Power Supply Operational Modes

Electrical Characteristics—SPI

(TIming specifications are guaranteed by design and not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MASTER MODE						
SPI Master Operating Frequency	f_{MCK}	f_{SYS_CLK} = 96MHz, $f_{MCK(MAX)} = f_{SYS_CLK}/2$			48	MHz
SPI Master SCK Period	t_{MCK}			$1/f_{MCK}$		ns
SCK Output Pulse-Width High/Low	t_{MCH}, t_{MCL}		$t_{MCK}/2$			ns
MOSI Output Hold Time After SCK Sample Edge	t_{MOH}		$t_{MCK}/2$			ns
MOSI Output Valid to Sample Edge	t_{MOV}		$t_{MCK}/2$			ns
MISO Input Valid to SCK Sample Edge Setup	t_{MIS}			5		ns
MISO Input to SCK Sample Edge Hold	t_{MIH}			$t_{MCK}/2$		ns
SLAVE MODE						
SPI Slave Operating Frequency	f_{SCK}				48	MHz
SPI Slave SCK Period	t_{SCK}			$1/f_{SCK}$		ns
SCK Input Pulse-Width High/Low	t_{SCH}, t_{SCL}			$t_{SCK}/2$		
SSx Active to First Shift Edge	t_{SSE}			10		ns
MOSI Input to SCK Sample Edge Rise/Fall Setup	t_{SIS}			5		ns
MOSI Input from SCK Sample Edge Transition Hold	t_{SIH}			1		ns
MISO Output Valid After SCLK Shift Edge Transition	t_{SOV}			5		ns
SCK Inactive to SSx Inactive	t_{SSD}			10		ns
SSx Inactive Time	t_{SSH}			$1/f_{SCK}$		µs
MISO Hold Time After SSx Deassertion	t_{SLH}			10		ns

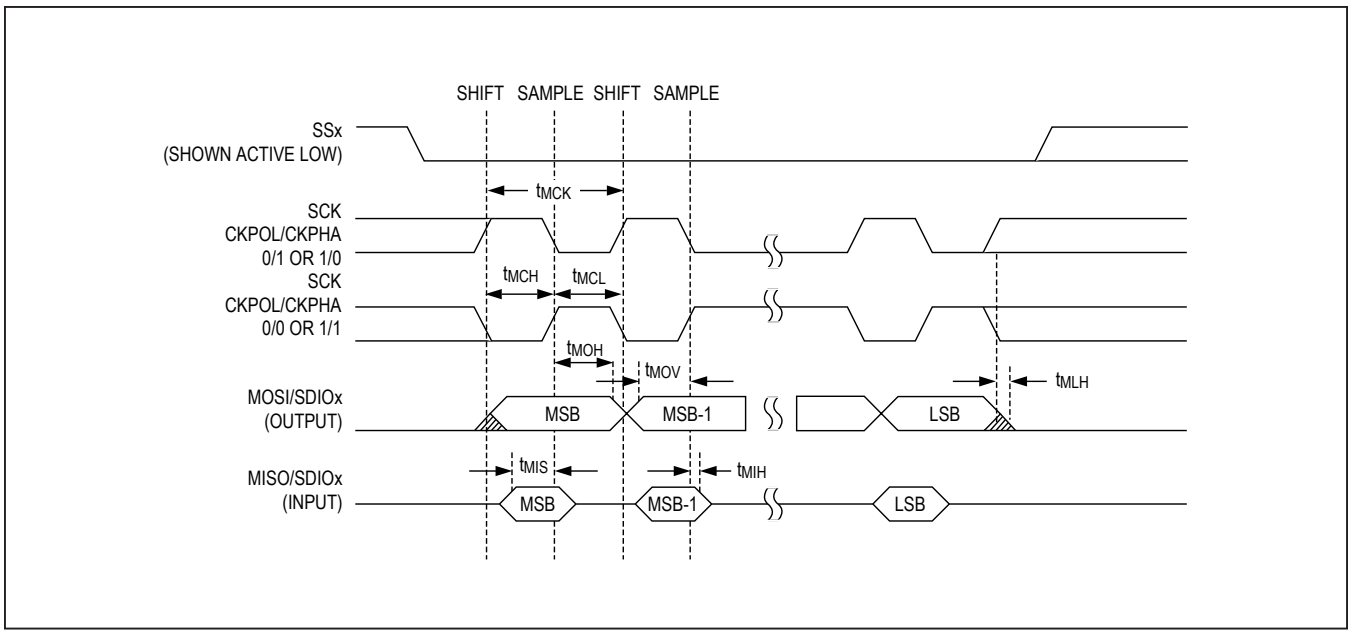


Figure 2. SPI Master Mode Timing Diagram

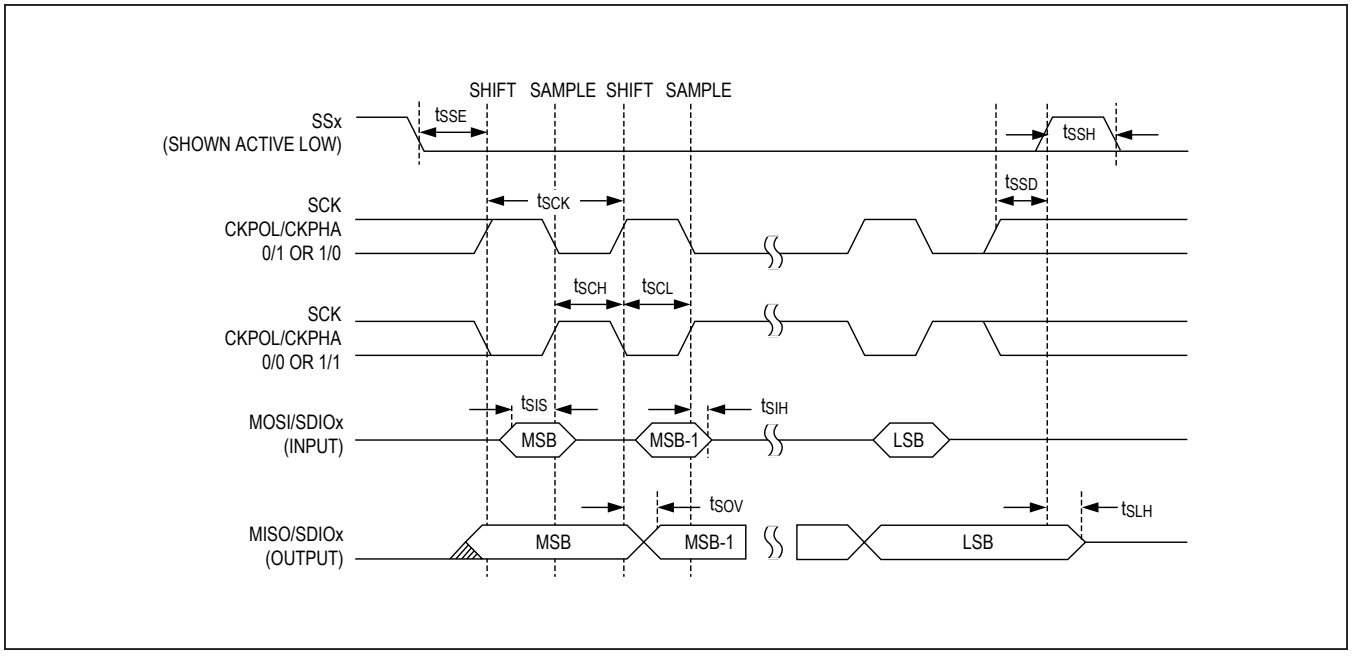


Figure 3. SPI Slave Mode Timing Diagram

Electrical Characteristics—I²C

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
STANDARD MODE						
Output Fall Time	t_{OF}	Standard mode, from $V_{OL_I2C(MIN)}$ to $V_{OL_I2C(MAX)}$		150		ns
SCL Clock Frequency	f_{SCL}		0		100	kHz
Low Period SCL Clock	t_{LOW}		4.7			µs
High Time SCL Clock	t_{HIGH}		4.0			µs
Setup Time for Repeated Start Condition	$t_{SU;STA}$		4.7			µs
Hold Time for Repeated Start Condition	$t_{HD;STA}$		4.0			µs
Data Setup Time	$t_{SU;DAT}$			300		ns
Data Hold Time	$t_{HD;DAT}$			10		ns
Rise Time for SDA and SCL	t_R			800		ns
Fall Time for SDA and SCL	t_F			200		ns
Setup Time for a Stop Condition	$t_{SU;STO}$		4.0			µs
Bus Free Time Between a Stop and Start Condition	t_{BUS}		4.7			µs
Data Valid Time	$t_{VD;DAT}$		3.45			µs
Data Valid Acknowledge Time	$t_{VD;ACK}$		3.45			µs
FAST MODE						
Output Fall Time	t_{OF}	From $V_{OL_I2C(MIN)}$ to $V_{OL_I2C(MAX)}$		150		ns
Pulse Width Suppressed by Input Filter	t_{SP}			75		ns
SCL Clock Frequency	f_{SCL}		0		400	kHz
Low Period SCL Clock	t_{LOW}		1.3			µs
High Time SCL Clock	t_{HIGH}		0.6			µs
Setup Time for Repeated Start Condition	$t_{SU;STA}$		0.6			µs
Hold Time for Repeated Start Condition	$t_{HD;STA}$		0.6			µs
Data Setup Time	$t_{SU;DAT}$			125		ns
Data Hold Time	$t_{HD;DAT}$			10		ns
Rise Time for SDA and SCL	t_R			30		ns
Fall Time for SDA and SCL	t_F			30		ns
Setup Time for a Stop Condition	$t_{SU;STO}$		0.6			µs

Electrical Characteristics—I²C (continued)

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Bus Free Time Between a Stop and Start Condition	t_{BUS}		1.3			µs
Data Valid Time	$t_{VD;DAT}$		0.9			µs
Data Valid Acknowledge Time	$t_{VD;ACK}$		0.9			µs
FAST MODE PLUS						
Output Fall Time	t_{OF}	From $V_{OL_I2C(MIN)}$ to $V_{OL_I2C(MAX)}$		80		ns
Pulse Width Suppressed by Input Filter	t_{SP}			75		ns
SCL Clock Frequency	f_{SCL}		0		1000	kHz
Low Period SCL Clock	t_{LOW}		0.5			µs
High Time SCL Clock	t_{HIGH}		0.26			µs
Setup Time for Repeated Start Condition	$t_{SU;STA}$		0.26			µs
Hold Time for Repeated Start Condition	$t_{HD;STA}$		0.26			µs
Data Setup Time	$t_{SU;DAT}$			50		ns
Data Hold Time	$t_{HD;DAT}$			10		ns
Rise Time for SDA and SCL	t_R			50		ns
Fall Time for SDA and SCL	t_F			30		ns
Setup Time for a Stop Condition	$t_{SU;STO}$		0.26			µs
Bus Free Time Between a Stop and Start Condition	t_{BUS}		0.5			µs
Data Valid Time	$t_{VD;DAT}$		0.45			µs
Data Valid Acknowledge Time	$t_{VD;ACK}$		0.45			µs

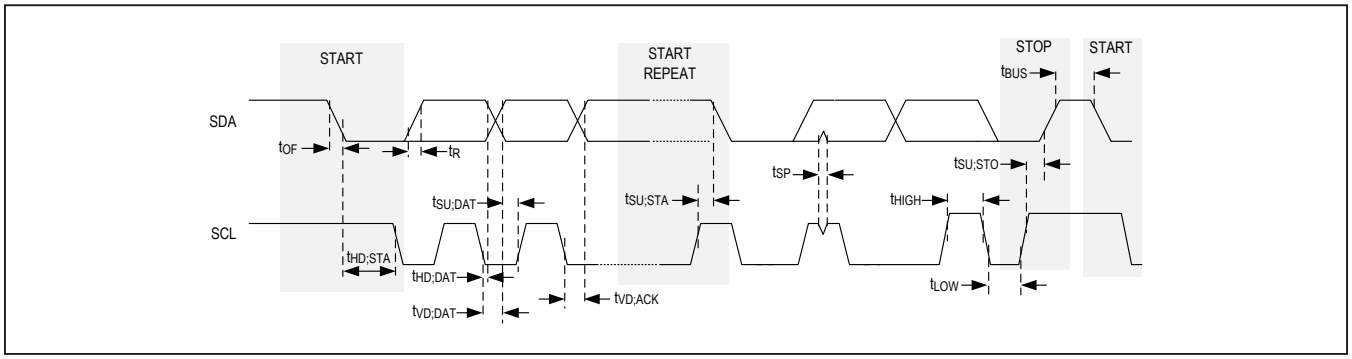


Figure 4. I²C Timing Diagram

Electrical Characteristics—I²S Slave

(Limits are 100% tested at T_A = +25°C and T_A = +105°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Specifications marked GBD are guaranteed by design and not production tested. Specifications to the minimum operating temperature are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Bit Clock Frequency	f_{BCLK}	96kHz LRCLK frequency			3.072	MHz
BCLK High Time	t_{WBCLKH}			0.5		$1/f_{BCLK}$
BCLK Low Time				0.5		$1/f_{BCLK}$
LRCLK Setup Time	t_{LRCLK_BLCK}			25		ns
Delay Time, BCLK to SD (Output) Valid	t_{BCLK_SDO}			12		ns
Setup Time for SD (Input)	t_{SU_SDI}			6		ns
Hold Time SD (Input)	t_{HD_SDI}			3		ns

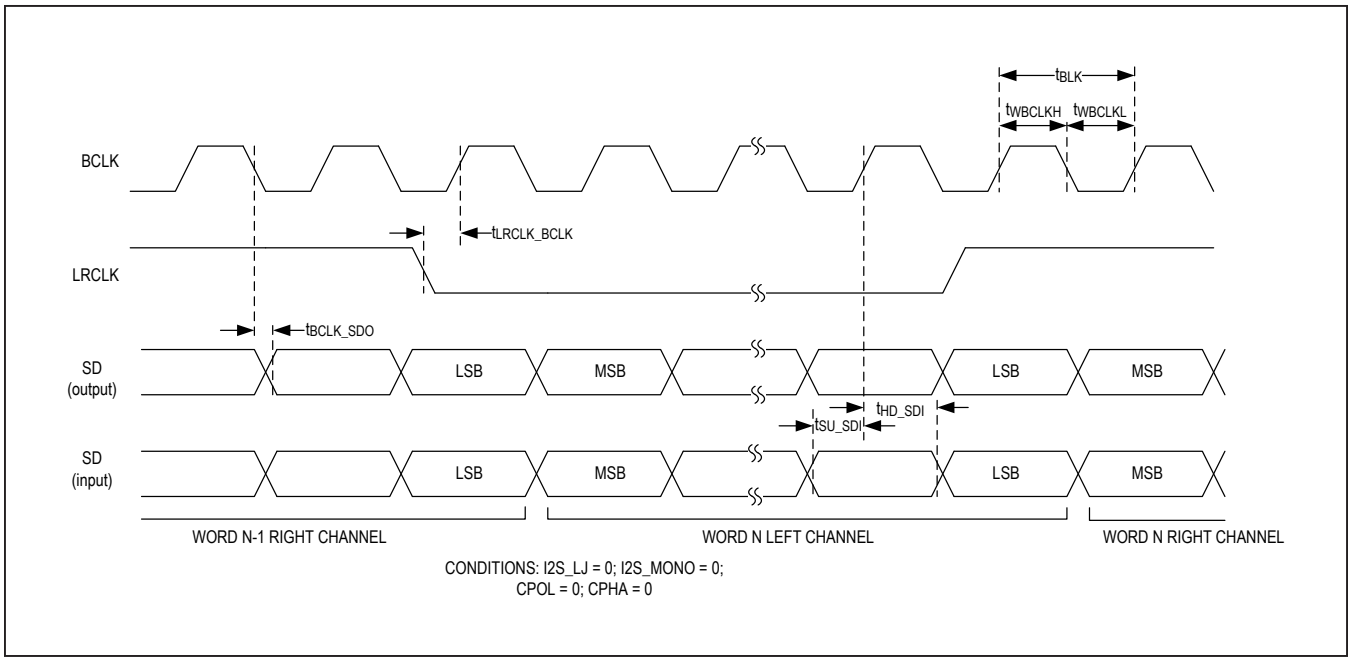
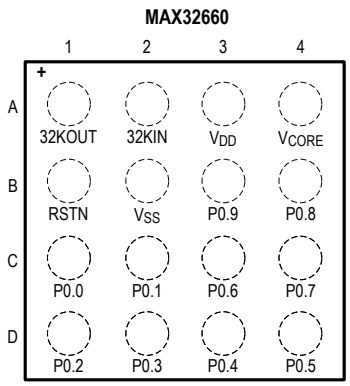


Figure 5. I²S Timing Diagram

Pin Configurations

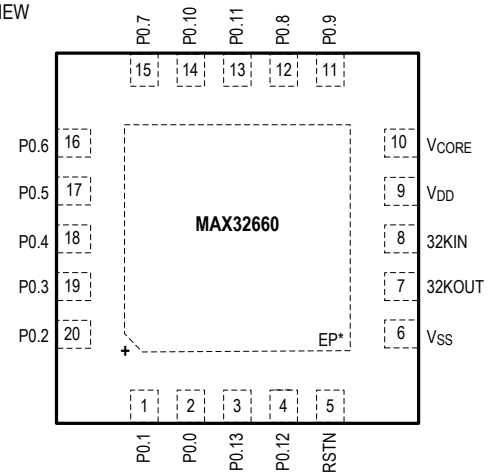
TOP VIEW



16 WLP

1.6mm x 1.6mm

TOP VIEW

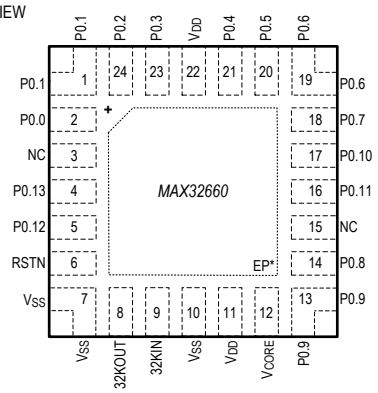


20 TQFN-EP

4mm x 4mm

*EP = EXPOSED PAD.

TOP VIEW



24 TQFN-EP

3mm x 3mm

*EP = EXPOSED PAD

Pin Description

PIN			NAME	FUNCTION
16 WLP	20 TQFN-EP	24 TQFN-EP		
POWER				
A3	9	11, 22	V_{DD}	Digital Supply Voltage. This pin must be bypassed to V_{SS} with a 1.0µF capacitor as close as possible to the package. The device can operate soley from this one power supply pin without the need to connect V_{CORE} by utilizing the internal V_{CORE} regulator. The internal V_{CORE} regulator automatically operates if the presence of a voltage on the V_{CORE} pin is not detected. This provides single supply battery operation capability.

Pin Description (continued)

PIN			NAME	FUNCTION
16 WLP	20 TQFN-EP	24 TQFN-EP		
A4	10	12	V_{CORE}	Core Supply Voltage. This pin provides dual supply operation to support PMIC-based systems and should be left open-circuit for single supply operation. This pin must always be bypassed to V_{SS} with a 1.0µF capacitor as close as possible to the package regardless of the supply mode of operation.
B2	6	7, 10	V_{SS}	Digital Ground
—	—	—	EP	Exposed Pad (TQFN only). This pad must be connected to V_{SS}. Refer to Application Note 3273: *Exposed Pads: A Brief Introduction* for additional information.
CLOCK				
A2	8	9	32KIN	32.768kHz Crystal Oscillator Input. Connect a 6pF 32.768kHz crystal between 32KIN and 32KOUT for RTC operation. Optionally, an external clock source can be driven on 32KIN if the 32KOUT pin is left unconnected.
A1	7	8	32KOUT	32.768kHz Crystal Oscillator Output
RESET				
B1	5	6	RSTN	Hardware Power Reset (Active-Low) Input. The device remains in reset while this pin is in its active state. When the pin transitions to its inactive state, the device performs a POR reset (resetting all logic on all supplies except for real-time clock circuitry) and begins execution. This pin is internally connected with an internal pullup to the V_{DD} supply as indicated in the *Electrical Characteristics* table. This pin should be left unconnected if the system design does not provide a reset signal to the device.
GENERAL-PURPOSE I/O (See Table 3 and Table 4 for pin mapping.)				
C1	2	2	P0.0	General-Purpose I/O. Most port pins have multiple special functions. See Table 3 and Table 4 for details.
C2	1	1	P0.1	
D1	20	24	P0.2	
D2	19	23	P0.3	
D3	18	21	P0.4	
D4	17	20	P0.5	
C3	16	19	P0.6	
C4	15	18	P0.7	
B4	12	14	P0.8	
B3	11	13	P0.9	
—	14	17	P0.10	
—	13	16	P0.11	
—	4	5	P0.12	
—	3	4	P0.13	

Detailed Description

The MAX32660 is an ultra-low power, cost-effective, highly-integrated microcontroller designed for battery-powered devices and wireless sensors. It combines a flexible and versatile power management unit with the powerful Arm Cortex-M4 processor with FPU. The device enables designs with complex sensor processing without compromising battery life. It also offers legacy designs an easy and cost optimal upgrade path from 8- or 16-bit microcontrollers. The device integrates up to 256KB of flash memory and 96KB of RAM to accommodate application and sensor code.

The device features four powerful and flexible power modes. It can operate from a single- or dual-supply battery voltage, typically provided by a PMIC. The I^2C port supports standard, fast, fast-plus, and high-speed modes, operating up to 3400kbps. The SPI ports can run up to 48MHz in both master and slave mode, and the UARTs can run up to 4000kbaud. Three general-purpose 32-bit timers, a watchdog timer, and a real-time clock are also provided. An I^2S interface provides audio streaming to a codec.

Memory

Internal Flash Memory

256KB of internal flash memory provides nonvolatile storage of program and data memory.

Internal SRAM

The internal 96KB SRAM provides low-power retention of application information in all power modes except shutdown. The SRAM can be divided into granular banks that create a flexible SRAM retention architecture. This data retention feature is optional, and is configurable. This granularity allows the application to minimize its power consumption by only retaining the most essential data.

Clocking Scheme

The high-frequency internal oscillator (HFIO) operates at a nominal frequency of 96MHz.

Optionally, two other oscillators can be selected depending upon power needs:

- 80kHz nano-ring oscillator
- 32.768kHz oscillator (external crystal required)

This clock is the primary clock source for the digital logic and peripherals.

An external 32.768kHz timebase is required when using the RTC.

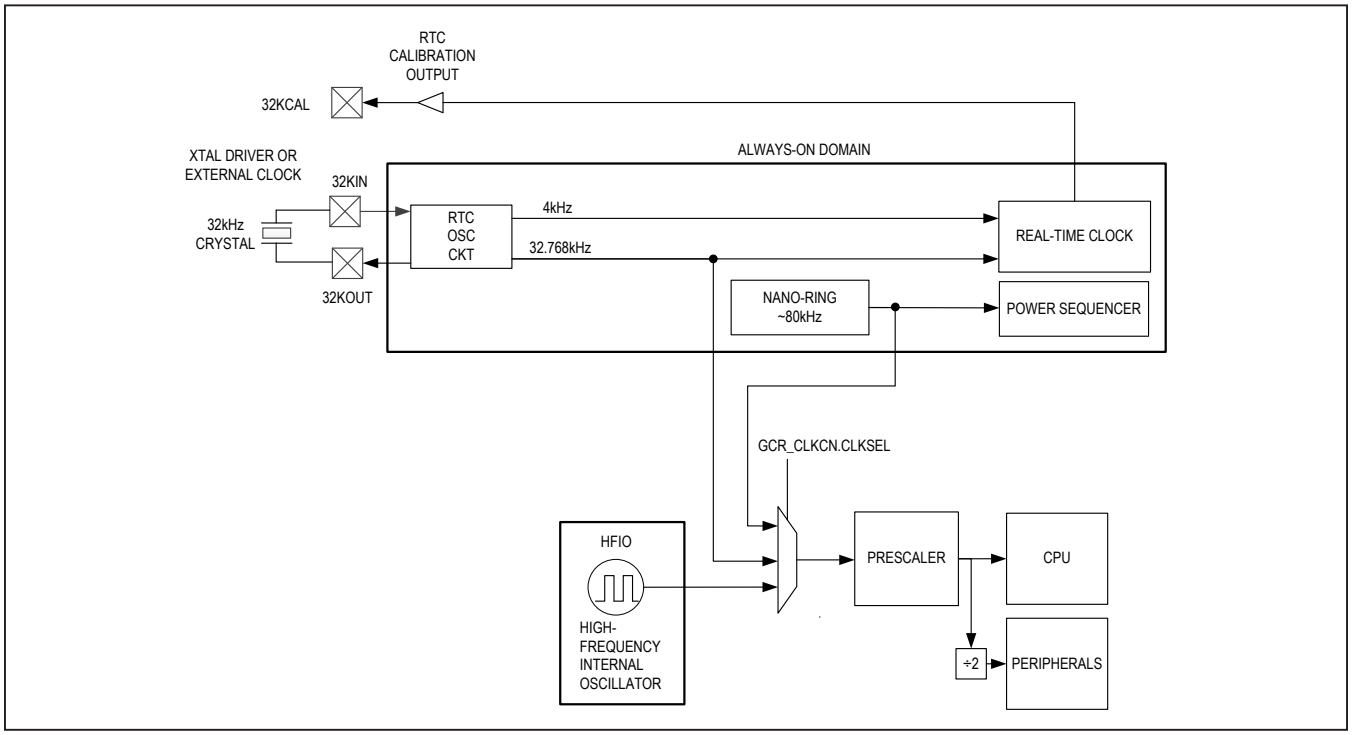


Figure 6. System Clocking Diagram

General-Purpose I/O and Special Function Pins

Most general-purpose I/O (GPIO) pins share both a firmware-controlled I/O function and one or more special function signals associated with peripheral modules. Pins can be individually enabled for GPIO or peripheral special function use. Configuring a pin as a special function usually supersedes its use as a firmware-controlled I/O. Though this multiplexing between peripheral and GPIO functions is usually static, it can also be done dynamically. The electrical characteristics of a GPIO pin are identical whether the pin is configured as an I/O or special function, except where explicitly noted in the *Electrical Characteristics* tables.

In GPIO mode, each pin of a port has an interrupt function that can be independently enabled, and configured as a level- or edge-sensitive interrupt. All GPIOs share the same interrupt vector. Some packages do not have all of the GPIOs available.

When configured as GPIOs, the following features are provided. These features can be independently enabled or disabled on a per-pin basis.

- Configurable as input, output, bidirectional, or high-impedance
- Optional internal pullup resistor or internal pulldown resistor when configured as input
- Exit from low-power modes on rising or falling edge
- Selectable standard- or high-drive modes

The MAX32660 provides up to 14 GPIOs for the 20-pin TQFN and up to 10 GPIOs for the 16-bump WLP.

Standard DMA Controller

The standard DMA (direct memory access) controller provides a means to off-load the CPU for memory/peripheral data transfer leading to a more power-efficient system. It allows automatic one-way data transfer between two entities. These entities can be either memories or peripherals. The transfers are done without using CPU resources. The following transfer modes are supported:

- 4 channel
- Peripheral to data memory
- Data memory to peripheral
- Data memory to data memory
- Event support

All DMA transactions consist of an AHB burst read into the DMA FIFO followed immediately by an AHB burst write from the FIFO.

Power Management

Power Management Unit

The power management unit (PMU) provides high-performance operation while minimizing power consumption. It exercises intelligent, precise control of power distribution to the CPU and peripheral circuitry.

The PMU provides the following features:

- User-configurable system clock
- Automatic enabling and disabling of crystal oscillators based on power mode
- Multiple clock domains
- Fast wake-up of powered-down peripherals when activity detected

Active Mode

In this mode, the CPU is executing application code and all digital and analog peripherals are available on demand. Dynamic clocking disables peripherals not in use, providing the optimal mix of high-performance and low-power consumption.

Sleep Mode

This mode allows for low-power consumption operation. The CPU is asleep, peripherals are on and the standard DMA block is available. The GPIO or any active peripheral can be configured to interrupt and cause transition to the Active mode.

Deep-Sleep Mode

This mode corresponds to the Arm Cortex-M4 processor with FPU Deep-sleep mode. In this mode, the register settings and all volatile memory is preserved. The GPIO pins retain their state in this mode. The high-speed oscillator that generates the 96MHz system clock can be shut down to provide additional power savings over Sleep mode.

Multiple system events can cause the device to wake from Deep-sleep mode and return to the Active mode, including:

- RTC alarm
- Enabled GPIO interrupt

Backup Mode

This mode places the CPU in a static, low-power state. In Backup mode, all of the SRAM can be retained. Data retention in this mode is maintained by the V_{DD} supply only. SRAM retention can be 0KB, 16KB, 32KB, 64KB, or full 96KB. Backup mode supports the same wake-up sources as Deep-sleep mode.

Real-Time Clock

A real-time clock (RTC) keeps the time of day in absolute seconds. The 32-bit seconds register can count up to approximately 136 years and be translated to calendar format by application software.

The RTC provides a time-of-day alarm that can be programmed to any future value between 1 second and 12 days. When configured for long intervals, the time-of-day alarm can be used as a power-saving timer, allowing the device to remain in an extremely low-power mode, but still awaken periodically to perform assigned tasks. A second independent 32-bit 1/4096 subsecond alarm can be programmed between 244µs and 12 days. Both can be configured as recurring alarms. When enabled, either alarm can cause an interrupt or wake the device from most low power modes.

The time base is generated by a 32.768kHz crystal or an external clock source that must meet the electrical/timing requirements in the *Electrical Characteristics* table.

An RTC calibration feature provides the ability for user-software to compensate for minor variations in the RTC oscillator, crystal, temperature, and board layout. Enabling the 32KCAL alternate function outputs a timing signal derived from the RTC. External hardware can measure the frequency and adjust the RTC frequency in increments of ±127ppm with 1ppm resolution. Under most circumstances, the oscillator does not require any calibration.

Watchdog Timer

Microcontrollers are often used in harsh environments where electrical noise and electromagnetic interference (EMI) are abundant. Without proper safeguards, these hazards can disturb device operation and corrupt program execution. One of the most effective countermeasures is the watchdog timer (WDT), which detects runaway code or system unresponsiveness.

The WDT is a 32-bit, free-running counter with a configurable prescaler. When enabled, the WDT must be periodically reset by the application software. Failure to reset the WDT within the user-configurable timeout period indicates that the application software is not operating correctly and results in a WDT timeout. A WDT timeout can trigger an interrupt, system reset, or both. Either response forces the instruction pointer to a known good location before resuming instruction execution.

The MAX32660 provides one instance of the watchdog timer (WDT0).

Programmable Timers

General-purpose, 32-bit timers provide timing, capture/compare, or generation of pulse-width modulated (PWM) signals with minimal software interaction. Each of the 32-bit timers can also be split into two 16-bit timers.

The timer provides the following features:

- 32-bit up/down autoreload
- Programmable prescaler
- PWM output generation
- Capture, compare, and capture/compare capability
- External pin multiplexed with GPIO for timer input, clock gating, or capture
- Timer output pin
- Configurable as 2 × 16-bit general-purpose timers
- Timer interrupt

The MAX32660 provides three 32-bit timers: TIMER0, TIMER1, and TIMER2.

I/O functionality is supported for TIMER0 only (TIMER_TMR0 pin). Note that the function of a port can be multiplexed with other functions on the GPIO pins, so it might not be possible to use all the ports depending on the device configuration.

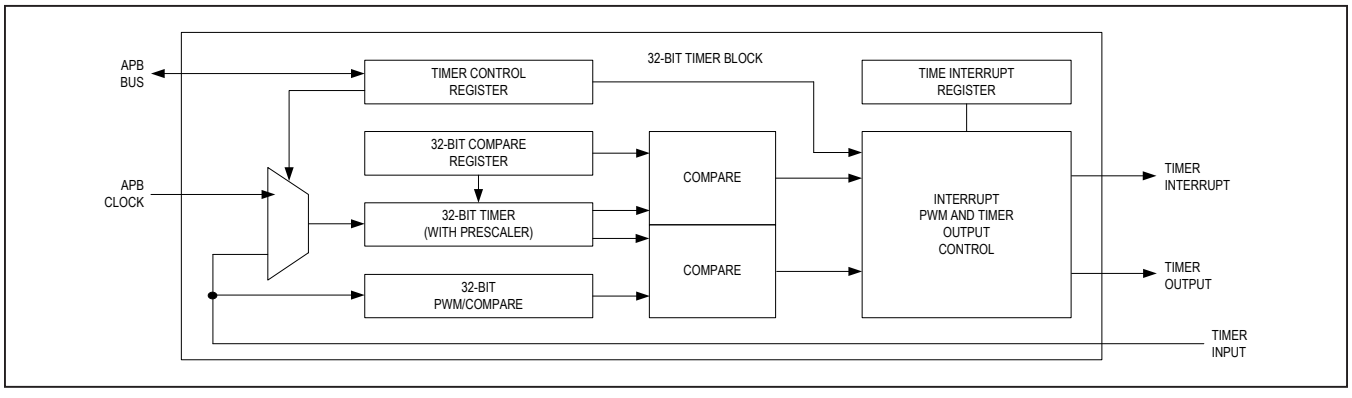


Figure 7. 32-Bit Timer

Serial Peripherals

I2C Interface

The I2C interface is a bidirectional, two-wire serial bus that provides a medium-speed communications network. It can operate as a one-to-one, one-to-many or many-to-many communications medium. These engines support standard-mode, fast-mode, fast-mode plus and high-speed mode I2C speeds. It provides the following features:

- Master or slave mode operation
  - Supports up to 4 different slave addresses in slave mode
- Supports standard 7-bit addressing or 10-bit addressing
- RESTART condition
- Interactive receive mode
- Tx FIFO preloading
- Support for clock stretching to allow slower slave devices to operate on higher speed busses
- Multiple transfer rates
  - Standard mode: 100kbps
  - Fast mode: 400kbps
  - Fast mode plus: 1000kbps
  - High-speed mode: 3400kbps
- Internal filter to reject noise spikes
- Receiver FIFO depth of 8 bytes
- Transmitter FIFO depth of 8 bytes

The MAX32660 provides two instances of the I2C peripheral (I2C0 and I2C1).

Serial Peripheral Interface

The serial peripheral interface (SPI) is a highly configurable, flexible, and efficient synchronous interface between multiple SPI devices on a single bus. The bus uses a single clock signal and multiple data signals, and one or more slave select lines to address only the intended target device. The SPI operates independently and requires minimal processor overhead.

The provided SPI peripherals can operate in either slave or master mode and provide the following features:

- SPI modes 0, 1, 2, 3 for single-bit communication
- 3- or 4-wire mode for single-bit slave device communication
- Full-duplex operation in single-bit, 4-wire mode
- Multimaster mode fault detection
- Programmable interface timing
- Programmable SCK frequency and duty cycle
- 32-byte transmit and receive FIFOs
- Slave select assertion and deassertion timing with respect to leading/trailing SCK edge

The MAX32660 provides two instances of this SPI peripheral (SPI0, SPI1) with the following specifications (Table 1):

Table 1. SPI Configuration Options

INSTANCE	DATA	SLAVE SELECT LINES		MAXIMUM FREQUENCY (MASTER MODE) (MHz)	MAXIMUM FREQUENCY (SLAVE MODE) (MHz)
		20 TQFN	16 WLP		
SPI0	3 wire, 4 wire	1	1	48	48
SPI1	3 wire, 4 wire	1	1	48	48

I2S Interface

The I2S interface is a bidirectional, four-wire serial bus that provides serial communications for codecs and audio amplifiers compliant with the I2S Bus Specification, June 5, 1996. It provides the following features:

- Slave mode operation
- Normal and left-justified data alignment
- 16-bit audio transfer
- Wake-up on FIFO status (full/empty/threshold)
- Interrupts generated for FIFO status
- Receiver FIFO depth of 32 bytes
- Transmitter FIFO depth of 32 bytes

The MAX32660 provides one instance of the I2S peripheral that is multiplexed with the SPI1 peripheral.

UART

The universal asynchronous receiver-transmitter (UART) interface supports full-duplex asynchronous communication with optional hardware flow control (HFC) modes to prevent data overruns. If HFC mode is enabled on a given port, the system uses two extra pins to implement the industry standard request to send (RTS) and clear to send (CTS) flow control signaling. Each UART is individually programmable.

- 2-wire interface or 4-wire interface with flow control
- 8-byte send/receive FIFO
- Full-duplex operation for asynchronous data transfers
- Interrupts available for frame error, parity error, CTS, Rx FIFO overrun and FIFO full/partially full conditions
- Automatic parity and frame error detection
- Independent baud-rate generator
- Programmable 9th bit parity support
- Multidrop support
- Start/stop bit support
- Hardware flow control using RTS/CTS
- 4000kb maximum baud rate
- Two DMA channels can be connected (read and write FIFOs)
- Programmable word size (5 bits to 8 bits)

The MAX32660 provides two instances of the UART peripheral (UART0 and UART1) with the specifications shown in Table 2.

Table 2. UART Configuration Options

INSTANCE	FLOW CONTROL		MAXIMUM BAUD RATE (KB)
	20 TQFP	16 WLP	
UART0	Yes	Yes	4000
UART1	Yes	No	4000

Bootloader

The MAX32660 bootloader is a small embedded firmware that provides the MAX32660 with the ability to update application code by a host microcontroller. The bootloader can be accessed through the I2C, SPI, or UART interface. These interfaces provide the data channel and the control channel for communicating between the host microcontroller and the MAX32660. The bootloader application load mode is enabled and disabled by either a serial command or hardware connectivity. The serial command is interpreted by the application, which configures the device to enter the bootloader mode. When using the hardware connectivity option, a single GPIO pin and the RSTN pin on the MAX32660 can be configured to allow the MAX32660 to enter the bootloader mode. For detailed information, refer to the MAX32660 Bootloader User Guide (UG6471).

Debug and Development Interface (SWD)

The serial wire debug interface is used for code loading and ICE debug activities. All devices in mass production have the debugging/development interface enabled.

Additional Documentation and Technical Support

Designers must have the following documents to use all the features of this device:

- This data sheet, which contains electrical/timing specifications, package information, and pin descriptions
- The corresponding revision-specific errata sheet
- The corresponding user guide, which contains detailed information and programming guidelines for core features and peripherals

Applications Information

Table 3. GPIO and Alternate Function Matrix, 16 WLP

GPIO	ALTERNATE FUNCTION 1	ALTERNATE FUNCTION 2	ALTERNATE FUNCTION 3
P0.0	SWDIO**	SPI1_MISO (I2S_SDI)†	UART1_TX**
P0.1	SWDCLK**	SPI1_MOSI (I2S_SDO)†	UART1_RX**
P0.2	I2C1_SCL	SPI1_SCK (I2S_BCLK)†	32KCAL
P0.3	I2C1_SDA	SPI1_SS0 (I2S_LRCLK)†	TMR0
P0.4	SPI0_MISO	UART0_TX	—
P0.5	SPI0_MOSI	UART0_RX	—
P0.6	SPI0_SCK	UART0_CTS	UART1_TX**
P0.7	SPI0_SS0	UART0_RTS	UART1_RX**
P0.8	I2C0_SCL	SWDIO**	—
P0.9	I2C0_SDA	SWDCLK**	—
P0.10*	—	—	—
P0.11*	—	—	—
P0.12*	—	—	—
P0.13*	—	—	—

**GPIO not pinned out.*

***This signal can be mapped to more than one GPIO, but there is only one instance of this peripheral.*

†These pins support I^2S functionality. Refer to the User Guide for details.

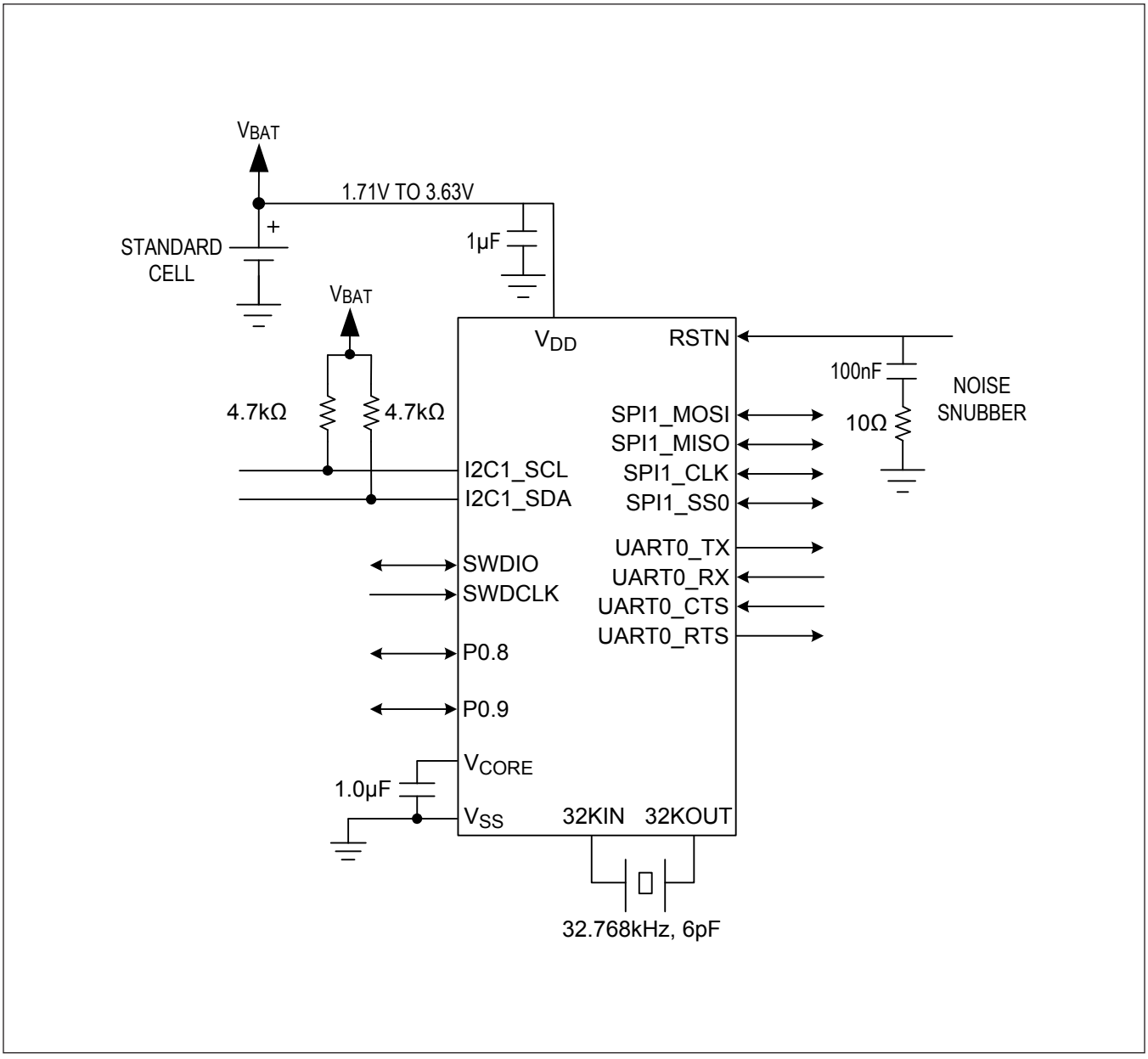
Table 4. GPIO and Alternate Function Matrix, 20 TQFN and 24 TQFN

GPIO	ALTERNATE FUNCTION 1	ALTERNATE FUNCTION 2	ALTERNATE FUNCTION 3
P0.0	SWDIO**	SPI1_MISO (I2S_SDI)†**	UART1_TX**
P0.1	SWDCLK**	SPI1_MOSI (I2S_SDO)†**	UART1_RX**
P0.2	I2C1_SCL	SPI1_SCK (I2S_BCLK)†**	32KCAL
P0.3	I2C1_SDA	SPI1_SS0 (I2S_LRCLK)†**	TMR0
P0.4	SPI0_MISO	UART0_TX	—
P0.5	SPI0_MOSI	UART0_RX	—
P0.6	SPI0A_SCK	UART0_CTS	UART1_TX**
P0.7	SPI0A_SS0	UART0_RTS	UART1_RX**
P0.8	I2C0_SCL	SWDIO**	—
P0.9	I2C0_SDA	SWDCLK**	—
P0.10	SPI1_MISO (I2S_SDI)†**	UART1_TX	—
P0.11	SPI1_MOSI (I2S_SDO)†**	UART1_RX	—
P0.12	SPI1_SCK (I2S_BCLK)†**	UART1_CTS	—
P0.13	SPI1_SS0 (I2S_LRCLK)†**	UART1_RTS	—

***This signal can be mapped to more than one GPIO, but there is only one instance of this peripheral.*

†I2S_BCLK, I2S_LRCLK, I2S_SDI, I2S_SDO when enabled.

Typical Application Circuit



Ordering Information

PART	FLASH (KB)	SRAM (KB)	BOOT LOADER	PIN-PACKAGE
MAX32660GWE+	256	96	No	16 WLP (1.6mm x 1.6mm x 0.65mm, 0.35mm pitch)
MAX32660GWE+T	256	96	No	16 WLP (1.6mm x 1.6mm x 0.65mm, 0.35mm pitch)
MAX32660GTP+	256	96	No	20 TQFN-EP (4mm x 4mm x 0.75mm, 0.5mm pitch)
MAX32660GTP+T	256	96	No	20 TQFN-EP (4mm x 4mm x 0.75mm, 0.5mm pitch)
MAX32660GTG+	256	96	No	24 TQFN-EP (3mm x 3mm x 0.75mm, 0.4mm pitch)
MAX32660GTG+T	256	96	No	24 TQFN-EP (3mm x 3mm x 0.75mm, 0.4mm pitch)
MAX32660GWEBL+	256	96	Yes	16 WLP (1.6mm x 1.6mm x 0.65mm, 0.35mm pitch)
MAX32660GWEBL+T	256	96	Yes	16 WLP (1.6mm x 1.6mm x 0.65mm, 0.35mm pitch)
MAX32660GTGBL+	256	96	Yes	24 TQFN-EP (3mm x 3mm x 0.75mm, 0.4mm pitch)
MAX32660GTGBL+T	256	96	Yes	24 TQFN-EP (3mm x 3mm x 0.75mm, 0.5mm pitch)
MAX32660GWELA+*	128	64	No	16 WLP (1.6mm x 1.6mm x 0.65mm, 0.35mm pitch)
MAX32660GWELA+T*	128	64	No	16 WLP (1.6mm x 1.6mm x 0.65mm, 0.35mm pitch)
MAX32660GTGLA+*	128	64	No	24 TQFN-EP (3mm x 3mm x 0.75mm, 0.4mm pitch)
MAX32660GTGLA+T*	128	64	No	24 TQFN-EP (3mm x 3mm x 0.75mm, 0.4mm pitch)
MAX32660GWELB+*	64	32	No	16 WLP (1.6mm x 1.6mm x 0.65mm, 0.35mm pitch)
MAX32660GWELB+T*	64	32	No	16 WLP (1.6mm x 1.6mm x 0.65mm, 0.35mm pitch)
MAX32660GTGLB+*	64	32	No	24 TQFN-EP (3mm x 3mm x 0.75mm, 0.4mm pitch)
MAX32660GTGLB+T*	64	32	No	24 TQFN-EP (3mm x 3mm x 0.75mm, 0.4mm pitch)

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel. Full reel.
**Future product—contact factory for availability.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/18	Initial release	—
1	4/18	Updated *General Description*, *Applications*, *Benefits and Features*, *Absolute Maximum Ratings*, *Package Information*, *Electrical Characteristics* table, *Pin Configurations*, *Pin Descriptions*, Table 4 title, *Ordering Information*, and added *Typical Application Circuit*	1, 3, 8, 15, 16, 22–24
2	6/18	Updated *Simplified Block Diagram*, *Electrical Characteristics* table, Figure 1, Figure 2, Figure 3, *Clocking Scheme* section, Figure 6, and *Ordering Information* table	2, 4–6, 8–10, 11, 17, 24
3	8/18	Updated *Ordering Information*	24
4	8/18	Updated *Ordering Information*	24
5	10/18	Updated title and *General Description*	1–25
6	12/18	Updated *Ordering Information*	24
7	2/19	Updated title, *General Description*, *Pin Configuration*, *Ordering Information*, *Additional Documentation and Technical Support*, and added *Bootloader* section	1–25
8	9/19	Updated *Benefits and Features*, *Simplified Block Diagram*, *Electrical Characteristics* table, *Clocking Scheme*, Figure 6, *Real-Time Clock*, UART, Table 4	1, 2, 4–6, 8, 17, 19, 21, 22

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