

FEATURES

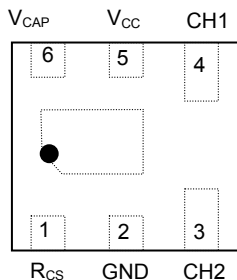
- Extremely Low supply current ($<1\mu\text{A}$).
- Shunt operation hence distortion free.
- Instantaneous. Power-up and Power-down muting.
- No external microcontroller signal needed.
- ESD protected outputs.
- 1.5V to 5V supply operation.
- Handle up to 3.5V RMS signal.
- Compact 2 x 2 x 0.8mm 6L DFN.
- Standard 8L SO-8 package.

APPLICATIONS

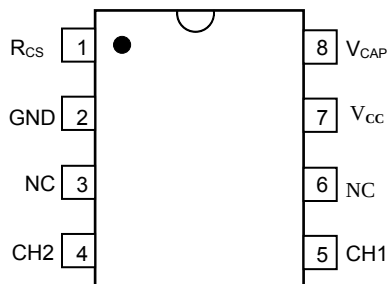
- Cell phones
- PDA's
- Portable DVD players
- Portable MP3 players
- Notebook Audio
- Set-top boxes
- Digital Video Recorders
- LCD TVs
- Home Theater systems

Pin Layout and Description

Pin# DFN-6	Pin # SOIC-8	Description	Notes
1	1	RCS	Power ON delay capacitor
2	2	GND	Ground
	3	NC	No Connect
3	4	Ch2	Channel 2 control signal
4	5	Ch1	Channel 1 control signal
	6	NC	No Connect
5	7	Vcc	Vcc
6	8	Cap	Holding capacitor



DFN-6
Top View



SOIC-8
Top View

GENERAL DESCRIPTION

PA4220 is a low power ($I_{CC} < 1\mu\text{A}$) monolithic mixed signal device. PA4220's function is to control the power supply transition noise in audio systems. PA4220 boasts several features that make it a "one of a kind" product on the market. Most prominent is the feature is that it does not require any external signal to suppress POPUP and SHUTDOWN Noise.

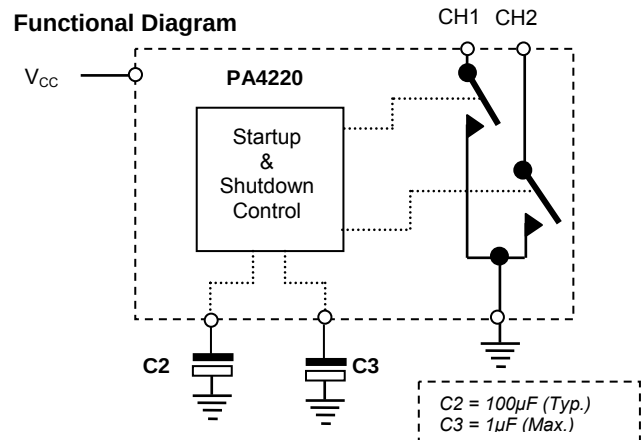
PA4220 requires few external components for its operation, working from low to medium supply voltages of up to 5V. The ramp time of the supply should be greater than 50ms.

On power-up and power-down the output of the amplifier stage is switched to a convenient low impedance voltage rail hence muting the amplifiers, preventing the audible pop, which is normally heard in the headset or speakers.

PA4220 operates as a passive shunt device hence the designer does not have to worry about the device introducing any kind of noise or distortion into the system. It has extremely low current consumption ($<1\mu\text{A}$).

PA4220 is equipped with ESD (Human Body Model) protection circuitry on the outputs.

PA4220 is available as an 6L low profile 0.8mm DFN package and 8L SO-8 package. It is specified for operation over the -40°C to $+85^{\circ}\text{C}$ temperature range.



Ordering Information

Temp Range	Package	Part Number
-40 to +85°C	SOIC-8	PA4220DQ-T7
	DFN-6	PA4220DN-T7

ABSOLUTE MAXIMUM RATINGS

(All Voltages are referenced to GND)

V_{CC} +6V
 Continuous Current (I_{IN} , I_{OUT})..... $\pm 150\text{mA}$
 Continuous Current (All Other Pins) $\pm 20\text{mA}$
 Continuous Power Dissipation ($T_A = +70^\circ\text{C}$)

Operating Temperature Range -40°C to $+85^\circ\text{C}$
 Storage Temperature Range -65°C to $+150^\circ\text{C}$
 Junction Temperature $+150^\circ\text{C}$
 Lead Temperature (soldering, 10s) $+300^\circ\text{C}$

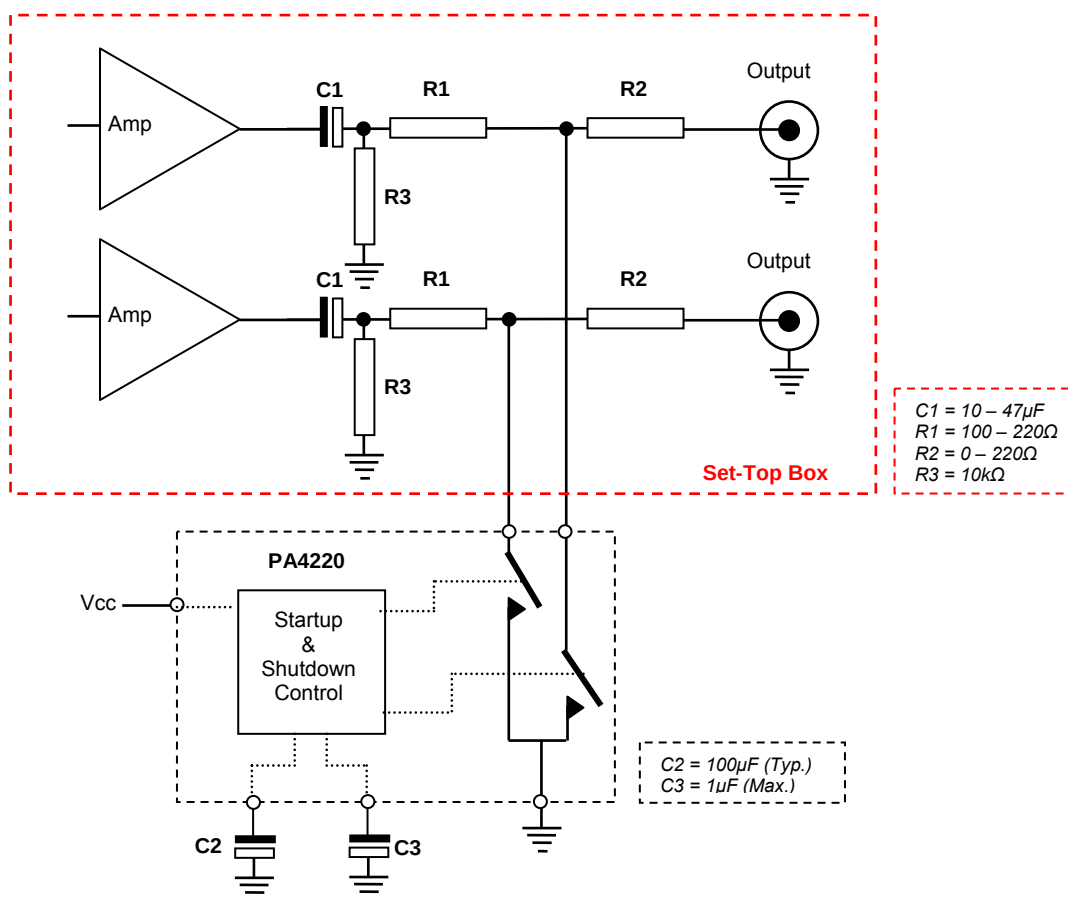
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS:
DC OPERATING CONDITIONS

 Unless otherwise specified, $V_{DD} = 5 \pm 10\%$, $T_A = \text{Ambient Temperature} = 25^\circ\text{C}$.

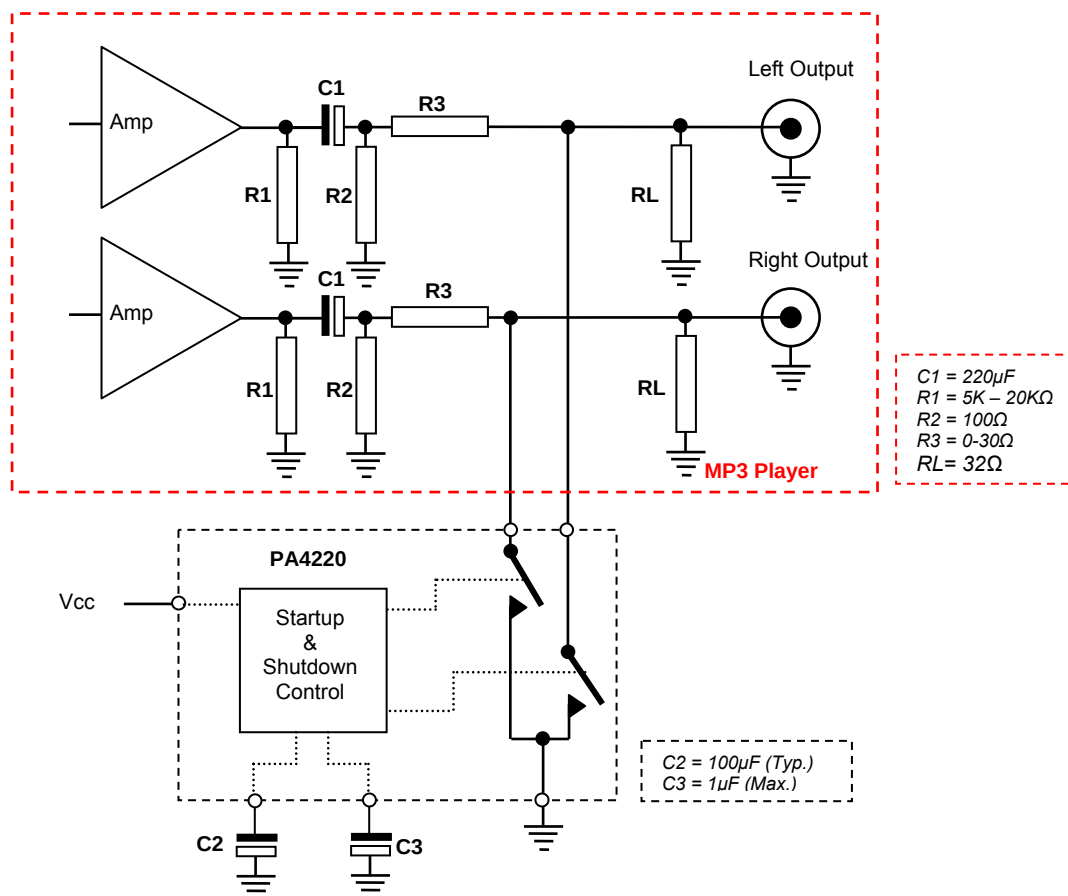
Symbol	Parameter	Condition	Limit			Unit
			Min	Typical	Max	
V_{DD}	Power Supply	Normal Operation	2.3		5.0	V
I_{DD}	Supply Current	Normal Operation			1	μA
T_A	Ambient Temperature	Normal Operation	-40		85	$^\circ\text{C}$
V_{OH}	Logic High O/P Voltage	$I_{OH} = 100\mu\text{A}$	$V_{DD} - 0.1$			V
V_{OL}	Logic Low O/P Voltage	$I_{OL} = -100\mu\text{A}$			0.2	V
V_{IH}	Logic High I/P Voltage	$I_{IH} = 1\mu\text{A}$	$V_{DD} - 0.3$			V
V_{IL}	Logic Low I/P Voltage	$I_{IL} = 1\mu\text{A}$			0.3	V
R_{ON}	Switch ON Resistance	$V_{DD} = 5\text{V}$		3	4	Ω
THD	Total Harmonic Distortion	$R_L = 32\Omega$, 30mW, $f = 1\text{kHz}$		.020		%
V_{SIG}	Analog Signal Range	Normal Operation			3.5	V_{RMS}

Typical Applications



Typical Connection Configuration for PA4220 in Set Top Box Application

Applications continued



Typical Connection Configuration for PA4220 in MP3 Player Application

THEORY OF OPERATION

STARTUP

During Startup, the Power supply ramps from 0V to V_{CC} . It is critical that this rise time be around 50ms for the PA4220 to perform well. This sudden rise in V_{CC} causes the DC Blocking Capacitor to charge and thereby the pop up noise. The PA4220 senses this sudden change in voltage and clamps the output line to a low impedance state and suppresses the Pop noise.

The capacitor at the R_{CS} pin determines the time for which the line can be kept in low impedance state during startup after which the switch is released and normal operation is started.

SHUTDOWN

During Shutdown, the reverse process happens. As the power supply reaches the threshold on its way down, the PA4220 turns the internal switches ON and hence clamping the output stage to low impedance state suppressing the shutdown noise. This operation is governed by the charge stored in the capacitor connected to V_{CAP} pin.

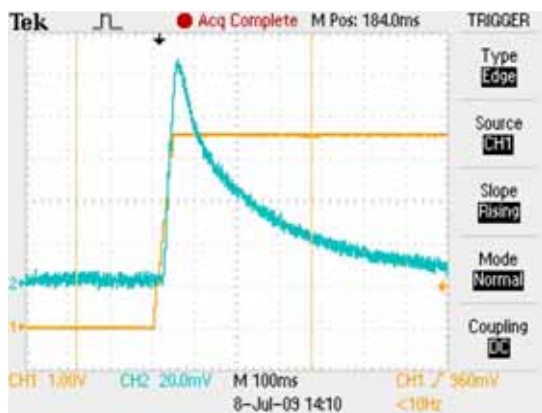


Figure 1: Startup Pop-Noise without PA4220 (32 Ω load)

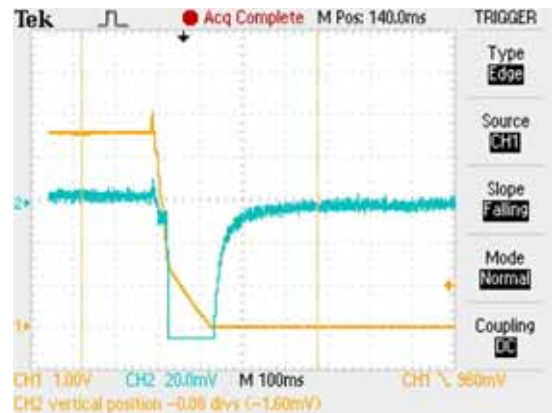


Figure 3: Shutdown Noise without PA4220 (32 Ω load)

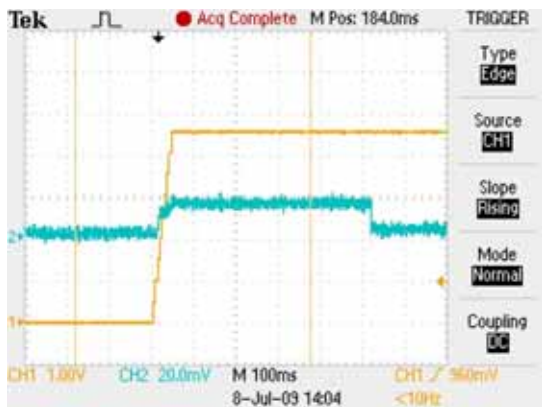


Figure 2: Startup Pop-Noise Reduction with PA4220 (32 Ω load)

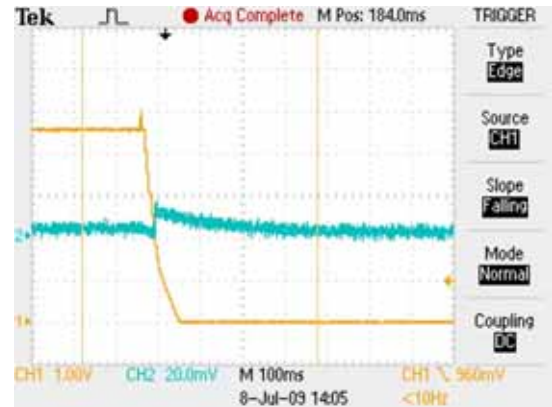
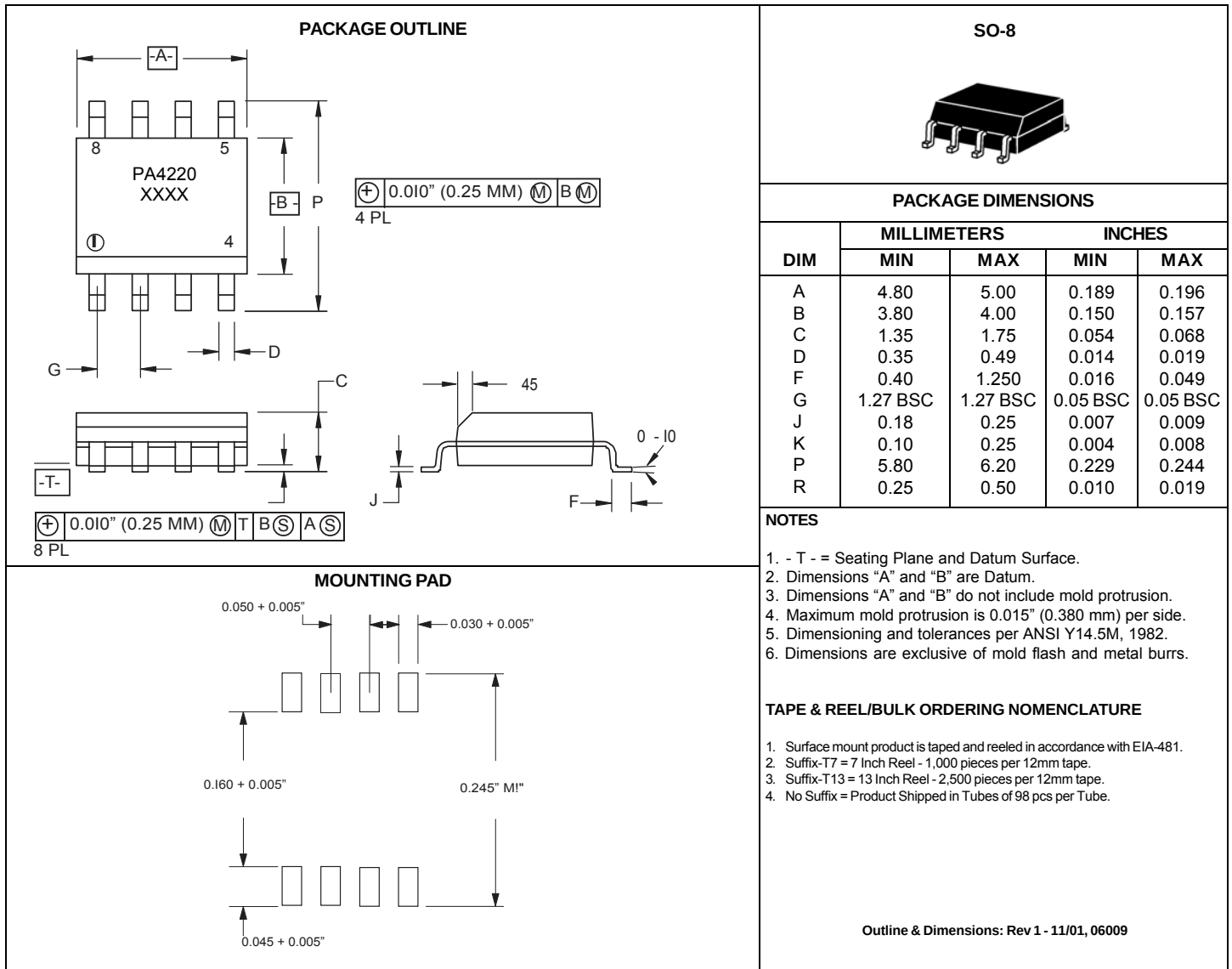
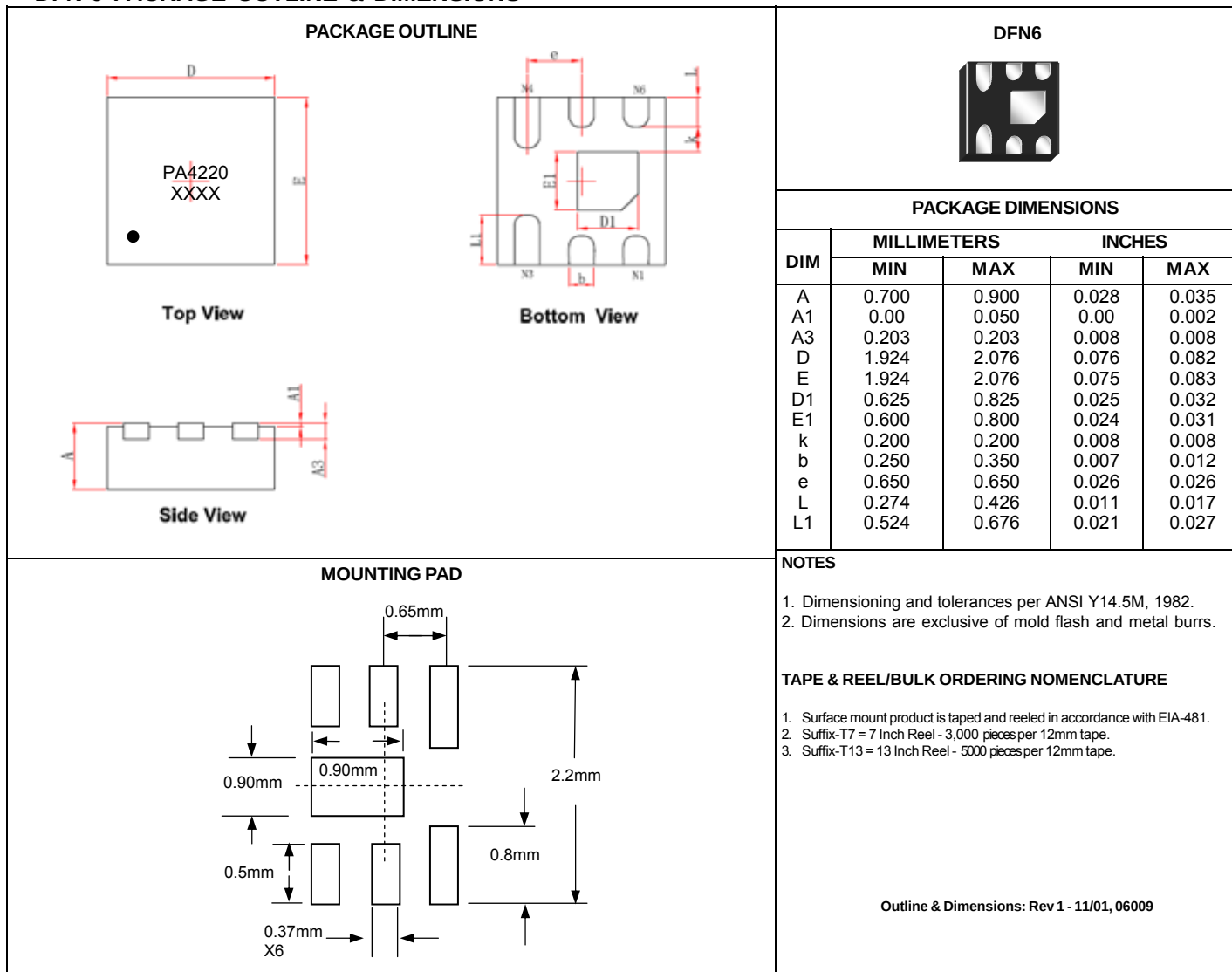


Figure 4: Shutdown Noise with PA4220 (32 Ω load)

SO-8 PACKAGE OUTLINE & DIMENSIONS



DFN-6 PACKAGE OUTLINE & DIMENSIONS



Tape and Reel Specifications (Dimensions in mm)

Reel Dia	A0	B0	K0	D	E	F	W	P0	P2	P	t-max
178 (7")	2.0±0.10	2.0±0.10	0.90±0.10	1.50±0.10	1.75±0.10	3.50±0.05	8.00±0.30	4.00±0.10	2.00±0.05	4.00±0.10	0.25

