THREE CHANNEL E3/DS3/STS-1 LINE INTERFACE UNIT WITH SONET DESYNCHRONIZER

JUNE 2003 *REV. 1.0.0*

GENERAL DESCRIPTION

The XRT75L03D is a three-channel fully integrated Line Interface Unit (LIU) with Jitter Attenuator for E3/DS3/STS-1 applications. It incorporates 3 independent Receivers, Transmitters and Jitter Attenuators in a single 128 pin LQFP package.

Each channel of the XRT75L03D can be independently configured to operate in the data rate, E3 (34.368 MHz), DS3 (44.736 MHz) or STS-1 (51.84 MHz). Each transmitter can be turned off and tri-stated for redundancy support or for conserving power.

The XRT75L03D's differential receiver provides high noise interference margin and is able to receive the data over 1000 feet of cable or with up to 12 dB of cable attenuation.

The XRT75L03D incorporates an advanced crystal-less jitter attenuator per channel that can be selected either in the transmit or receive path. The jitter attenuator performance meets the ETSI TBR-24 and Bellcore GR-499 specifications.

The XRT75L03D provides both Serial Microprocessor Interface as well as Hardware mode for programming and control.

The XRT75L03D supports local, remote and digital loop-backs. The device also has a built-in Pseudo Random Binary Sequence (PRBS) generator and detector with the ability to insert and detect single bit error for diagnostic purposes.

FEATURES

RECEIVER:

- On chip Clock and Data Recovery circuit for high input jitter tolerance
- Meets E3/DS3/STS-1 Jitter Tolerance Requirement
- Detects and Clears LOS as per G.775
- Receiver Monitor mode handles up to 20 dB flat loss with 6 dB cable attenuation
- On chip B3ZS/HDB3 encoder and decoder that can be either enabled or disabled
- On-chip clock synthesizer provides the appropriate rate clock from a single 12.288 MHz Clock
- Provides low jitter output clock

TRANSMITTER:

- Compliant with Bellcore GR-499, GR-253 and ANSI T1.102 Specification for transmit pulse
- Tri-state Transmit output capability for redundancy applications
- Each Transmitter can be turned on or off
- Transmitters provide Current Drive Output

JITTER ATTENUATOR:

- On chip advanced crystal-less Jitter Attenuator for each channel
- Jitter Attenuator can be selected in Receive or Transmit paths
- Meets ETSI TBR 24 Jitter Transfer Requirements
- Compliant with jitter transfer template outlined in ITU G.751, G.752, G.755 and GR-499-CORE,1995 standards
- Jitter Attenuator can be disabled

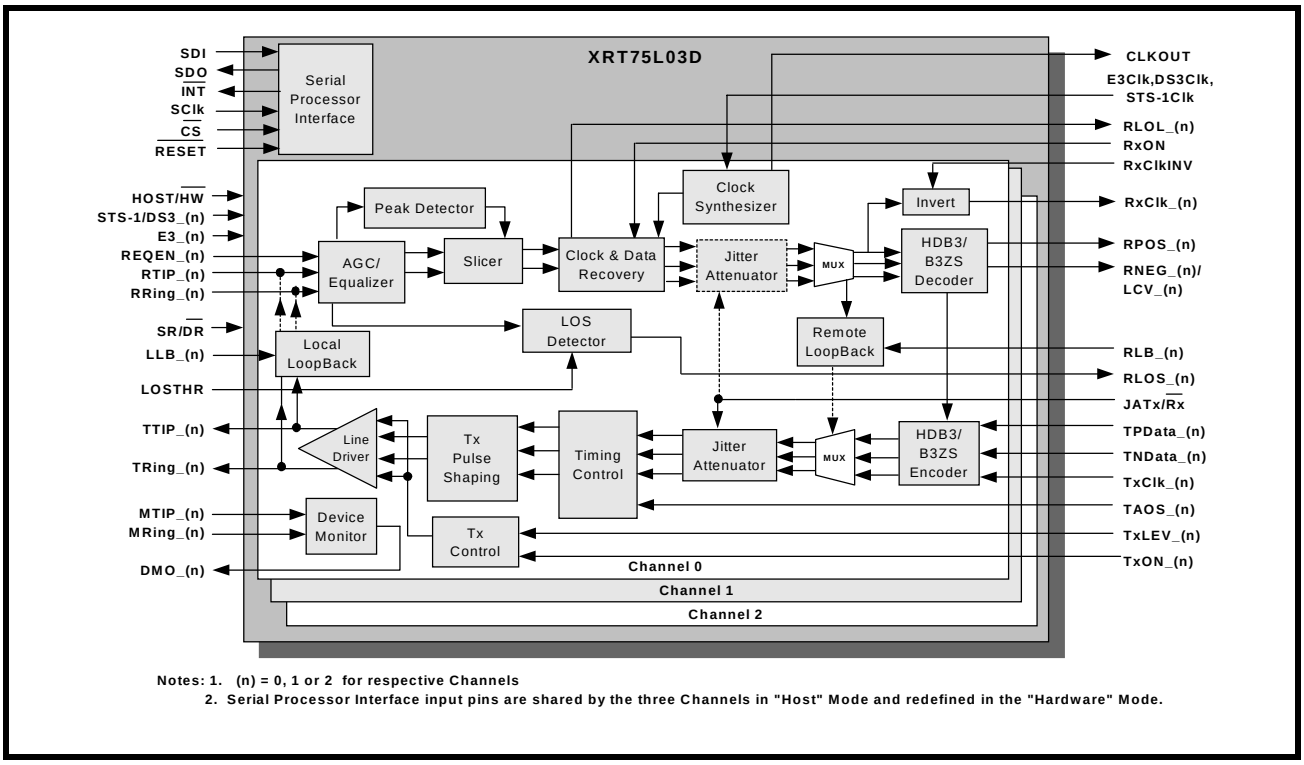
CONTROL AND DIAGNOSTICS:

- 5 wire Serial Microprocessor Interface for control and configuration
- Supports optional internal Transmit driver monitoring
- Hardware Mode for control and configuration
- Each channel supports Local, Remote and Digital Loop-backs
- Single 3.3 V ± 5% power supply
- 5 V Tolerant I/O
- Available in 128 pin Thermally enhanced LQFP Package
- - 40°C to 85°C Industrial Temperature Range

APPLICATIONS

- E3/DS3 Access Equipment
- STS1-SPE to DS3 De-Synchronizing
- DSLAMs
- Digital Cross Connect Systems
- CSU/DSU Equipment
- Routers
- Fiber Optic Terminals

FIGURE 1. BLOCK DIAGRAM OF THE XRT 75L03D



Notes: 1. (n) = 0, 1 or 2 for respective Channels
2. Serial Processor Interface input pins are shared by the three Channels in "Host" Mode and redefined in the "Hardware" Mode.

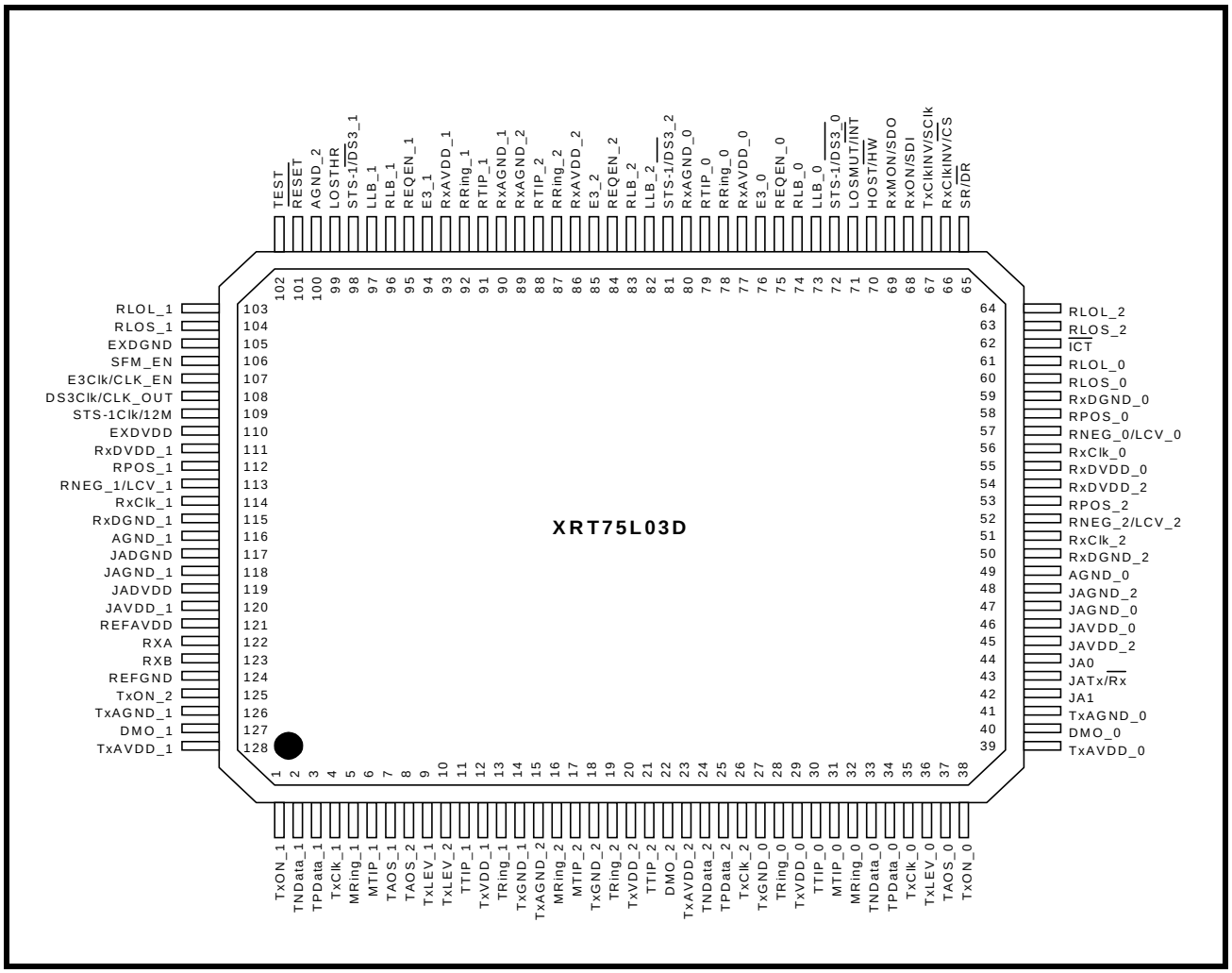
TRANSMIT INTERFACE CHARACTERISTICS

- Accepts either Single-Rail or Dual-Rail data from Terminal Equipment and generates a bipolar signal to the line
- Integrated Pulse Shaping Circuit
- Built-in B3ZS/HDB3 Encoder (which can be disabled)
- Accepts Transmit Clock with duty cycle of 30%-70%
- Generates pulses that comply with the ITU-T G.703 pulse template for E3 applications
- Generates pulses that comply with the DSX-3 pulse template, as specified in Bellcore GR-499-CORE and ANSI T1.102_1993
- Generates pulses that comply with the STSX-1 pulse template, as specified in Bellcore GR-253-CORE
- Transmitter can be turned off in order to support redundancy designs

RECEIVE INTERFACE CHARACTERISTICS

- Integrated Adaptive Receive Equalization (optional) for optimal Clock and Data Recovery
- Declares and Clears the LOS defect per ITU-T G.775 requirements for E3 and DS3 applications
- Meets Jitter Tolerance Requirements, as specified in ITU-T G.823_1993 for E3 Applications
- Meets Jitter Tolerance Requirements, as specified in Bellcore GR-499-CORE for DS3 Applications
- Declares Loss of Signal (LOS) and Loss of Lock (LOL) Alarms
- Built-in B3ZS/HDB3 Decoder (which can be disabled)
- Recovered Data can be muted while the LOS Condition is declared
- Outputs either Single-Rail or Dual-Rail data to the Terminal Equipment

FIGURE 2. PIN OUT OF THE XRT75L03D



ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT75L03DIV	128 Pin LQFP	- 40°C to + 85°C

GENERAL DESCRIPTION 1
FEATURES 1
APPLICATIONS 1
TRANSMIT INTERFACE CHARACTERISTICS 2
RECEIVE INTERFACE CHARACTERISTICS 2
Figure 1. Block Diagram of the XRT 75L03D 2
Figure 2. Pin Out of the XRT75L03D 3
ORDERING INFORMATION 3
PIN DESCRIPTIONS (BY FUNCTION) 4
SYSTEM-SIDE TRANSMIT INPUT AND TRANSMIT CONTROL PINS 4
TRANSMIT LINE SIDE PINS 8
SYSTEM-SIDE RECEIVE OUTPUT AND RECEIVE CONTROL PINS 10
RECEIVE LINE SIDE PINS 17
CLOCK INTERFACE 18
GENERAL CONTROL PINS 19
CONTROL AND ALARM INTERFACE 21
JITTER ATTENUATOR INTERFACE 21
POWER SUPPLY AND GROUND PINS 24
XRT75L03D PIN LISTING IN NUMERICAL ORDER 26
1.0 ELECTRICAL CHARACTERISTICS 31
TABLE 1: ABSOLUTE MAXIMUM RATINGS 31
TABLE 2: DC ELECTRICAL CHARACTERISTICS: 31
2.0 TIMING CHARACTERISTICS 32
Figure 3. Typical interface between terminal equipment and the XRT75L03D (dual-rail data) 32
Figure 4. Transmitter Terminal Input Timing 32
Figure 5. Receiver Data output and code violation timing 33
Figure 6. Transmit Pulse Amplitude test circuit for E3, DS3 and STS-1 Rates 33
3.0 LINE SIDE CHARACTERISTICS: 34
3.1 E3 LINE SIDE PARAMETERS: 34
Figure 7. Pulse Mask for E3 (34.368 mbits/s) interface as per itu-t G.703 34
TABLE 3: E3 TRANSMITTER LINE SIDE OUTPUT AND RECEIVER LINE SIDE INPUT SPECIFICATIONS 35
Figure 8. Bellcore GR-253 CORE Transmit Output Pulse Template for SONET STS-1 Applications 36
TABLE 4: STS-1 PULSE MASK EQUATIONS 36
TABLE 5: STS-1 TRANSMITTER LINE SIDE OUTPUT AND RECEIVER LINE SIDE INPUT SPECIFICATIONS (GR-253) . 37
Figure 9. Transmit Ouput Pulse Template for DS3 as per Bellcore GR-499 38
TABLE 6: DS3 PULSE MASK EQUATIONS 38
TABLE 7: DS3 TRANSMITTER LINE SIDE OUTPUT AND RECEIVER LINE SIDE INPUT SPECIFICATIONS (GR-499) 39
Figure 10. Microprocessor Serial Interface Structure 39
Figure 11. Timing Diagram for the Microprocessor Serial Interface 40
TABLE 8: MICROPROCESSOR SERIAL INTERFACE TIMINGS (TA = 250C, VDD=3.3V± 5% AND LOAD = 10PF) 40
FUNCTIONAL DESCRIPTION: 41
4.0 The Transmitter Section: 41
Figure 12. Single-Rail or NRZ Data Format (Encoder and Decoder are Enabled) 41
Figure 13. Dual-Rail Data Format (encoder and decoder are disabled) 41
4.1 TRANSMIT CLOCK: 42
4.2 B3ZS/HDB3 ENCODER: 42
4.2.1 B3ZS Encoding: 42
4.2.2 HDB3 Encoding: 42
Figure 14. B3ZS Encoding Format 42
Figure 15. HDB3 Encoding Format 42
4.3 TRANSMIT PULSE SHAPER: 43
4.3.1 Guidelines for using Transmit Build Out Circuit: 43
4.3.2 Interfacing to the line: 43
4.4 TRANSMIT DRIVE MONITOR: 44
4.5 TRANSMITTER SECTION ON/OFF: 44
5.0 The Receiver Section: 44

5.1 AGC/EQUALIZER: 44
Figure 16. Transmit Driver Monitor set-up. 44
5.1.1 Interference Tolerance: 45
Figure 17. Interference Margin Test Set up for DS3/STS-1 45
5.2 CLOCK AND DATA RECOVERY: 46
Figure 18. Interference Margin Test Set up for E3. 46
TABLE 9: INTERFERENCE MARGIN TEST RESULTS 46
5.3 B3ZS/HDB3 DECODER: 47
5.4 LOS (LOSS OF SIGNAL) DETECTOR: 47
5.4.1 DS3/STS-1 LOS Condition: 47
DISABLING ALOS/DLOS DETECTION: 47
5.4.2 E3 LOS Condition: 47
TABLE 10: THE ALOS (ANALOG LOS) DECLARATION AND CLEARANCE THRESHOLDS FOR A GIVEN SETTING OF LOSTHR AND REQEN (DS3 AND STS-1 APPLICATIONS) 47
Figure 19. Loss Of Signal Definition for E3 as per ITU-T G.775 48
Figure 20. Loss of Signal Definition for E3 as per ITU-T G.775. 48
5.4.3 Muting the Recovered Data with LOS condition: 49
6.0 Jitter: 49
6.1 JITTER TOLERANCE - RECEIVER: 49
6.1.1 DS3/STS-1 Jitter Tolerance Requirements: 49
Figure 21. Jitter Tolerance Measurements 49
6.1.2 E3 Jitter Tolerance Requirements: 50
Figure 22. Input Jitter Tolerance For DS3/STS-1 50
Figure 23. Input Jitter Tolerance for E3 50
6.2 JITTER TRANSFER - RECEIVER/TRANSMITTER: 51
6.3 JITTER ATTENUATOR: 51
TABLE 11: JITTER AMPLITUDE VERSUS MODULATION FREQUENCY (JITTER TOLERANCE) 51
TABLE 12: JITTER TRANSFER SPECIFICATION/REFERENCES 51
6.3.1 Jitter Generation: 52
7.0 Serial Host interface: 52
TABLE 13: JITTER TRANSFER PASS MASKS 52
Figure 24. Jitter Transfer Requirements and Jitter Attenuator Performance 52
TABLE 14: FUNCTIONS OF SHARED PINS 53
TABLE 15: XRT75L03D REGISTER MAP - QUICK LOOK 54
..... 56
THE REGISTER MAP AND DESCRIPTION FOR THE XRT75L03D 3-CHANNEL DS3/E3/STS-1 LIU IC .. 56
Legend: 56
TABLE 16: COMMAND REGISTER ADDRESS MAP, WITHIN THE XRT75L03D 3-CHANNEL DS3/E3/STS-1 LIU W/ JITTER ATTENUATOR IC 56
THE GLOBAL/CHIP-LEVEL REGISTERS 58
..... 58
REGISTER DESCRIPTION - GLOBAL REGISTERS 58
TABLE 17: LIST AND ADDRESS LOCATIONS OF GLOBAL REGISTERS 58
TABLE 18: APS/REDUNDANCY CONTROL REGISTER - CR0 (ADDRESS LOCATION = 0X00) 58
TABLE 19: BLOCK LEVEL INTERRUPT ENABLE REGISTER - CR32 (ADDRESS LOCATION = 0X20) 61
TABLE 20: BLOCK LEVEL INTERRUPT STATUS REGISTER - CR33 (ADDRESS LOCATION = 0X21) 62
TABLE 21: DEVICE/PART NUMBER REGISTER - CR62 (ADDRESS LOCATION = 0X3E) 63
..... 64
THE PER-CHANNEL REGISTERS 64
TABLE 22: CHIP REVISION NUMBER REGISTER - CR63 (ADDRESS LOCATION = 0X3F) 64
TABLE 23: COMMAND REGISTER ADDRESS MAP, WITHIN THE XRT75L03D 3-CHANNEL DS3/E3/STS-1 LIU W/ JITTER ATTENUATOR IC 64
REGISTER DESCRIPTION - PER CHANNEL REGISTERS 66
TABLE 24: SOURCE LEVEL INTERRUPT ENABLE REGISTER - CHANNEL 0 ADDRESS LOCATION = 0X01 66
TABLE 25: SOURCE LEVEL INTERRUPT STATUS REGISTER - CHANNEL 0 ADDRESS LOCATION = 0X02 68

TABLE 26: ALARM STATUS REGISTER - CHANNEL 0 ADDRESS LOCATION = 0X03 70
TABLE 27: TRANSMIT CONTROL REGISTER - CHANNEL 0 ADDRESS LOCATION = 0X04 75
TABLE 28: RECEIVE CONTROL REGISTER - CHANNEL 0 ADDRESS LOCATION = 0X05 78
TABLE 29: CHANNEL CONTROL REGISTER - CHANNEL 0 ADDRESS LOCATION = 0X06 80
TABLE 30: JITTER ATTENUATOR CONTROL REGISTER - CHANNEL 0 ADDRESS LOCATION = 0X07 83
8.0 Diagnostic Features: 85
8.1 PRBS GENERATOR AND DETECTOR: 85
8.2 LOOPBACKS: 85
8.2.1 ANALOG LOOPBACK: 85
Figure 25. PRBS MODE 85
Figure 26. Analog Loopback 86
8.2.2 DIGITAL LOOPBACK: 87
8.2.3 REMOTE LOOPBACK: 87
Figure 27. Digital Loopback 87
Figure 28. Remote Loopback 87
8.3 TRANSMIT ALL ONES (TAOS): 88
Figure 29. Transmit All Ones (TAOS) 88
9.0 THE SONET/SDH DE-SYNC FUNCTION WITHIN THE XRT75L03D 89
9.1 BACKGROUND AND DETAILED INFORMATION - SONET DE-SYNC APPLICATIONS 89
Figure 30. A Simple Illustration of a DS3 signal being mapped into and transported over the SONET Network 90
9.2 MAPPING/DE-MAPPING JITTER/WANDER 91
9.2.1 HOW DS3 DATA IS MAPPED INTO SONET 91
Figure 31. A Simple Illustration of the SONET STS-1 Frame 92
Figure 32. A Simple Illustration of the STS-1 Frame Structure with the TOH and the Envelope Capacity Bytes Designated 93
Figure 33. The Byte-Format of the TOH within an STS-1 Frame 94
Figure 34. The Byte-Format of the TOH within an STS-1 Frame 95
Figure 35. Illustration of the Byte Structure of the STS-1 SPE 96
Figure 36. An Illustration of Telcordia GR-253-CORE's Recommendation on how map DS3 data into an STS-1 SPE 97
Figure 37. A Simplified "Bit-Oriented" Version of Telcordia GR-253-CORE's Recommendation on how to map DS3 data into an STS-1 SPE 97
9.2.2 DS3 Frequency Offsets and the Use of the "Stuff Opportunity" Bits 98
Figure 38. A Simple Illustration of a DS3 Data-Stream being Mapped into an STS-1 SPE, via a PTE 99
Figure 39. An Illustration of the STS-1 SPE traffic that will be generated by the "Source" PTE, when mapping in a DS3 signal that has a bit rate of 44.736Mbps + 1ppm, into an STS-1 signal 100
9.3 JITTER/WANDER DUE TO POINTER ADJUSTMENTS 102
9.3.1 The Concept of an STS-1 SPE Pointer 102
Figure 40. An Illustration of the STS-1 SPE traffic that will be generated by the Source PTE, when mapping a DS3 signal that has a bit rate of 44.736Mbps - 1ppm, into an STS-1 signal 102
Figure 41. An Illustration of an STS-1 SPE straddling across two consecutive STS-1 frames 103
9.3.2 Pointer Adjustments within the SONET Network 104
Figure 42. The Bit-format of the 16-Bit Word (consisting of the H1 and H2 bytes) with the 10 bits, reflecting the location of the J1 byte, designated 104
Figure 43. The Relationship between the Contents of the "Pointer Bits" (e.g., the 10-bit expression within the H1 and H2 bytes) and the Location of the J1 Byte within the Envelope Capacity of an STS-1 Frame ... 104
9.3.3 Causes of Pointer Adjustments 105
Figure 44. An Illustration of an STS-1 signal being processed via a Slip Buffer 106
Figure 45. An Illustration of the Bit Format within the 16-bit word (consisting of the H1 and H2 bytes) with the "I" bits designated 107
Figure 46. An Illustration of the Bit-Format within the 16-bit word (consisting of the H1 and H2 bytes) with the "D" bits designated 108
9.3.4 Why are we talking about Pointer Adjustments? 109
9.4 CLOCK GAPPING JITTER 109
Figure 47. Illustration of the Typical Applications for the XRT75L03D in a SONET De-Sync Application 109

9.5 A REVIEW OF THE CATEGORY I INTRINSIC JITTER REQUIREMENTS (PER TELCORDIA GR-253-CORE) FOR DS3 APPLICATIONS 110
TABLE 31: SUMMARY OF "CATEGORY I INTRINSIC JITTER REQUIREMENT PER TELCORDIA GR-253-CORE, FOR DS3 APPLICATIONS 110
9.5.1 DS3 De-Mapping Jitter 111
9.5.2 Single Pointer Adjustment 111
Figure 48. Illustration of Single Pointer Adjustment Scenario 111
9.5.3 Pointer Burst 112
9.5.4 Phase Transients 112
Figure 49. Illustration of Burst of Pointer Adjustment Scenario 112
Figure 50. Illustration of "Phase-Transient" Pointer Adjustment Scenario 112
9.5.5 87-3 Pattern 113
9.5.6 87-3 Add 113
Figure 51. An Illustration of the 87-3 Continuous Pointer Adjustment Pattern 113
9.5.7 87-3 Cancel 114
Figure 52. Illustration of the 87-3 Add Pointer Adjustment Pattern 114
Figure 53. Illustration of 87-3 Cancel Pointer Adjustment Scenario 114
9.5.8 Continuous Pattern 115
9.5.9 Continuous Add 115
Figure 54. Illustration of Continuous Periodic Pointer Adjustment Scenario 115
9.5.10 Continuous Cancel 116
Figure 55. Illustration of Continuous-Add Pointer Adjustment Scenario 116
Figure 56. Illustration of Continuous-Cancel Pointer Adjustment Scenario 116
9.6 A REVIEW OF THE DS3 WANDER REQUIREMENTS PER ANSI T1.105.03B-1997. 117
9.7 A REVIEW OF THE INTRINSIC JITTER AND WANDER CAPABILITIES OF THE XRT75L03D IN A TYPICAL SYSTEM APPLICATION 117
9.7.1 Intrinsic Jitter Test results 117
TABLE 32: SUMMARY OF "CATEGORY I INTRINSIC JITTER TEST RESULTS" FOR SONET/DS3 APPLICATIONS 117
9.7.2 Wander Measurement Test Results 118
9.8 DESIGNING WITH THE XRT75L03D 118
9.8.1 How to design and configure the XRT75L03D to permit a system to meet the above-mentioned Intrinsic Jitter and Wander requirements 118
Figure 57. Illustration of the XRT75L03D being connected to a Mapper IC for SONET De-Sync Applications .. 118
CHANNEL CONTROL REGISTER - CHANNEL 0 ADDRESS LOCATION = 0X06 119
CHANNEL 1 ADDRESS LOCATION = 0X0E 119
CHANNEL 2 ADDRESS LOCATION = 0X16 119
CHANNEL CONTROL REGISTER - CHANNEL 0 ADDRESS LOCATION = 0X06 120
CHANNEL 1 ADDRESS LOCATION = 0X0E 120
CHANNEL 2 ADDRESS LOCATION = 0X16 120
JITTER ATTENUATOR CONTROL REGISTER - (CHANNEL 0 ADDRESS LOCATION = 0X07 120
CHANNEL 1 ADDRESS LOCATION = 0X0F 120
CHANNEL 2 ADDRESS LOCATION = 0X17 120
9.8.2 Recommendations on Pre-Processing the Gapped Clocks (from the Mapper/ASIC Device) prior to routing this DS3 Clock and Data-Signals to the Transmit Inputs of the XRT75L03D 121
JITTER ATTENUATOR CONTROL REGISTER - CHANNEL 0 ADDRESS LOCATION = 0X07 121
CHANNEL 1 ADDRESS LOCATION = 0X0F 121
CHANNEL 2 ADDRESS LOCATION = 0X17 121
JITTER ATTENUATOR CONTROL REGISTER - CHANNEL 0 ADDRESS LOCATION = 0X07 121
CHANNEL 1 ADDRESS LOCATION = 0X0F 121
CHANNEL 2 ADDRESS LOCATION = 0X17 121
Figure 58. Illustration of MINOR PATTERN P1 122
Figure 59. Illustration of MINOR PATTERN P2 123
Figure 60. Illustration of Procedure which is used to Synthesize MAJOR PATTERN A 123
Figure 61. Illustration of MINOR PATTERN P3 124
Figure 62. Illustration of Procedure which is used to Synthesize PATTERN B 124
Figure 63. Illustration of the SUPER PATTERN which is output via the "OC-N to DS3" Mapper IC 125

Figure 64. Simple Illustration of the XRT75L03D being used in a SONET De-Synchronizer" Application ... 125
9.8.3 How does the XRT75L03D permit the user to comply with the SONET APS Recovery Time requirements of 50ms (per Telcordia GR-253-CORE)? ... 126
TABLE 33: MEASURED APS RECOVERY TIME AS A FUNCTION OF DS3 PPM OFFSET ... 126
9.8.4 How should one configure the XRT75L03D, if one needs to support "Daisy-Chain" Testing at the end Customer's site? ... 127
JITTER ATTENUATOR CONTROL REGISTER - CHANNEL 0 ADDRESS LOCATION = 0X07 ... 127
CHANNEL 1 ADDRESS LOCATION = 0X0F ... 127
CHANNEL 2 ADDRESS LOCATION = 0X17 ... 127
JITTER ATTENUATOR CONTROL REGISTER - CHANNEL 0 ADDRESS LOCATION = 0X07 ... 127
CHANNEL 1 ADDRESS LOCATION = 0X0F ... 127
CHANNEL 2 ADDRESS LOCATION = 0X17 ... 127
ORDERING INFORMATION ... 128
PACKAGE DIMENSIONS - 14X20 MM, 128 PIN PACKAGE ... 128
REVISIONS ... 129

PIN DESCRIPTIONS (BY FUNCTION)

SYSTEM-SIDE TRANSMIT INPUT AND TRANSMIT CONTROL PINS

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
38 1 125	TxON_0 TxON_1 TxON_2	I	**Transmitter ON Input - Channel 0:** **Transmitter ON Input - Channel 1:** **Transmitter ON Input - Channel 2:** These input pins are used to either enable or disable the Transmit Output Driver corresponding to Channel_n. "Low" - Disables the Transmit Output Driver of the corresponding Channel. In this setting, the corresponding TTIP_n and TRING_n output pins will be tri-stated. "High" - Enables the Transmit Output Driver of the corresponding Channel. In this setting, the corresponding TTIP_n and TRING_n output pins will be enabled. ***NOTES:*** *1. Even when the XRT75L03D is configured in HOST mode, these pins will be active. To enable software control of the Transmit Output Driver outputs, pull these pins "High".* *2. When Transmitters are turned off either in Host or Hardware mode, the TTIP and TRing outputs are Tri-stated.* *3. These pins are internally pulled "High"*
35 4 26	TxClk_0 TxClk_1 TxClk_2	I	**Transmit Clock Input - Channel 0:** **Transmit Clock Input f - Channel 1:** **Transmit Clock Input - Channel 2:** These input pins have two functions: • They function as the timing source for the Transmit Section of the corresponding channel within the XRT75L03D. • They also are used by the Transmit Section of the LIU IC to sample the corresponding TPDATA_n and TNDATA_n input pin. ***NOTE:*** *The user is expected to supply a 44.736MHz ± 20ppm clock signal (for DS3 applications), 34.368MHz ± 20 ppm clock signal (for E3 applications) or a 51.84MHz ± 4.6ppm clock signal (for STS-1, Stratum 3E or better applications).*

SYSTEM-SIDE TRANSMIT INPUT AND TRANSMIT CONTROL PINS

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
34 3 25	TPDATA_0/TxDATA_0 TPDATA_1/TxDATA_1 TPDATA_2/TxDATA_2	I	**Transmit Positive Data Input - Channel 0**: **Transmit Positive Data Input - Channel 1**: **Transmit Positive Data Input - Channel 2**: Transmit Positive Data/Data Input - Channel n: The function of these input pins depends upon whether the corresponding channel has been configured to operate in the Single-Rail or Dual-Rail Mode. Single Rail Mode - Transmit Data Input - Channel n: If the Channel has been configured to operate in the Single-Rail Mode, then all transmit output data will be serially applied to this input pin. This signal will latched into the Transmit Section circuitry upon either the rising or falling edge of the TxCLK_n signal, depending upon user configuration. In the Single-Rail Mode, the Transmit Section of the LIU IC will then encode this data into either the B3ZS line code (for DS3 and STS-1 applications) or the HDB3 line code (for E3 applications). **Dual Rail Mode - Transmit Positive Data Input - Channel n:** If the Channel has been configured to operate in the Dual-Rail Mode, then the user should apply a pulse to this input pin, anytime the Transmit Section of the LIU IC is suppose to generate and transmit a positive-polarity pulse onto the line. This signal will be latched into the Transmit Section circuitry upon either the rising or falling edge of the TxCLK_n signal, depending upon user configuration. In the Dual-Rail Mode, the Transmit Section of the LIU IC will NOT encode this data into either the B3ZS or HDB3 line codes. If the user configures the LIU IC to operate in the Dual-Rail Mode, then B3ZS/HDB3 encoding must have already been done prior to providing the transmit output data to this input pin.
33 2 24	TNData_0 TNData_1 TNData_2	I	**Transmit Negative Data Input - Channel 0:** **Transmit Negative Data Input - Channel 1:** **Transmit Negative Data Input - Channel 2:** If a Channel has been configured to operate in the Dual-Rail Mode, then the user should apply a pulse to this input pin anytime the Transmit Section of the LIU IC is suppose to generate and transmit a negative-polarity pulse onto the line. This signal will be latched into the Transmit Section circuitry upon either the rising or falling edge of the TxCLK_n signal, depending upon user configuration. ***NOTE:*** *If the Channel has been configured operate in the Single-Rail Mode, then this input pin has no function, and should be tied to GND.*

SYSTEM-SIDE TRANSMIT INPUT AND TRANSMIT CONTROL PINS

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
37 7 8	TAOS_0 TAOS_1 TAOS_2	I	**Transmit "All Ones" Input - Channel 0:** **Transmit "All Ones" Input - Channel 1:** **Transmit "All Ones" Input - Channel 2:** These input pin are used to configure the Transmit Section of the corresponding channel to generate and transmit an unframed "All Ones" pattern via the DS3, E3 or STS-1 line signal to the remote terminal equipment. When this configuration is implemented the Transmit Section will ignore the data that it is accepting from the System-side equipment and will overwrite this data will the "All Ones" Pattern. "Low" - Does not configure the channel to transmit an unframed "All Ones" Pattern to the remote terminal equipment. In this mode, the Transmit Section of the Channel will output data based upon the signals that are applied to the TxPOS_n and TxNEG_n input pins. "High" - Configures the Channel to transmit an unframed "All Ones" Pattern to the remote terminal equipment. In this mode, the Transmit Section will override the data that is applied to the TxPOS_n and TxNEG_n input pins, and will proceed to generate and transmit an unframed "All Ones" pattern. *4. This input pin is ignored if the XRT75L03D is operating in the HOST Mode and should be tied to GND.* *5. These input pins are internally pulled down.*
36 9 10	TxLEV_0 TxLEV_1 TxLEV_2	I	**Transmit Line Build-Out Enable/Disable Select - Channel 0:** **Transmit Line Build-Out Enable/Disable Select - Channel 1:** **Transmit Line Build-Out Enable/Disable Select - Channel 2:** These input pins are used to enable or disable the Transmit Line Build-Out (e.g., pulse-shaping) circuit within the corresponding channel. The user should set these input pins either "High" or "Low" based upon the following guidelines. "Low" - If the cable length between the Transmit Output of the corresponding Channel and the DSX-3/STSX-1 location is 225 feet or less. "High" - If the cable length between the Transmit Output of the corresponding Channel and the DSX-3/STSX-1 location is 225 feet or more. ***NOTES:*** *1. These guidelines must be followed in order to insure that the Transmit Section of Channel_n will always generate a DS3 pulse that complies with the Isolated Pulse Template requirements per Bellcore GR-499-CORE, or an STS-1 pulse that complies with the Pulse Template requirements per Telcordia GR-253-CORE.* *2. This input pin is inactive if the XRT75L03D has been configured to operate in the Host Mode, or if the corresponding channel has been configured to operate in the E3 Mode. If either of these cases are true, then tie this input pin to GND.* *3. These input pins are internally pulled "Low".*

SYSTEM-SIDE TRANSMIT INPUT AND TRANSMIT CONTROL PINS

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
40 127 22	DMO_0 DMO_1 DMO_2	O	**Drive Monitor Output - Channel 0:** **Drive Monitor Output - Channel 1:** **Drive Monitor Output - Channel 2:** These output signals are used to indicate some sort of fault condition within the Transmit Output signal path. This output pin will toggle "High" anytime the Transmit Drive Monitor circuitry either, via the corresponding MTIP and MRING input pins or internally, detects no bipolar pulses via the Transmit Output line signal (e.g., via the TTIP_n and TRING_n output pins) for 128 bit-periods. This output pin will be driven "Low" anytime the Transmit Drive Monitor circuitry has detected at least one bipolar pulse via the Transmit Output line signal within the last 128 bit periods.
67	TxClkINV/ SClk	I	**Hardware Mode: Transmit Clock Invert** **Host Mode: Serial Clock Input:** **Hardware mode** This input pin is used to select the edge of the TxCLK_n input that the Transmit Section of all channels will use to sample the TPDATA_n and TNDATA_n input pins. Setting this input pin “High” configures all three Transmitters to sample the TPData_n and TNData_n data on the rising edge of the TxClk_n . Setting this input pin “Low” configures all three Transmitters to sample the TPData_n and TNData_n data on the falling edge of the TxClk_n . **Host Mode** In the Host Mode this pin functions as SClk input pin please refer to the pin descriptions for the Microprocessor interface.

TRANSMIT LINE SIDE PINS

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
30 11 21	TTIP_0 TTIP_1 TTIP_2	O	**Transmit TTIP Output - Positive Polarity Signal - Channel 0:** **Transmit TTIP Output - Positive Polarity Signal - Channel 1:** **Transmit TTIP Output - Positive Polarity Signal - Channel 2:** These output pins along with the corresponding TRING_n output pins, function as the Transmit DS3/E3/STS-1 Line output signal drivers for a given channel, of the XRT75L03D. Connect this signal and the corresponding TRING_n output signal to a 1:1 transformer. Whenever the Transmit Section of the Channel generates and transmits a positive-polarity pulse onto the line, this output pin will be pulsed to a "higher-voltage" than its corresponding TRING_n output pins. Conversely, whenever the Transmit Section of the Channel generates and transmit a negative-polarity pulse onto the line, this output pin will be pulsed to a "lower-voltage" than its corresponding TRING_n output pin. ***NOTE:*** *This output pin will be tri-stated whenever the corresponding TxON_n input pin or bit-field is set to "0".*
28 13 19	TRing_0 TRing_1 TRing_2	O	**Transmit Ring Output - Negative Polarity Signal - Channel 0:** **Transmit Ring Output - Negative Polarity Signal - Channel 1:** **Transmit Ring Output - Negative Polarity Signal - Channel 2:** These output pins along with the corresponding TTIP_n output pins, function as the Transmit DS3/E3/STS-1 Line output signal drivers for a given channel, within the XRT75L03D. Connect this signal and the corresponding TTIP_n output signal to a 1:1 transformer. Whenever the Transmit Section of the Channel generates and transmits a positive-polarity pulse onto the line. This output pin will be pulsed to a "lower-voltage" than its corresponding TTIP_n output pins. Conversely, whenever the Transmit Section of the Channel generates and transmit a negative-polarity pulse onto the line. This output pin will be pulsed to a "higher-voltage" than its corresponding TTIP_n output pin. ***NOTE:*** *This output pin will be tri-stated whenever the corresponding TxON_n input pin or bit-field is set to "0".*

TRANSMIT LINE SIDE PINS

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
31 6 17	MTIP_0 MTIP_1 MTIP_2	I	**Monitor Tip Input - Positive Polarity Signal - Channel 0:** **Monitor Tip Input - Positive Polarity Signal - Channel 1:** **Monitor Tip Input - Positive Polarity Signal - Channel 2:** These input pins along with MRING_n function as the Transmit Drive Monitor Output (DMO) input monitoring pins. To (1) monitor the Transmit Output line signal and (2) to perform this monitoring externally, then this pin MUST be connected to the corresponding TTIP_n output pin via a 274 ohm series resistor. Similarly, the MRING_n input pin MUST also be connected to its corresponding TRING_n output pin via a 274 ohm series resistor. The MTIP_n and MRING_n input pins will continuously monitor the Transmit Output line signal via the TTIP_n and TRING_n output pins for bipolar activity. If these pins do not detect any bipolar activity for 128 bit periods, then the Transmit Drive Monitor circuit will drive the corresponding DMO_n output pin "High" in order to denote a possible fault condition in the Transmit Output Line signal path. ***NOTES:*** *1. These input pins are inactive if the user choose to internally monitor the Transmit Output line signal.* *2. Internal Monitoring is only available as an option if the XRT75L03D in is being operated in the Host Mode.*
32 5 16	MRing_0 MRing_1 MRing_2	I	**Monitor Ring Input - Channel 0:** **Monitor Ring Input - Channel 1:** **Monitor Ring Input - Channel 2:** These input pins along with MTIP_n function as the Transmit Drive Monitor Output (DMO) input monitoring pins. To (1) monitor the Transmit Output line signal and (2) to perform this monitoring externally, then this input pin MUST be connected to the corresponding TRING_n output pin via a 274 ohm series resistor. Similarly, the MTIP_n input pin MUST be connected to its corresponding TTIP_n output pin via a 274 ohm series resistor. The MTIP_n and MRING_n input pins will continuously monitor the Transmit Output line signal via the TTIP_n and TRING_n output pins for bipolar activity. If these pins do not detect any bipolar activity for 128 bit periods, then the Transmit Drive Monitor circuit will drive the corresponding DMO_n output pin "High" to indicate a possible fault condition in the Transmit Output Line signal path. ***NOTES:*** *1. These input pins are inactive if the user chooses to internally monitor the Transmit Output line signal.* *2. Internal Monitoring is only available as an option if the XRT75L03D is being operated in the Host Mode.*

SYSTEM-SIDE RECEIVE OUTPUT AND RECEIVE CONTROL PINS

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
60 104 63	RLOS_0 RLOS_1 RLOS_2	O	**Receive Loss of Signal Output Indicator - Channel 0:** **Receive Loss of Signal Output Indicator - Channel 1:** **Receive Loss of Signal Output Indicator - Channel 2:** This output pin indicates whether or not the corresponding channel is declaring the Loss of Signal (LOS) Defect condition. "Low" - Indicates that the corresponding Channel is NOT currently declaring the LOS defect condition. "High" - Indicates that the corresponding Channel is currently declaring the LOS defect condition.
61 103 64	RLOL_0 RLOL_1 RLOL_2	O	**Receive Loss of Lock Output Indicator - Channel 0:** **Receive Loss of Lock Output Indicator - Channel 1:** **Receive Loss of Lock Output Indicator - Channel 2:** This output pin indicates whether or not the corresponding channel is declaring the Loss of Lock (LOL) Condition. "Low" - Indicates that the corresponding Channel is NOT declaring the LOL condition. "High" - Indicates that the corresponding Channel is currently declaring the LOL condition. ***NOTE:*** *The Receive Section of a given channel will declare the LOL condition anytime the frequency of the Recovered Clock (RCLK) signal differs from that of the E3CLK input clock signal (if the channel is operating in the E3 Mode), the DS3CLK input clock signal (if the channel is operating in the DS3 Mode) the STS-1CLK input clock signal (if the channel is operating in the STS-1 Mode), or that clock signal which is derived from the SFM Clock Synthesizer block (if the chip is operating in the Single-Frequency Mode) by 0.5% (or 5000ppm) or more.*
58 112 53	RPOS_0/RDATA_0 RPOS_1/RDATA_1 RPOS_2/RDATA_2	O	**Receive Positive Data Output - Receive Data Output - Channel 0:** **Receive Positive Data Output - Receive Data Output - Channel 1:** **Receive Positive Data Output - Receive Data Output - Channel 2:** The function of these output pins depends upon whether the channel/device has been configured to operate in the Single-Rail or Dual-Rail Mode. **Dual-Rail Mode - Receive Positive Polarity Data Output** If the channel/device has been configured to operate in the Dual-Rail Mode, then all positive-polarity data will be output via this output pin. The negative-polarity data will be output via the corresponding RNEG_n output pin. In other words, the Receive Section of the corresponding Channel will pulse this output pin "High" for one period of RCLK_n anytime it receives a positive-polarity pulse via the RTIP/RRING input pins. The data that is output via this pin is updated upon a user-selectable edge of the RCLK_n output clock signal. **Single-Rail Mode - Receive Data Output** If the channel/device has been configured to operate in the Single-Rail Mode, then all Receive (or Recovered) data will be output via this output pin. The data that is output via this pin is updated upon a user-selectable edge of the RCLK_n output clock signal.

SYSTEM-SIDE RECEIVE OUTPUT AND RECEIVE CONTROL PINS

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
57 113 52	RNEG_0/LCV_0 RNEG_1/LCV_1 RNEG_2/LCV_2	O	**Receive Negative Data Output/Line Code Violation Indicator - Channel 0:** **Receive Negative Data Output/Line Code Violation Indicator - Channel 1:** **Receive Negative Data Output/Line Code Violation Indicator - Channel 2:** The function of these pins depends on whether the XRT75L03D is configured in Single Rail or Dual Rail mode. **Dual-Rail Mode - Receive Negative Polarity Data Output** If the channel/device has been configured to operate in the Dual-Rail Mode, then all negative-polarity data will be output via this output pin. The positive-polarity data will be output via the corresponding RPOS_n output pin. In other words, the Receive Section of the corresponding Channel will pulse this output pin "High" for one period of RCLK_n anytime it receives a negative-polarity pulse via the RTIP/RRING input pins. The data that is output via this pin is updated upon a user-selectable edge of the RCLK_n output clock signal. **Single-Rail Mode - Line Code Violation Indicator Output** If the channel/device has been configured to operate in the Single-Rail Mode, then this particular output pin will function as the Line Code Violation indicator output. In this configuration, the Receive Section of the Channel will pulse this output pin "High" for at least one RCLK period whenever it detects either an LCV (Line Code Violation) or an EXZ (Excessive Zero Event). The data that is output via this pin is updated upon a user-selectable edge of the RCLK_n output clock signal.
56 114 51	RxClk_0 RxClk_1 RxClk_2	O	**Receive Clock Output - Channel 0:** **Receive Clock Output - Channel 1:** **Receive Clock Output - Channel 2:** This output pin functions as the Receive or recovered clock signal. All Receive (or recovered) data will output via the RPOS_n and RNEG_n outputs upon the user-selectable edge of this clock signal. Additionally, if the device/channel has been configured to operate in the Single-Rail Mode, then the RNEG_n/LCV_n output pins will also be updated upon the user-selectable edge of this clock signal.
75 95 84	REQEN_0 REQEN_1 REQEN_2	I	**Receive Equalization Enable Input - Channel 0:** **Receive Equalization Enable Input - Channel 1:** **Receive Equalization Enable Input - Channel 2:** These input pins are used to either enable or disable the Receive Equalizer block within the Receive Section of the corresponding channel. "Low" - Disables the Receive Equalizer within the corresponding channel. "High" - Enables the Receive Equalizer within the corresponding channel. ***NOTES:*** *1. For virtually all applications, it is recommend that this input pin be pulled "High" and enable the Receive Equalizer.* *2. This input pin ignored and should be tied to GND if the XRT75L03D has been configured to operate in the Host Mode.* *3. These input pins are internally pulled low.*

SYSTEM-SIDE RECEIVE OUTPUT AND RECEIVE CONTROL PINS

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
71	LOSMUT/ $\overline{\text{INT}}$	I/O	**Muting Upon LOS Enable/Interrupt Output Pin** This input pin is used to configure the Receive Section, in each of the three channels within the chip, to automatically pull their corresponding Recovered Data Output pins (e.g. RPOS_n and RNEG_n) to GND anytime and for the duration that the Receive Section declares the LOS defect condition. In other words, this feature if enabled will cause the Receive Channel to automatically mute the Recovered data anytime and for the duration that the Receive Section declares the LOS defect condition. "Low" - Disables the Muting upon LOS feature. In this setting the Receive Section will NOT automatically mute the Recovered Data whenever it is declaring the LOS defect condition. "High" - Enables the Muting upon LOS feature. In this setting the Receive Section will automatically mute the Recovered Data whenever it is declaring the LOS defect condition. ***NOTES:*** *1. This input pin is will function as the Interrupt Request output pin within the Microprocessor Serial Interface, if the XRT75L03D has been configured to operate in the Host Mode.* *2. This configuration setting applies globally to each of the three (3) channels within the XRT75L03D.*
99	LOSTHR	I	**Analog LOS Detector Threshold Level Select Input:** This input pin permits the user to select both of the following parameters for the Analog LOS Detector within each of the three Receive Sections within the XRT75L03D. **1.** The Analog LOS Defect Declaration Threshold (e.g., the maximum signal level that the Receive Section of a given channel must detect before declaring the LOS Defect condition), and **2.** The Analog LOS Defect Clearance Threshold (e.g., the minimum signal level that the Receive Section of a given channel must detect before clearing the LOS Defect condition) Setting this input pin "High" selects one set of Analog LOS Defect Declaration and Clearance thresholds. Setting this input pin "Low" selects the other set of Analog LOS Defect Declaration and Clearance thresholds. Please see Table 10 for more details. ***NOTE:*** *This input pin is only active if at least one channel within the XRT75L03D has been configured to operate in the DS3 or STS-1 Modes.*

SYSTEM-SIDE RECEIVE OUTPUT AND RECEIVE CONTROL PINS

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
69	RxMON/ SDO	I	**Receiver Monitor Mode Enable:** This input pin permits the user to configure each of the three (3) Receive Sections within the XRT75L03D, into the Receiver Monitor Mode. If the user configures each of the Receive Sections into the Receive Monitor Mode, then each of the Receiver Sections will be able to receive a nominal DSX-3/STSX-1 signal that has been attenuated by 20dB of flat loss along with 6dB of cable loss, in an error-free manner, and without declaring the LOS defect condition. "Low" - Configures each of the Receive Sections to operate in the Normal Mode. "High" - Configures each of the Receive Sections to operate in the Receive Monitor Mode. ***NOTES:*** *1. This input pin will function as the SDO (Serial Data Output pin within the Microprocessor Serial Interface) whenever the XRT75L03D has been configured to operate in the Host Mode.* *2. This configuration setting applies globally to all three (3) of the channels within the XRT75L03D.*
68	RxON/ SDI	I	**Receive ON:** This input pin permits the user to either turn on or turn off each of the three (3) Receive Sections within the XRT75L03D. If the user turns on the Receive Sections of each channel, then all three channels will begin to receive the incoming DS3, E3 or STS-1 data-streams via the RTIP_n and RRING_n input pins. Conversely, if the user turns off the Receive Section, then the entire Receive Section (e.g., the AGC and Receive Equalizer blocks, Clock Recovery PLL, etc.) will be powered down. "Low" - Shuts off the Receive Sections within each of the three (3) Channels in the XRT75L03D. "High" - Turns on the Receive Sections within each of the three (3) Channels in the XRT75L03D. ***NOTES:*** *1. This input pin will function as the SDI (Serial Data Input pin within the Microprocessor Serial Interface) whenever the XRT75L03D has been configured to operate in the Host Mode.* *2. This configuration setting applies globally to all three (3) of the channels within the XRT75L03D.* *3. This pin is internally pulled low.*

SYSTEM-SIDE RECEIVE OUTPUT AND RECEIVE CONTROL PINS

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
66	RxClkINV/ $\overline{CS}$	I	Receive Clock Invert Input - Chip Selectl: In Hardware Mode is pin is used to configure the Receive Sections of the three (3) channels in the XRT75L03D to either output the recovered data via the RPOS_n or RNEG_n/LCV_n output pins upon either the rising or falling edge of the RCLK_n clock output signal. "Low" - Configures each of the Receive Sections to output the recovered data via the RPOS_n and RNEG_n/LCV_n output pins upon the rising edge of the RCLK_n output clock signal. "High" - Configures each of the Receive Sections to output the recovered data via the RPOS_n and RNEG_n/LCV_n output pins upon the falling edge of the RCLK_n output clock signal. ***NOTES:*** *1. This input pin will function as the $\overline{CS}$ (Chip Select Input pin) of the Microprocessor Serial Interface when the XRT75L03D has been configured to operate in the Host Mode.* *2. This configuration setting applies globally to all three (3) of the channels within the XRT75L03D.* *3. If the Receive Sections are configured to operate in the Single-Rail Mode, then the LCV_n output pin will be updated on the user-selected edge of the RCLK_n signal, per this configuration selection.*
106	SFM_EN	I	**Single Frequency Mode Enable:** This input pin is used to configure the XRT75L03D to operate in the SFM (Single Frequency) Mode. When this feature is invoked the Single-Frequency Mode Synthesizer will become active. By applying a 12.288MHz clock signal to pin 109, STS-1CLK/12M the XRT75L03D will, depending upon which mode the user has configured each of the three channels, generate all of the appropriate clock signals (e.g., 34.368MHz, 44.736MHz or 51.84. Further, the XRT75L03D internal circuitry will route each of these synthesized clock signals to the appropriate nodes of the corresponding three channels in the XRT75L03D. "Low" - Disables the Single Frequency Mode. In this configuration setting, the user is required to supply to the E3CLK, DS3CLK or STS-1CLK input pins all of the relevant clock signals that are to be used within the chip. "High" - Enables the Single-Frequency Mode. A 12.288MHz clock signal MUST be applied to pin 109 (STS-1CLK/12M). ***NOTE:*** *This input pin is internally pulled low.*

SYSTEM-SIDE RECEIVE OUTPUT AND RECEIVE CONTROL PINS

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
107	E3Clk/ CLK_EN	I	E3 Reference Clock Input/SFM Clock Output Enable: The function of this chip depends upon whether or not the XRT75L03D has been configured to operate in the Single-Frequency Mode. **If NOT operating in the Single-Frequency Mode** If the XRT75L03D has NOT been configured to operate in the SFM (Single Frequency) Mode, and if at least one channel is to be operated in the E3 Mode, then a 34.368MHz clock signal must be applied to this input pin. If the user does not intend to operate the device in the SFM Mode nor operate any of the channels in the E3 Mode tie this input signal to GND. **If operating in the Single-Frequency Mode** If the XRT75L03D is operated in the SFM Mode and is to output a clock signal that is synthesized from the SFM Clock Synthesizer PLL so that the user's system can use this clock signal as a timing source, pull this input pin to a logic "High". If the user pull this input pin "High", then the XRT75L03D will output the line rate clock signal that has been synthesized for Channel 1, via pin 108 (DS3CLK/ CLK_OUT). For example, if Channel 1 is configured to operate in the STS-1 Mode and this input pin is pulled "High", then the XRT75L03D will output a 51.84MHz clock signal via the CLK_OUT pin.

SYSTEM-SIDE RECEIVE OUTPUT AND RECEIVE CONTROL PINS

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
108	DS3Clk/ CLK_OUT	I/O	**DS3 Reference Clock Input/SFM Synthesizer Clock Output:** The function of this chip depends upon whether or not the XRT75L03D has been configured to operate in the SFM Mode. **If NOT operating in the Single-Frequency Mode** If the XRT75L03D has NOT been configured to operate in the SFM Mode, and if at least one channel of the XRT75L03D is configured in the DS3 Mode, then a clock signal with a frequency of 44.736 MHz ± 20ppm must be applied to this input pin. If the XRT75L03D is not configured to operate in the SFM Mode and none of the channels are to be operated in the DS3 Mode, tie this input signal to GND. **If operating in the Single-Frequency Mode** If the XRT75L03D is configured to operate in the SFM Mode, and if pin 107 (E3CLK/CLKEN) is pulled to a logic "High", then the SFM Clock Synthesizer PLL generated line rate clock signal for Channel 1 will be output via this output pin. In this mode, this particular output pin can be used by the user's system as a timing source.
109	STS-1Clk/ 12M	I	**STS-1 Reference Clock Input/12.288MHz SFM Reference Clock Input:** The function of this pin depends upon whether or not the XRT75L03D has been configured to operate in the SFM Mode. **If NOT operating in the Single-Frequency Mode** If the XRT75L03D has NOT been configured to operate in the SFM Mode and if at least one channel is intended to operate in the STS-1 Mode, then the user must supply a clock signal with a frequency of 51.84MHz ± 4.6ppm to this input pin If the XRT75L03D is not to be operatedin the SFM Mode and none of the channels are to be operated in the STS-1 Mode, tie this input signal to GND. **If operating in the Single-Frequency Mode** If the user has configured the XRT75L03D has been configured to operate in the SFM Mode a clock signal with a frequency of 12.288MHz ± 20ppm MUST be applied to this input pin. The SFM Synthesizer will then synthesize one of the appropriate line rate frequencies (e.g., 34.368MHz for E3, 44.736MHz for DS3, and 51.84MHz for STS-1) based upon this 12.288MHz Reference Clock source.

RECEIVE LINE SIDE PINS

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
79 91 88	RTIP_0 RTIP_1 RTIP_2	I	**Receive TIP Input - Channel 0:** **Receive TIP Input - Channel 1:** **Receive TIP Input - Channel 2:** These input pins along with the corresponding RRing_n input pin function as the Receive DS3/E3/STS-1 Line input signal receiver for a given channel of the XRT75L03D. Cconnect this signal and the corresponding RRING_n input signal to a 1:1 transformer. Whenever the RTIP/RRING input pins are receiving a positive-polarity pulse within the incoming DS3, E3 or STS-1 line signal, then this input pin will be pulsed to a "higher-voltage" than its corresponding RRING_n input pin. Conversely, whenever the RTIP/RRING input pins are receiving a negative-polarity pulse within the incoming DS3, E3 or STS-1 line signal, then this input pin will be pulsed to a "lower-voltage" than its corresponding RRING_n input pin.
78 92 87	RRing_0 RRing_1 RRing_2	I	**Receive Ring Input - Channel 0:** **Receive Ring Input - Channel 1:** **Receive Ring Input - Channel 2:** These input pins along with the corresponding RTIP_n input pin function as the Receive DS3/E3/STS-1 Line input signal receiver for a given channel of the XRT75L03D. Connect this signal and the corresponding RTIP_n input signal to a 1:1 transformer. Whenever the RTIP/RRING input pins are receiving a positive-polarity pulse within the incoming DS3, E3 or STS-1 line signal, then this input pin will be pulsed to a "lower-voltage" than its corresponding RTIP_n input pin. Conversely, whenever the RTIP/RRING input pins are receiving a negative-polarity pulse within the incoming DS3, E3 or STS-1 line signal, then this input pin will be pulsed to a "higher-voltage" than its corresponding RTIP_n input pin.

CLOCK INTERFACE

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
107	E3Clk/ CLK_EN	I	**E3 Clock Input (34.368 MHz ± 20 ppm):** If all the 3 channels or any one of the channels is configured in E3 mode, a reference clock 34.368 MHz ± 20 ppm is input to this pin.. **Clock Output Enable:** If the Single Frequency Mode is selected, tie this pin “High” to enable the clock output through the CLK_OUT pin (pin 108).
108	DS3Clk/ CLK_OUT	I/O	**DS3 Clock Input (44.736 MHz ± 20 ppm):** If all the 3 channels or any one of the channels is configured in DS3 mode, a reference clock 44.736 MHz ± 20 ppm is input to this pin. **Clock Output:** When the Single Frequency Mode is enabled, this pin is configured as the clock output from Channel 1.This clock frequency is determined by the Channel 1 setting.. ***NOTE:*** *This low jitter output clock can be used as the input clock source for the framer device. thus eliminating the need for a separate clock source for the framer.*
109	STS-1Clk/ 12M	I	**STS-1 Clock Input (51.84 MHz ± 20 ppm):** If all the 3 channels or any one of the channels is configured in STS-1 mode, a reference clock 51.84 MHz ± 20 ppm is input to this pin. **Single Frequency Mode Clock Input:** In Single Frequency Mode, a reference clock of 12.288 MHz ± 20 ppm is connected to this pin and the internal clock synthesizer generates the appropriate clock frequencies based on the configuration of the rates (E3 or DS3 or STS-1).

GENERAL CONTROL PINS

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
65	SR/$\overline{DR}$	I	**Single-Rail/Dual-Rail Select Input - Chip Level** This input pin is used to configure the XRT75L03D to operate in either the Single-Rail or Dual-Rail Mode. If the XRT75L03D is configured to operate in the Single-Rail Mode, then all of the following will happen. • All of the B3ZS/HDB3 Encoder and Decoder blocks in the XRT75L03D will be enabled. • The Transmit Section of each channel will accept all of the outbound data from the System-side Equipment via the TPDATA_n (or TxDATA_n) input pin. • The Receive Section of each channel will output all of the recovered data to the System-side Equipment via the RPOS output pin. • Each of the RNEG/LCV output pins will now function as the LCV (Line Code Violation or Excessive Zero Event) indicator output pin. If the user configures the device to operate in the Dual-Rail Mode, then all of the following will happen. • All of the B3ZS/HDB3 Encoder and Decoder blocks in the XRT75L03D will be disabled.· • The Transmit Section of each channel will accept positive-polarity data via the TPDATA_n input pin, and negative-polarity data via the TNDATA_n input pin. • The Receive Section of each channel will pulse the RPOS_n output pin "High" for one period of RCLK_n for each time a positive-polarity pulse is received via the RTIP_n/RRING_n input pins • Likewise, the Receive Section of each channel will also pulse the RNEG_n output pin "High" for one period of RCLK_n for each time a negative-polarity pulse is received via the RTIP_n/RRING_n input pins. "Low" - Configures the XRT75L03D to operate in the Dual-Rail Mode. "High" - Configures the XRT75L03D to operate in the Single-Rail Mode. ***NOTES:*** *1. This input pin is ignored and should be tied to GND if the XRT75L03D has been configured to operate in the Host Mode.* *2. This pin is internally pulled "Low".*
76 94 85	E3_0 E3_1 E3_2	I	**E3 Mode Select Input - Channel 0** **E3 Mode Select Input - Channel1** **E3 Mode Select Input - Channel 2** This input pin, along with the corresponding STS-1/$\overline{DS3}$_n input pin is used the to configure a given channel within the XRT75L03D into either the DS3, E3 or STS-1 Modes. "High" - Configures the corresponding channel to operate in the E3 Mode. "Low" - Configures the corresponding channel to operate in either the DS3 or STS-1 Modes, depending upon the setting of the corresponding STS-1/$\overline{DS3}$_n input pin. ***NOTES:*** *1. This input pin is ignored and should be tied to GND if the XRT75L03D has been configured to operate in the Host Mode.* *2. This input pin is internally pulled low.*

GENERAL CONTROL PINS

<table>
<tr><th>PIN #</th><th>SIGNAL NAME</th><th>TYPE</th><th>DESCRIPTION</th></tr>
<tr><td>72
98
81</td><td>STS-1/$\overline{\text{DS3}}$_0
STS-1/$\overline{\text{DS3}}$_1
STS-1/$\overline{\text{DS3}}$_2</td><td>I</td><td>STS-1/DS3 Select Input - Channel 0
STS-1/DS3 Select Input - Channel 1
STS-1/DS3 Select Input - Channel 2
This input pin, along with the corresponding E3_n input pin is used the to configure a given channel within the XRT75L03D into either the DS3, E3 or STS-1 Modes.
"High" - Configures the corresponding channel to operate in the STS-1 Mode provided that the corresponding E3_n input pin is pulled "Low".
"Low" - Configures the corresponding channel to operate in DS3 Mode provided that the corresponding E3_n input pin is pulled "Low".
NOTES:
1. This input pin is ignored and should be tied to GND if the XRT75L03D has been configured to operate in the Host Mode or if the corresponding E3_n input pin is pulled "High".
2. This input pin is internally pulled low.</td></tr>
<tr><td>74
96
83</td><td>RLB_0
RLB_1
RLB_2</td><td>I</td><td>Remote Loop-back - RLB Input - Channel 0:
Remote Loop-back - RLB Input - Channel 1:
Remote Loop-back - RLB Input - Channel 2:
This input pin along with LLB_n is used to configure different Loop-Back modes.
<table><tr><th>RLB_n</th><th>LLB_n</th><th>Loopback Mode</th></tr><tr><td>0</td><td>0</td><td>Normal (No Loop-Back) Mode</td></tr><tr><td>0</td><td>1</td><td>Analog Loop-Back Mode</td></tr><tr><td>1</td><td>0</td><td>Remote Loop-Back Mode</td></tr><tr><td>1</td><td>1</td><td>Digital Local Loop-Back Mode</td></tr></table>NOTE: This input pin is ignored and should be connected to GND if the XRT75L03D is operating in the HOST Mode.</td></tr>
<tr><td>73
97
82</td><td>LLB_0
LLB_1
LLB_2</td><td>I</td><td>Loop-Back Select - LLB Input - Channel 0
Loop-Back Select - LLB Input - Channel 1
Loop-Back Select - LLB Input - Channel 2
Please see description above for RLB_n</td></tr>
<tr><td>102</td><td>TEST</td><td>****</td><td>Factory Test Mode Input Pin
This pin must be connected to GND for normal operation.
NOTE: This input pin is internally pulled "Low".</td></tr>
</table>

GENERAL CONTROL PINS

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
62	$\overline{ICT}$	I	**In-Circuit Test Input:** Setting this pin "Low" causes all digital and analog outputs to go into a high-impedance state to allow for in-circuit testing. For normal operation, set this pin "High". ***NOTE:*** *This pin is internally pulled "High".*
70	HOST/$\overline{HW}$	I	**HOST/Hardware Mode Select:** Tie this pin "High" to configure the XRT75L03D in HOST mode. Tie this "Low" to configure in Hardware mode. When the XRT75L03D is configured in HOST mode, the states of many of the discrete input pins are controlled by internal register bits. ***NOTE:*** *This pin is internally pulled up.*

CONTROL AND ALARM INTERFACE

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
122	RXA	****	**External Resistor of 3.01K Ω ± 1%.** Should be connected between RxA and RxB for internal bias.
123	RXB	****	**External Resistor of 3.01K Ω ± 1%.** Should be connected between RxA and RxB for internal bias.

JITTER ATTENUATOR INTERFACE

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
44	JA0	I	**Jitter Attenuator Select 0:** In Hardware Mode, this pin along with pin 42 configures the Jitter Attenuator as shown in the table below.

JA0	JA1	Mode
0	0	FIFO Depth = 16 bits
0	1	FIFO Depth = 32 bits
1	0	SONET/SDH De-Sync Mode
1	1	Jitter Attenuator Disabled

NOTES:

1. *The setting of these input pins applies globally to all three (3) channels in the XRT75L03D.*
2. *This input pin is ignored and should be tied to GND if the XRT75L03D is configured to operate in the Host Mode.*

JITTER ATTENUATOR INTERFACE

42	JA1	I	**Jitter Attenuator Select 1:** Please see the Description above for JA0
43	JATx/$\overline{Rx}$	I	Jitter Attenuator in Transmit/Receive Path Select Input: This input pin is used to configure the Jitter Attenuator to operate in either the Transmit or Receive path within each of the three (3) channels of the XRT75L03D. "Low" - Configures the Jitter Attenuator within each channel to operate in the Receive Path. "High" - Configures the Jitter Attenuator within each channel to operate in the Transmit Path. ***NOTES:*** *1. The setting of this input pin applies globally to all three (3) channels of the XRT75L03D.* *2. This input pin is ignored and should be tied to GND if the XRT75L03D is configured to operate in the Host Mode or if the Jitter Attenuators are disabled.*

MICROPROCESSOR SERIAL INTERFACE - (HOST MODE)

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
69	SDO/RxMON	I/O	**Microprocessor Serial Interface - Serial Data Output:** This pin serially outputs the contents of a specified on-chip Command Register during READ Operations via the Microprocessor Serial Interface. The data which is output via this pin is updated upon the falling edge of the SCLK clock signal. This output pin will be tri-stated upon completion of a given READ operation. ***NOTE:*** *This pin functions as the RxMON input pin if the XRT75L03D has been configured to operate in the Hardware Mode.*
68	SDI/RxON	I	**Microprocessor Serial Interface - Serial Data Input:** This input pin functions as the Serial Data Input pin for the Microprocessor Serial Interface. In particular, this input pin will accept all of the following data in a serial manner during READ and WRITE operations with the Microprocessor Serial Interface. • The READ/WRITE indicator bit. • The Address Value of the Targeted Command Register for this particular READ or WRITE operation. • The Data to be written into the targeted Command Register for a given WRITE operation. All data that is applied to this input will be sampled upon the rising edge of the SCLK input clock signal. ***NOTE:*** *This input pin will function as the RxON input pin if the XRT75L03D has been configured to operate in the Hardware Mode.*

MICROPROCESSOR SERIAL INTERFACE - (HOST MODE)

PIN #	SIGNAL NAME	TYPE	DESCRIPTION
67	SClk/TCLKINV	I	**Microprocessor Serial Interface -Serial Clock Input:** This input pin functions as the Clock Source for the Microprocessor Serial Interface. Each time the user wishes to perform a READ or WRITE operate with the on-chip Command Registers via the Microprocessor Serial Interface, the user MUST do the following. • Assert the $\overline{CS}$ input pin by toggling it "Low", and • Provide 16 Clock Periods to this particular input pin for each READ and WRITE operation. The Microprocessor Serial Interface will sample any data residing upon the SDI input pin, upon the rising edge of this clock signal. Further, for READ operations, the Microprocessor Serial Interface will serially output the contents of a target Command Register upon the falling edge of this clock signal. ***NOTE:*** *The maximum frequency of this particular clock signal is 10MHz.*
66	$\overline{CS}$/RCLKINV	I	**Microprocessor Serial Interface - Chip Select Input:** This input pin should be pulled "Low" whenever a READ or WRITE operation is to be executed to the on-chip Command Registers, via the Microprocessor Serial Interface. This input pin should remain "Low" until the READ or WRITE operation has been completed. This input pin should be pulled "High" at all other times. ***NOTE:*** *If the XRT75L03D has been configured to operate in the Host Mode then this input pin will function as the RCLKINV input pin.*
71	$\overline{INT}$/LOSMUT	O	Microprocessor Serial Interface - Interrupt Request Output: If the XRT75L03D has been configured to operate in the Host Mode, then this pin becomes the Interrupt Request Output for the XRT75L03D. During normal conditions, this output pin will be pulled "High". However, if the user enables certain interrupts within the device, and if those conditions occur, then the XRT75L03D will request an interrupt from the Microprocessor by toggling this output pin "Low". ***NOTES:*** *1. If the XRT75L03D is configured to operate in the Hardware Mode, then this pin functions as the LOSMUT input pin.* *2. This pin will remain "Low" until the Interrupt has been served.*
101	$\overline{RESET}$	I	**Microprocessor Serial Interface - H/W RESET Input:** Pulsing this input "Low" causes the XRT75L03D to reset the contents of the on-chip Command Registers to their default values. As a consequence, the XRT75L03D will then also be operating in its default condition. For normal operation pull this input pin to a logic "High". ***NOTE:*** *This input pin is internally pulled high.*

POWER SUPPLY AND GROUND PINS

PIN #	PIN NAME	TYPE	DESCRIPTION
			RECEIVE ANALOG VDD
77 93 86	RxAVDD_0 RxAVDD_1 RxAVDD_2	****	
			TRANSMIT ANALOG VDD
39 128 23 121	TxAVDD_0 TxAVDD_1 TxAVDD_2 REFAVDD	****	
			JITTER ATTENUATOR ANALOG VDD
46 120 45	JAVDD_0 JAVDD_1 JAVDD_2	****	
			DIGITAL VDD
29 12 20 55 111 54 119 110	TxVDD_0 TxVDD_1 TxVDD_2 RxDVDD_0 RxDVDD_1 RxDVDD_2 JADVDD EXDVDD	****	

POWER SUPPLY AND GROUND PINS

PIN #	PIN NAME	TYPE	DESCRIPTION
		GROUNDS	
41	TxAGND_0	****	
126	TxAGND_1		
15	TxAGND_2		
80	RxAGND_0		
90	RxAGND_1		
89	RxAGND_2		
47	JAGND_0		
118	JAGND_1		
48	JAGND_2		
49	AGND_0		
116	AGND_1		
100	AGND_2		
124	REFGND		
27	TxGND_0		
14	TxGND_1		
18	TxGND_2		
59	RxDGND_0		
115	RxDGND_1		
50	RxDGND_2		
117	JADGND		
105	EXDGND		

XRT75L03D PIN LISTING IN NUMERICAL ORDER

PIN #	PIN NAME	TYPE	COMMENTS
1	TxON_1	I	This input pin is internally pulled 'High'.
2	TNDATA_1	I	
3	TPDATA_1	I	
4	TCLK_1	I	
5	MRING_1	I	
6	MTIP_1	I	
7	TAOS_1	I	**1.** Not Active while in Host Mode **2.** This input pin is internally pulled low.
8	TAOS_2	I	**1.** Not Active while in Host Mode **2.** This input pin is internally pulled low.
9	TxLEV_1	I	**1.** Not Active while in Host Mode **2.** This input pin is internally pulled low.
10	TxLEV_2	I	**1.** Not Active while in Host Mode **2.** This input pin is internally pulled low.
11	TTIP_1	O	
12	DVDD	***	
13	TRING_1	O	
14	TxAGND_1	***	
15	TxAGND_2	***	
16	MRING_2	I	
17	MTIP_2	I	
18	GND	***	
19	TRING_2	O	
20	TxVDD_2	***	
21	TTIP_2	O	
22	DMO_2	O	
23	TxAVDD_2	***	
24	TNDATA_2	I	
25	TPDATA_2	I	
26	TCLK_2	I	
27	TxGND_0	***	
28	TRING_0	O	
29	TxVDD_0	***	
30	TTIP_0	O	

XRT75L03D PIN LISTING IN NUMERICAL ORDER

PIN #	PIN NAME	TYPE	COMMENTS
31	MTIP_0	I	
32	MRING_0	I	
33	TNDATA_0	I	
34	TPDATA_0	I	
35	TAOS_0	I	Not Active while in Host Mode
36	TxLEV_0	I	**1.** Not Active while in Host Mode **2.** This input pin is internally pulled low.
37	TAOS_0	I	**1.** Not Active while in Host Mode **2.** This input pin is internally pulled low.
38	TxON_0	I	This input pin is internally pulled 'High'.
39	TxAVDD_0	***	
40	DMO_0	O	
41	TxAGND_0	***	
42	JA1	I	Not Active while in Host Mode
43	JATx/$\overline{Rx}$	I	Not Active while in Host Mode
44	JA0	I	Not Active while in Host Mode
45	JAVDD_2	***	
46	JAVDD_0	***	
47	JAGND_0	***	
48	JAGND_2	***	
49	AGND_0	***	
50	RxDGND_2	***	
51	RCLK_2	O	
52	RNEG_2/LCV_2	O	
53	RPOS_2	O	
54	RxDVDD_2	***	
55	RxDVDD_0	***	
56	RCLK_0	O	
57	RNEG_0/LCV_0	O	
58	RPOS_0	O	
59	RxDGND_0	***	
60	RLOS_0	O	
61	RLOL_0	O	
62	$\overline{ICT}$	I	This input pin is internally pulled low.

XRT75L03D PIN LISTING IN NUMERICAL ORDER

PIN #	PIN NAME	TYPE	COMMENTS
63	RLOS_2	O	
64	RLOL_2	O	
65	SR/$\overline{DR}$	I	**1.** Not Active while in Host Mode **2.** This input pin is internally pulled low.
66	RCLKINV ($\overline{CS}$)	I	
67	TCLKINV (SCLK)	I	
68	RxON (SDI)	I	This input pin is internally pulled low.
69	RxMON (SDO)	I/O	
70	HOST/$\overline{HW}$	I	This input pin is internally pulled low.
71	LOSMUT ($\overline{INT}$)	I/O	
72	STS-1/$\overline{DS3}$_0	I	**1.** Not Active while in Host Mode **2.** This input pin is internally pulled low.
73	LLB_0	I	Not Active while in Host Mode
74	RLB_0	I	Not Active while in Host Mode
75	REQEN_0	I	**1.** Not Active while in Host Mode **2.** This input pin is internally pulled low.
76	E3_0	I	**1.** Not Active while in Host Mode **2.** This input pin is internally pulled low.
77	RxAVDD_0	***	
78	RRING_0	I	
79	RTIP_0	I	
80	RxAGND_0	***	
81	STS-1/$\overline{DS3}$_2	I	**1.** Not Active while in Host Mode **2.** This input pin is internally pulled low.
82	LLB_2	I	Not Active while in Host Mode
83	RLB_2	I	Not Active while in Host Mode
84	REQEN_2	I	**1.** Not Active while in Host Mode **2.** This input pin is internally pulled low.
85	E3_2	I	**1.** Not Active while in Host Mode **2.** This input pin is internally pulled low.
86	RxAVDD_2	***	
87	RRING_2	I	
88	RTIP_2	I	
89	RxAGND_2	***	
90	RxAGND_1	***	
91	RTIP_1	I	

XRT75L03D PIN LISTING IN NUMERICAL ORDER

PIN #	PIN NAME	TYPE	COMMENTS
92	RRING_1	I	
93	RxAVDD_1	***	
94	E3_1	I	**1.** Not Active while in Host Mode **2.** This input pin is internally pulled low.
95	REQEN_1	I	**1.** Not Active while in Host Mode **2.** This input pin is internally pulled low.
96	RLB_1	I	Not Active while in Host Mode
97	LLB_1	I	Not Active while in Host Mode
98	STS-1/$\overline{\text{DS3}}$_1	I	**1.** Not Active while in Host Mode **2.** This input pin is internally pulled low.
99	LOSTHR	I	
100	AGND_2	***	
101	$\overline{\text{RESET}}$	I	This input pin is internally pulled high.
102	TEST	I	This input pin is internally pulled low.
103	RLOL_1	O	
104	RLOS_1	O	
105	EXDGND	***	
106	SFM_EN	I	This input pin is internally pulled low.
107	E3CLK/CLK_EN	I	
108	DS3CLK/ CLK_OUT	I/O	
109	STS-1CLK/12M	I	
110	EXDVDD	***	
111	RxDVDD_1	***	
112	RPOS_1	O	
113	RNEG_1/LCV_1	O	
114	RCLK_1	O	
115	RxDGND_1	***	
116	AGND_1	***	
117	JADGND	***	
118	JAGND_1	***	
119	JADVDD	***	
120	JADVDD_1	***	
121	REFAVDD	***	
122	RXA	***	

XRT75L03D PIN LISTING IN NUMERICAL ORDER

PIN #	PIN NAME	TYPE	COMMENTS
123	RXB	***	
124	REFGND	***	
125	TxON_2	I	This input pin is internally pulled 'High'.
126	TxAGND_1	***	
127	DMO_1	O	
128	TxAVDD_1	***	

1.0 ELECTRICAL CHARACTERISTICS

TABLE 1: ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	MIN	MAX	UNITS	COMMENTS
V_{DD}	Supply Voltage	-0.5	6.0	V	Note 1
V_{IN}	Input Voltage at any Pin	-0.5	5.5	V	Note 1
I_{IN}	Input current at any pin		100	mA	Note 1
S_{TEMP}	Storage Temperature	-65	150	^0C	Note 1
A_{TEMP}	Ambient Operating Temperature	-40	85	^0C	linear airflow 0 ft./min
Theta JA	Thermal Resistance		23	$^0C/W$	linear air flow 0ft/min (See Note 3 below)
M_{LEVL}	Exposure to Moisture	5		level	EIA/JEDEC JESD22-A112-A
ESD	ESD Rating	2000		V	Note 2

NOTES:

1. *Exposure to or operating near the Min or Max values for extended period may cause permanent failure and impair reliability of the device.*
2. *ESD testing method is per MIL-STD-883D,M-3015.7*
3. *With Linear Air flow of 200 ft/min, reduce Theta JA by 20%, Theta JC is unchanged.*

TABLE 2: DC ELECTRICAL CHARACTERISTICS:

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
DV_{DD}	Digital Supply Voltage	3.135	3.3	3.465	V
AV_{DD}	Analog Supply Voltage	3.135	3.3	3.465	V
I_{CC}	Supply current requirements		480	530	mA
P_{DD}	Power Dissipation		1.3	1.5	W
V_{IL}	Input Low Voltage			0.8	V
V_{IH}	Input High Voltage	2.0		5.5	V
V_{OL}	Output Low Voltage, I_{OUT} = - 4mA			0.4	V
V_{OH}	Output High Voltage, I_{OUT} = 4 mA	2.4			V
I_L	Input Leakage Current[1]			±10	µA
C_I	Input Capacitance			10	pF
C_L	Load Capacitance			10	pF

NOTES:

1. *Not applicable for pins with pull-up or pull-down resistors.*
2. *The Digital inputs and outputs are TTL 5V compliant.*

2.0 TIMING CHARACTERISTICS

FIGURE 3. TYPICAL INTERFACE BETWEEN TERMINAL EQUIPMENT AND THE XRT75L03D (DUAL-RAIL DATA)

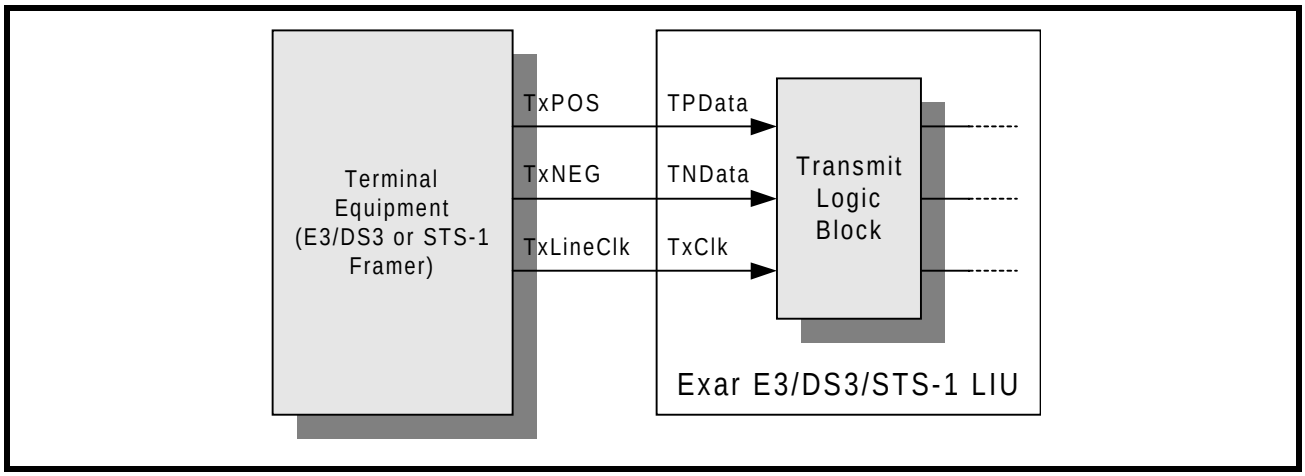
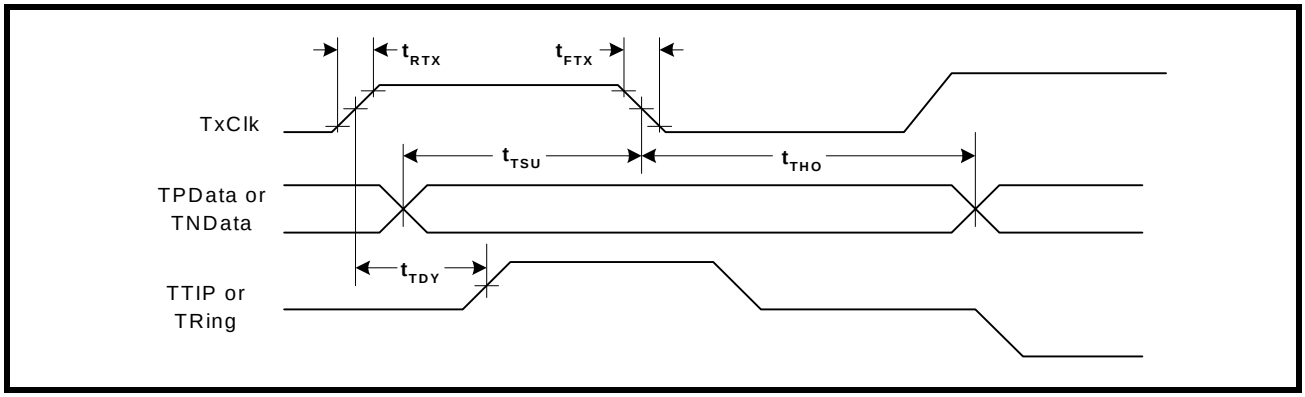
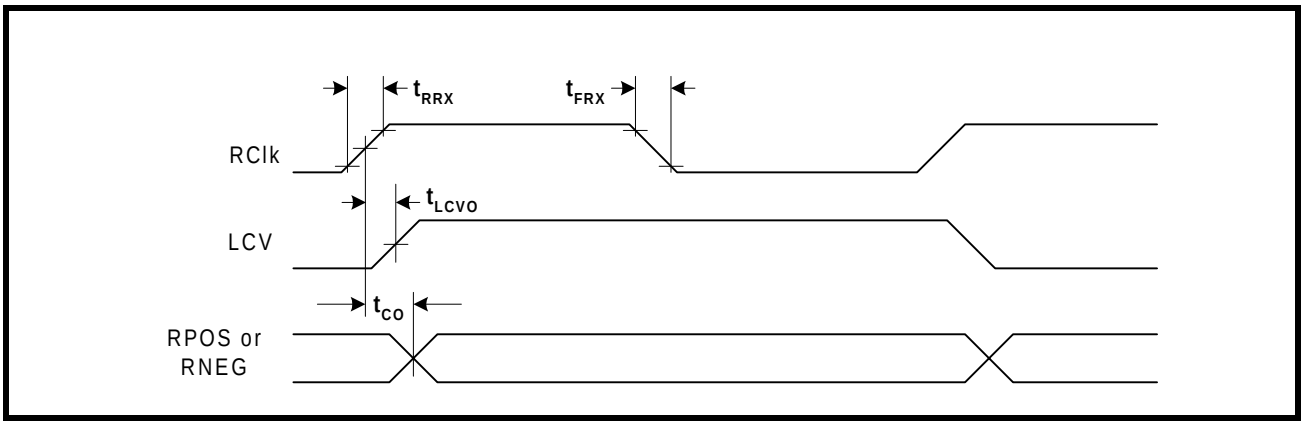


FIGURE 4. TRANSMITTER TERMINAL INPUT TIMING



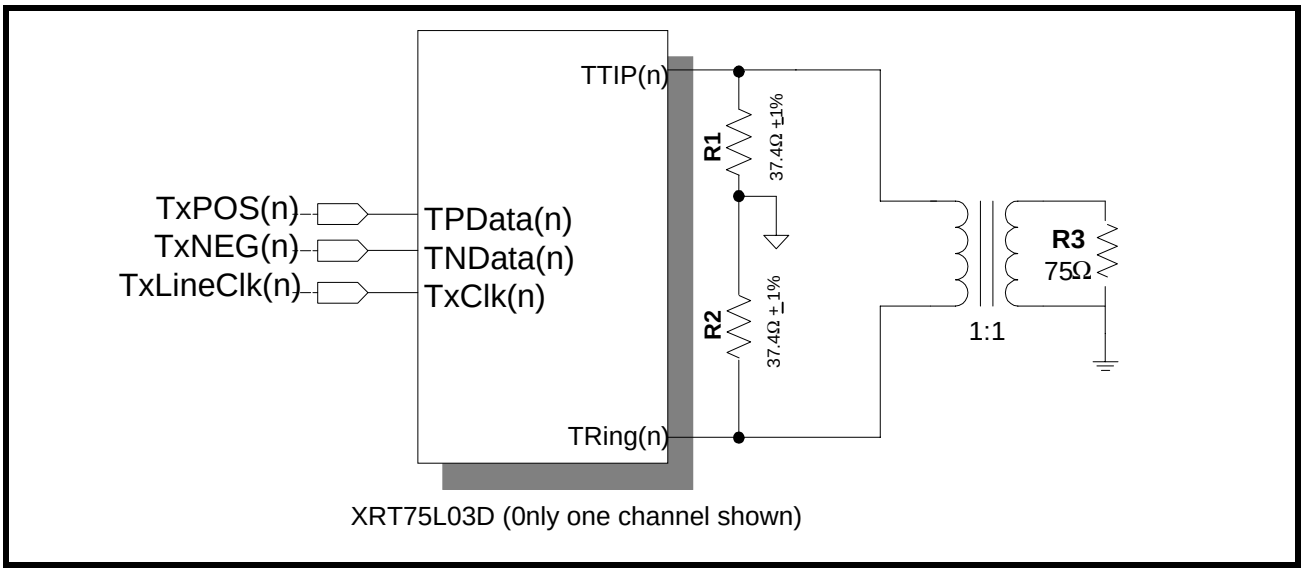
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
TxClk	Duty Cycle E3 DS3 STS-1	30	50 34.368 44.736 51.84	70	% MHz MHz MHz
t_{RTX}	TxClk Rise Time (10% to 90%)			4	ns
t_{FTX}	TxClk Fall Time (10% to 90%)			4	ns
t_{TSU}	TPData/TNData to TxClk falling set up time	3			ns
t_{THO}	TPData/TNData to TxClk falling hold time	3			ns
t_{TDY}	TTIP/TRing to TxClk rising propagation delay time		8		ns

FIGURE 5. RECEIVER DATA OUTPUT AND CODE VIOLATION TIMING



SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
RxClk	Duty Cycle	45	50	55	%
	E3		34.368		MHz
	DS3		44.736		MHz
	STS-1		51.84		MHz
t_{RRX}	RxClk rise time (10% o 90%)		2	4	ns
t_{FRX}	RxClk falling time (10% to 90%)		2	4	ns
t_{CO}	RxClk to RPOS/RNEG delay time			4	ns
t_{LCVO}	RxClk to rising edge of LCV output delay		2.5		ns

FIGURE 6. TRANSMIT PULSE AMPLITUDE TEST CIRCUIT FOR E3, DS3 AND STS-1 RATES



3.0 LINE SIDE CHARACTERISTICS:

3.1 E3 line side parameters:

The XRT75L03D line output at the transformer output meets the pulse shape specified in ITU-T G.703 for 34.368 Mbits/s operation. The pulse mask as specified in ITU-T G.703 for 34.368 Mbits/s is shown in Figure 7.

FIGURE 7. PULSE MASK FOR E3 (34.368 MBITS/S) INTERFACE AS PER ITU-T G.703

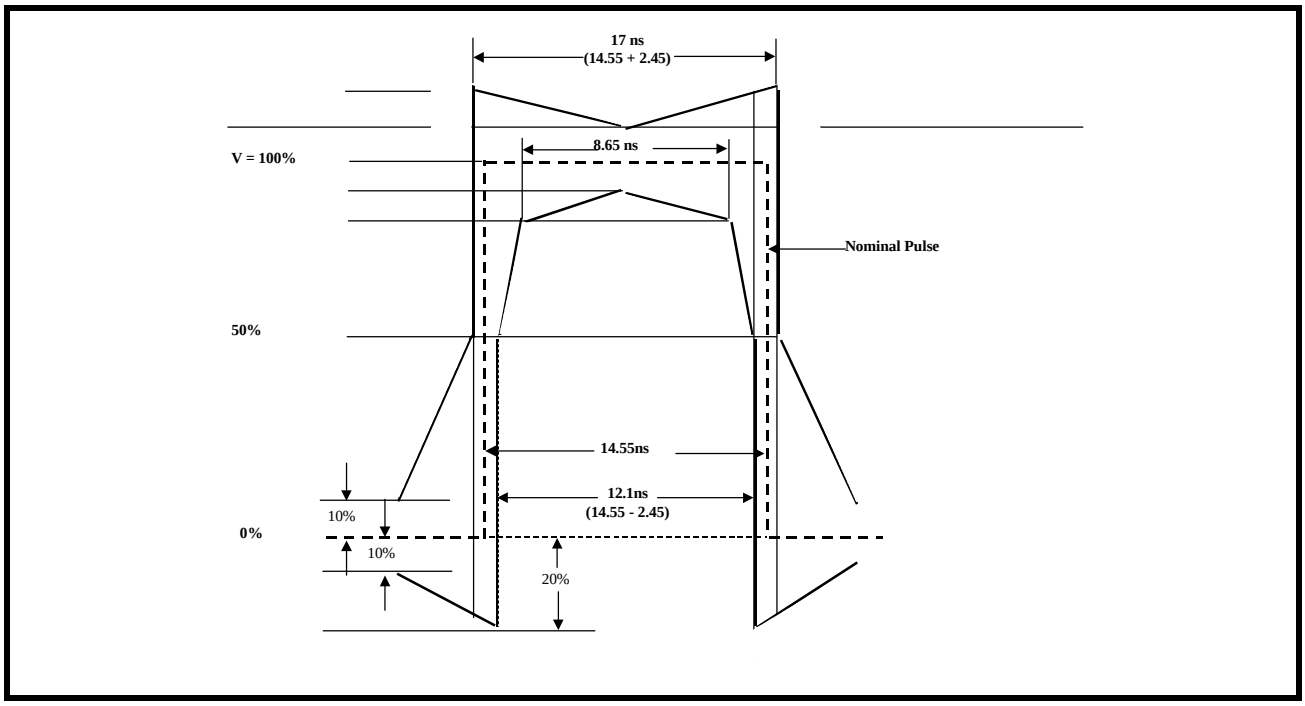


TABLE 3: E3 TRANSMITTER LINE SIDE OUTPUT AND RECEIVER LINE SIDE INPUT SPECIFICATIONS

PARAMETER	MIN	TYP	MAX	UNITS
TRANSMITTER LINE SIDE OUTPUT CHARACTERISTICS				
Transmit Output Pulse Amplitude (Measured at secondary of the transformer)	0.9	1.0	1.1	V_{pk}
Transmit Output Pulse Amplitude Ratio	0.95	1.00	1.05	
Transmit Output Pulse Width	12.5	14.55	16.5	ns
Transmit Intrinsic Jitter (without Jitter Attenuator in theTransmit path)		0.01	0.015	UI_{PP}
Transmit Intrinsic Jitter (with Jitter Attenuator in the Transmit path)		0.02	0.03	UI_{PP}
RECEIVER LINE SIDE INPUT CHARACTERISTICS				
Receiver Sensitivity (length of cable)	900	1200		feet
Interference Margin	-20	-14		dB
Jitter Tolerance @ Jitter Frequency 800KHz	0.15	0.28		UI_{PP}
Signal level to Declare Loss of Signal			-35	dB
Signal Level to Clear Loss of Signal	-15			dB
Occurence of LOS to LOS Declaration Time	10		255	UI
Termination of LOS to LOS Clearance Time	10		255	UI

NOTE: *The above values are at TA = 25^0C and V_{DD} = 3.3 V± 5%.*

FIGURE 8. BELLCORE GR-253 CORE TRANSMIT OUTPUT PULSE TEMPLATE FOR SONET STS-1 APPLICATIONS

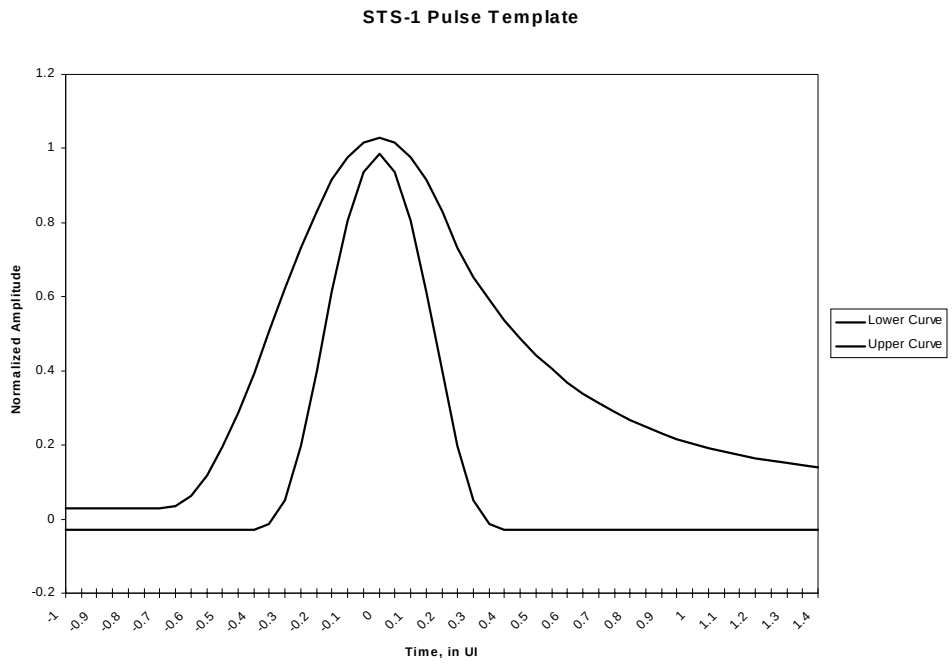


TABLE 4: STS-1 PULSE MASK EQUATIONS

TIME IN UNIT INTERVALS	NORMALIZED AMPLITUDE
LOWER CURVE	
$-0.85 \leq T \leq -0.38$	- 0.03
$-0.38 \leq T \leq 0.36$	$0.5\left[1 + \sin\left\{\frac{\pi}{2}\left(1 + \frac{T}{0.18}\right)\right\}\right] - 0.03$
$0.36 \leq T \leq 1.4$	- 0.03
UPPER CURVE	
$-0.85 \leq T \leq -0.68$	0.03
$-0.68 \leq T \leq 0.26$	$0.5\left[1 + \sin\left\{\frac{\pi}{2}\left(1 + \frac{T}{0.34}\right)\right\}\right] + 0.03$
$0.26 \leq T \leq 1.4$	$0.1 + 0.61 \times e^{-2.4[T-0.26]}$

TABLE 5: STS-1 TRANSMITTER LINE SIDE OUTPUT AND RECEIVER LINE SIDE INPUT SPECIFICATIONS (GR-253)

PARAMETER	MIN	TYP	MAX	UNITS
TRANSMITTER LINE SIDE OUTPUT CHARACTERISTICS				
Transmit Output Pulse Amplitude (measured with TxLEV = 0)	0.65	0.75	0.9	V_{pk}
Transmit Output Pulse Amplitude (measured with TxLEV = 1)	0.9	1.0	1.1	V_{pk}
Transmit Output Pulse Width	8.6	9.65	10.6	ns
Transmit Output Pulse Amplitude Ratio	0.9	1.0	1.1	
Transmit Intrinsic Jitter (without Jitter Attenuator in Transmit path)		0.01	0.015	UI_{pp}
Transmit Intrinsic Jitter (with Jitter Attenuator in Transmit path)		0.02	0.04	UI_{pp}
RECEIVER LINE SIDE INPUT CHARACTERISTICS				
Receiver Sensitivity (length of cable)	900	1100		feet
Jitter Tolerance @ Jitter Frequency 400 KHz	0.15			UI_{pp}
Signal Level to Declare Loss of Signal	Refer to Table 10			
Signal Level to Clear Loss of Signal	Refer to Table 10			

NOTE: *The above values are at TA = 25^0C and V_{DD} = 3.3 V ± 5%.*

FIGURE 9. TRANSMIT OUPUT PULSE TEMPLATE FOR DS3 AS PER BELLCORE GR-499

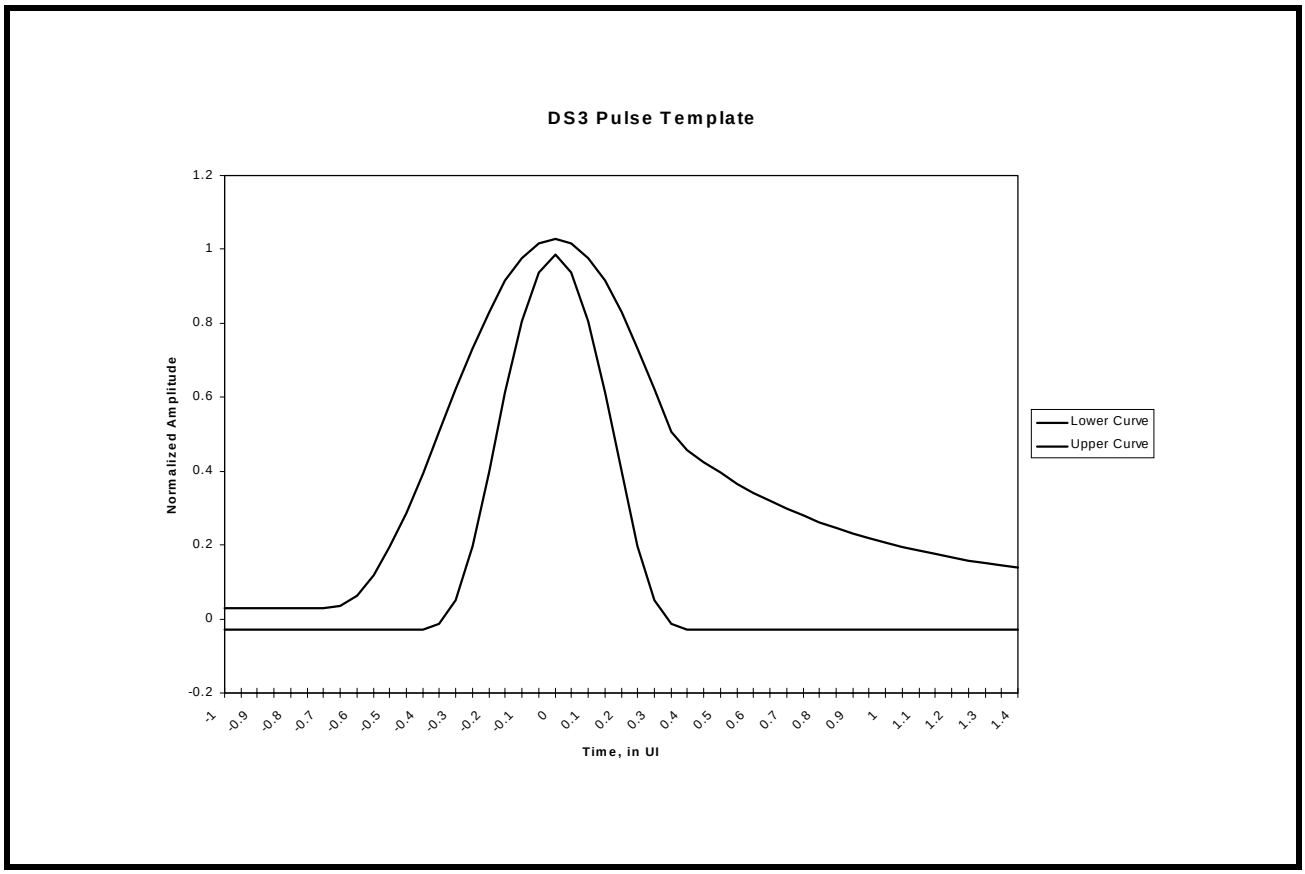


TABLE 6: DS3 PULSE MASK EQUATIONS

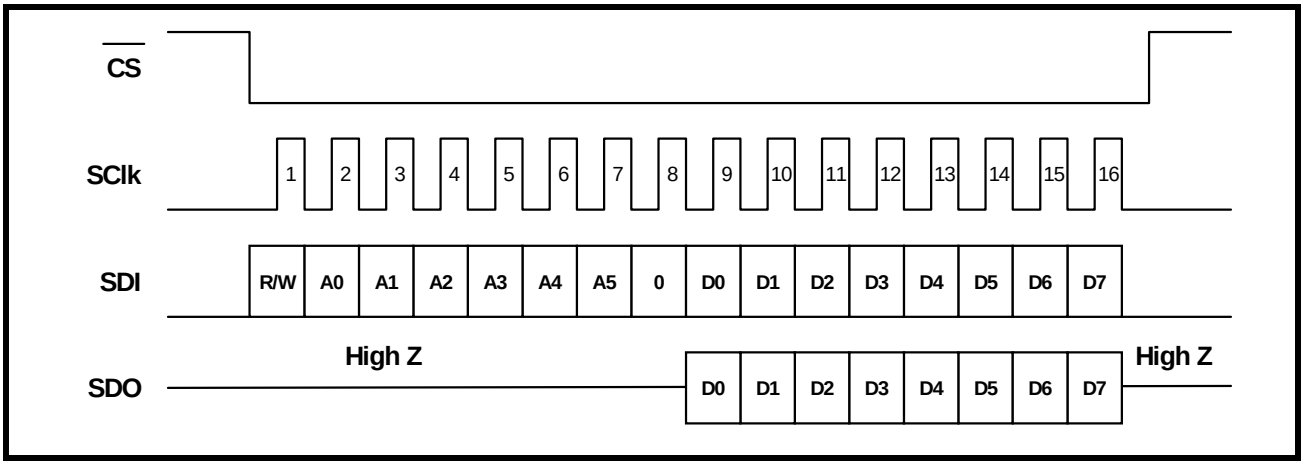
TIME IN UNIT INTERVALS	NORMALIZED AMPLITUDE
LOWER CURVE	
$-0.85 \leq T \leq -0.36$	- 0.03
$-0.36 \leq T \leq 0.36$	$0.5\left[1 + \sin\left\{\frac{\pi}{2}\left(1 + \frac{T}{0.18}\right)\right\}\right] - 0.03$
$0.36 \leq T \leq 1.4$	- 0.03
UPPER CURVE	
$-0.85 \leq T \leq -0.68$	0.03
$-0.68 \leq T \leq 0.36$	$0.5\left[1 + \sin\left\{\frac{\pi}{2}\left(1 + \frac{T}{0.34}\right)\right\}\right] + 0.03$
$0.36 \leq T \leq 1.4$	$0.08 + 0.407 \times e^{-1.84[T-0.36]}$

TABLE 7: DS3 TRANSMITTER LINE SIDE OUTPUT AND RECEIVER LINE SIDE INPUT SPECIFICATIONS (GR-499)

PARAMETER	MIN	TYP	MAX	UNITS
TRANSMITTER LINE SIDE OUTPUT CHARACTERISTICS				
Transmit Output Pulse Amplitude (measured with TxLEV = 0)	0.65	0.75	0.85	V_{pk}
Transmit Output Pulse Amplitude (measured with TxLEV = 1)	0.9	1.0	1.1	V_{pk}
Transmit Output Pulse Width	10.10	11.18	12.28	ns
Transmit Output Pulse Amplitude Ratio	0.9	1.0	1.1	
Transmit Intrinsic Jitter (without Jitter Attenuator in Transmit path)		0.01	0.015	UI_{pp}
Transmit Intrinsic Jitter (withJitter Attenuator in Transmit path)		0.02	0.04	UI_{pp}
RECEIVER LINE SIDE INPUT CHARACTERISTICS				
Receiver Sensitivity (length of cable)	900	1100		feet
Jitter Tolerance @ 400 KHz (Cat II)	0.15			UI_{pp}
Signal Level to Declare Loss of Signal	Refer to Table 10			
Signal Level to Clear Loss of Signal	Refer to Table 10			

NOTE: *The above values are at TA = 25^0C and V_{DD} = 3.3V ± 5%.*

FIGURE 10. MICROPROCESSOR SERIAL INTERFACE STRUCTURE



NOTE: *If the R/W bit is set to "1", then this denotes a "READ" operation with the Microprocessor Serial Interface. Conversely, if the R/W bit is set to "0", then this denotes a "WRITE" operation.*

FIGURE 11. TIMING DIAGRAM FOR THE MICROPROCESSOR SERIAL INTERFACE

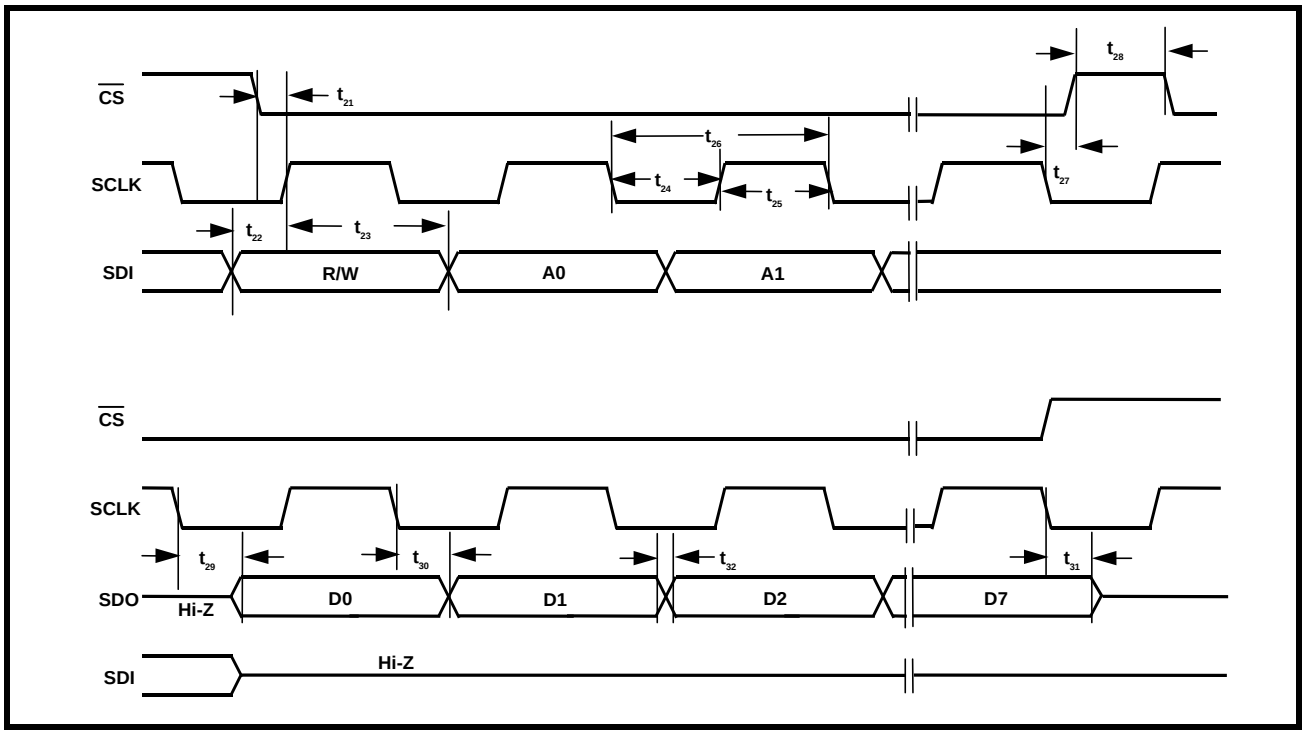


TABLE 8: MICROPROCESSOR SERIAL INTERFACE TIMINGS ($T_A = 25^0C$, V_{DD}=3.3V± 5% AND LOAD = 10PF)

SYMBOL	PARAMETER	MIN.	TYP.	MAX	UNITS
t_{21}	$\overline{CS}$ Low to Rising Edge of SClk	5			ns
t_{22}	SDI to Rising Edge of SClk	5			ns
t_{23}	SDI to Rising Edge of SClk Hold Time	5			ns
t_{24}	SClk "Low" Time	50			ns
t_{25}	SClk "High" Time	50			ns
t_{26}	SClk Period	100			ns
t_{27}	Falling Edge of SClk to rising edge of $\overline{CS}$	0			ns
t_{28}	$\overline{CS}$ Inactive Time	50			ns
t_{29}	Falling Edge of SClk to SDO Valid Time			20	ns
t_{30}	Falling Edge of SClk to SDO Invalid Time			10	ns
t_{31}	Rising edge of $\overline{CS}$ to High Z			25	ns
t_{32}	Rise/Fall time of SDO Output			5	ns

FUNCTIONAL DESCRIPTION:

Figure 1 shows the functional block diagram of the device. Each channel can be independently configured either by Hardware Mode or by Host Mode to support E3, DS3 or STS-1 modes. A detailed operation of each section is described below.

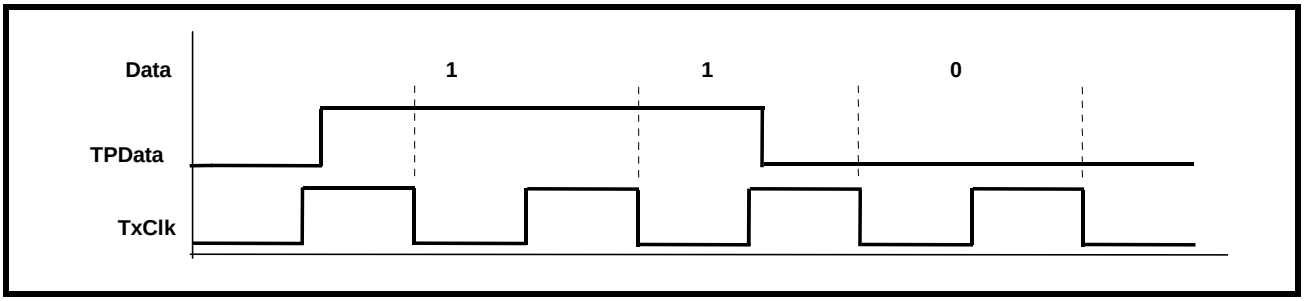
Each channel consists of the following functional blocks:

4.0 THE TRANSMITTER SECTION:

The Transmitter Section, within each Channel, accepts TTL/CMOS level signals from the Terminal Equipment in selectable data formats.

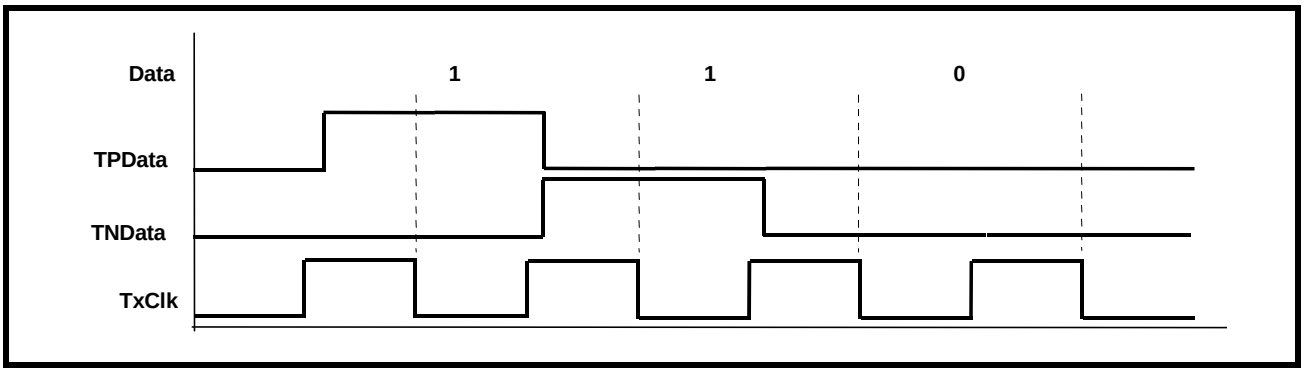
- Convert the CMOS level B3ZS or HDB3 encoded data into pulses with shapes that are compliant with the various industry standard pulse template requirements. Figures 7, 8 and 9 illustrate the pulse template requirements.
- Encode the un-encoded NRZ data into either B3ZS format for (DS3 or STS-1) or HDB3 format (for E3) and convert to pulses with shapes and width that are compliant with industry standard pulse template requirements. Figures 7, 8 and 9 illustrate the pulse template requirements.
- In Single-Rail or un-encoded Non-Return-to-Zero (NRZ) mode, data is input via TPData_n pins while TNData_n pins must be grounded. The NRZ or Single-Rail mode is selected when the SR/$\overline{DR}$ input pin is “High” (in Hardware Mode) or bit 0 of channel control register is “1” (in Host Mode). Figure 12 illustrates the Single-Rail or NRZ format.

FIGURE 12. SINGLE-RAIL OR NRZ DATA FORMAT (ENCODER AND DECODER ARE ENABLED)



- In Dual-Rail mode, data is input via TPData_n and TNData_n pins. TPData_n contains positive data and TNData_n contains negative data. The SR/$\overline{DR}$ input pin = “Low” (in Hardware Mode) or bit 0 of channel register = “0” (in Host Mode) enables the Dual-Rail mode. Figure 13 illustrates the Dual-Rail data format.

FIGURE 13. DUAL-RAIL DATA FORMAT (ENCODER AND DECODER ARE DISABLED)



4.1 *TRANSMIT CLOCK:*

The Transmit Clock applied via TxClk_n pins, for the selected data rate (for E3 = 34.368 MHz, DS3 = 44.736 MHz or STS-1 = 51.84 MHz), is duty cycle corrected by the internal PLL circuit to provide a 50% duty cycle clock to the pulse shaping circuit. This allows a 30% to 70% duty cycle Transmit Clock to be supplied.

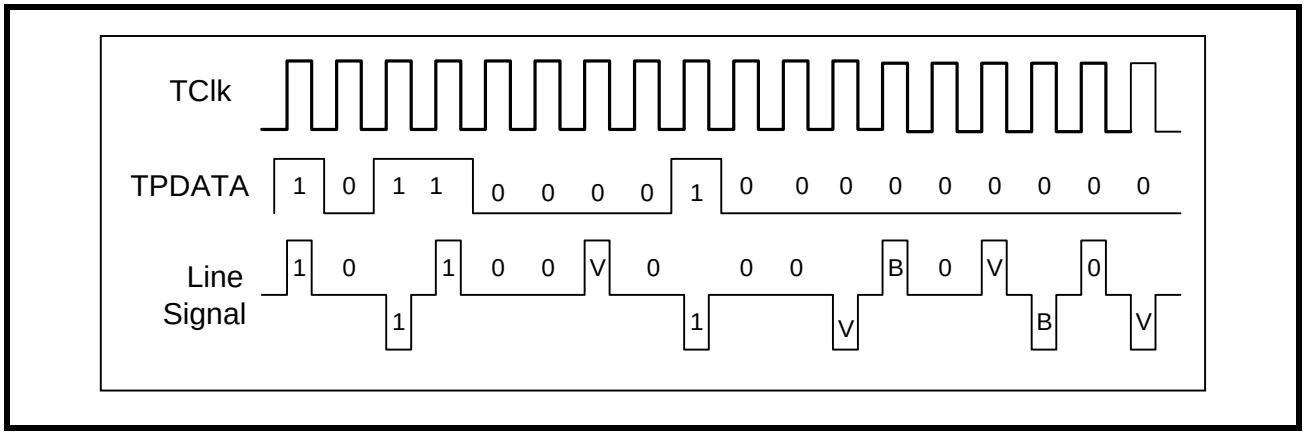
4.2 *B3ZS/HDB3 ENCODER:*

When the Single-Rail (NRZ) data format is selected, the Encoder Block encodes the data into either B3ZS format (for either DS3 or STS-1) or HDB3 format (for E3).

4.2.1 B3ZS Encoding:

An example of B3ZS encoding is shown in Figure 14. If the encoder detects an occurrence of three consecutive zeros in the data stream, it is replaced with either B0V or 00V, where 'B' refers to Bipolar pulse that is compliant with the Alternating polarity requirement of the AMI (Alternate Mark Inversion) line code and 'V' refers to a Bipolar Violation (e.g., a bipolar pulse that violates the AMI line code). The substitution of B0V or 00V is made so that an odd number of bipolar pulses exist between any two consecutive violation (V) pulses. This avoids the introduction of a DC component into the line signal.

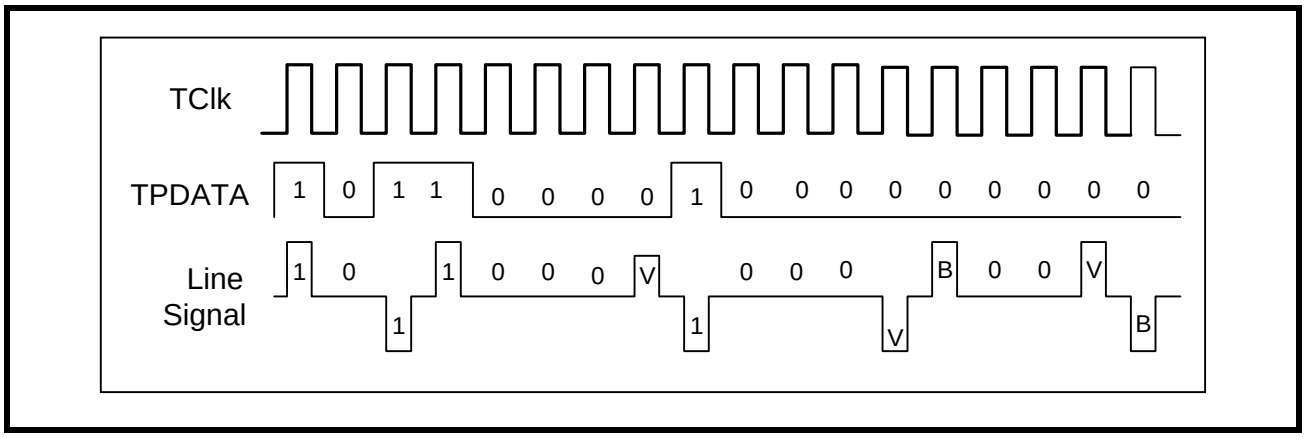
FIGURE 14. B3ZS ENCODING FORMAT



4.2.2 HDB3 Encoding:

An example of the HDB3 encoding is shown in Figure 15. If the HDB3 encoder detects an occurrence of four consecutive zeros in the data stream, then the four zeros are substituted with either 000V or B00V pattern. The substitution code is made in such a way that an odd number of bipolar (B) pulses exist between any consecutive V pulses. This avoids the introduction of DC component into the analog signal.

FIGURE 15. HDB3 ENCODING FORMAT



NOTES:

1. *When Dual-Rail data format is selected, the B3ZS/HDB3 Encoder is automatically disabled.*
2. *In Dual-Rail format, the Bipolar Violations in the incoming data stream is converted to valid data pulses.*
3. *Encoder and Decoder is enabled only in Single-Rail mode.*

4.3 *TRANSMIT PULSE SHAPER:*

The Transmit Pulse Shaper converts the B3ZS encoded digital pulses into a single analog Alternate Mark Inversion (AMI) pulse that meet the industry standard mask template requirements for STS-1 and DS3. See Figures 8 and 9.

For E3 mode, the pulse shaper converts the HDB3 encoded pulses into a single full amplitude square shaped pulse with very little slope. This is illustrated in Figure 7.

The Pulse Shaper Block also includes a Transmit Build Out Circuit, which can either be disabled or enabled by setting the TxLEV_n input pin “High” or “Low” (in Hardware Mode) or setting the TxLEV_n bit to “1” or “0” in the control register (in Host Mode).

For DS3/STS-1 rates, the Transmit Build Out Circuit is used to shape the transmit waveform that ensures that transmit pulse template requirements are met at the Cross-Connect system. The distance between the transmitter output and the Cross-Connect system can be between 0 to 450 feet.

For E3 rate, since the output pulse template is measured at the secondary of the transformer and since there is no Cross-Connect system pulse template requirements, the Transmit Build Out Circuit is always disabled.

4.3.1 Guidelines for using Transmit Build Out Circuit:

If the distance between the transmitter and the DSX3 or STSX-1, Cross-Connect system, is less than 225 feet, enable the Transmit Build Out Circuit by setting the TxLEV_n input pin “Low” (in Hardware Mode) or setting the TxLEV_n control bit to “0” (in Host Mode).

If the distance between the transmitter and the DSX3 or STSX-1 is greater than 225 feet, disable the Transmit Build Out Circuit.

4.3.2 Interfacing to the line:

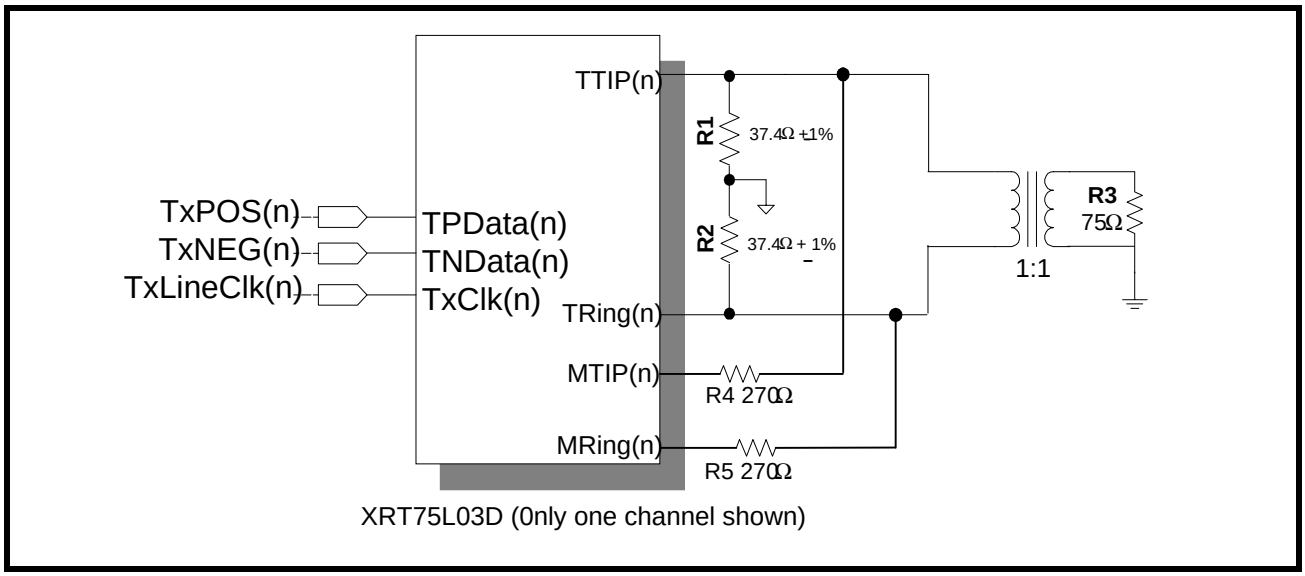
The differential line driver increases the transmit waveform to appropriate level and drives into the 75Ω load as shown in Figure 6.

4.4 *Transmit Drive Monitor:*

This feature is used for monitoring the transmit line for occurrence of fault conditions such as a short circuit on the line or a defective line driver.

To activate this function, connect MTIP_n pins to the TTIP_n lines via a 270 Ω resistor and MRing_n pins to TRing_n lines via 270 Ω resistor as shown in Figure 16.

FIGURE 16. TRANSMIT DRIVER MONITOR SET-UP.



When the MTIP_n and MRing_n are connected to the TTIP_n and TRing_n lines, the drive monitor circuit monitors the line for transitions. The DMO_n (Drive Monitor Output) will be asserted “Low” as long as the transitions on the line are detected via MTIP_n and MRing_n.

If no transitions on the line are detected for 128 ± 32 TxClk_n periods, the DMO_n output toggles “High” and when the transitions are detected again, DMO_n toggles “Low”.

NOTE: *The Drive Monitor Circuit is only for diagnostic purpose and does not have to be used to operate the transmitter.*

4.5 *Transmitter Section On/Off:*

The transmitter section of each channel can either be turned on or off. To turn on the transmitter, set the input pin TxON_n to “High” (in Hardware Mode) or write a “1” to the TxON_n control bits (in Host Mode) and TxON_n pins tied “High”.

When the transmitter is turned off, TTIP_n and TRing_n are tri-stated.

NOTES:

1. *This feature provides support for Redundancy.*
2. *If the XRT75L03D is configured in Host mode, to permit a system designed for redundancy to quickly shut-off the defective line card and turn on the back-up line card, writing a “1” to the TxON_n control bits transfers the control to TxON_n pins.*

5.0 THE RECEIVER SECTION:

This section describes the detailed operation of the various blocks in the receiver. The receiver recovers the TTL/CMOS level data from the incoming bipolar B3ZS or HDB3 encoded input pulses.

5.1 *AGC/Equalizer:*

The Adaptive Gain Control circuit amplifies the incoming analog signal and compensates for the various flat losses and also for the loss at one-half symbol rate. The AGC has a dynamic range of 30 dB.

The Equalizer restores the integrity of the signal and compensates for the frequency dependent attenuation of up to 900 feet of coaxial cable (1300 feet for E3). The Equalizer also boosts the high frequency content of the

signal to reduce Inter-Symbol Interference (ISI) so that the slicer slices the signal at 50% of peak voltage to generate Positive and Negative data.

The Equalizer can either be “IN” or “OUT” by setting the REQEN_n pin “High” or “Low” (in Hardware Mode) or setting the REQEN_n control bit to “1” or “0” (in Host Mode).

RECOMMENDATIONS FOR EQUALIZER SETTINGS:

The Equalizer has two gain settings to provide optimum equalization. In the case of normally shaped DS3/ STS-1 pulses (pulses that meet the template requirements) that has been driven through 0 to 900 feet of cable, the Equalizer can be left “IN” by setting the REQEN_n pin to “High” (in Hardware Mode) or setting the REQEN_n control bit to “1” (in Host Mode).

However, for square-shaped pulses such as E3 or for DS3/STS-1 high pulses (that does not meet the pulse template requirements), it is recommended that the Equalizer be left “OUT” for cable length less than 300 feet by setting the REQEN_n pin “Low” (in Hardware Mode) or by setting the REQEN_n control bit to “0” (in Host Mode).This would help to prevent over-equalization of the signal and thus optimize the performance in terms of better jitter transfer characteristics.

NOTE: The results of extensive testing indicates that even when the Equalizer was left “IN” (REQEN_n = “HIGH”), regardless of the cable length, the integrity of the E3 signal was restored properly over 0 to 12 dB cable loss at Industrial Temperature.

The Equalizer also contain an additional 20 dB gain stage to provide the line monitoring capability of the resistively attenuated signals which may have 20dB flat loss. This capability can be turned on by writing a “1” to the RxMON_n bits in the control register or by setting the RxMON pin (pin 69) “High”.

5.1.1 Interference Tolerance:

For E3 mode, ITU-T G.703 Recommendation specifies that the receiver be able to recover error-free clock and data in the presence of a sinusoidal interfering tone signal. For DS3 and STS-1 modes, the same recommendation is being used. Figure 17 shows the configuration to test the interference margin for DS3/ STS1. Figure 18 shows the set up for E3.

FIGURE 17. INTERFERENCE MARGIN TEST SET UP FOR DS3/STS-1

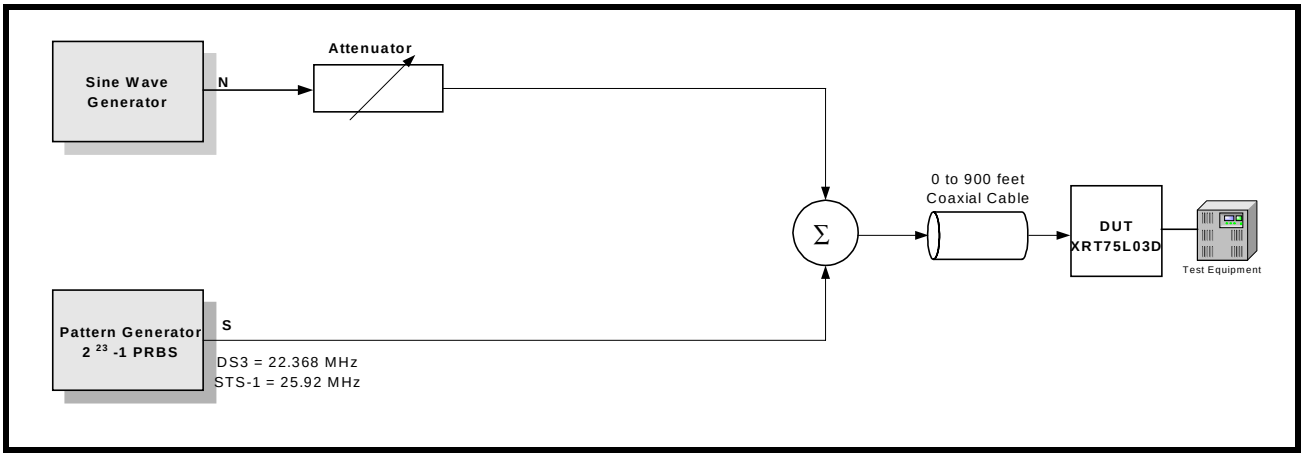


FIGURE 18. INTERFERENCE MARGIN TEST SET UP FOR E3.

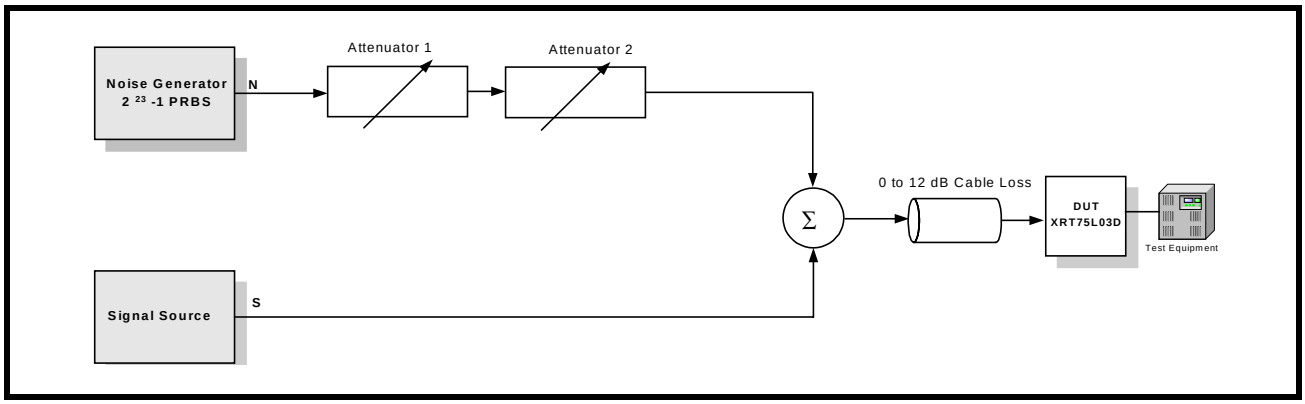


TABLE 9: INTERFERENCE MARGIN TEST RESULTS

MODE	CABLE LENGTH (ATTENUATION)	INTERFERENCE TOLERANCE
E3	0 dB	Equalizer "IN"
		-17 dB
	12 dB	-14 gB
DS3	0 feet	-15 dB
	225 feet	-15 dB
	450 feet	-14 dB
STS-1	0 feet	-15 dB
	225 feet	-14 dB
	450 feet	-14 dB

5.2 *Clock and Data Recovery:*

The Clock and Data Recovery Circuit extracts the embedded clock, RxClk_n from the sliced digital data stream and provides the retimed data to the B3ZS (HDB3) decoder.

The Clock Recovery PLL can be in one of the following two modes:

TRAINING MODE:

In the absence of input signals at RTIP_n and RRing_n pins, or when the frequency difference between the recovered line clock signal and the reference clock applied on the ExClk_n input pins exceed 0.5%, a Loss of Lock condition is declared by toggling RLOL_n output pin "High" (in Hardware Mode) or setting the RLOL_n bit to "1" in the control registers (in Host Mode). Also, the clock output on the RxClk_n pins are the same as the reference clock applied on ExClk_n pins.

DATA/CLOCK RECOVERY MODE:

In the presence of input line signals on the RTIP_n and RRing_n input pins and when the frequency difference between the recovered clock signal and the reference clock signal is less than 0.5%, the clock that is output on the RxClk_n out pins is the Recovered Clock signal.

5.3 *B3ZS/HDB3 Decoder:*

The decoder block takes the output from clock and data recovery block and decodes the B3ZS (for DS3 or STS-1) or HDB3 (for E3) encoded line signal and detects any coding errors or excessive zeros in the data stream.

Whenever the input signal violates the B3ZS or HDB3 coding sequence for bipolar violation or contains three (for B3ZS) or four (for HDB3) or more consecutive zeros, an active “High” pulse is generated on the RLCV_n output pins to indicate line code violation.

NOTE: In Dual-Rail mode, the decoder is bypassed.

5.4 *LOS (Loss of Signal) Detector:*

5.4.1 DS3/STS-1 LOS Condition:

A Digital Loss of SIgnal (DLOS) condition occurs when a string of 175 ± 75 consecutive zeros occur on the line. When the DLOS condition occurs, the DLOS_n bit is set to “1” in the status control register. DLOS condition is cleared when the detected average pulse density is greater than 33% for 175 ± 75 pulses.

Analog Loss of Signal (ALOS) condition occurs when the amplitude of the incoming line signal is below the threshold as shown in the Table 10.The status of the ALOS condition is reflected in the ALOS_n status control register.

RLOS is the logical OR of the DLOS and ALOS states. When the RLOS condition occurs the RLOS_n output pin is toggled “High” and the RLOS_n bit is set to “1” in the status control register.

TABLE 10: THE ALOS (ANALOG LOS) DECLARATION AND CLEARANCE THRESHOLDS FOR A GIVEN SETTING OF LOSTHR AND REQEN (DS3 AND STS-1 APPLICATIONS)

APPLICATION	REQEN SETTING	LOSTHR SETTING	SIGNAL LEVEL TO DECLARE ALOS DEFECT	SIGNAL LEVEL TO CLEAR ALOS DEFECT
DS3	0	0	< 75mVpk	> 130mVpk
	1	0	< 45mVpk	> 60mVpk
	0	1	< 120mVpk	> 45mVpk
	1	1	< 55mVpk	> 180mVpk
STS-1	0	0	< 120mVpk	> 170mVpk
	1	0	< 50mVpk	> 75mVpk
	0	1	< 125mVpk	> 205mVpk
	1	1	< 55mVpk	> 90mVpk

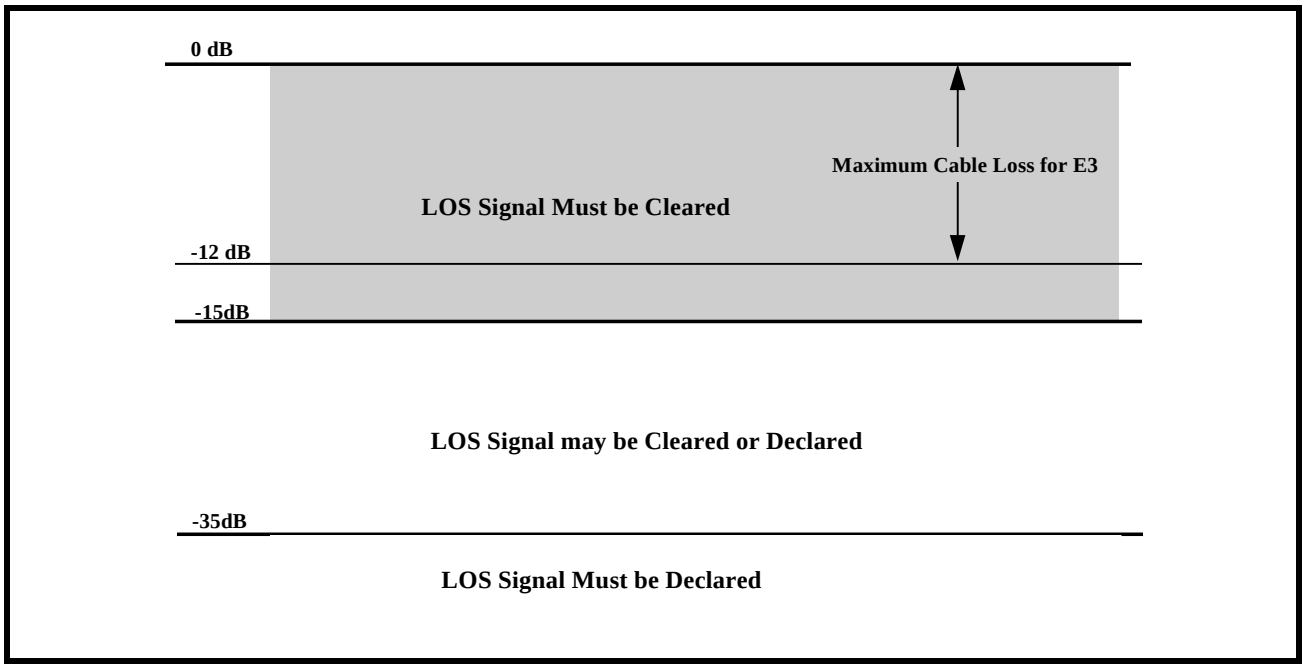
DISABLING ALOS/DLOS DETECTION:

For debugging purposes it is useful to disable the ALOS and/or DLOS detection. Writing a “1” to both ALOSDIS_n and DLOSDIS_n bits disables the LOS detection on a per channel basis.

5.4.2 E3 LOS Condition:

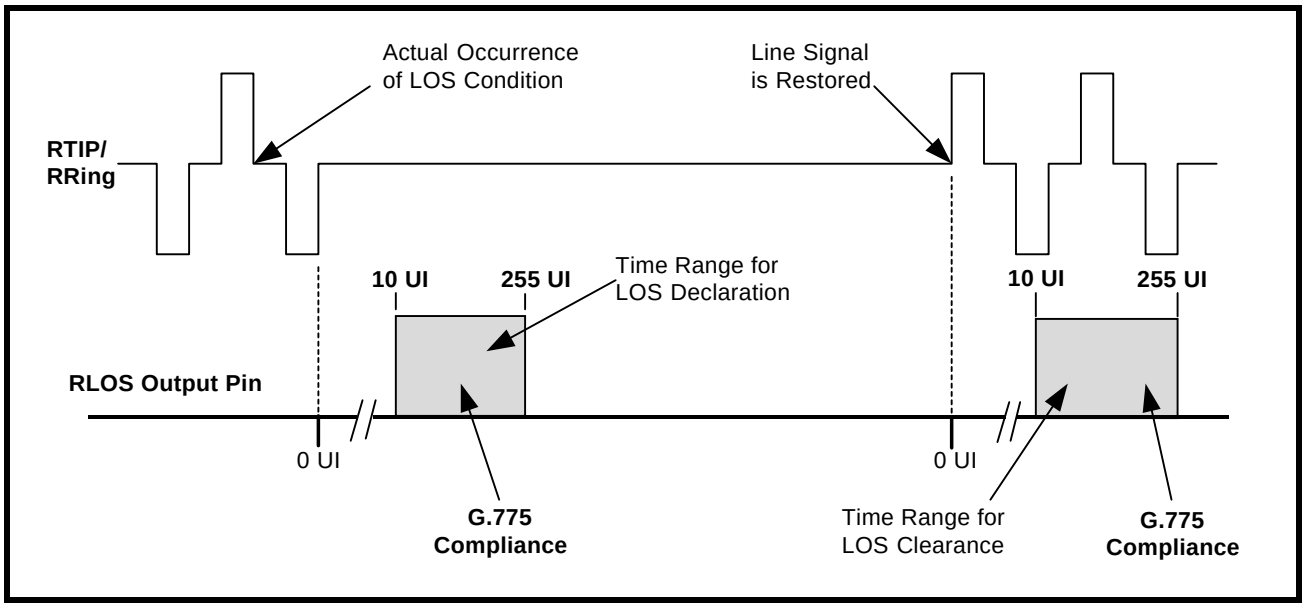
If the level of incoming line signal drops below the threshold as described in the ITU-T G.775 standard, the LOS condition is detected. Loss of signal level is defined to be between 15 and 35 dB below the normal level. If the signal drops below 35 dB for 10 to 255 consecutive pulse periods, LOS condition is declared. This is illustrated in Figure 19.

FIGURE 19. LOSS OF SIGNAL DEFINITION FOR E3 AS PER ITU-T G.775



As defined in ITU-T G.775, an LOS condition is also declared between 10 and 255 UI (or E3 bit periods) after the actual time the LOS condition has occurred. The LOS condition is cleared within 10 to 255 UI after restoration of the incoming line signal. Figure 20 shows the LOS declaration and clearance conditions.

FIGURE 20. LOSS OF SIGNAL DEFINITION FOR E3 AS PER ITU-T G.775.



5.4.3 Muting the Recovered Data with LOS condition:

When the LOS condition is declared, the clock recovery circuit locks into the reference clock applied to the ExClk_n pin and output this clock on the RxClk_n output.In Single Frequency Mode (SFM), the clock recovery locks into the rate clock generated and output this clock on the RxClk_n pins. The data on the RPOS_n and RNEG_n pins can be forced to zero by pulling the LOSMUT pin “High” (in Hardware Mode) or by setting the LOSMUT_n bits in the individual channel control register to “1” (in Host Mode).

NOTE: When the LOS condition is cleared, the recovered data is output on RPOS_n and RNEG_n pins.

6.0 JITTER:

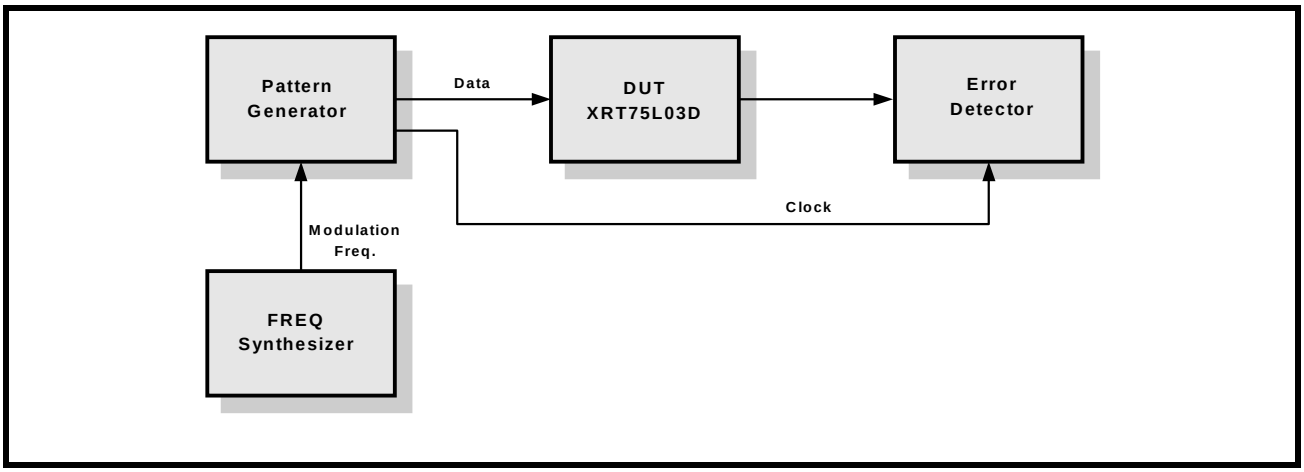
There are three fundamental parameters that describe circuit performance relative to jitter:

- **Jitter Tolerance (Receiver)**
- **Jitter Transfer (Receiver/Transmitter)**
- **Jitter Generation**

6.1 *JITTER TOLERANCE - RECEIVER:*

Jitter tolerance is a measure of how well a Clock and Data Recovery unit can successfully recover data in the presence of various forms of jitter. It is characterized by the amount of jitter required to produce a specified bit error rate. The tolerance depends on the frequency content of the jitter. Jitter Tolerance is measured as the jitter amplitude over a jitter spectrum for which the clock and data recovery unit achieves a specified bit error rate (BER). To measure the jitter tolerance as shown in Figure 21, jitter is introduced by the sinusoidal modulation of the serial data bit sequence.

FIGURE 21. JITTER TOLERANCE MEASUREMENTS

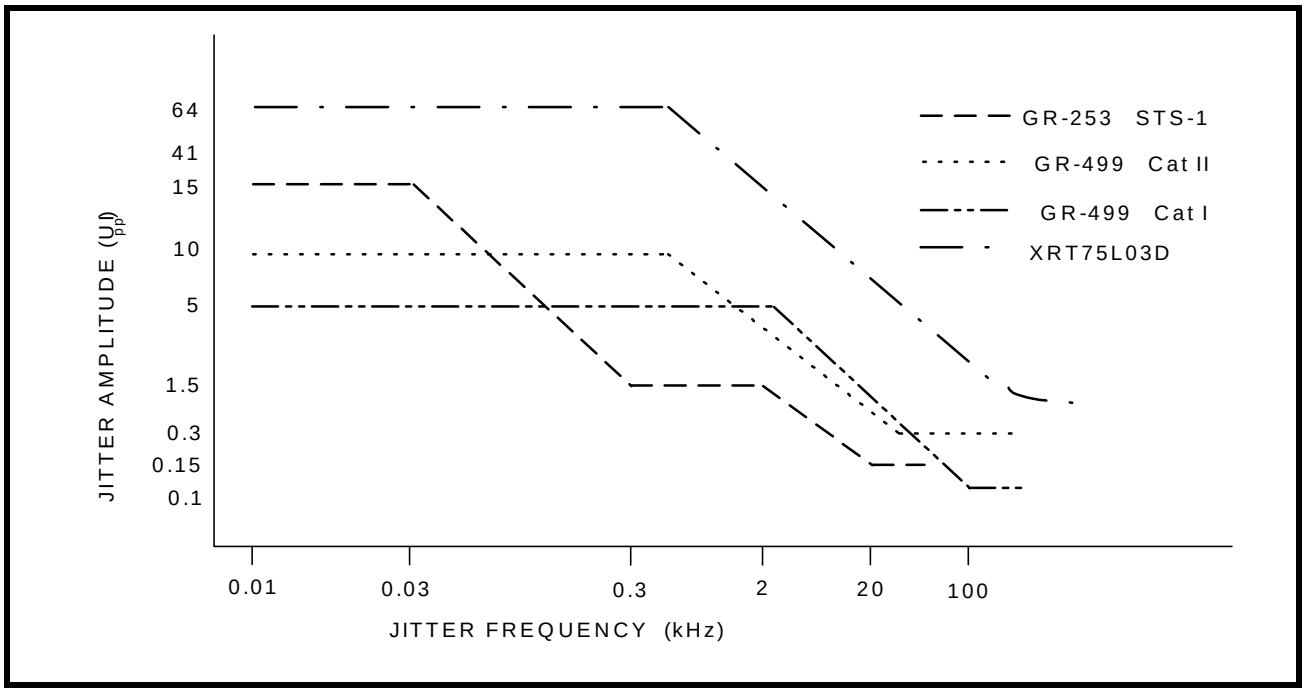


Input jitter tolerance requirements are specified in terms of compliance with jitter mask which is represented as a combination of points.Each point corresponds to a minimum amplitude of sinusoidal jitter at a given jitter frequency.

6.1.1 DS3/STS-1 Jitter Tolerance Requirements:

Bellcore GR-499 CORE, Issue 1, December 1995 specifies the minimum requirement of jitter tolerance for Category I and Category II. The jitter tolerance requirement for Category II is the most stringent. Figure 22 shows the jitter tolerance curve as per GR-499 specification.

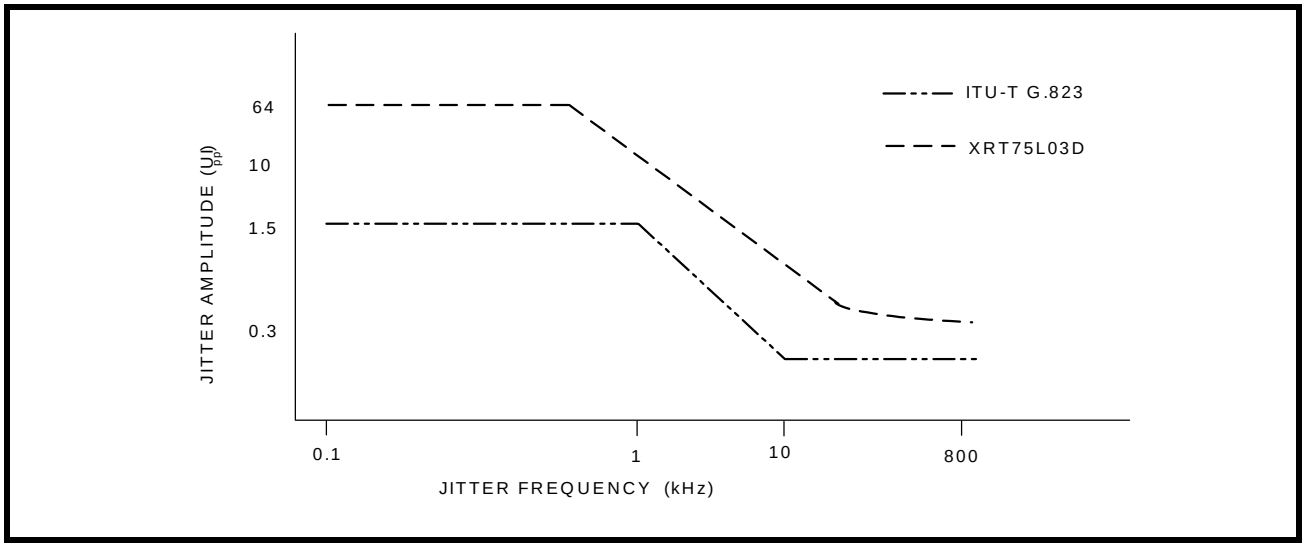
FIGURE 22. INPUT JITTER TOLERANCE FOR DS3/STS-1



6.1.2 E3 Jitter Tolerance Requirements:

ITU-T G.823 standard specifies that the clock and data recovery unit must be able to accommodate and tolerate jitter up to certain specified limits. Figure 23 shows the tolerance curve.

FIGURE 23. INPUT JITTER TOLERANCE FOR E3



As shown in the Figures 22 and 23 above, in the jitter tolerance measurement, the dark line indicates the minimum level of jitter that the E3/DS3/STS-1 compliant component must tolerate.

The Table 11 below shows the jitter amplitude versus the modulation frequency for various standards.

TABLE 11: JITTER AMPLITUDE VERSUS MODULATION FREQUENCY (JITTER TOLERANCE)

BIT RATE (KB/S)	STANDARD	INPUT JITTER AMPLITUDE (UI_{P-P})			MODULATION FREQUENCY				
		A1	A2	A3	F1(HZ)	F2(HZ)	F3(KHZ)	F4(KHZ)	F5(KHZ)
34368	ITU-T G.823	1.5	0.15	-	100	1000	10	800	-
44736	GR-499 CORE Cat I	5	0.1	-	10	2.3k	60	300	-
44736	GR-499 CORE Cat II	10	0.3	-	10	669	22.3	300	-
51840	GR-253 CORE Cat II	15	1.5	0.15	10	30	300	2	20

6.2 *JITTER TRANSFER - RECEIVER/TRANSMITTER:*

Jitter Transfer function is defined as the ratio of jitter on the output relative to the jitter applied on the input versus frequency.

There are two distinct characteristics in jitter transfer: jitter gain (jitter peaking) defined as the highest ratio above 0dB; and jitter transfer bandwidth.The overall jitter transfer bandwidth is controlled by a low bandwidth loop, typically using a voltage-controller crystal oscillator (VCXO).

The jitter transfer function is a ratio between the jitter output and jitter input for a component, or system often expressed in dB. A negative dB jitter transfer indicates the element removed jitter. A positive dB jitter transfer indicates the element added jitter.A zero dB jitter transfer indicates the element had no effect on jitter.

Table 12 shows the jitter transfer characteristics and/or jitter attenuation specifications for various data rates:

TABLE 12: JITTER TRANSFER SPECIFICATION/REFERENCES

E3	DS3	STS-1
ETSI TBR-24	GR-499 CORE section 7.3.2 Category I and Category II	GR-253 CORE section 5.6.2.1

The above specifications can be met only with a jitter attenuator that supports E3/DS3/STS-1 rates.

6.3 *Jitter Attenuator:*

An advanced crystal-less jitter attenuator per channel is included in the XRT75L03D. The jitter attenuator requires no external crystal nor high-frequency reference clock.

In Host mode, by clearing or setting the JATx/Rx_n bits in the channel control registers selects the jitter attenuator either in the Receive or Transmit path on per channel basis. In Hardware mode, JATx/Rx pin selects globally all three channels either in Receive or Transmit path.

The FIFO size can be either 16-bit or 32-bit. In HOST mode, the bits JA0_n and JA1_n can be set to appropriate combination to select the different FIFO sizes or to disable the Jitter Attenuator on a per channel basis. In Hardware mode, appropriate setting of the pins JA0 and JA1 selects the different FIFO sizes or disables the Jitter Attenuator for all three channels. Data is clocked into the FIFO with the associated clock signal (TxClk or RxClk) and clocked out of the FIFO with the dejittered clock. When the FIFO is within two bits of overflowing or underflowing, the FIFO limit status bit, FL_n is set to “1” in the Alarm status register. Reading this bit clears the FIFO and resets the bit into default state.

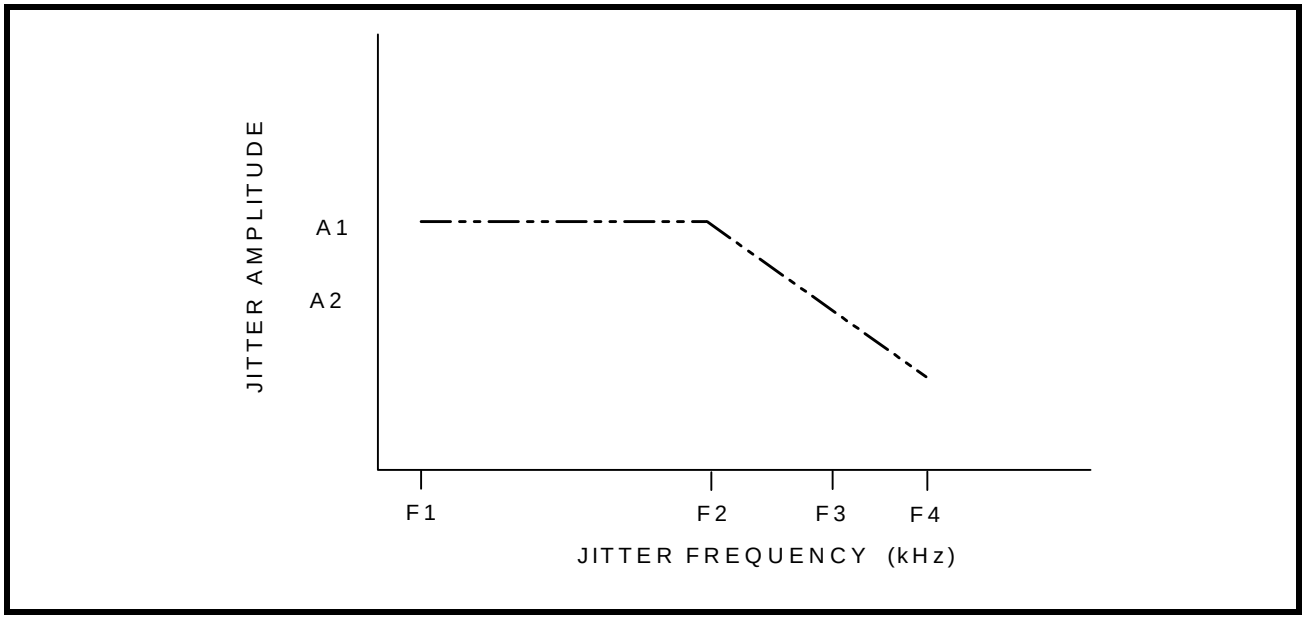
NOTE: *It is recommended to select the 16-bit FIFO for delay-sensitive applications as well as for removing smaller amounts of jitter. Table 13 specifies the jitter transfer mask requirements for various data rates:*

TABLE 13: JITTER TRANSFER PASS MASKS

RATE (KBITS)	MASK	F1 (HZ)	F2 (HZ)	F3 (HZ)	F4 (KHZ)	A1(dB)	A2(dB)
34368	G.823 ETSI-TBR-24	100	300	3K	800K	0.5	-19.5
44736	GR-499, Cat I GR-499, Cat II GR-253 CORE	10 10 10	10k 56.6k 40	- - -	15k 300k 15k	0.1 0.1 0.1	- - -
51840	GR-253 CORE	10	40k	-	400k	0.1	-

The jitter attenuator within the XRT75L03D meets the latest jitter attenuation specifications and/or jitter transfer characteristics as shown in the Figure 24.

FIGURE 24. JITTER TRANSFER REQUIREMENTS AND JITTER ATTENUATOR PERFORMANCE



6.3.1 JITTER GENERATION:

Jitter Generation is defined as the process whereby jitter appears at the output port of the digital equipment in the absence of applied input jitter. Jitter Generation is measured by sending jitter free data to the clock and data recovery circuit and measuring the amount of jitter on the output clock or the re-timed data. Since this is essentially a noise measurement, it requires a definition of bandwidth to be meaningful. The bandwidth is set according to the data rate. In general, the jitter is measured over a band of frequencies.

7.0 SERIAL HOST INTERFACE:

A serial microprocessor interface is included in the XRT75L03D. The interface is generic and is designed to support the common microprocessors/microcontrollers. The XRT75L03D operates in Host mode when the HOST/$\overline{HW}$ pin is tied “High”. The serial interface includes a serial clock (SClk), serial data input (SDI), serial data output (SDO), chip select (CS) and interrupt output (INT). The serial interface timing is shown in Figure 11.

The active low interrupt output signal ($\overline{INT}$ pin) indicates alarm conditions like LOS, DMO and FL to the processor.

When the XRT75L03D is configured in Host mode, the following input pins,TxLEV_n, TAOS_n, RLB_n, LLB_n, E3_n, STS-1/DS3_n, REQEN_n, JATx/Rx, JA0 and JA1 are disabled and must be connected to ground.

The Table 14 below illustrates the functions of the shared pins in either Host mode or in Hardware mode.

TABLE 14: FUNCTIONS OF SHARED PINS

PIN NUMBER	IN HOST MODE	IN HARDWARE MODE
66	$\overline{CS}$	RxClkINV
67	SClk	TxClkINV
68	SDI	RxON
69	SDO	RxMON
71	$\overline{INT}$	LOSMUT

NOTE: *While configured in Host mode, the TxON_n input pins will be active if the TxON_n bits in the control register are set to "1", and can be used to turn on and off the transmit output drivers. This permits a system designed for redundancy to quickly switch out a defective line card and switch-in the backup line card.*

TABLE 15: XRT75L03D REGISTER MAP - QUICK LOOK

ADDRESS LOCATION	REGISTER NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0x00	APS/Redundancy Control Register	Reserved	RxON Ch 2	RxON Ch 1	RxON Ch 0	Reserved	TxON Ch 2	TxON Ch 1	TxON Ch 0
CHANNEL 0 REGISTERS									
0x01	Source Level Interrupt Enable Register - Ch 0	Reserved				Change of FL Alarm Condition Interrupt Enable	Change of RLOL Condition Interrupt Enable	Change of RLOS Defect Condition Interrupt Enable	Change of DMO Condition Interrupt Enable
0x02	Source Level Interrupt Status Register - Ch 0	Reserved				Change of FL Alarm Condition Interrupt Status	Change of RLOL Condition Interrupt Status	Change of RLOS Condition Interrupt Status	Change of DMO Condition Interrupt Status
0x03	Alarm Status Register - Ch 0	Reserved	Loss of PRBS Pattern Sync	DLOS Defect Declared	ALOS Defect Declared	FL Alarm Declared	RLOL Condition Declared	RLOS Defect Condition	DMO Condition Status
0x04	Transmit Control Register - Ch 0	Reserved		Internal Transmit Drive Monitoring	Insert PRBS Error	Unused	TAOS	TxCLK INV	TxLEV
0x05	Receive Control Register - Ch 0	Reserved		DisableD-LOS Detector	DisableA-LOS Detec-tor	RxCLK INV	LOSMUTEn-able	Receive Monitor Mode Enable	Receive Equalizer Enable
0x06	Channel Control Register - Ch 0	Reserved		PRBS Enable	RLB	LLB	E3 Mode	STS-1/$\overline{DS3}$ Mode	SR/$\overline{DR}$ Mode
0x07	Jitter Attenuator Control Register - Ch 0	Reserved			SONET APS Recovery Time Mode Disable	JA RESET	JA1 (JA Mode Select Bit 1)	JA in TxPath	JA0 (JA Mode Select 0)
CHANNEL 1 REGISTERS									
0x08	Reserved			Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0x09	Source Level Interrupt Enable Register - Ch 0	Reserved				Change of FL Alarm Condition Interrupt Enable	Change of RLOL Condition Interrupt Enable	Change of RLOS Defect Condition Interrupt Enable	Change of DMO Condition Interrupt Enable
0x0A	Source Level Interrupt Status Register - Ch 0	Reserved				Change of FL Alarm Condition Interrupt Status	Change of RLOL Condition Interrupt Status	Change of RLOS Condition Interrupt Status	Change of DMO Condition Interrupt Status

TABLE 15: XRT75L03D REGISTER MAP - QUICK LOOK

ADDRESS LOCATION	REGISTER NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0x0B	Alarm Status Register - Ch 0	Reserved	Loss of PRBS Pattern Sync	DLOS Defect Declared	ALOS Defect Declared	FL Alarm Declared	RLOL Condition Declared	RLOS Defect Condition	DMO Condition Status
0x0C	Transmit Control Register - Ch 0	Reserved		Internal Transmit Drive Monitoring	Insert PRBS Error	Unused	TAOS	TxCLK INV	TxLEV
0x0D	Receive Control Register - Ch 0	Reserved		DisableD-LOS Detector	DisableA-LOS Detec-tor	RxCLK INV	LOSMUTEn-able	Receive Monitor Mode Enable	Receive Equalizer Enable
0x0E	Channel Control Register - Ch 0	Reserved		PRBS Enable	RLB	LLB	E3 Mode	STS-1/$\overline{DS3}$ Mode	SR/$\overline{DR}$ Mode
0x0F	Jitter Attenuator Control Register - Ch 0	Reserved			SONET APS Recovery Time Mode Disable	JA RESET	JA1 (JA Mode Select Bit 1)	JA in TxPath	JA0 (JA Mode Select 0)
CHANNEL 2 REGISTERS									
0x10	Reserved			Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0x11	Source Level Interrupt Enable Register - Ch 0	Reserved				Change of FL Alarm Condition Interrupt Enable	Change of RLOL Condition Interrupt Enable	Change of RLOS Defect Condition Interrupt Enable	Change of DMO Condition Interrupt Enable
0x12	Source Level Interrupt Status Register - Ch 0	Reserved				Change of FL Alarm Condition Interrupt Status	Change of RLOL Condition Interrupt Status	Change of RLOS Condition Interrupt Status	Change of DMO Condition Interrupt Status
0x13	Alarm Status Register - Ch 0	Reserved	Loss of PRBS Pattern Sync	DLOS Defect Declared	ALOS Defect Declared	FL Alarm Declared	RLOL Condition Declared	RLOS Defect Condition	DMO Condition Status
0x14	Transmit Control Register - Ch 0	Reserved		Internal Transmit Drive Monitoring	Insert PRBS Error	Unused	TAOS	TxCLK INV	TxLEV
0x15	Receive Control Register - Ch 0	Reserved		DisableD-LOS Detector	DisableA-LOS Detec-tor	RxCLK INV	LOSMUTEn-able	Receive Monitor Mode Enable	Receive Equalizer Enable
0x16	Channel Control Register - Ch 0	Reserved		PRBS Enable	RLB	LLB	E3 Mode	STS-1/$\overline{DS3}$ Mode	SR/$\overline{DR}$ Mode

TABLE 15: XRT75L03D REGISTER MAP - QUICK LOOK

ADDRESS LOCATION	REGISTER NAME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0x17	Jitter Attenuator Control Register - Ch 0	Reserved			SONET APS Recovery Time Mode Disable	JA RESET	JA1 (JA Mode Select Bit 1)	JA in TxPath	JA0 (JA Mode Select 0)
0x19 - 0x1F	Reserved	Reserved							
0x20	Block Level Interrupt Enable Register - Ch 32								
0x21	Block Level Interrupt Enable Register - Ch 33								
0x22 - 0x3D	Reserved	Reserved							
0x3E	Device Part Number Register	0	1	1	1	0	0	1	1
0x3F	Chip Revision Number Register	0	0	0	0	Revision Number Value			
0x40 - 0xFF	Reserved	Reserved							

LEGEND:

	Denotes Reserved (or Unused) Register Bits
	Denotes Read/Write Bits
	Denotes Read-Only Bits
	Denotes Reset-Upon-Read Bits

THE REGISTER MAP AND DESCRIPTION FOR THE XRT75L03D 3-CHANNEL DS3/E3/STS-1 LIU IC

TABLE 16: COMMAND REGISTER ADDRESS MAP, WITHIN THE XRT75L03D 3-CHANNEL DS3/E3/STS-1 LIU W/ JITTER ATTENUATOR IC

ADDRESS	COMMAND REGISTER	TYPE	REGISTER NAME
0x00	CR0	R/W	APS/Redundancy Control Register
CHANNEL 0 CONTROL REGISTERS			
0x01	CR1	R/O	Source Level Interrupt Enable Register - Channel 0
0x02	CR2	R/W	Source Level Interrupt Status Register Channel 0
0x03	CR3	R/O	Alarm Status Register - Channel 0

TABLE 16: COMMAND REGISTER ADDRESS MAP, WITHIN THE XRT75L03D 3-CHANNEL DS3/E3/STS-1 LIU W/ JITTER ATTENUATOR IC

ADDRESS	COMMAND REGISTER	TYPE	REGISTER NAME
0x04	CR4	R/W	Transmit Control Register - Channel 0
0x05	CR5	R/W	Receive Control Register - Channel 0
0x06	CR6	R/W	Channel Control Register - Channel 0
0x07	CR7	R/W	Jitter Attenuator Control Register - Channel 0
CHANNEL 1 CONTROL REGISTERS			
0x08	CR8	R/O	Reserved
0x09	CR9	R/W	Source Level Interrupt Enable Register - Channel 1
0x0A	CR10	RUR	Source Level Interrupt Status Register - Channel 1
0x0B	CR11	R/O	Alarm Status Register - Channel 1
0x0C	CR12	R/W	Transmit Control Register - Channel 1
0x0D	CR13	R/W	Receive Control Register - Channel 1
0x0E	CR14	R/W	Channel Control Register - Channel 1
0x0F	CR15	R/W	Jitter Attenuator Control Register - Channel 1
CHANNEL 2 CONTROL REGISTERS			
0x10	CR16	R/W	Reserved
0x11	CR17	R/W	Source Level Interrupt Enable Register - Channel 2
0x12	CR18	RUR	Source Level Interrupt Status Register - Channel 2
0x13	CR19	R/O	Alarm Status Register - Channel 2
0x14	CR20	R/W	Transmit Control Register - Channel 2
0x15	CR21	R/W	Receive Control Register - Channel 2
0x16	CR22	R/W	Channel Control Register - Channel 2
0x17	CR23	R/W	Jitter Attenuator Control Register - Channel 2
0x18 - 0x1F	Reserved		
BLOCK LEVEL INTERRUPT ENABLE/STATUS REGISTERS (CHANNELS 0 - 2)			
0x20	CR32	R/W	Block Level Interrupt Enable Register
0x21	CR33	R/O	Block Level Interrupt Status Register
0x22 - 0x3D	Reserved		Reserved
DEVICE IDENTIFICATION REGISTERS			
0x3E	CR62	R/O	Device Part Number Register
0x3F	CR63	R/O	Chip Revision Number Register

THE GLOBAL/CHIP-LEVEL REGISTERS

The register set, within the XRT75L03D consists of five "Global" or "Chip-Level" Registers and 21 per-Channel Registers. This section will present detailed information on the Global Registers.

TABLE 17: LIST AND ADDRESS LOCATIONS OF GLOBAL REGISTERS

ADDRESS	COMMAND REGISTER	TYPE	REGISTER NAME
0x00	CR0	R/W	APS/Redundancy Control Register
0x01 - 0x1F	Bank of Per-Channel Registers		
0x20	CR32	R/W	Block Level Interrupt Enable Register
0x21	CR33	R/O	Block Level Interrupt Status Register
0x22 - 0x3D	Reserved Registers		
0x3E	CR62	R/O	Device/Part Number Register
0x3F	CR63	R/O	Chip Revision Number Register

REGISTER DESCRIPTION - GLOBAL REGISTERS

TABLE 18: APS/REDUNDANCY CONTROL REGISTER - CR0 (ADDRESS LOCATION = 0X00)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved	RxONCh 2	RxON Ch 1	RxON Ch 0	Reserved	TxON Ch 2	TxON Ch 1	TxON Ch 0
R/O	R/W	R/W	R/W	R/O	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
7	Reserved	R/O	0	
6	RxON Ch 2	R/W	0	**Receiver Section ON - Channel 2** This READ/WRITE bit-field is used to either turn on or turn off the Receive Section of Channel 2. If the user turns on the Receive Section, then Channel 2 will begin to receive the incoming DS3, E3 or STS-1 data-stream via the RTIP_2 and RRING_2 input pins. Conversely, if the user turns off the Receive Section, then the entire Receive Section (e.g., AGC and Receive Equalizer Block, Clock Recovery PLL, etc) will be powered down. 0 - Shuts off the Receive Section of Channel 2. 1 - Turns on the Receive Section of Channel 2.

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
5	RxON Ch 1	R/W	0	**Receiver Section ON - Channel 1** This READ/WRITE bit-field is used to either turn on or turn off the Receive Section of Channel 1. If the user turns on the Receive Section, then Channel 1 will begin to receive the incoming DS3, E3 or STS-1 data-stream via the RTIP_1 and RRING_1 input pins. Conversely, if the user turns off the Receive Section, then the entire Receive Section (e.g., AGC and Receive Equalizer Block, Clock Recovery PLL, etc) will be powered down. 0 - Shuts off the Receive Section of Channel 1. 1 - Turns on the Receive Section of Channel 1.
4	RxON Ch 0	R/W	0	**Receiver Section ON - Channel 0** This READ/WRITE bit-field is used to either turn on or turn off the Receive Section of Channel 0. If the user turns on the Receive Section, then Channel 0 will begin to receive the incoming DS3, E3 or STS-1 data-stream via the RTIP_0 and RRING_0 input pins. Conversely, if the user turns off the Receive Section, then the entire Receive Section (e.g., AGC and Receive Equalizer Block, Clock Recovery PLL, etc) will be powered down. 0 - Shuts off the Receive Section of Channel 0. 1 - Turns on the Receive Section of Channel 0.
3	Reserved	R/O	0	
2	TxON Ch 2	R/W	0	**Transmit Driver ON - Channel 2** This READ/WRITE bit-field is used to either turn on or turn off the Transmit Driver associated with Channel 2. If the user turns on the Transmit Driver, then Channel 2 will begin to transmit DS3, E3 or STS-1 pulses on the line via the TTIP_2 and TRING_ 2 output pins. Conversely, if the user turns off the Transmit Driver, then the TTIP_2 and TRING_2 output pins will be tri-stated. 0 - Shuts off the Transmit Driver associated with Channel 2 and tri-states the TTIP_2 and TRING_ 2 output pins. 1 - Turns on or enables the Transmit Driver associated with Channel 2. ***NOTE:*** *If the user wishes to exercise software control over the state of the Transmit Driver associated with Channel 2, then it is imperative that the user pull the TxON_2 (pin 125) to a logic "High" level.*

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
1	TxON Ch 1	R/W	0	**Transmit Section ON - Channel 1** This READ/WRITE bit-field is used to either turn on or turn off the Transmit Driver associated with Channel 1. If the user turns on the Transmit Driver, then Channel 1 will begin to transmit DS3, E3 or STS-1 pulses on the line via the TTIP_1 and TRING_ 1 output pins. Conversely, if the user turns off the Transmit Driver, then the TTIP_1 and TRING_1 output pins will be tri-stated. 0 - Shuts off the Transmit Driver associated with Channel 1 and tri-states the TTIP_1 and TRING_ 1 output pins. 1 - Turns on or enables the Transmit Driver associated with Channel 1. ***NOTE:*** *If the user wishes to exercise software control over the state of the Transmit Driver associated with Channel 1, then it is imperative that the user pull the TxON_1 (pin 1) to a logic "High" level.*
0	TxON Ch 0	R/W	0	**Transmit Section ON - Channel 0** This READ/WRITE bit-field is used to either turn on or turn off the Transmit Driver associated with Channel 0. If the user turns on the Transmit Driver, then Channel 0 will begin to transmit DS3, E3 or STS-1 pulses on the line via the TTIP_0 and TRING_ 0 output pins. Conversely, if the user turns off the Transmit Driver, then the TTIP_0 and TRING_0 output pins will be tri-stated. 0 - Shuts off the Transmit Driver associated with Channel 0 and tri-states the TTIP_0 and TRING_ 0 output pins. 1 - Turns on or enables the Transmit Driver associated with Channel 0. ***NOTE:*** *If the user wishes to exercise software control over the state of the Transmit Driver associated with Channel 0, then it is imperative that the user pull the TxON_0 (pin 38) to a logic "High" level.*

TABLE 19: BLOCK LEVEL INTERRUPT ENABLE REGISTER - CR32 (ADDRESS LOCATION = 0X20)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved					Channel 2 Interrupt Enable	Channel 1 Interrupt Enable	Channel 0 Interrupt Enable
R/O	R/O	R/O	R/O	R/O	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
7 - 3	Unused	R/O	0	
2	Channel 2 Interrupt Enable	R/W	0	**Channel 2 Interrupt Enable Bit:** This READ/WRITE bit-field is used to do either of the following • To enable Channel 2 for Interrupt Generation at the Block Level • To disable all Interrupts associated with Channel 2 within the XRT75L03D If the user enables Channel 2-related Interrupts at the Block Level, then this means that a given Channel 2-related interrupt (e.g., Change in LOS Defect Condition - Channel 2) will be enabled if the user has also enabled this particular interrupt at the Source Level. If the user disables Channel 2-related Interrupts at the Block Level, then this means that the XRT75L03D will NOT generate any Channel 2-Related Interrupts at all. 0 - Disables all Channel 2-related Interrupt. 1 - Enables Channel 2-related Interrupts at the Block Level. The user must still enable individual Channel 2-related Interrupts at the source level, before they are enabled for interrupt generation.
1	Channel 1 Interrupt Enable	R/W	0	**Channel 1 Interrupt Enable Bit:** Please see the description for Bit 2 Channel 2 Interrupt Enable.
0	Channel 0 Interrupt Enable	R/W	0	**Channel 0 Interrupt Enable Bit:** Please see the description for Bit 2 Channel 2 Interrupt Enable.

TABLE 20: BLOCK LEVEL INTERRUPT STATUS REGISTER - CR33 (ADDRESS LOCATION = 0X21)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reserved					Channel 2 Interrupt Status	Channel 1 Interrupt Status	Channel 0 Interrupt Status
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
7 - 3	Unused	R/O	0	
2	Channel 2 Interrupt Status	R/O	0	**Channel 2 Interrupt Status Bit:** This READ-ONLY bit-field indicates whether or not the XRT75L03D has a pending Channel 2-related interrupt that is awaiting service. 0 - Indicates that there is NO Channel 2-related Interrupt awaiting service. 1 - Indicates that there is at least one Channel 2-related Interrupt awaiting service. In this case, the user's Interrupt Service routine should be written such that the Microprocessor will now proceed to read out the contents of the Source Level Interrupt Status Register - Channel 2 (Address Location = 0x12) in order to determine the exact cause of the interrupt request. ***NOTE:*** *Once this bit-field is set to "1", it will not be cleared back to "0" until the user has read out the contents of the Source-Level Interrupt Status Register bit, that corresponds with the interrupt request.*

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
1	Channel 1 Interrupt Enable	R/W	0	**Channel 1 Interrupt Enable Bit:** This READ-ONLY bit-field indicates whether or not the XRT75L03D has a pending Channel 1-related interrupt that is awaiting service. 0 - Indicates that there is NO Channel 1-related Interrupt awaiting service. 1 - Indicates that there is at least one Channel 1-related Interrupt awaiting service. In this case, the user's Interrupt Service routine should be written such that the Microprocessor will now proceed to read out the contents of the Source Level Interrupt Status Register - Channel 1 (Address Location = 0x0A) in order to determine the exact cause of the interrupt request. ***NOTE:*** *Once this bit-field is set to "1", it will not be cleared back to "0" until the user has read out the contents of the Source-Level Interrupt Status Register bit, that corresponds with the interrupt request.*
0	Channel 0 Interrupt Enable	R/W	0	**Channel 0 Interrupt Enable Bit:** This READ-ONLY bit-field indicates whether or not the XRT75L03D has a pending Channel 0-related interrupt that is awaiting service. 0 - Indicates that there is NO Channel 0-related Interrupt awaiting service. 1 - Indicates that there is at least one Channel 0-related Interrupt awaiting service. In this case, the user's Interrupt Service routine should be written such that the Microprocessor will now proceed to read out the contents of the Source Level Interrupt Status Register - Channel 0 (Address Location = 0x02) in order to determine the exact cause of the interrupt request. ***NOTE:*** *Once this bit-field is set to "1", it will not be cleared back to "0" until the user has read out the contents of the Source-Level Interrupt Status Register bit, that corresponds with the interrupt request.*

TABLE 21: DEVICE/PART NUMBER REGISTER - CR62 (ADDRESS LOCATION = 0X3E)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Part Number ID Value							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	1	1	1	0	0	1	1

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
7 - 0	Part Number ID Value	R/O	0x73	**Part Number ID Value:** This READ-ONLY register contains a unique value that represents the XRT75L03D.

TABLE 22: CHIP REVISION NUMBER REGISTER - CR63 (ADDRESS LOCATION = 0X3F)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Chip Revision Number Value							
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	X	X	X	X

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
7 - 0	Chip Revision Number Value	R/O	0x0#	**Chip Revision Number Value:** This READ-ONLY register contains a value that represents the current revision of this XRT75L03D. This revision number will always be in the form of "0x0#", where "#" is a hexadecimal value that specifies the current revision of the chip. For example, the very first revision of this chip will contain the value "0x01".

THE PER-CHANNEL REGISTERS

The XRT75L03D consists of 21 per-Channel Registers. Table 23 presents the overall Register Map with the Per-Channel Registers shaded.

TABLE 23: COMMAND REGISTER ADDRESS MAP, WITHIN THE XRT75L03D 3-CHANNEL DS3/E3/STS-1 LIU W/ JITTER ATTENUATOR IC

ADDRESS	COMMAND REGISTER	TYPE	REGISTER NAME
0x00	CR0	R/W	APS/Redundancy Control Register
CHANNEL 0 CONTROL REGISTERS			
0x01	CR1	R/O	Source Level Interrupt Enable Register - Channel 0
0x02	CR2	R/W	Source Level Interrupt Status Register Channel 0
0x03	CR3	R/O	Alarm Status Register - Channel 0
0x04	CR4	R/W	Transmit Control Register - Channel 0
0x05	CR5	R/W	Receive Control Register - Channel 0
0x06	CR6	R/W	Channel Control Register - Channel 0
0x07	CR7	R/W	Jitter Attenuator Control Register - Channel 0
CHANNEL 1 CONTROL REGISTERS			
0x08	CR8	R/O	Reserved
0x09	CR9	R/W	Source Level Interrupt Enable Register - Channel 1
0x0A	CR10	RUR	Source Level Interrupt Status Register - Channel 1
0x0B	CR11	R/O	Alarm Status Register - Channel 1
0x0C	CR12	R/W	Transmit Control Register - Channel 1

TABLE 23: COMMAND REGISTER ADDRESS MAP, WITHIN THE XRT75L03D 3-CHANNEL DS3/E3/STS-1 LIU W/ JITTER ATTENUATOR IC

ADDRESS	COMMAND REGISTER	TYPE	REGISTER NAME
0x0D	CR13	R/W	Receive Control Register - Channel 1
0x0E	CR14	R/W	Channel Control Register - Channel 1
0x0F	CR15	R/W	Jitter Attenuator Control Register - Channel 1
CHANNEL 2 CONTROL REGISTERS			
0x10	CR16	R/W	Reserved
0x11	CR17	R/W	Source Level Interrupt Enable Register - Channel 2
0x12	CR18	RUR	Source Level Interrupt Status Register - Channel 2
0x13	CR19	R/O	Alarm Status Register - Channel 2
0x14	CR20	R/W	Transmit Control Register - Channel 2
0x15	CR21	R/W	Receive Control Register - Channel 2
0x16	CR22	R/W	Channel Control Register - Channel 2
0x17	CR23	R/W	Jitter Attenuator Control Register - Channel 2
0x18 - 0x1F	Reserved		
BLOCK LEVEL INTERRUPT ENABLE/STATUS REGISTERS (CHANNELS 0 - 2)			
0x20	CR32	R/W	Block Level Interrupt Enable Register
0x21	CR33	R/O	Block Level Interrupt Status Register
0x22 - 0x3D	Reserved		Reserved
DEVICE IDENTIFICATION REGISTERS			
0x3E	CR62	R/O	Device Part Number Register
0x3F	CR63	R/O	Chip Revision Number Register

REGISTER DESCRIPTION - PER CHANNEL REGISTERS

TABLE 24: SOURCE LEVEL INTERRUPT ENABLE REGISTER - CHANNEL 0 ADDRESS LOCATION = 0X01

Channel 1 Address Location = 0x09

Channel 2 Address Location = 0x11)

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				Change of FL Condition Interrupt Enable Ch 0	Change of LOL Condition Interrupt Enable Ch 0	Change of LOS Condition Interrupt Enable Ch 0	Change of DMO Condition Interrupt Enable Ch 0
R/O	R/O	R/O	R/O	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
7 - 4	Reserved	R/O	0	
3	Change of FL Condition Interrupt Enable - Ch 0	R/W	0	**Change of FL (FIFO Limit Alarm) Condition Interrupt Enable - Ch 0:** This READ/WRITE bit-field is used to either enable or disable the Change of FL Condition Interrupt. If the user enables this interrupt, then the XRT75L03D will generate an interrupt any time any of the following events occur. • Whenever the Jitter Attenuator (within Channel 0) declares the FL (FIFO Limit Alarm) condition. • Whenever the Jitter Attenuator (within Channel 0) clears the FL (FIFO Limit Alarm) condition. 0 - Disables the Change in FL Condition Interrupt. 1 - Enables the Change in FL Condition Interrupt.
2	Change of LOL Condition Interrupt Enable	R/W	0	**Change of Receive LOL (Loss of Lock) Condition Interrupt Enable - Channel 0:** This READ/WRITE bit-field is used to either enable or disable the Change of Receive LOL Condition Interrupt. If the user enables this interrupt, then the XRT75L03D will generate an interrupt any time any of the following events occur. • Whenever the Receive Section (within Channel 0) declares the Loss of Lock Condition. • Whenever the Receive Section (within Channel 0) clears the Loss of Lock Condition. 0 - Disables the Change in Receive LOL Condition Interrupt. 1 - Enables the Change in Receive LOL Condition Interrupt.

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
1	Change of LOS Condition Interrupt Enable	R/W	0	**Change of the Receive LOS (Loss of Signal) Defect Condition Interrupt Enable - Ch 0:** This READ/WRITE bit-field is used to either enable or disable the Change of the Receive LOS Defect Condition Interrupt. If the user enables this interrupt, then the XRT75L03D will generate an interrupt any time any of the following events occur. • Whenever the Receive Section (within Channel 0) declares the LOS Defect Condition. • Whenever the Receive Section (within Channel 0) clears the LOS Defect condition. 0 - Disables the Change in the LOS Defect Condition Interrupt. 1 - Enables the Change in the LOS Defect Condition Interrupt.
0	Change of DMO Condition Interrupt Enable	R/W	0	**Change of Transmit DMO (Drive Monitor Output) Condition Interrupt Enable - Ch 0:** This READ/WRITE bit-field is used to either enable or disable the Change of Transmit DMO Condition Interrupt. If the user enables this interrupt, then the XRT75L03D will generate an interrupt any time any of the following events occur. • Whenever the Transmit Section toggles the DMO output pin (or bit-field) to "1". • Whenever the Transmit Section toggles the DMO output pin (or bit-field) to "0". 0 - Disables the Change in the DMO Condition Interrupt. 1 - Enables the Change in the DMO Condition Interrupt.

TABLE 25: SOURCE LEVEL INTERRUPT STATUS REGISTER - CHANNEL 0 ADDRESS LOCATION = 0X02

Channel 1 Address Location = 0x0A

Channel 2 Address Location = 0x12

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused				Change of FL Condition Interrupt Status Ch_n	Change of LOL Condition Interrupt Status Ch_n	Change of LOS Condition nterrupt Status Ch_n	Change of DMO Condition Interrupt Status Ch_n
R/O	R/O	R/O	R/O	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
7 - 4	Unused	R/O	0	
3	Change of FL Condition Interrupt Status	RUR	0	**Change of FL (FIFO Limit Alarm) Condition Interrupt Status - Ch 0:** This RESET-upon-READ bit-field indicates whether or not the Change of FL Condition Interrupt (for Channel 0) has occurred since the last read of this register. 0 - Indicates that the Change of FL Condition Interrupt has NOT occurred since the last read of this register. 1 - Indicates that the Change of FL Condition Interrupt has occurred since the last read of this register. ***NOTE:*** *The user can determine the current state of the FIFO Alarm condition by reading out the contents of Bit 3 (FL Alarm Declared) within the Alarm Status Register.*
2	Change of LOL Condition Interrupt Status	RUR	0	**Change of Receive LOL (Loss of Lock) Condition Interrupt Status - Ch 0:** This RESET-upon-READ bit-field indicates whether or not the Change of Receive LOL Condition Interrupt (for Channel 0) has occurred since the last read of this register. 0 - Indicates that the Change of Receive LOL Condition Interrupt has NOT occurred since the last read of this register. 1 - Indicates that the Change of Receive LOL Condition Interrupt has occurred since the last read of this register. ***NOTE:*** *The user can determine the current state of the Receive LOL Defect condition by reading out the contents of Bit 2 (Receive LOL Defect Declared) within the Alarm Status Register.*

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
1	Change of LOS Condition Interrupt Status	RUR	0	**Change of Receive LOS (Loss of Signal) Defect Condition Interrupt Status:** This RESET-upon-READ bit-field indicates whether or not the Change of the Receive LOS Defect Condition Interrupt (for Channel 0) has occurred since the last read of this register. 0 - Indicates that the Change of the Receive LOS Defect Condition Interrupt has NOT occurred since the last read of this register. 1 - Indicates that the Change of the Receive LOS Defect Condition Interrupt has occurred since the last read of this register. ***NOTE:*** *The user can determine the current state of the Receive LOS Defect condition by reading out the contents of Bit 1 (Receive LOS Defect Declared) within the Alarm Status Register.*
0	Change of DMO Condition Interrupt Status	RUR	0	**Change of Transmit DMO (Drive Monitor Output) Condition Interrupt Status - Ch 0:** This RESET-upon-READ bit-field indicates whether or not the Change of the Transmit DMO Condition Interrupt (for Channel 0) has occurred since the last read of this register. 0 - Indicates that the Change of the Transmit DMO Condition Interrupt has NOT occurred since the last read of this register. 1 - Indicates that the Change of the Transmit DMO Condition Interrupt has occurred since the last read of this register. ***NOTE:*** *The user can determine the current state of the Transmit DMO Condition by reading out the contents of Bit 0 (Transmit DMO Condition) within the Alarm Status Register.*

TABLE 26: ALARM STATUS REGISTER - CHANNEL 0 ADDRESS LOCATION = 0X03

Channel 1 Address Location = 0x0B

Channel 2 Address Location = 0x13

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused	Loss of PRBS Pattern Sync	Digital LOS Defect Declared	Analog LOS Defect Declared	FL (FIFO Limit) Alarm Declared	Receive LOL Defect Declared	Receive LOS Defect Declared	Transmit DMO Condition
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
7	Unused	R/O	0	
6	Loss of PRBS Pattern Lock	R/O	0	**Loss of PRBS Pattern Lock Indicator:** This READ-ONLY bit-field indicates whether or not the PRBS Receiver (within the Receive Section of Channel 0) is declaring PRBS Lock within the incoming PRBS pattern. If the PRBS Receiver detects a very large number of bit-errors within its incoming data-stream, then it will declare the Loss of PRBS Lock Condition. Conversely, if the PRBS Receiver were to detect its pre-determined PRBS pattern with the incoming DS3, E3 or STS-1 data-stream, (with little or no bit errors) then the PRBS Receiver will clear the Loss of PRBS Lock condition. 0 - Indicates that the PRBS Receiver is currently declaring the PRBS Lock condition within the incoming DS3, E3 or STS-1 data-stream. 1 - Indicates that the PRBS Receiver is currently declaring the Loss of PRBS Lock condition within the incoming DS3, E3 or STs-1 data-stream. ***NOTE:*** *This register bit is only valid if all of the following are true.* **a.** The PRBS Generator block (within the Transmit Section of the Chip is enabled). **b.** The PRBS Receiver is enabled. **c.** The PRBS Pattern (that is generated by the PRBS Generator) is somehow looped back into the Receive Path (via the Line-Side) and in-turn routed to the receive input of the PRBS Receiver.

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
5	Digital LOS Defect Declared	R/O	0	**Digital LOS Defect Declared:** This READ-ONLY bit-field indicates whether or not the Digital LOS (Loss of Signal) detector is declaring the LOS Defect condition. For DS3 and STS-1 applications, the Digital LOS Detector will declare the LOS Defect condition whenever it detects an absence of pulses (within the incoming DS3 or STS-1 data-stream) for 160 consecutive bit-periods. Further, (again for DS3 and STS-1 applications) the Digital LOS Detector will clear the LOS Defect condition whenever it determines that the pulse density (within the incoming DS3 or STS-1 signal) is at least 33%. 0 - Indicates that the Digital LOS Detector is NOT declaring the LOS Defect Condition. 1 - Indicates that the Digital LOS Detector is currently declaring the LOS Defect condition. ***NOTES:*** *1. LOS Detection (within each channel of the XRT75L03D) is performed by both an Analog LOS Detector and a Digital LOS Detector. The LOS state of a given Channel is simply a WIRED-OR of the LOS Defect Declare states of these two detectors.* *2. The current LOS Defect Condition (for the channel) can be determined by reading out the contents of Bit 1 (Receive LOS Defect Declared) within this register.*

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
4	Analog LOS Defect Declared	R/O	0	**Analog LOS Defect Declared:** This READ-ONLY bit-field indicates whether or not the Analog LOS (Loss of Signal) detector is declaring the LOS Defect condition. For DS3 and STS-1 applications, the Analog LOS Detector will declare the LOS Defect condition whenever it determines that the amplitude of the pulses (within the incoming DS3/STS-1 line signal) drops below a certain Analog LOS Defect Declaration threshold level. Conversely, (again for DS3 and STS-1 applications) the Analog LOS Detector will clear the LOS Defect condition whenever it determines that the amplitude of the pulses (within the incoming DS3/STS-1 line signal) has risen above a certain Analog LOS Defect Clearance threshold level. It should be noted that, in order to prevent "chattering" within the Analog LOS Detector output, there is some built-in hysteresis between the Analog LOS Defect Declaration and the Analog LOS Defect Clearance threshold levels. 0 - Indicates that the Analog LOS Detector is NOT declaring the LOS Defect Condition. 1 - Indicates that the Analog LOS Detector is currently declaring the LOS Defect condition. ***NOTES:*** *1. LOS Detection (within each channel of the XRT75L03D) is performed by both an Analog LOS Detector and a Digital LOS Detector. The LOS state of a given Channel is simply a WIRED-OR of the LOS Defect Declare states of these two detectors.* *2. The current LOS Defect Condition (for the channel) can be determined by reading out the contents of Bit 1 (Receive LOS Defect Declared) within this register.*

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
3	FL Alarm Declared	R/O	0	**FL (FIFO Limit) Alarm Declared:** This READ-ONLY bit-field indicates whether or not the Jitter Attenuator block (within Channel_n) is currently declaring the FIFO Limit Alarm. The Jitter Attenuator block will declare the FIFO Limit Alarm anytime the Jitter Attenuator FIFO comes within two bit-periods of either overflowing or under-running. Conversely, the Jitter Attenuator block will clear the FIFO Limit Alarm anytime the Jitter Attenuator FIFO is NO longer within two bit-periods of either overflowing or under-running. Typically, this Alarm will only be declared whenever there is a very serious problem with timing or jitter in the system. 0 - Indicates that the Jitter Attenuator block (within Channel_n) is NOT currently declaring the FIFO Limit Alarm condition. 1 - Indicates that the Jitter Attenuator block (within Channel_n) is currently declaring the FIFO Limit Alarm condition. ***NOTE:*** *This bit-field is only active if the Jitter Attenuator (within Channel_n) has been enabled.*
2	Receive LOL Condition Declared	R/O	0	**Receive LOL (Loss of Lock) Condition Declared:** This READ-ONLY bit-field indicates whether or not the Receive Section (within Channel_n) is currently declaring the LOL (Loss of Lock) condition. The Receive Section (of Channel_n) will declare the LOL Condition, if any one of the following conditions are met. • If the frequency of the Recovered Clock signal differs from that of the signal provided to the E3CLK input (for E3 applications), the DS3CLK input (for DS3 applications) or the STS-1CLK input (for STS-1 applications) by 0.5% (or 5000ppm) or more. • If the frequency of the Recovered Clock signal differs from the line-rate clock signal (for Channel_n) that has been generated by the SFM Clock Synthesizer PLL (for SFM Mode Operation) by 0.5% (or 5000ppm) or more. 0 - Indicates that the Receive Section of Channel_n is NOT currently declaring the LOL Condition. 1 - Indicates that the Receive Section of Channel_n is currently declaring the LOL Condition.

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
1	Receive LOS Defect Condition Declared	R/O	0	**Receive LOS (Loss of Signal) Defect Condition Declared:** This READ-ONLY bit-field indicates whether or not the Receive Section (within Channel_n) is currently declaring the LOS defect condition. The Receive Section (of Channel_n) will declare the LOS defect condition, if any one of the following conditions is met. • If the Digital LOS Detector declares the LOS defect condition (for DS3 or STS-1 applications) • If the Analog LOS Detector declares the LOS defect condition (for DS3 or STS-1 applications) • If the ITU-T G.775 LOS Detector declares the LOS defect condition (for E3 applications). 0 - Indicates that the Receive Section of Channel_n is NOT currently declaring the LOS Defect Condition. 1 - Indicates that the Receive Section of Channel_n is currently declaring the LOS Defect condition.
0	Transmit DMO Condition Declared	R/O	0	**Transmit DMO (Drive Monitor Output) Condition Declared:** This READ-ONLY bit-field indicates whether or not the Transmit Section of Channel_n is currently declaring the DMO Alarm condition. If configured accordingly, the Transmit Section will either internally or externally check the Transmit Output DS3/E3/STS-1 Line signal for bipolar pulses via the TTIP_n and TRING_n output signals. If the Transmit Section were to detect no bipolar for 128 consecutive bit-periods, then it will declare the Transmit DMO Alarm condition. This particular alarm can be used to check for fault conditions on the Transmit Output Line Signal path. The Transmit Section will clear the Transmit DMO Alarm condition the instant that it detects some bipolar activity on the Transmit Output Line signal. 0 - Indicates that the Transmit Section of Channel_n is NOT currently declaring the Transmit DMO Alarm condition. 1 - Indicates that the Transmit Section of Channel_n is currently declaring the Transmit DMO Alarm condition.

TABLE 27: TRANSMIT CONTROL REGISTER - CHANNEL 0 ADDRESS LOCATION = 0X04

Channel 1 Address Location = 0x0C

Channel 2 Address Location = 0x14

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		Internal Transmit Drive Monitor	Insert PRBS Error	Unused	TAOS	TxCLKINV	TxLEV
R/O	R/O	R/W	R/W	R/O	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
7 - 6	Unused	R/O	0	
5	Internal Transmit Drive Monitor	R/W	0	**Internal Transmit Drive Monitor Enable - Channel_n:** This READ/WRITE bit-field is used to configure the Transmit Section of Channel_n to either internally or externally monitor the TTIP_n and TRING_n output pins for bipolar pulses, in order to determine whether to declare the Transmit DMO Alarm condition. If the user configures the Transmit Section to externally monitor the TTIP_n and TRING_n output pins (for bipolar pulses) then the user must make sure that he/she has connected the MTIP_n and MRING_n input pins to their corresponding TTIP_n and TRING_n output pins (via a 274 ohm series resistor). If the user configures the Transmit Section to internally monitor the TTIP_n and TRING_n output pins (for bipolar pulses) then the user does NOT need to make sure that the MTIP_n and MRING_n input pins are connected to the TTIP_n and TRING_n output pins (via series resistors). This monitoring will be performed right at the TTIP_n and TRING_n output pads. 0 - Configures the Transmit Drive Monitor to externally monitor the TTIP_n and TRING_n output pins for bipolar pulses. 1 - Configures the Transmit Drive Monitor to internally monitor the TTIP_n and TRING_n output pins for bipolar pulses.

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
4	Insert PRBS Error	R/W	0	**Insert PRBS Error - Channel_n:** A "0 to 1" transition within this bit-field configures the PRBS Generator (within the Transmit Section of Channel_n) to generate a single bit error within the out-bound PRBS pattern-stream. ***NOTES:*** *1. This bit-field is only active if the PRBS Generator and Receiver have been enabled within the corresponding Channel.* *2. After writing the "1" into this register, the user must execute a write operation to clear this particular register bit to "0" in order to facilitate the next "0 to 1" transition in this bit-field.*
3	Unused	R/O	0	
2	TAOS	R/W	0	**Transmit All OneS Pattern - Channel_n:** This READ/WRITE bit-field is used to command the Transmit Section of Channel_n to generate and transmit an unframed, All Ones pattern via the DS3, E3 or STS-1 line signal (to the remote terminal equipment). Whenever the user implements this configuration setting then the Transmit Section will ignore the data that it is accepting from the System-side equipment and overwrite this data with the "All Ones" Pattern. 0 - Configures the Transmit Section to transmit the data that it accepts from the System-side Interface. 1 - Configures the Transmit Section to generate and transmit the Unframed, All Ones pattern.

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
1	TxCLKINV	R/W	0	**Transmit Clock Invert Select - Channel_n:** This READ/WRITE bit-field is used to select the edge of the TxCLK_n input that the Transmit Section of Channel_n will use to sample the TPDATA_n and TNDATA_n input pins, as described below. 0 - Configures the Transmit Section (within the corresponding channel) to sample the TPDATA_n and TNDATA_n input pins upon the falling edge of TxCLK_n. 1 - Configures the Transmit Section (within the corresponding channel) to sample the TPDATA_n and TNDATA_n input pins upon the rising edge of TxCLK_n. ***NOTE:*** *Whenever this configuration setting is accomplished via the Host Mode, it is done on a per-channel basis.*
0	TxLEV	R/W	0	**Transmit Line Build-Out Select - Channel_n:** This READ/WRITE bit-field is used to either enable or disable the Transmit Line Build-Out (e.g., pulse-shaping) circuit within the corresponding channel. The user should set this bit-field to either "0" or to "1" based upon the following guidelines. 0 - If the cable length between the Transmit Output (of the corresponding Channel) and the DSX-3/STSX-1 location is 225 feet or less. 1 - If the cable length between the Transmit Output (of the corresponding Channel) and the DSX-3/STSX-1 location is 225 feet or more. The user must follow these guidelines in order to insure that the Transmit Section (of Channel_n) will always generate a DS3 pulse that complies with the Isolated Pulse Template requirements per Bellcore GR-499-CORE, or an STS-1 pulse that complies with the Pulse Template requirements per Telcordia GR-253-CORE. ***NOTE:*** *This bit-field is ignored if the channel has been configured to operate in the E3 Mode.*

TABLE 28: RECEIVE CONTROL REGISTER - CHANNEL 0 ADDRESS LOCATION = 0X05

Channel 1 Address Location = 0x0D

Channel 2 Address Location = 0x15

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		Disable DLOS Detector	Disable ALOS Detector	RxCLKINV	LOSMUT Enable	Receive Monitor Mode Enable	Receive Equalizer Enable
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
7 - 6	Unused	R/O	0	
5	Disable DLOS Detector	R/W	0	**Disable Digital LOS Detector - Channel_n:** This READ/WRITE bit-field is used to either enable or disable the Digital LOS (Loss of Signal) Detector within Channel_n, as described below. 0 - Enables the Digital LOS Detector within Channel_n. ***NOTE:*** *This is the default condition.* 1 - Disables the Digital LOS Detector within Channel_n. ***NOTE:*** *This bit-field is only active if Channel_n has been configured to operate in the DS3 or STS-1 Modes.*
4	Disable ALOS Detector	R/W	0	**Disable Analog LOS Detector - Channel_n:** This READ/WRITE bit-field is used to either enable or disable the Analog LOS (Loss of Signal) Detector within Channel_n, as described below. 0 - Enables the Analog LOS Detector within Channel_n. ***NOTE:*** *This is the default condition.* 1 - Disables the Analog LOS Detector within Channel_n. ***NOTE:*** *This bit-field is only active if Channel_n has been configured to operate in the DS3 or STS-1 Modes.*
3	RxCLKINV	R/W	0	**Receive Clock Invert Select - Channel_n:** This READ/WRITE bit-field is used to select the edge of the RCLK_n output that the Receive Section of Channel_n will use to output the recovered data via the RPOS_n and RNEG_n output pins, as described below. 0 - Configures the Receive Section (within the corresponding channel) to output the recovered data via the RPOS_n and RNEG_n output pins upon the rising edge of RCLK_n. 1 - Configures the Receive Section (within the corresponding channel) to output the recovered data via the RPOS_n and RNEG_n output pins upon the falling edge of RCLK_n.

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
2	LOSMUT Enable	R/W	0	**Muting upon LOS Enable - Channel_n:** This READ/WRITE bit-field is used to configure the Receive Section (within Channel_n) to automatically pull their corresponding Recovered Data Output pins (e.g., RPOS_n and RNEG_n) to GND anytime (and for the duration that) the Receive Section declares the LOS defect condition. In other words, this feature (if enabled) will cause the Receive Channel to automatically mute the Recovered data anytime (and for the duration that) the Receive Section declares the LOS defect condition. 0 - Disables the Muting upon LOS feature. In this setting the Receive Section will NOT automatically mute the Recovered Data whenever it is declaring the LOS defect condition. 1 - Enables the Muting upon LOS feature. In this setting the Receive Section will automatically mute the Recovered Data whenever it is declaring the LOS defect condition.
1	Receive Monitor Mode Enable	R/W	0	**Receive Monitor Mode Enable - Channel_n:** This READ/WRITE bit-field is used to configure the Receive Section of Channel_n to operate in the Receive Monitor Mode. If the user configures the Receive Section to operate in the Receive Monitor Mode, then it will be able to receive a nominal DSX-3/STSX-1 signal that has been attenuator by 20dB of flat loss along with 6dB of cable loss, in an error-free manner, and without declaring the LOS defect condition. 0 - Configures the corresponding channel to operate in the Normal Mode. 1 - Configure the corresponding channel to operate in the Receive Monitor Mode.
0	Receive Equalizer Enable	R/W	0	**Receive Equalizer Enable - Channel_n:** This READ/WRITE register bit is used to either enable or disable the Receive Equalizer block within the Receive Section of Channel_n, as listed below. 0 - Disables the Receive Equalizer within the corresponding channel. 1 - Enables the Receive Equalizer within the corresponding channel. ***NOTE:*** *For virtually all applications, we recommend that the user set this bit-field to "1" (for all three channels) and enable the Receive Equalizer.*

TABLE 29: CHANNEL CONTROL REGISTER - CHANNEL 0 ADDRESS LOCATION = 0X06

Channel 1 Address Location = 0x0E

Channel 2 Address Location = 0x16

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		PRBS Enable Ch_n	RLB_n	LLB_n	E3_n	STS-1/$\overline{DS3}$_n	SR/$\overline{DR}$_n
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
7 - 6	Unused	R/O	0	
5	PRBS Enable	R/W	0	**PRBS Generator and Receiver Enable - Channel_n:** This READ/WRITE bit-field is used to either enable or disable the PRBS Generator and Receiver within a given Channel of the XRT75L03D. If the user enables the PRBS Generator and Receiver, then the following will happen. **1.** The PRBS Generator (which resides within the Transmit Section of the Channel) will begin to generate an unframed, 2^15-1 PRBS Pattern (for DS3 and STS-1 applications) and an unframed, 2^23-1 PRBS Pattern (for E3 applications). **2.** The PRBS Receiver (which resides within the Receive Section of the Channel) will now be enabled and will begin to search the incoming data for the above-mentioned PRBS patterns. 0 - Disables both the PRBS Generator and PRBS Receiver within the corresponding channel. 1 - Enables both the PRBS Generator and PRBS Receiver within the corresponding channel. ***NOTES:*** *1. To check and monitor PRBS Bit Errors, Bit 0 (SR/$\overline{DR}$_n) within this register Must be set to "0". This step will configure the RNEG_n/LCV_n output pin to function as the PRBS Error Indicator. In this case, external glue logic will be needed to monitor and count the number of PRBS Bit Errors that are detected by the PRBS Receiver.* *2. If the user enables the PRBS Generator and PRBS Receiver, then the Channel will ignore the data that is being accepted from the System-side Equipment (via the TPDATA_n and TNDATA_n input pins) and will overwrite this outbound data with the PRBS Pattern.* *3. Use of the PRBS Generator and Receiver is only available through the Host Mode.*

<table>
<tr><th>BIT NUMBER</th><th>NAME</th><th>TYPE</th><th>DEFAULT VALUE</th><th>DESCRIPTION</th></tr>
<tr><td>4</td><td>RLB_n</td><td>R/W</td><td>0</td><td>Loop-Back Select - RLB Bit - Channel_n:
This READ/WRITE bit-field along with the corresponding LLB_n bit-field is used to configure a given channel (within the XRT75L03D) into various loop-back modes.
The relationship between the settings for this input pin, the corresponding LLB_n bit-field and the resulting Loop-back Mode is presented below.

<table>
<tr><th>LLB_n</th><th>RLB_n</th><th>Loop-back Mode</th></tr>
<tr><td>0</td><td>0</td><td>Normal (No Loop-back) Mode</td></tr>
<tr><td>0</td><td>1</td><td>Remote Loop-back Mode</td></tr>
<tr><td>1</td><td>0</td><td>Analog Local Loop-back Mode</td></tr>
<tr><td>1</td><td>1</td><td>Digital Local Loop-back Mode</td></tr>
</table>
</td></tr>
<tr><td>3</td><td>LLB_n</td><td>R/W</td><td>0</td><td>Loop-Back Select - LLB Bit-field - Channel_n:
Please see the description (above) for RLB_n.</td></tr>
<tr><td>2</td><td>E3_n</td><td>R/W</td><td>0</td><td>E3 Mode Select - Channel_n:
This READ/WRITE bit-field, along with Bit 1 (STS-1/ $\overline{DS3}$_n) within this particular register, is used to configure a given channel (of the XRT75L03D) into either the DS3, E3 or STS-1 Modes, as depicted below.
0 - Configures Channel_n to operate in either the DS3 or STS-1 Modes, depending upon the state of Bit 1 (STS-1/ $\overline{DS3}$_n) within this same register.
1- Configures Channel_n to operate in the E3 Mode.</td></tr>
</table>

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
1	STS-1/$\overline{DS3}$_n	R/W	0	**STS-1/DS3 Mode Select - Channel_n:** This READ/WRITE bit-field, along with Bit 2 (E3_n) is used to configure a given channel (within the XRT75L03D) into either the DS3, E3 or STS-1 Modes. 0 - Configures Channel_n to operate in the DS3 Mode (provided by Bit 2 [E3_n], within this same register) has been set to "0"). 1 - Configures Channel_n to operate in the STS-1 Mode (provided that Bit 2 [E3_n], within the same register) has been set to "0". ***NOTE:*** *This bit-field is ignored if Bit 2 (E3_n) has been set to "1". In this case, Channel_n will be configured to operate in the E3 Mode.*
0	SR/$\overline{DR}$_n	R/W	0	**Single-Rail/Dual-Rail Select - Channel_n:** This READ/WRITE bit-field is used to configure Channel_n to operate in either the Single-Rail or Dual-Rail Mode. If the user configures the Channel to operate in the Single-Rail Mode, then all of the following will happen. • The B3ZS/HDB3 Encoder and Decoder blocks (within Channel_n) will be enabled. • The Transmit Section of Channel_n will accept all of the outbound data (from the System-side Equipment) via the TPDATA_n (or TxDATA_n) input pin. • The Receive Section of each channel will output all of the recovered data (to the System-side Equipment) via the RPOS_n output pin. • The corresponding RNEG_n/LCV_n output pin will now function as the LCV (Line Code Violation or Excessive Zero Event) indicator output pin for Channel_n. If the user configures Channel_n to operate in the Dual-Rail Mode, then all of the following will happen. • The B3ZS/HDB3 Encoder and Decoder blocks of Channel_n will be disabled. • The Transmit Section of Channel_n will be configured to accept positive-polarity data via the TPDATA_n input pin and negative-polarity data via the TNDATA_n input pin. • The Receive Section of Channel_n will pulse the RPOS_n output pin "High" (for one period of RCLK_n) for each time a positive-polarity pulse is received via the RTIP_n/RRING_n input pins. Likewise, the Receive Section of each channel will also pulse the RNEG_n output pin "High" (for one period of RCLK_n) for each time a negative-polarity pulse is received via the RTIP_n/RRING_n input pins. 0 - Configures Channel_n to operate in the Dual-Rail Mode. 1 - Configures Channel_n to operate in the Single-Rail Mode.

TABLE 30: JITTER ATTENUATOR CONTROL REGISTER - CHANNEL 0 ADDRESS LOCATION = 0X07

Channel 1 Address Location = 0x0F

Channel 2 Address Location = 0x17

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			SONET APS Recovery Time Disable Ch_n	JA RESET Ch_n	JA1 Ch_n	JA in Tx Path Ch_n	JA0 Ch_n
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	NAME	TYPE	DEFAULT VALUE	DESCRIPTION
7 - 3	Unused	R/O	0	
4	SONET APS Recovery Time Mode Disable Ch_n	R/W	O	**SONET APS Recovery Time Mode Disable - Channel n:** This READ/WRITE bit-field is used to either enable or disable the "SONET APS Recovery Time" Mode within the Jitter Attenuator, associated with Channel n. If this feature is enabled the Jitter Attenuator (associated with Channel n) will be configured such that the user's system will be able to comply with the APS Recovery Time requirements of 50ms (per Telcordia GR-253-CORE). If this feature is disabled the System using the XRT75L03D will NOT comply with the APS Recovery Time requirements of 50ms. ***NOTE:*** *In this case, "APS Recovery Time" is defined as the amount of time that will elapse between (a) the instant that Automatic Protection Switching (APS) is employed (either "automatically" or upon Software Command), and (b) the instant that an entity (which is responsible for acquiring and maintaining DS3/E3 frame synchronization with the DS3/E3 data-stream that has been de-mapped from SONET by the Mapper device) has re-acquired DS3/E3 frame synchronization, after the APS event.* 0 - Enables the "SONET APS Recovery Time" Mode. 1 - Disables the "SONET APS Recovery Time" Mode.

<table>
<tr><th>BIT NUMBER</th><th>NAME</th><th>TYPE</th><th>DEFAULT VALUE</th><th>DESCRIPTION</th></tr>
<tr><td>3</td><td>JA RESET Ch_n</td><td>R/W</td><td>0</td><td>Jitter Attenuator RESET - Channel_n:
Writing a "0 to 1" transition within this bit-field will configure the Jitter Attenuator (within Channel_n) to execute a RESET operation.
Whenever the user executes a RESET operation, then all of the following will occur.
• The READ and WRITE pointers (within the Jitter Attenuator FIFO) will be reset to their default values.
• The contents of the Jitter Attenuator FIFO will be flushed.
NOTE: The user must follow up any "0 to 1" transition with the appropriate write operate to set this bit-field back to "0", in order to resume normal operation with the Jitter Attenuator.</td></tr>
<tr><td>2</td><td>JA1 Ch_n</td><td>R/W</td><td>0</td><td>Jitter Attenuator Configuration Select Input - Bit 1:
This READ/WRITE bit-field, along with Bit 0 (JA0 Ch_n) is used to do any of the following.
• To enable or disable the Jitter Attenuator corresponding to Channel_n.
• To select the FIFO Depth for the Jitter Attenuator within Channel_n.
The relationship between the settings of these two bit-fields and the Enable/Disable States, and FIFO Depths is presented below.
<table><tr><th>JA0</th><th>JA1</th><th>Jitter Attenuator Mode</th></tr><tr><td>0</td><td>0</td><td>FIFO Depth = 16 bits</td></tr><tr><td>0</td><td>1</td><td>FIFO Depth = 32 bits</td></tr><tr><td>1</td><td>0</td><td>SONET/SDH De-Sync Mode</td></tr><tr><td>1</td><td>1</td><td>Jitter Attenuator Disabled</td></tr></table></td></tr>
<tr><td>1</td><td>JA in Tx Path Ch_n</td><td>R/W</td><td>0</td><td>Jitter Attenuator in Transmit/Receive Path Select Bit:
This input pin is used to configure the Jitter Attenuator (within Channel_n) to operate in either the Transmit or Receive path, as described below.
0 - Configures the Jitter Attenuator (within Channel_n) to operate in the Receive Path.
1 - Configures the Jitter Attenuator (within Channel_n) to operate in the Transmit Path.</td></tr>
<tr><td>0</td><td>JA0 Ch_n</td><td>R/W</td><td>0</td><td>Jitter Attenuator Configuration Select Input - Bit 0:
Please see the description for Bit 2 (JA1 Ch_n).</td></tr>
</table>

8.0 DIAGNOSTIC FEATURES:

8.1 *PRBS Generator and Detector:*

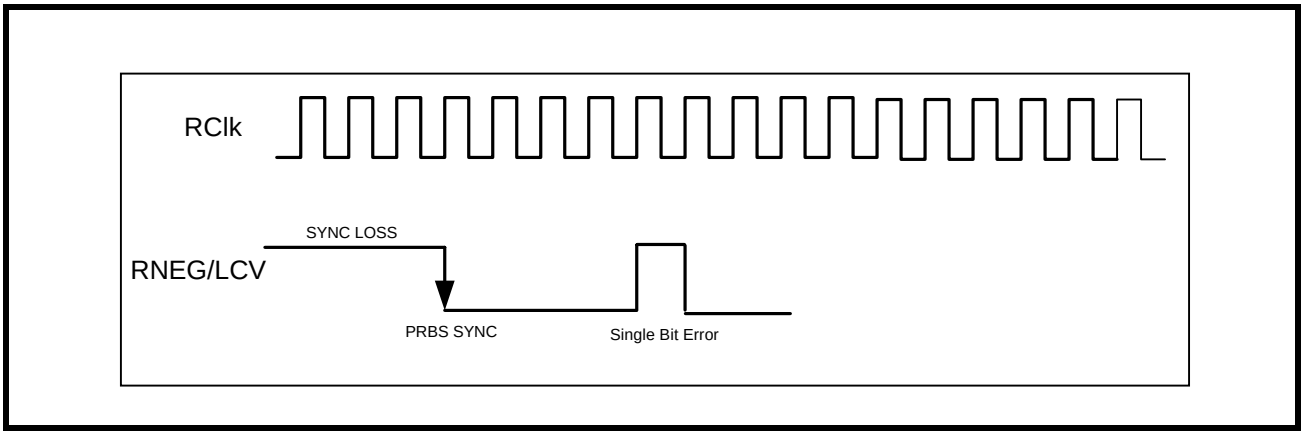
The XRT75L03D contains an on-chip Pseudo Random Binary Sequence (PRBS) generator and detector for diagnostic purpose. This feature is only available in Host mode. With the PRBSEN_n bit = "1", the transmitter will send out PRBS of 2^{23}-1 in E3 rate or 2^{15}-1 in STS-1/DS3 rate. At the same time, the receiver PRBS detector is also enabled. When the correct PRBS pattern is detected by the receiver, the RNEG/LCV pin will go "Low" to indicate PRBS synchronization has been achieved. When the PRBS detector is not in sync the PRBSLS bit will be set to "1" and RNEG/LCV pin will go "High".

With the PRBS mode enabled, the user can also insert a single bit error by toggling "INSPRBS" bit. This is done by writing a "1" to INSPRBS bit. The receiver at RNEG/LCV pin will pulse "High" for one RxClk cycle for every bit error detected. Any subsequent single bit error insertion must be done by first writing a "0" to INSPRBS bit and followed by a "1".

Figure 25 shows the status of RNEG/LCV pin when the XRT75L03D is configured in PRBS mode.

NOTE: *In PRBS mode, the device is forced to operate in Single-Rail Mode.*

FIGURE 25. PRBS MODE



8.2 *LOOPBACKS:*

The XRT75L03D offers three loopback modes for diagnostic purposes. In Hardware mode, the loopback modes are selected via the RLB_n and LLB_n pins. In Host mode, the RLB_n and LLB_n bits n the Channel control registers select the loopback modes.

8.2.1 ANALOG LOOPBACK:

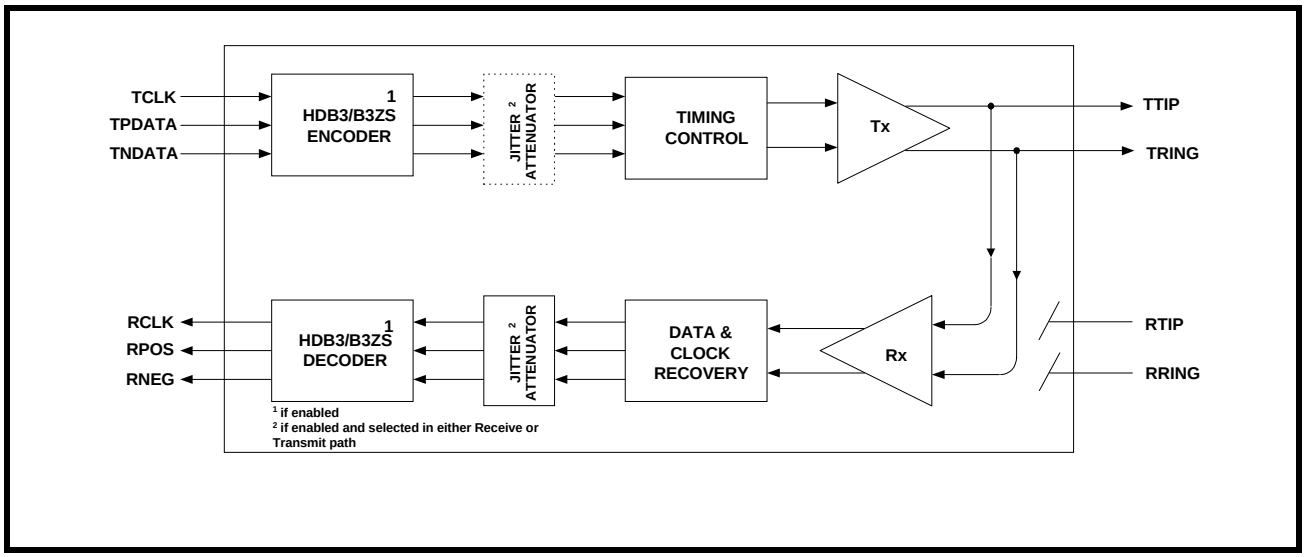
In this mode, the transmitter outputs (TTIP_n and TRING_n) are connected internally to the receiver inputs (RTIP_n and RRING_n) as shown in Figure 26. Data and clock are output at RCLK_n, RPOS_n and RNEG_n pins for the corresponding transceiver. Analog loopback exercises most of the functional blocks of the device including the jitter attenuator which can be selected in either the transmit or receive path.

XRT75L03D can be configured in Analog Loopback either in Hardware mode via the LLB_n and RLB_n pins or in Host mode via LLB_n and RLB_n bits in the channel control registers.

NOTES:

1. *In the Analog loopback mode, data is also output via TTIP_n and TRING_n pins.*
2. *Signals on the RTIP_n and RRING_n pins are ignored during analog loopback.*

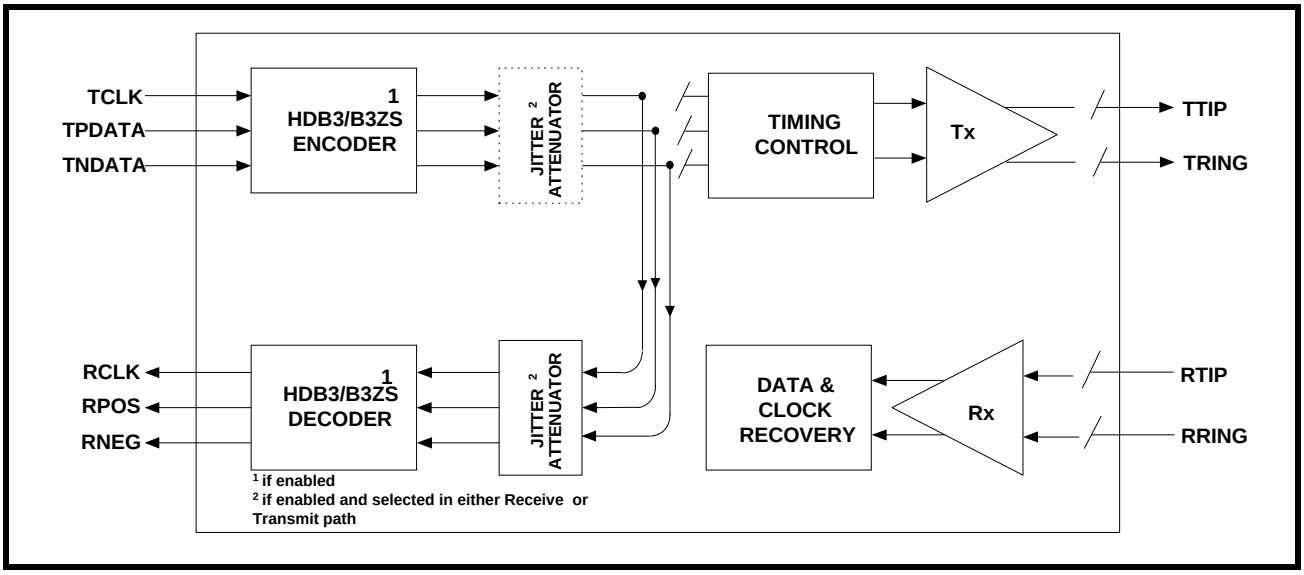
FIGURE 26. ANALOG LOOPBACK



8.2.2 DIGITAL LOOPBACK:

The Digital Loopback function is available either in Hardware mode or Host mode. When the Digital Loopback is selected, the transmit clock (TxClk_n) and transmit data inputs (TPDATA_n & TNDATA_n) are looped back and output onto the RxClk_n, RPOS_n and RNEG_n pins as shown in Figure 27.

FIGURE 27. DIGITAL LOOPBACK



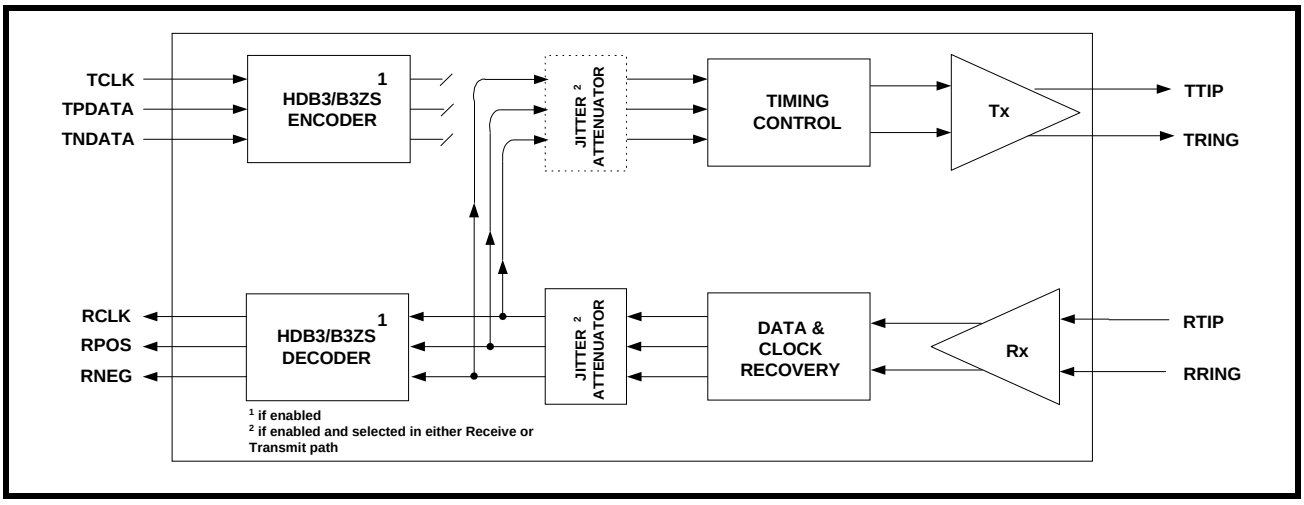
8.2.3 REMOTE LOOPBACK:

With Remote loopback activated as shown in Figure 28, the receive data on RTIP and RRING is looped back after the jitter attenuator (if selected in receive or transmit path) to the transmit path using RxClk as transmit timing. The receive data is also output via the RPOS and RNEG pins.

During the remote loopback mode, if the jitter attenuator is selected in the transmit path, the receive data after the Clock and Data Recovery Block is looped back to the transmit path and passed through the jitter attenuator using RxClk as the transmit timing.

NOTE: *Input signals on TxClk, TPDATA and TNDATA are ignored during Remote loopback.*

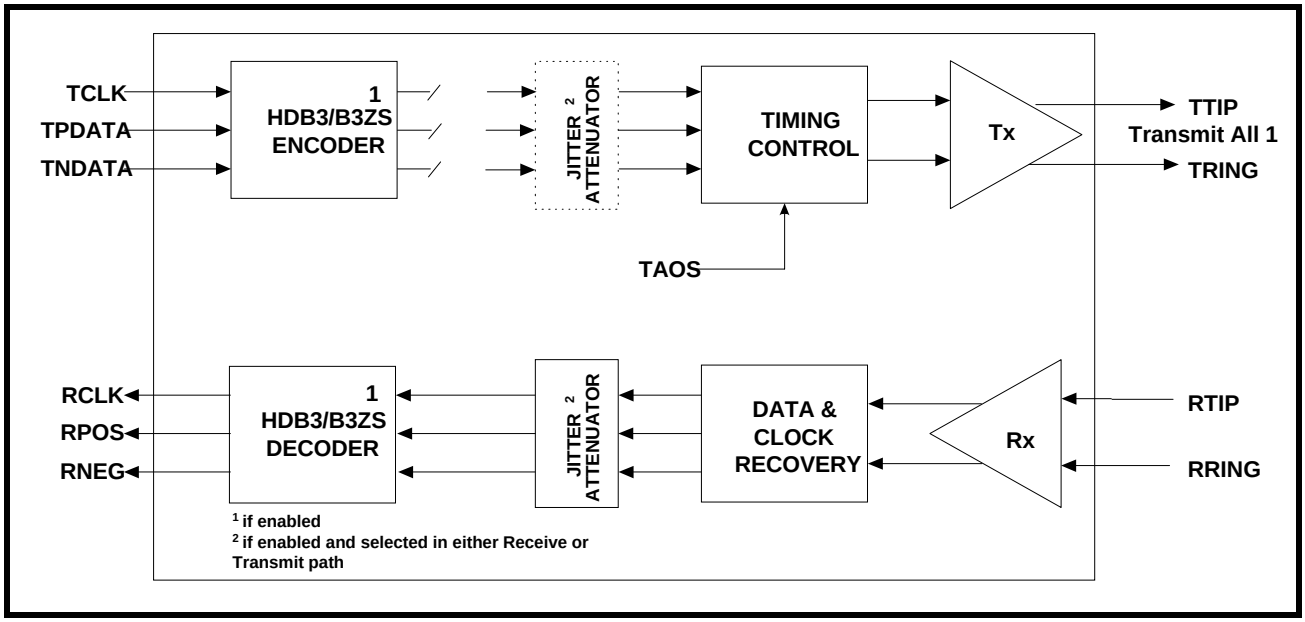
FIGURE 28. REMOTE LOOPBACK



8.3 *TRANSMIT ALL ONES (TAOS):*

Transmit All Ones (TAOS) can be set either in Hardware mode by pulling the TAOS_n pins “High” or in Host mode by setting the TAOS_n control bits to “1” in the Channel control registers. When the TAOS is set, the Transmit Section generates and transmits a continuous AMI all “1’s” pattern on TTIP_n and TRING_n pins. The frequency of this “1’s” pattern is determined by TClk_n.TAOS data path is shown in Figure 29. TAOS does not operate in Analog loopback or Remote Digital loopback mode. It will function in Digital loopback mode.

FIGURE 29. TRANSMIT ALL ONES (TAOS)



9.0 THE SONET/SDH DE-SYNC FUNCTION WITHIN THE XRT75L03D

The XRT75L03D LIU IC is very similar to the XRT75L03 in that they are both 3-Channel DS3/E3/STS-1 LIU devices that also contain Jitter Attenuator blocks within each of the three channels. They are also pin to pin compatible with each other. However, the Jitter Attenuators within the XRT75L03D has some enhancements over and above those within the XRT75L03 (non-D) device. The Jitter Attenuator blocks within the XRT75L03D will support all of the modes and features that exist in the XRT75L03 (non-D) device and in addition they also support a SONET/SDH De-Sync Mode not available within the XRT75L03D.

NOTE: *The "D" suffix within the part number, XRT75L03D stands for "De-Sync".*

The SONET/SDH De-Sync feature of the Jitter Attenuator blocks in the XRT75L03D permits the user to design a SONET/SDH PTE (Path Terminating Equipment) that will comply with all of the following Intrinsic Jitter and Wander requirements.

- **For SONET Applications**
  - Category I Intrinsic Jitter Requirements per Telcordia GR-253-CORE (for DS3 Applications)
  - ANSI T1.105.03b-1997 - SONET Jitter at Network Interfaces - DS3 Wander Supplement
- **For SDH Applications**
  - Jitter and Wander Generation Requirements per ITU-T G.783 (for DS3 and E3 Applications)

Specifically, if the user designs in the XRT75L03D along with a SONET/SDH Mapper IC (which can be realized as either a standard product or as a custom logic solution, in an ASIC or FPGA), then the followind can be accomplished;

- The Mapper can receive an STS-N or an STM-M signal (which is carrying asynchronously-mapped DS3 and/or E3 signals) and byte de-interleave this data into N STS-1 or 3*M VC-3 signals
- The Mapper will then terminate these STS-1 or VC-3 signals and will de-map out this DS3 or E3 data from the incoming STS-1 SPEs or VC-3s, and output this DS3 or E3 to the DS3/E3 Facility-side towards the XRT75L03D
- This DS3 or E3 signal (as it is output from these Mapper devices) will contain a large amount intrinsic jitter and wander due to (1) the process of asynchronously mapping a DS3 or E3 signal into a SONET or SDH signal, (2) the occurrence of Pointer Adjustments within the SONET or SDH signal (transporting these DS3 or E3 signals) as it traverses the SONET/SDH network, and (3) clock gapping.
- When the XRT75L03D has been configured to operate in the "SONET/SDH De-Sync" Mode, then it will (1) accept this jittery DS3 or E3 clock and data signal from the Mapper device (via the Transmit System-side interface) and (2) through the Jitter Attenuator, the XRT75L03D will reduce the Jitter and Wander amplitude within these DS3 or E3 signals such that they (when output onto the line) will comply with the above-mentioned intrinsic jitter and wander specifications.

9.1 *BACKGROUND AND DETAILED INFORMATION - SONET DE-SYNC APPLICATIONS*

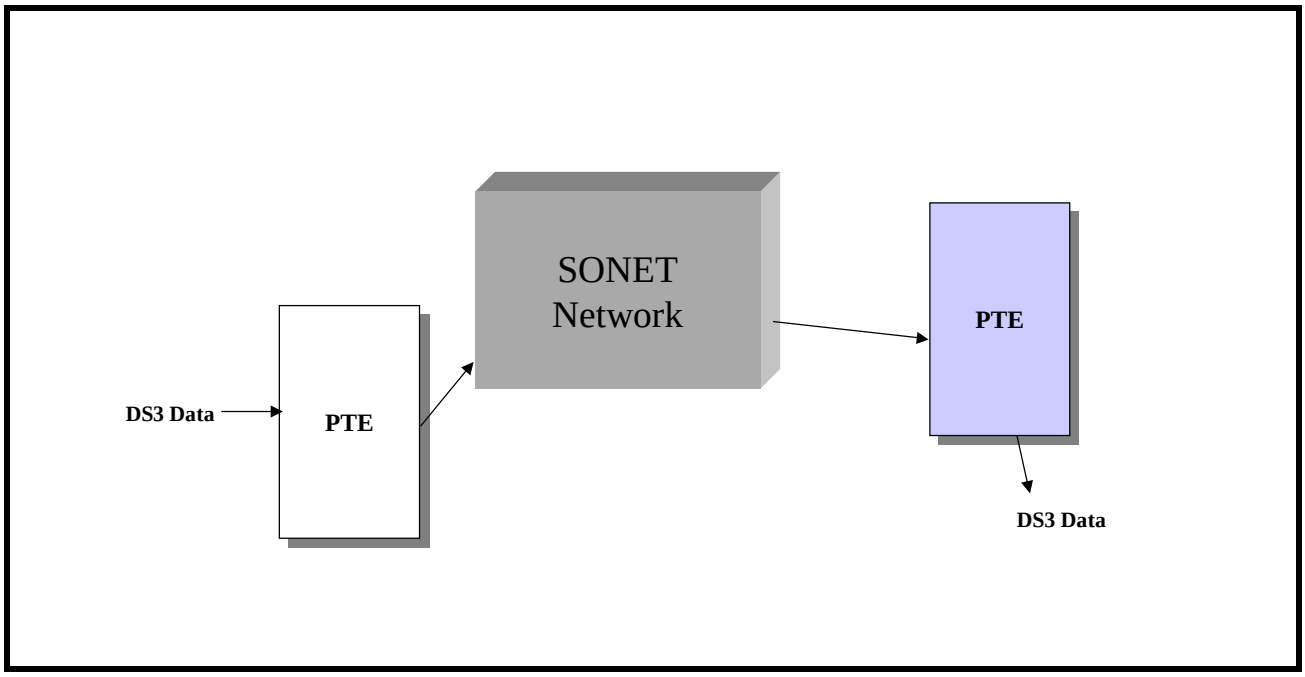
This section provides an in-depth discussion on the mechanisms that will cause Jitter and Wander within a DS3 or E3 signal that is being transported across a SONET or SDH Network. A lot of this material is introductory, and can be skipped by the engineer that is already experienced in SONET/SDH designs. In this case, the user should proceed directly to “Section 9.8, Designing with the XRT75L03D” on page 118, which describes how to configure the XRT75L03D in the appropriate set of modes in order to support this application.

In the wide-area network (WAN) in North America it is often necessary to transport a DS3 signal over a long distance (perhaps over a thousand miles) in order to support a particular service. Now rather than realizing this transport of DS3 data, by using over a thousand miles of coaxial cable (interspaced by a large number of DS3 repeaters) a common thing to do is to route this DS3 signal to a piece of equipment (such as a Terminal MUX, which in the "SONET Community" is known as a PTE or Path Terminating Equipment). This Terminal MUX will asynchronously map the DS3 signal into a SONET signal. At this point, the SONET network will now transport this asynchronously mapped DS3 signal from one PTE to another PTE (which is located at the other end of the SONET network). Once this SONET signal arrives at the remote PTE, this DS3 signal will then be extracted from the SONET signal, and will be output to some other DS3 Terminal Equipment for further processing.

Similar things are done outside of North America. In this case, this DS3 or E3 signal is routed to a PTE, where it is asynchronously mapped into an SDH signal. This asynchronously mapped DS3 or E3 signal is then transported across the SDH network (from one PTE to the PTE at the other end of the SDH network). Once this SDH signal arrives at the remote PTE, this DS3 or E3 signal will then be extracted from the SDH signal, and will be output to some other DS3/E3 Terminal Equipment for further processing.

Figure 30 presents an illustration of this approach to transporting DS3 data over a SONET Network

FIGURE 30. A SIMPLE ILLUSTRATION OF A DS3 SIGNAL BEING MAPPED INTO AND TRANSPORTED OVER THE SONET NETWORK



As mentioned above a DS3 or E3 signal will be asynchronously mapped into a SONET or SDH signal and then transported over the SONET or SDH network. At the remote PTE this DS3 or E3 signal will be extracted (or de-mapped) from this SONET or SDH signal, where it will then be routed to DS3 or E3 terminal equipment for further processing.

In order to insure that this "de-mapped" DS3 or E3 signal can be routed to any industry-standard DS3 or E3 terminal equipment, without any complications or adverse effect on the network, the Telcordia and ITU-T standard committees have specified some limits on both the Intrinsic Jitter and Wander that may exist within these DS3 or E3 signals as they are de-mapped from SONET/SDH. As a consequence, all PTEs that maps and de-mapped DS3/E3 signals into/from SONET/SDH must be designed such that the DS3 or E3 data that is de-mapped from SONET/SDH by these PTEs must meet these Intrinsic Jitter and Wander requirements.

As mentioned above, the XRT75L03D can assist the System Designer (of SONET/SDH PTE) by insuring that their design will meet these Intrinsic Jitter and Wander requirements.

This section of the data sheet will present the following information to the user.

- Some background information on Mapping DS3/E3 signals into SONET/SDH and de-mapping DS3/E3 signals from SONET/SDH.
- A brief discussion on the causes of jitter and wander within a DS3 or E3 signal that mapped into a SONET/SDH signal, and is transported across the SONET/SDH Network.
- A brief review of these Intrinsic Jitter and Wander requirements in both SONET and SDH applications.
- A brief review on the Intrinsic Jitter and Wander measurement results (of a de-mapped DS3 or E3 signal) whenever the XRT75L03D is used in a system design.

- A detailed discussion on how to design with and configure the XRT75L03D such that the end-system will meet these Intrinsic Jitter and Wander requirements.

In a SONET system, the relevant specification requirements for Intrinsic Jitter and Wander (within a DS3 signal that is mapped into and then de-mapped from SONET) are listed below.

- Telcordia GR-253-CORE Category I Intrinsic Jitter Requirements for DS3 Applications (Section 5.6), and
- ANSI T1.105.03b-1997 - SONET Jitter at Network Interfaces - DS3 Wander Supplement

In general, there are three (3) sources of Jitter and Wander within an asynchronously-mapped DS3 signal that the system designer must be aware of. These sources are listed below.

- Mapping/De-Mapping Jitter
- Pointer Adjustments
- Clock Gapping

Each of these sources of jitter/wander will be defined and discussed in considerable detail within this Section. In order to accomplish all of this, this particular section will discuss all of the following topics in details.

- How DS3 data is mapped into SONET, and how this mapping operation contributes to Jitter and Wander within this "eventually de-mapped" DS3 signal.
- How this asynchronously-mapped DS3 data is transported throughout the SONET Network, and how occurrences on the SONET network (such as pointer adjustments) will further contributes to Jitter and Wander within the "eventually de-mapped" DS3 signal.
- A review of the Category I Intrinsic Jitter Requirements (per Telcordia GR-253-CORE) for DS3 applications
- A review of the DS3 Wander requirements per ANSI T1.105.03b-1997
- A review of the Intrinsic Jitter and Wander Capabilities of the XRT75L03D in a typical system application
- An in-depth discussion on how to design with and configure the XRT75L03D to permit the system to the meet the above-mentioned Intrinsic Jitter and Wander requirements

NOTE: *An in-depth discussion on SDH De-Sync Applications will be presented in the next revision of this data sheet.*

9.2 *MAPPING/DE-MAPPING JITTER/WANDER*

Mapping/De-Mapping Jitter (or Wander) is defined as that intrinsic jitter (or wander) that is induced into a DS3 signal by the "Asynchronous Mapping" process. This section will discuss all of the following aspects of Mapping/De-Mapping Jitter.

- How DS3 data is mapped into an STS-1 SPE
- How frequency offsets within either the DS3 signal (being mapped into SONET) or within the STS-1 signal itself contributes to intrinsic jitter/wander within the DS3 signal (being transported via the SONET network).

9.2.1 HOW DS3 DATA IS MAPPED INTO SONET

Whenever a DS3 signal is asynchronously mapped into SONET, this mapping is typically accomplished by a PTE accepting DS3 data (from some remote terminal) and then loading this data into certain bit-fields within a given STS-1 SPE (or Synchronous Payload Envelope). At this point, this DS3 signal has now been asynchronously mapped into an STS-1 signal. In most applications, the SONET Network will then take this particular STS-1 signal and will map it into "higher-speed" SONET signals (e.g., STS-3, STS-12, STS-48, etc.) and will then transport this asynchronously mapped DS3 signal across the SONET network, in this manner. As this "asynchronously-mapped" DS3 signal approaches its "destination" PTE, this STS-1 signal will eventually be de-mapped from this STS-N signal. Finally, once this STS-1 signal reaches the "destination" PTE, then this asynchronously-mapped DS3 signal will be extracted from this STS-1 signal.

9.2.1.1 *A Brief Description of an STS-1 Frame*

In order to be able to describe how a DS3 signal is asynchronously mapped into an STS-1 SPE, it is important to define and understand all of the following.

- The STS-1 frame structure

- The STS-1 SPE (Synchronous Payload Envelope)
- Telcordia GR-253-CORE's recommendation on mapping DS3 data into an STS-1 SPE

An STS-1 frame is a data-structure that consists of 810 bytes (or 6480 bits). A given STS-1 frame can be viewed as being a 9 row by 90 byte column array (making up the 810 bytes). The frame-repetition rate (for an STS-1 frame) is 8000 frames/second. Therefore, the bit-rate for an STS-1 signal is (6480 bits/frame * 8000 frames/sec =) 51.84Mbps.

A simple illustration of this SONET STS-1 frame is presented below in Figure 31.

FIGURE 31. A SIMPLE ILLUSTRATION OF THE SONET STS-1 FRAME

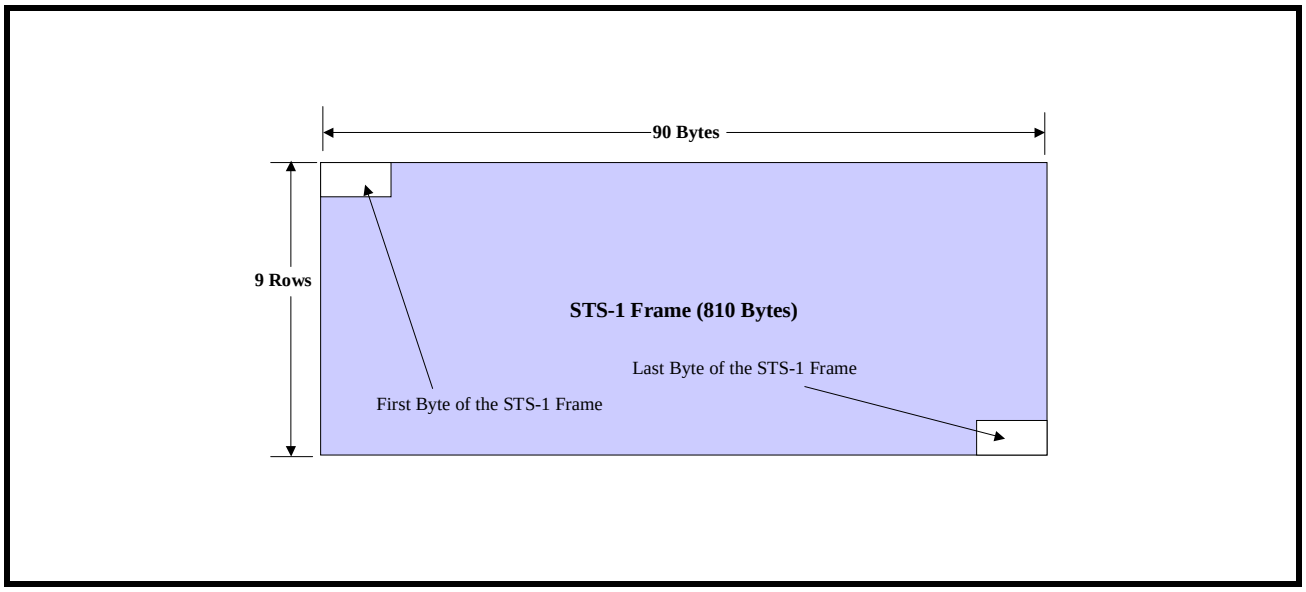


Figure 31 indicates that the very first byte of a given STS-1 frame (to be transmitted or received) is located in the extreme upper left hand corner of the 90 column by 9 row array, and that the very last byte of a given STS-1 frame is located in the extreme lower right-hand corner of the frame structure. Whenever a Network Element transmits a SONET STS-1 frame, it starts by transmitting all of the data, residing within the top row of the STS-1 frame structure (beginning with the left-most byte, and then transmitting the very next byte, to the right). After the Network Equipment has completed its transmission of the top or first row, it will then proceed to transmit the second row of data (again starting with the left-most byte, first). Once the Network Equipment has transmitted the last byte of a given STS-1 frame, it will proceed to start transmitting the very next STS-1 frame.

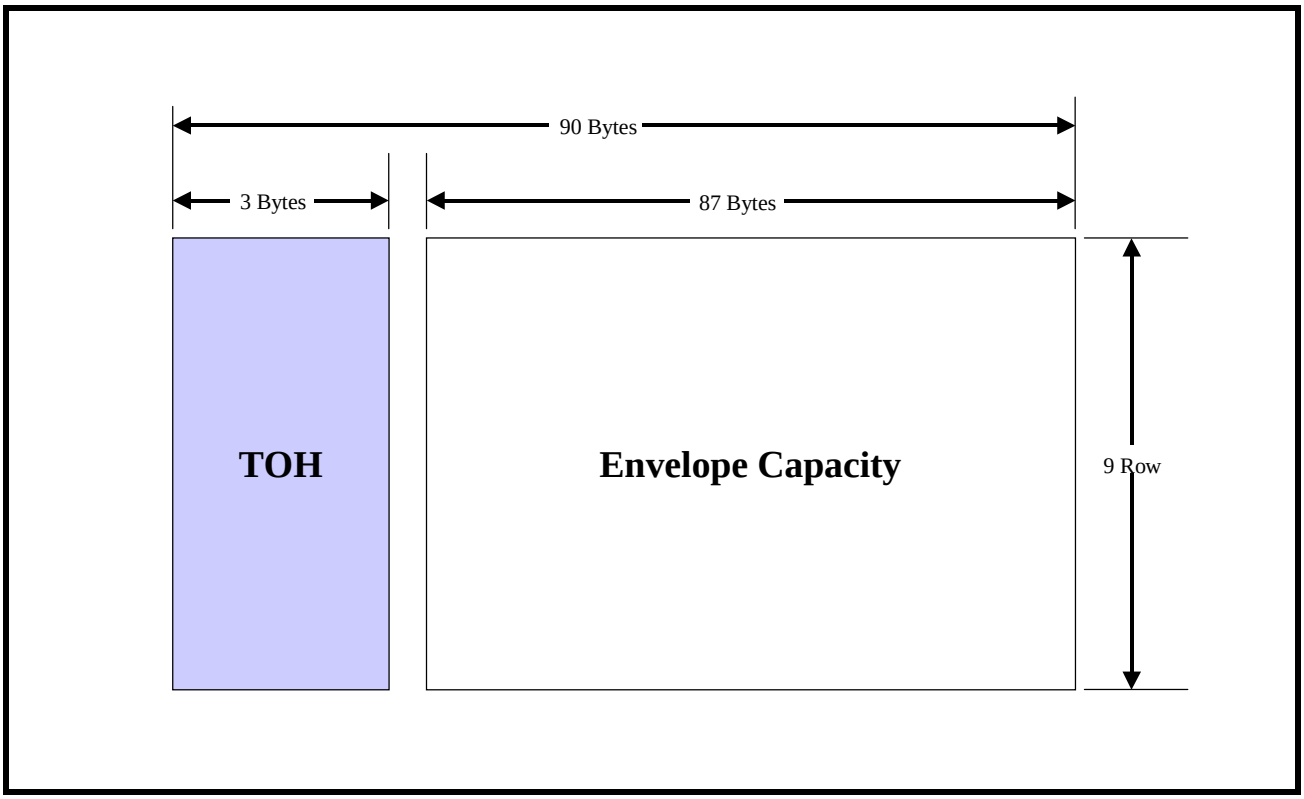
The illustration of the STS-1 frame (in Figure 31) is very simplistic, for multiple reasons. One major reason is that the STS-1 frame consists of numerous types of bytes. For the sake of discussion within this data sheet, the STS-1 frame will be described as consisting of the following types (or groups) of bytes.

- The Transport Overheads (or TOH) Bytes
- The Envelope Capacity Bytes

9.2.1.1.1 The Transport Overhead (TOH) Bytes

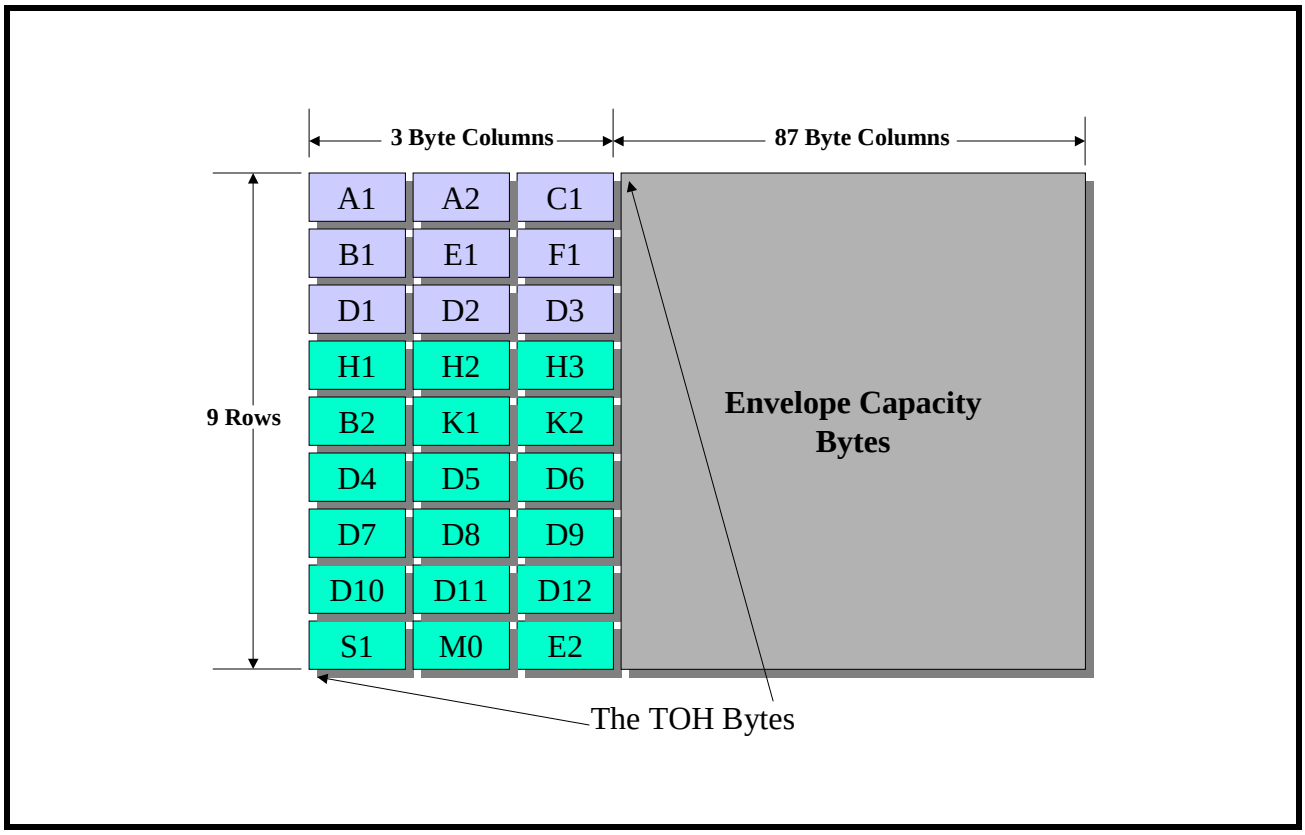
The Transport Overhead or TOH bytes occupy the very first three (3) byte columns within each STS-1 frame. Figure 32 presents another simple illustration of an STS-1 frame structure. However, in this case, both the TOH and the Envelope Capacity bytes are designated in this Figure.

FIGURE 32. A SIMPLE ILLUSTRATION OF THE STS-1 FRAME STRUCTURE WITH THE TOH AND THE ENVELOPE CAPACITY BYTES DESIGNATED



Since the TOH bytes occupy the first three byte columns of each STS-1 frame, and since each STS-1 frame consists of nine (9) rows, then we can state that the TOH (within each STS-1 frame) consists of 3 byte columns x 9 rows = 27 bytes. The byte format of the TOH is presented below in Figure 33.

FIGURE 33. THE BYTE-FORMAT OF THE TOH WITHIN AN STS-1 FRAME



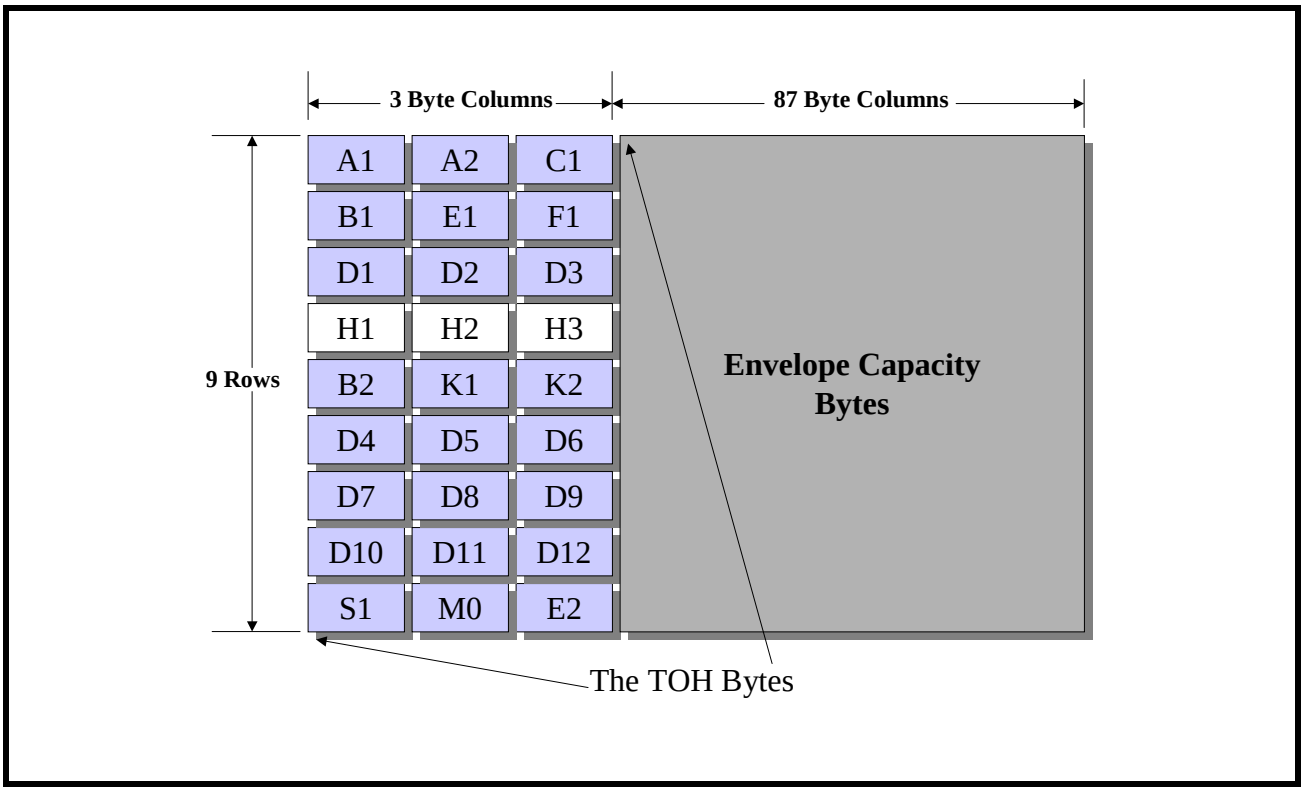
In general, the role/purpose of the TOH bytes is to fulfill the following functions.

- To support STS-1 Frame Synchronization
- To support Error Detection within the STS-1 frame
- To support the transmission of various alarm conditions such as RDI-L (Line - Remote Defect Indicator) and REI-L (Line - Remote Error Indicator)
- To support the Transmission and Reception of "Section Trace" Messages
- To support the Transmission and Reception of OAM&P Messages via the DCC Bytes (Data Communication Channel bytes - D1 through D12 byte)

The roles of most of the TOH bytes is beyond the scope of this Data Sheet and will not be discussed any further. However, there are a three TOH bytes that are important from the stand-point of this data sheet, and will discussed in considerable detail throughout this document. These are the H1 and H2 (e.g., the SPE Pointer) bytes and the H3 (e.g., the Pointer Action) byte.

Figure 34 presents an illustration of the Byte-Format of the TOH within an STS-1 Frame, with the H1, H2 and H3 bytes highlighted.

FIGURE 34. THE BYTE-FORMAT OF THE TOH WITHIN AN STS-1 FRAME



Although the role of the H1, H2 and H3 bytes will be discussed in much greater detail in “Section 9.3, Jitter/ Wander due to Pointer Adjustments” on page 102. For now, we will simply state that the role of these bytes is two-fold.

- To permit a given PTE (Path Terminating Equipment) that is receiving an STS-1 data to be able to locate the STS-1 SPE (Synchronous Payload Envelope) within the Envelope Capacity of this incoming STS-1 data stream and,
- To inform a given PTE whenever Pointer Adjustment and NDF (New Data Flag) events occur within the incoming STS-1 data-stream.

9.2.1.1.2 The Envelope Capacity Bytes within an STS-1 Frame

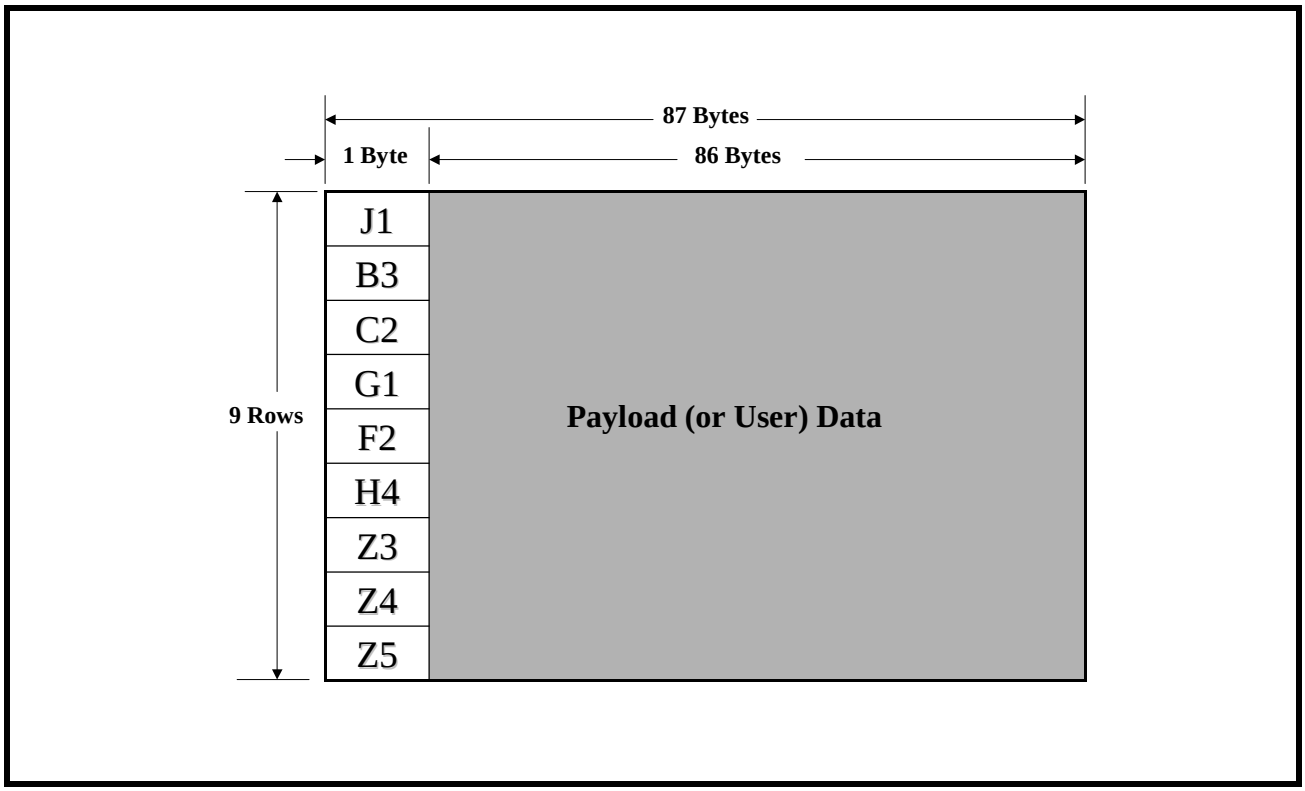
In general, the Envelope Capacity Bytes are any bytes (within an STS-1 frame) that exist outside of the TOH bytes. In short, the Envelope Capacity contains the STS-1 SPE (Synchronous Payload Envelope). In fact, every single byte that exists within the Envelope Capacity also exists within the STS-1 SPE. The only difference that exists between the "Envelope Capacity" as defined in Figure 33 and Figure 34 above and the STS-1 SPE is that the Envelope Capacity is aligned with the STS-1 framing boundaries and the TOH bytes; whereas the STS-1 SPE is NOT aligned with the STS-1 framing boundaries, nor the TOH bytes.

The STS-1 SPE is an "87 byte column x 9 row" data-structure (which is the exact same size as is the Envelope Capacity) that is permitted to "float" within the "Envelope Capacity". As a consequence, the STS-1 SPE (within an STS-1 data-stream) will typically straddle across an STS-1 frame boundary.

9.2.1.1.3 The Byte Structure of the STS-1 SPE

As mentioned above, the STS-1 SPE is an 87 byte column x 9 row structure. The very first column within the STS-1 SPE consists of some overhead bytes which are known as the "Path Overhead" (or POH) bytes. The remaining portions of the STS-1 SPE is available for "user" data. The Byte Structure of the STS-1 SPE is presented below in Figure 35.

FIGURE 35. ILLUSTRATION OF THE BYTE STRUCTURE OF THE STS-1 SPE



In general, the role/purpose of the POH bytes is to fulfill the following functions.

- To support error detection within the STS-1 SPE
- To support the transmission of various alarm conditions such as RDI-P (Path - Remote Defect Indicator) and REI-P (Path - Remote Error Indicator)
- To support the transmission and reception of "Path Trace" Messages

The role of the POH bytes is beyond the scope of this data sheet and will not be discussed any further.

9.2.1.2 *Mapping DS3 data into an STS-1 SPE*

Now that we have defined the STS-1 SPE, we can now describe how a DS3 signal is mapped into an STS-1 SPE. As mentioned above, the STS-1 SPE is basically an 87 byte column x 9 row structure of data. The very first byte column (e.g., in all 9 bytes) consists of the POH (Path Overhead) bytes. All of the remaining bytes within the STS-1 SPE is simply referred to as "user" or "payload" data because this is the portion of the STS-1 signal that is used to transport "user data" from one end of the SONET network to the other. Telcordia GR-253-CORE specifies the approach that one must use to asynchronously map DS3 data into an STS-1 SPE. In short, this approach is presented below in Figure 36.

FIGURE 36. AN ILLUSTRATION OF TELCORDIA GR-253-CORE'S RECOMMENDATION ON HOW MAP DS3 DATA INTO AN STS-1 SPE

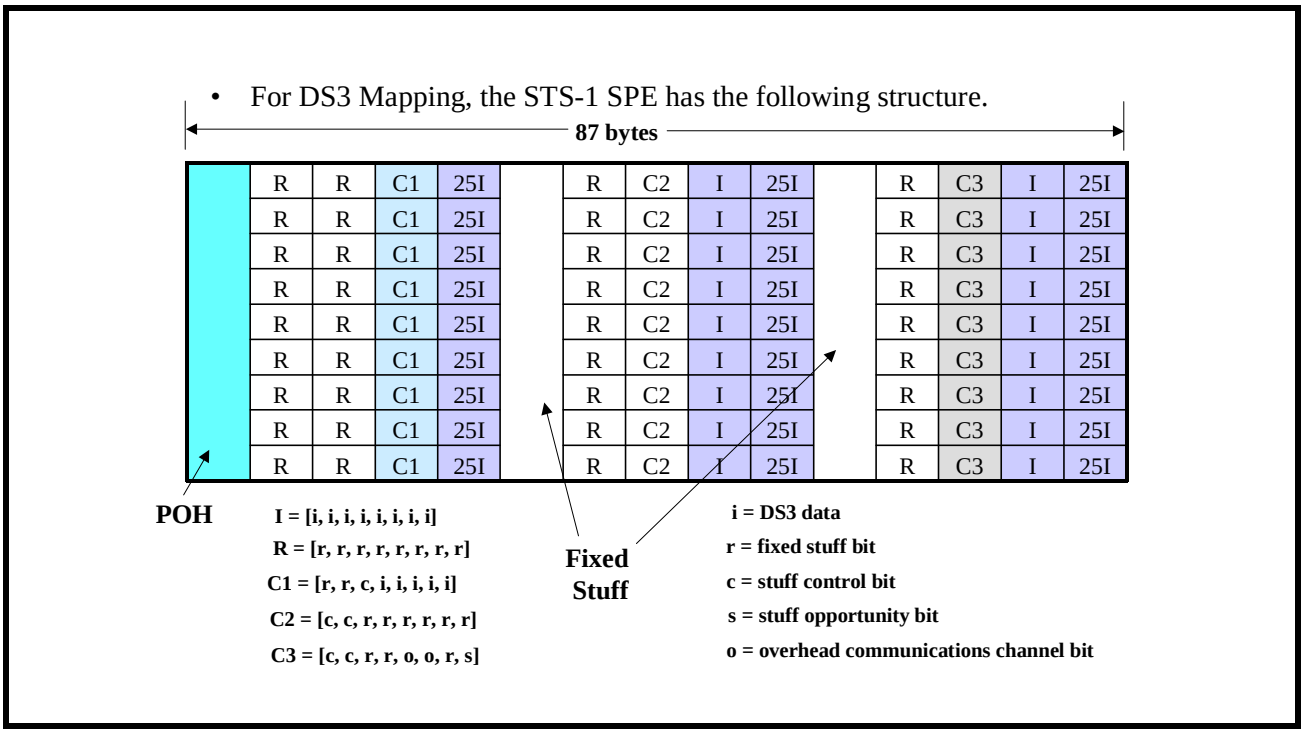


Figure 36 was copied directly out of Telcordia GR-253-CORE. However, this figure can be simplified and redrawn as depicted below in Figure 37.

FIGURE 37. A SIMPLIFIED "BIT-ORIENTED" VERSION OF TELCORDIA GR-253-CORE'S RECOMMENDATION ON HOW TO MAP DS3 DATA INTO AN STS-1 SPE

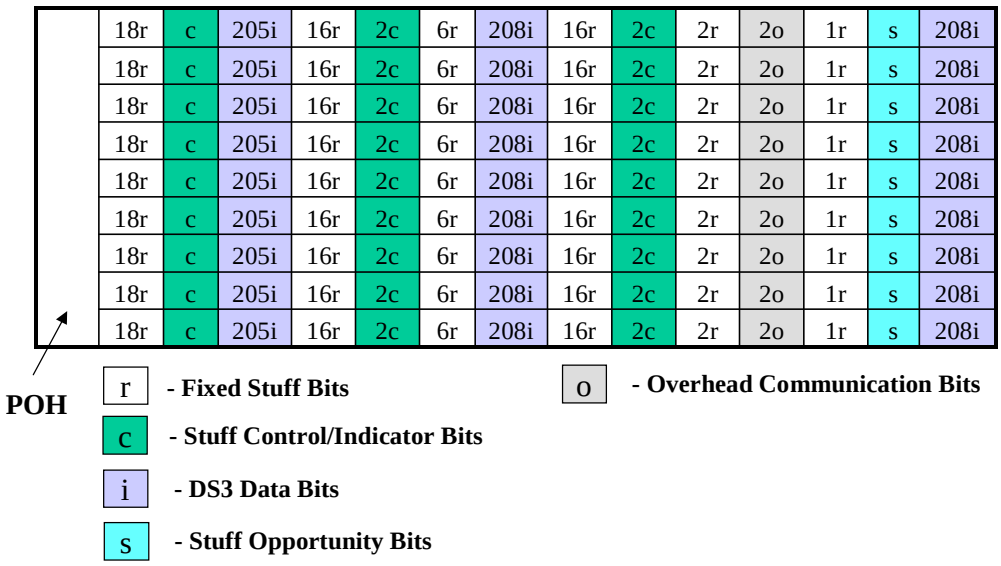


Figure 37 presents an alternative illustration of Telcordia GR-253-CORE's recommendation on how to asynchronously map DS3 data into an STS-1 SPE. In this case, the STS-1 SPE bit-format is expressed purely in the form of "bit-types" and "numbers of bits within each of these types of bits". If one studies this figure closely he/she will notice that this is the same "87 byte column x 9 row" structure that we have been talking about when defining the STS-1 SPE. However, in this figure, the "user-data" field is now defined and is said to consist of five (5) different types of bits. Each of these bit-types play a role when asynchronously mapping a DS3 signal into an STS-1 SPE. Each of these types of bits are listed and described below.

Fixed Stuff Bits

Fixed Stuff bits are simply "space-filler" bits that simply occupy space within the STS-1 SPE. These bit-fields have no functional role other than "space occupation". Telcordia GR-253-CORE does not define any particular value that these bits should be set to. Each of the 9 rows, within the STS-1 SPE will contain 59 of these "fixed stuff" bits.

DS3 Data Bits

The DS3 Data-Bits are (as its name implies) used to transport the DS3 data-bits within the STS-1 SPE. If the STS-1 SPE is transporting a framed DS3 data-stream, then these DS3 Data bits will carry both the "DS3 payload data" and the "DS3 overhead bits". Each of the 9 rows, within the STS-1 SPE will contain 621 of these "DS3 Data bits". This means that each STS-1 SPE contains 5,589 of these DS3 Data bit-fields.

Stuff Opportunity Bits

The "Stuff" Opportunity bits will function as either a "stuff" (or junk) bit, or it will carry a DS3 data-bit. The decision as to whether to have a "Stuff Opportunity" bit transport a "DS3 data-bit" or a "stuff" bit depends upon the "timing differences" between the DS3 data that is being mapped into the STS-1 SPE and the timing source that is driving the STS-1 circuitry within the PTE.

As will be described later on, these "Stuff Opportunity" Bits play a very important role in "frequency-justifying" the DS3 data that is being mapped into the STS-1 SPE. These "Stuff Opportunity" bits also play a critical role in inducing Intrinsic Jitter and Wander within the DS3 signal (as it is de-mapped by the remote PTE).

Each of the 9 rows, within the STS-1 SPE consists of one (1) Stuff Opportunity bit. Hence, there are a total of nine Stuff Opportunity" bits within each STS-1 SPE.

Stuff Control/Indicator Bits

Each of the nine (9) rows within the STS-1 SPE contains five (5) Stuff Control/Indicator bits. The purpose of these "Stuff Control/Indicator" bits is to indicate (to the de-mapping PTE) whether the "Stuff Opportunity" bits (that resides in the same row) is a "Stuff" bit or is carrying a DS3 data bit.

If all five of these "Stuff Control/Indicator" bits, within a given row are set to "0", then this means that the corresponding "Stuff Opportunity" bit (e.g., the "Stuff Opportunity" bit within the same row) is carrying a DS3 data bit.

Conversely, if all five of these "Stuff Control/Indicator" bits, within a given row are set to "1" then this means that the corresponding "Stuff Opportunity" bit is carrying a "stuff" bit.

Overhead Communication Bits

Telcordia GR-253-CORE permits the user to use these two bits (for each row) as some sort of "Communications" bit. Some Mapper devices, such as the XRT94L43 12-Channel DS3/E3/STS-1 to STS-12/ STM-1 Mapper and the XRT94L33 3-Channel DS3/E3/STS-1 to STS-3/STM-1 Mapper IC (both from Exar Corporation) do permit the user to have access to these bit-fields.

However, in general, these particular bits can also be thought of as "Fixed Stuff" bits, that mostly have a "space occupation" function.

9.2.2 DS3 Frequency Offsets and the Use of the "Stuff Opportunity" Bits

In order to fully convey the role that the "stuff-opportunity" bits play, when mapping DS3 data into SONET, we will present a detailed discussion of each of the following "Mapping DS3 into STS-1" scenarios.

- The Ideal Case (e.g., with no frequency offsets)
- The 44.736Mbps + 1 ppm Case

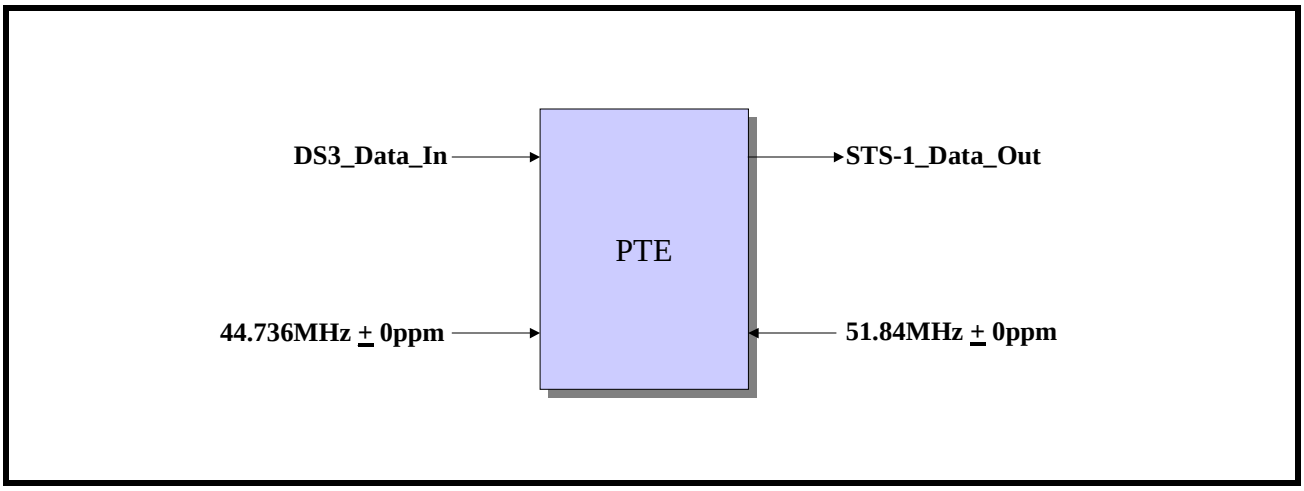
- The 44.736MHz - 1ppm Case

Throughout each of these cases, we will discuss how the resulting "bit-stuffing" (that was done when mapping the DS3 signal into SONET) affects the amount of intrinsic jitter and wander that will be present in the DS3 signal, once it is ultimately de-mapped from SONET.

9.2.2.1 *The Ideal Case for Mapping DS3 data into an STS-1 Signal (e.g., with no Frequency Offsets)*

Let us assume that we are mapping a DS3 signal, which has a bit rate of exactly 44.736Mbps (with no frequency offset) into SONET. Further, let us assume that the SONET circuitry within the PTE is clocked at exactly 51.84MHz (also with no frequency offset), as depicted below.

FIGURE 38. A SIMPLE ILLUSTRATION OF A DS3 DATA-STREAM BEING MAPPED INTO AN STS-1 SPE, VIA A PTE



Given the above-mentioned assumptions, we can state the following.

- The DS3 data-stream has a bit-rate of exactly 44.736Mbps
- The PTE will create 8000 STS-1 SPE's per second
- In order to properly map a DS3 data-stream into an STS-1 data-stream, then each STS-1 SPE must carry (44.736Mbps/8000 =) 5592 DS3 data bits.

Is there a Problem?

According to Figure 37, each STS-1 SPE only contains 5589 bits that are specifically designated for "DS3 data bits". In this case, each STS-1 SPE appears to be three bits "short".

No there is a Simple Solution

No, earlier we mentioned that each STS-1 SPE consists of nine (9) "Stuff Opportunity" bits. Therefore, these three additional bits (for DS3 data) are obtained by using three of these "Stuff Opportunity" bits. As a consequence, three (3) of these nine (9) "Stuff Opportunity" bits, within each STS-1 SPE, will carry DS3 data-bits. The remaining six (6) "Stuff Opportunity" bits will typically function as "stuff" bits.

In summary, for the "Ideal Case"; where there is no frequency offset between the DS3 and the STS-1 bit-rates, once this DS3 data-stream has been mapped into the STS-1 data-stream, then each and every STS-1 SPE will have the following "Stuff Opportunity" bit utilization.

3 "Stuff Opportunity" bits will carry DS3 data bits.

6 "Stuff Opportunity" bits will function as "stuff" bits

In this case, this DS3 signal (which has now been mapped into STS-1) will be transported across the SONET network. As this STS-1 signal arrives at the "Destination PTE", this PTE will extract (or de-map) this DS3 data-stream from each incoming STS-1 SPE. Now since each and every STS-1 SPE contains exactly 5592 DS3 data bits; then the bit rate of this DS3 signal will be exactly 44.736Mbps (such as it was when it was mapped into SONET, at the "Source" PTE).

As a consequence, no "Mapping/De-Mapping" Jitter or Wander is induced in the "Ideal Case".

9.2.2.2 *The 44.736Mbps + 1ppm Case*

The "above example" was a very ideal case. In reality, there are going to be frequency offsets in both the DS3 and STS-1 signals. For instance Bellcore GR-499-CORE mandates that a DS3 signal have a bit rate of 44.736Mbps ± 20ppm. Hence, the bit-rate of a "Bellcore" compliant DS3 signal can vary from the exact correct frequency for DS3 by as much of 20ppm in either direction. Similarly, many SONET applications mandate that SONET equipment use at least a "Stratum 3" level clock as its timing source. This requirement mandates that an STS-1 signal must have a bit rate that is in the range of 51.84 ± 4.6ppm. To make matters worse, there are also provisions for SONET equipment to use (what is referred to as) a "SONET Minimum Clock" (SMC) as its timing source. In this case, an STS-1 signal can have a bit-rate in the range of 51.84Mbps ± 20ppm.

In order to convey the impact that frequency offsets (in either the DS3 or STS-1 signal) will impose on the bit-stuffing behavior, and the resulting bit-rate, intrinsic jitter and wander within the DS3 signal that is being transported across the SONET network; let us assume that a DS3 signal, with a bit-rate of 44.736Mbps + 1ppm is being mapped into an STS-1 signal with a bit-rate of 51.84Mbps + 0ppm. In this case, the following things will occur.

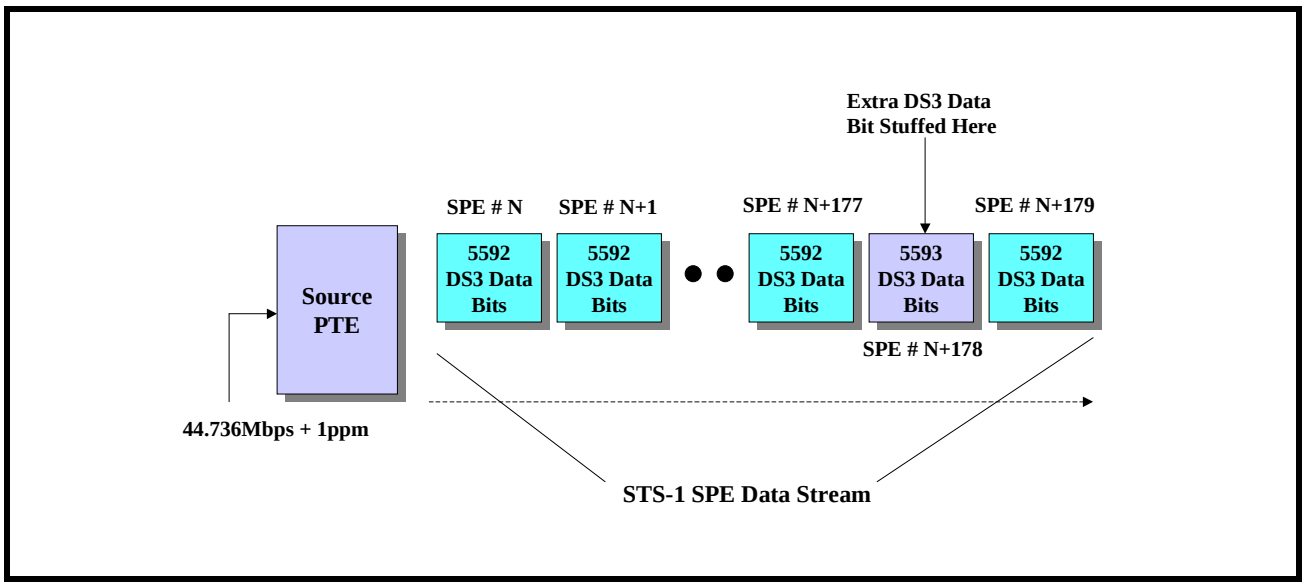
- In general, most of the STS-1 SPE's will each transport 5592 DS3 data bits.
- However, within a "one-second" period, a DS3 signal that has a bit-rate of 44.736Mbps + 1 ppm will deliver approximately 44.7 additional bits (over and above that of a DS3 signal with a bit-rate of 44.736Mbps + 0 ppm). This means that this particular signal will need to "negative-stuff" or map in an additional DS3 data bit every (1/44.736 =) 22.35ms. In other words, this additional DS3 data bit will need to be mapped into about one in every (22.35ms · 8000 =) 178.8 STS-1 SPEs in order to avoid dropping any DS3 data-bits.

What does this mean at the "Source" PTE?

All of this means that as the "Source" PTE maps this DS3 signal, with a data rate of 44.736Mbps + 1ppm into an STS-1 signal, most of the resulting "outbound" STS-1 SPEs will transport 5592 DS3 data bits (e.g., 3 Stuff Opportunity bits will be carrying DS3 data bits, the remaining 6 Stuff Opportunity bits are "stuff" bits, as in the "Ideal" case). However, in approximately one out of 178.8 "outbound" STS-1 SPEs, there will be a need to insert an additional DS3 data bit within this STS-1 SPE. Whenever this occurs, then (for these particular STS-1 SPEs) the SPE will be carrying 5593 DS3 data bits (e.g., 4 Stuff Opportunity bits will be carrying DS3 data bits, the remaining 5 Stuff Opportunity bits are "stuff" bits).

Figure 39 presents an illustration of the STS-1 SPE traffic that will be generated by the "Source" PTE, during this condition.

FIGURE 39. AN ILLUSTRATION OF THE STS-1 SPE TRAFFIC THAT WILL BE GENERATED BY THE "SOURCE" PTE, WHEN MAPPING IN A DS3 SIGNAL THAT HAS A BIT RATE OF 44.736MBPS + 1PPM, INTO AN STS-1 SIGNAL



What does this mean at the "Destination" PTE?

In this case, this DS3 signal (which has now been mapped into an STS-1 data-stream) will be transported across the SONET network. As this STS-1 signal arrives at the "Destination" PTE, this PTE will extract (or de-map) this DS3 data from each incoming STS-1 SPE. Now, in this case most (e.g., 177/178.8) of the incoming STS-1 SPEs will contain 5592 DS3 data-bits. Therefore, the nominal data rate of the DS3 signal being de-mapped from SONET will be 44.736Mbps. However, in approximately 1 out of every 178 incoming STS-1 SPEs, the SPE will carry 5593 DS3 data-bits. This means that (during these times) the data rate of the de-mapped DS3 signal will have an instantaneous frequency that is greater than 44.736Mbps. These "excursion" of the de-mapped DS3 data-rate, from the nominal DS3 frequency can be viewed as occurrences of "mapping/ de-mapping" jitter. Since each of these "bit-stuffing" events involve the insertion of one DS3 data bit, we can say that the amplitude of this "mapping/de-mapping" jitter is approximately 1UI-pp. From this point on, we will be referring to this type of jitter (e.g., that which is induced by the mapping and de-mapping process) as "de-mapping" jitter.

Since this occurrence of "de-mapping" jitter is periodic and occurs once every 22.35ms, we can state that this jitter has a frequency of 44.7Hz.

9.2.2.3 *The 44.736Mbps - 1ppm Case*

In this case, let us assume that a DS3 signal, with a bit-rate of 44.736Mbps - 1ppm is being mapped into an STS-1 signal with a bit-rate of 51.84Mbps + 0ppm. In this case, the following this will occur.

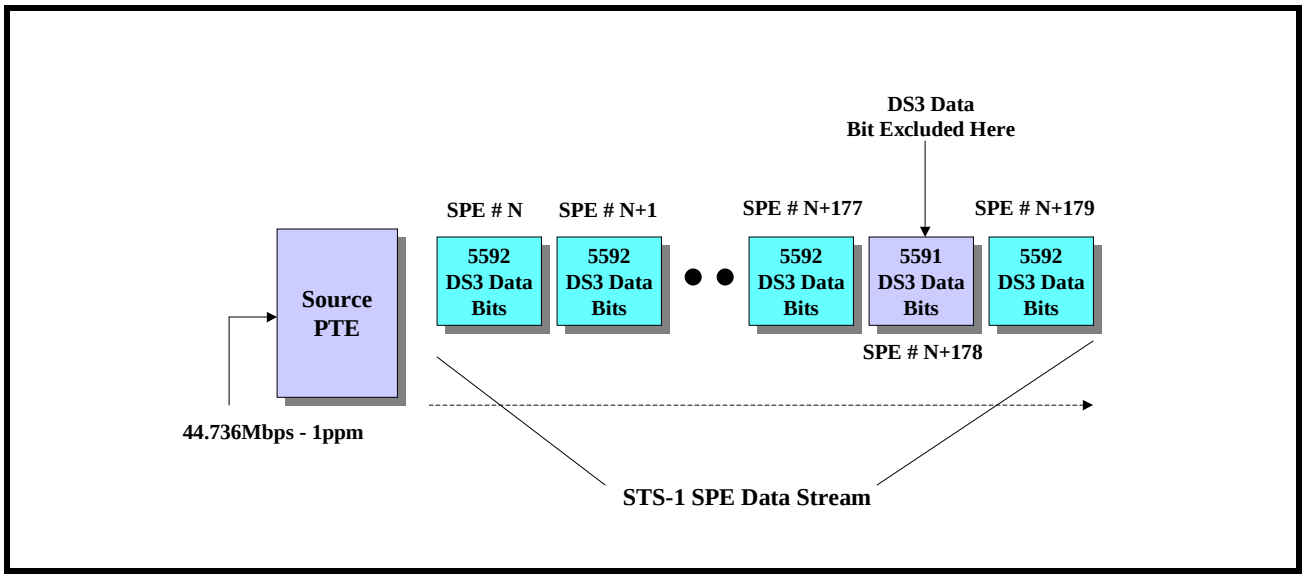
- In general, most of the STS-1 SPEs will each transport 5592 DS3 data bits.
- However, within a "one-second" period a DS3 signal that has a bit-rate of 44.736Mbps - 1ppm will deliver approximately 45 too few bits below that of a DS3 signal with a bit-rate of 44.736Mbps + 0ppm. This means that this particular signal will need to "positive-stuff" or exclude a DS3 data bit from mapping every (1/44.736) = 22.35ms. In other words, we will need to avoid mapping this DS3 data-bit about one in every (22.35ms*8000) = 178.8 STS-1 SPEs.

What does this mean at the "Source" PTE?

All of this means that as the "Source" PTE maps this DS3 signal, with a data rate of 44.736Mbps - 1ppm into an STS-1 signal, most of the resulting "outbound" STS-1 SPEs will transport 5592 DS3 data bits (e.g., 3 Stuff Opportunity bits will be carrying DS3 data bits, the remaining 6 Stuff Opportunity bits are "stuff" bits). However, in approximately one out of 178.8 "outbound" STS-1 SPEs, there will be a need for a "positive-stuffing" event. Whenever these "positive-stuffing" events occur then (for these particular STS-1 SPEs) the SPE will carry only 5591 DS3 data bits (e.g., in this case, only 2 Stuff Opportunity bits will be carrying DS3 data-bits, and the remaining 7 Stuff Opportunity bits are "stuff" bits).

Figure 40 presents an illustration of the STS-1 SPE traffic that will be generated by the "Source" PTE, during this condition.

FIGURE 40. AN ILLUSTRATION OF THE STS-1 SPE TRAFFIC THAT WILL BE GENERATED BY THE SOURCE PTE, WHEN MAPPING A DS3 SIGNAL THAT HAS A BIT RATE OF 44.736MBPS - 1PPM, INTO AN STS-1 SIGNAL



What does this mean at the Destination PTE?

In this case, this DS3 signal (which has now been mapped into an STS-1 data-stream) will be transported across the SONET network. As this STS-1 signal arrives at the "Destination" PTE, this PTE will extract (or de-map) this DS3 data from each incoming STS-1 SPE. Now, in this case, most (e.g., 177/178.8) of the incoming STS-1 SPEs will contain 5592 DS3 data-bits. Therefore, the nominal data rate of the DS3 signal being de-mapped from SONET will be 44.736Mbps. However, in approximately 1 out of every 178 incoming STS-1 SPEs, the SPE will carry only 5591 DS3 data bits. This means that (during these times) the data rate of the de-mapped DS3 signal will have an instantaneous frequency that is less than 44.736Mbps. These "excursions" of the de-mapped DS3 data-rate, from the nominal DS3 frequency can be viewed as occurrences of mapping/de-mapping jitter with an amplitude of approximately 1UI-pp.

Since this occurrence of "de-mapping" jitter is periodic and occurs once every 22.35ms, we can state that this jitter has a frequency of 44.7Hz.

We talked about De-Mapping Jitter, What about De-Mapping Wander?

The Telcordia and Bellcore specifications define "Wander" as "Jitter with a frequency of less than 10Hz". Based upon this definition, the DS3 signal (that is being transported by SONET) will cease to contain jitter and will now contain "Wander", whenever the frequency offset of the DS3 signal being mapped into SONET is less than 0.2ppm.

9.3 *Jitter/Wander due to Pointer Adjustments*

In the previous section, we described how a DS3 signal is asynchronously-mapped into SONET, and we also defined "Mapping/De-mapping" jitter. In this section, we will describe how occurrences within the SONET network will induce jitter/wander within the DS3 signal that is being transported across the SONET network.

In order to accomplish this, we will discuss the following topics in detail.

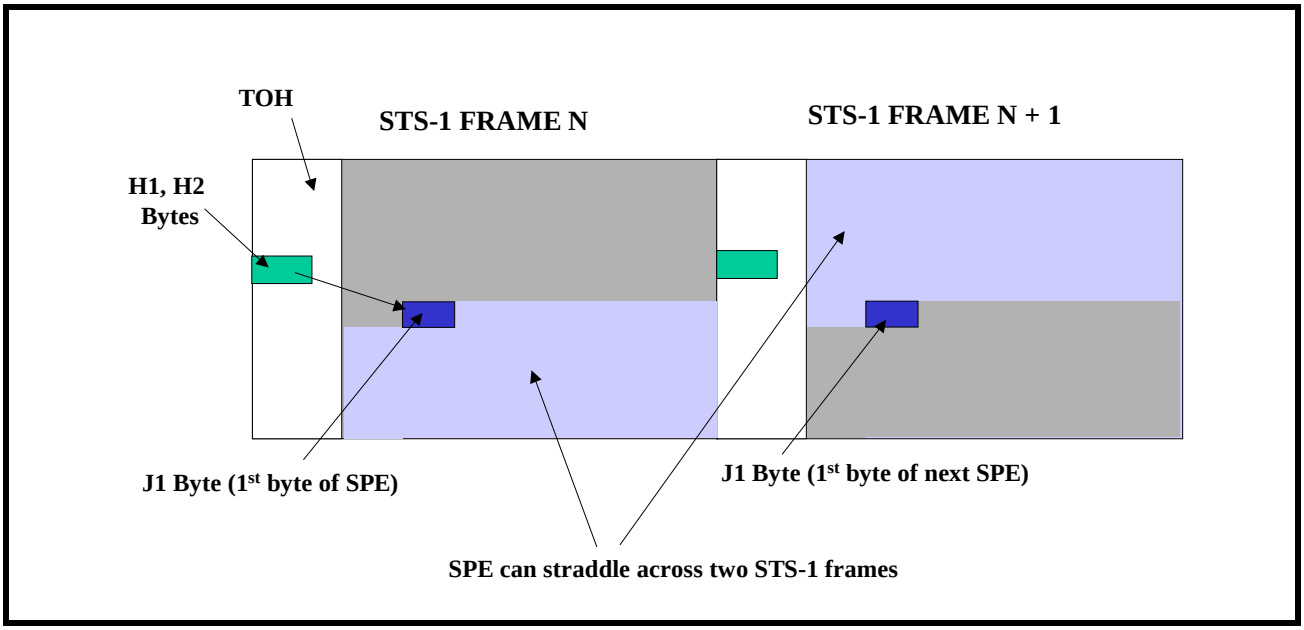
- The concept of an STS-1 SPE pointer
- The concept of Pointer Adjustments
- The causes of Pointer Adjustments
- How Pointer Adjustments induce jitter/wander within a DS3 signal being transported by that SONET network.

9.3.1 The Concept of an STS-1 SPE Pointer

As mentioned earlier, the STS-1 SPE is not aligned to the STS-1 frame boundaries and is permitted to "float" within the Envelope Capacity. As a consequence, the STS-1 SPE will often times "straddle" across two

consecutive STS-1 frames. Figure 41 presents an illustration of an STS-1 SPE straddling across two consecutive STS-1 frames.

FIGURE 41. AN ILLUSTRATION OF AN STS-1 SPE STRADDLING ACROSS TWO CONSECUTIVE STS-1 FRAMES



A PTE that is receiving and terminating an STS-1 data-stream will perform the following tasks.

- It will acquire and maintain STS-1 frame synchronization with the incoming STS-1 data-stream.
- Once the PTE has acquired STS-1 frame synchronization, then it will locate the J1 byte (e.g., the very byte within the very next STS-1 SPE) within the Envelope Capacity by reading out the contents of the H1 and H2 bytes.

The H1 and H2 bytes are referred to (in the SONET standards) as the SPE Pointer Bytes. When these two bytes are concatenated together in order to form a 16-bit word (with the H1 byte functioning as the "Most Significant Byte") then the contents of the "lower" 10 bit-fields (within this 16-bit word) reflects the location of the J1 byte within the Envelope Capacity of the incoming STS-1 data-stream. Figure 42 presents an illustration of the bit format of the H1 and H2 bytes, and indicates which bit-fields are used to reflect the location of the J1 byte.

FIGURE 42. THE BIT-FORMAT OF THE 16-BIT WORD (CONSISTING OF THE H1 AND H2 BYTES) WITH THE 10 BITS, REFLECTING THE LOCATION OF THE J1 BYTE, DESIGNATED

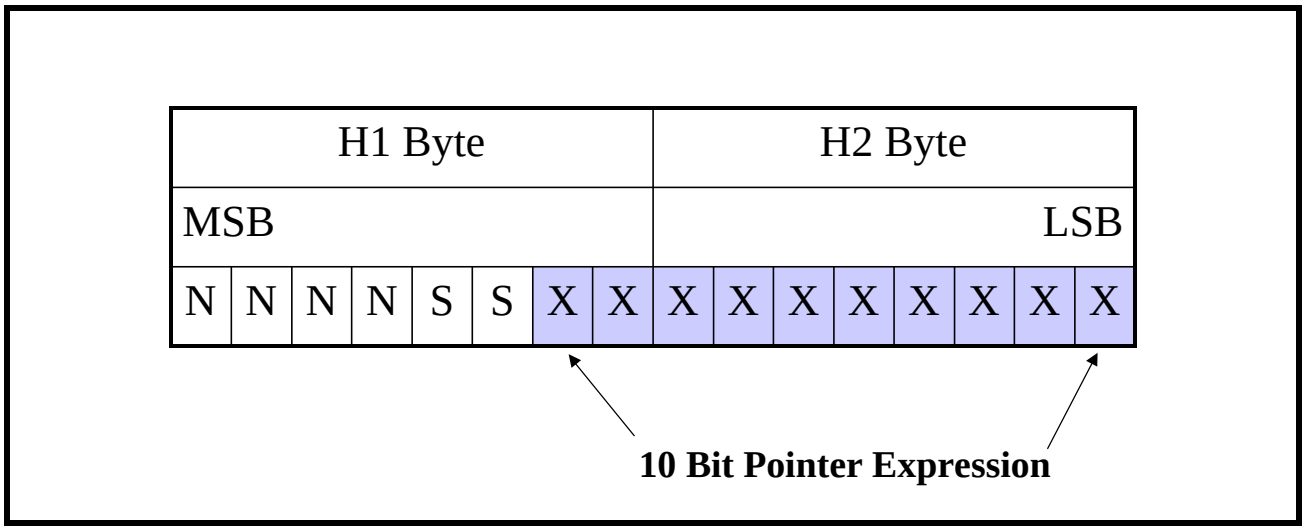
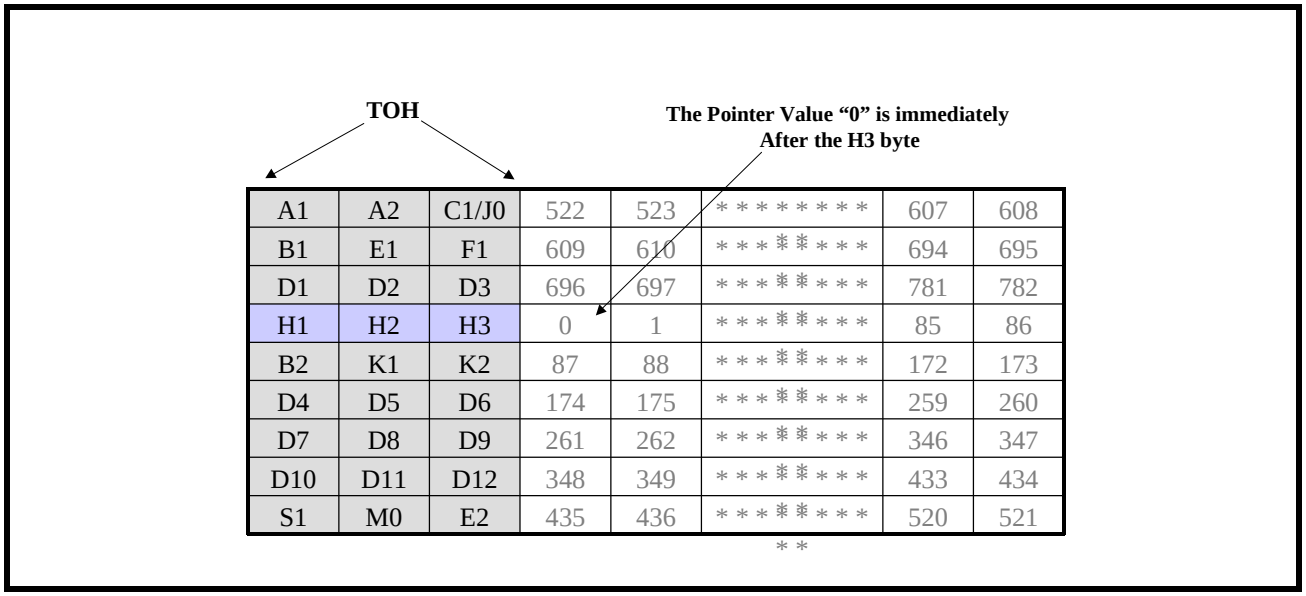


Figure 43 relates the contents within these 10 bits (within the H1 and H2 bytes) to the location of the J1 byte (e.g., the very first byte of the STS-1 SPE) within the Envelope Capacity.

FIGURE 43. THE RELATIONSHIP BETWEEN THE CONTENTS OF THE "POINTER BITS" (E.G., THE 10-BIT EXPRESSION WITHIN THE H1 AND H2 BYTES) AND THE LOCATION OF THE J1 BYTE WITHIN THE ENVELOPE CAPACITY OF AN STS-1 FRAME



NOTES:

1. *If the content of the "Pointer Bits" is "0x00" then the J1 byte is located immediately after the H3 byte, within the Envelope Capacity.*
2. *If the contents of the 10-bit expression exceed the value of 0x30F (or 782, in decimal format) then it does not contain a valid pointer value.*

9.3.2 Pointer Adjustments within the SONET Network

The word SONET stands for "Synchronous Optical NETwork. This name implies that the entire SONET network is synchronized to a single clock source. However, because the SONET (and SDH) Networks can

span thousands of miles, traverse many different pieces of equipments, and even cross International boundaries; in practice, the SONET/SDH network is NOT synchronized to a single clock source.

In practice, the SONET/SDH network can be thought of as being divided into numerous "Synchronization Islands". Each of these "Synchronization Islands" will consist of numerous pieces of SONET Terminal Equipment. Each of these pieces of SONET Terminal Equipment will all be synchronized to a single Stratum-1 clock source which is the most accurate clock source within the Synchronization Island. Typically a "Synchronization Island" will consist of a single "Timing Master" equipment along with multiple "Timing Slave" pieces of equipment. This "Timing Master" equipment will be directly connected to the Stratum-1 clock source and will have the responsibility of distributing a very accurate clock signal (that has been derived from the Stratum 1 clock source) to each of the "Timing Slave" pieces of equipment within the "Synchronization Island". The purpose of this is to permit each of the "Timing Slave" pieces of equipment to be "synchronized" with the "Timing Master" equipment, as well as the Stratum 1 Clock source. Typically this "clock distribution" is performed in the form of a BITS (Building Integrated Timing Supply) clock, in which a very precise clock signal is provided to the other pieces of equipment via a T1 or E1 line signal.

Many of these "Synchronization Islands" will use a Stratum-1" clock source that is derived from GPS pulses that are received from Satellites that operate at Geo-synchronous orbit. Other "Synchronization Islands" will use a Stratum-1" clock source that is derived from a very precise local atomic clock. As a consequence, different "Synchronization Islands" will use different Stratum 1 clock sources. The up-shot of having these "Synchronization Islands" that use different "Stratum-1 clock" sources, is that the Stratum 1 Clock frequencies, between these "Synchronization Islands" are likely to be slightly different from each other. These "frequency-differences" within Stratum 1 clock sources will result in "clock-domain changes" as a SONET signal (that is traversing the SONET network) passes from one "Synchronization Island" to another.

The following section will describe how these "frequency differences" will cause a phenomenon called "pointer adjustments" to occur in the SONET Network.

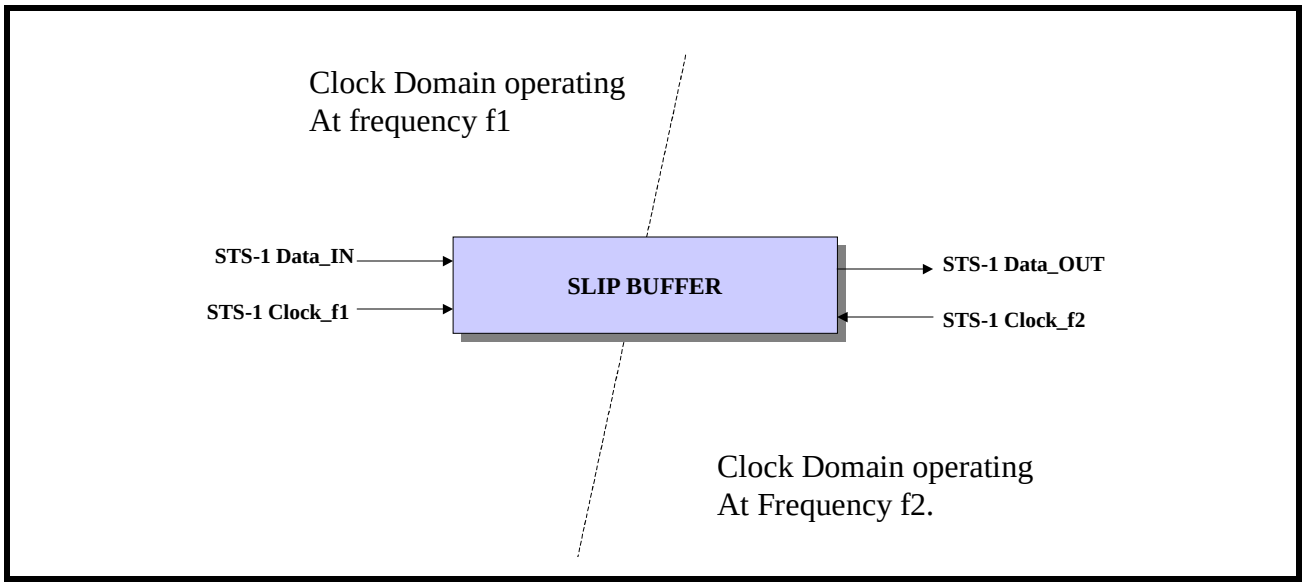
9.3.3 Causes of Pointer Adjustments

The best way to discuss how pointer adjustment events occur is to consider an STS-1 signal, which is driven by a timing reference of frequency f1; and that this STS-1 signal is being routed to a network equipment (that resides within a different "Synchronization Island") and processes STS-1 data at a frequency of f2.

NOTE: *Clearly, both frequencies f1 and f2 are at the STS-1 rate (e.g., 51.84MHz). However, these two frequencies are likely to be slightly different from each other.*

Now, since the STS-1 signal (which is of frequency f1) is being routed to the network element (which is operating at frequency f2), the typical design approach for handling "clock-domain" differences is to route this STS-1 signal through a "Slip Buffer" as illustrated below.

FIGURE 44. AN ILLUSTRATION OF AN STS-1 SIGNAL BEING PROCESSED VIA A SLIP BUFFER



In the "Slip Buffer, the "input" STS-1 data (labeled "STS-1 Data_IN") is latched into the FIFO, upon a given edge of the corresponding "STS-1 Clock_f1" input clock signal. The STS-1 Data (labeled "STS-1 Data_OUT") is clocked out of the Slip Buffer upon a given edge of the "STS-1 Clock_f2" input clock signal.

The behavior of the data, passing through the "Slip Buffer" is now described for each possible relationship between frequencies f1 and f2.

If f1 = f2

If both frequencies, f1 and f2 are exactly equal, then the STS-1 data will be "clocked" into the "Slip Buffer" at exactly the same rate that it is "clocked out". In this case, the "Slip Buffer" will neither fill-up nor become depleted. As a consequence, no pointer-adjustments will occur in this STS-1 data stream. In other words, the STS-1 SPE will remain at a constant location (or offset) within each STS-1 envelope capacity for the duration that this STS-1 signal is supporting this particular service.

If f1 < f2

If frequency f1 is less than f2, then this means that the STS-1 data is being "clocked out" of the "Slip Buffer" at a faster rate than it is being clocked in. In this case, the "Slip Buffer" will eventually become depleted. Whenever this occurs, a typical strategy is to "stuff" (or insert) a "dummy byte" into the data stream. The purpose of stuffing this "dummy byte" is to compensate for the frequency differences between f1 and f2, and attempt to keep the "Slip Buffer, at a somewhat constant fill level.

NOTE: *This "dummy byte" does not carry any valuable information (not for the user, nor for the system).*

Since this "dummy byte" carries no useful information, it is important that the "Receiving PTE" be notified anytime this "dummy byte" stuffing occurs. This way, the Receiving Terminal can "know" not to treat this "dummy byte" as user data.

Byte-Stuffing and Pointer Incrementing in a SONET Network

Whenever this "byte-stuffing" occurs then the following other things occur within the STS-1 data stream.

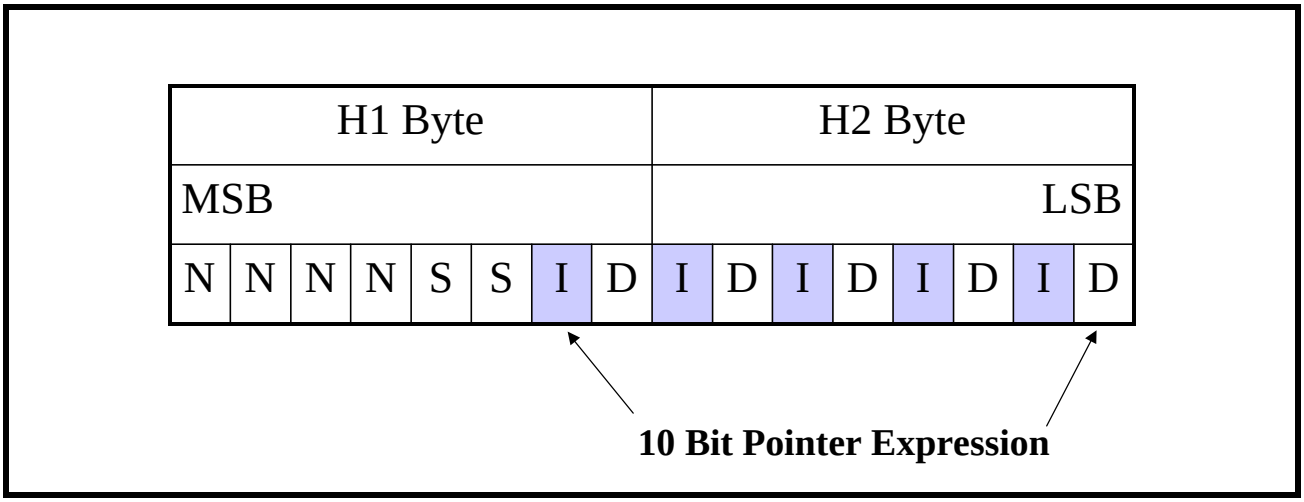
During the STS-1 frame that contains the "Byte-Stuffing" event

a. The "stuff-byte" will be inserted into the byte position immediately after the H3 byte. This insertion of the "dummy byte" immediately after the H3 byte position will cause the J1 byte (and in-turn, the rest of the SPE) to be "byte-shifted" away from the H3 byte. As a consequence, the offset between the H3 byte position and the STS-1 SPE will now have been increased by 1 byte.

b. The "Transmitting" Network Equipment will notify the remote terminal of this byte-stuffing event, by inverting certain bits within the "pointer word" (within the H1 and H2 bytes) that are referred to as "I" bits.

Figure 45 presents an illustration of the bit-format within the 16-bit word (consist of the H1 and H2 bytes) with the "I" bits designated.

FIGURE 45. AN ILLUSTRATION OF THE BIT FORMAT WITHIN THE 16-BIT WORD (CONSISTING OF THE H1 AND H2 BYTES) WITH THE "I" BITS DESIGNATED



NOTE: *At this time the "I" bits are inverted in order to denote that an "incrementing" pointer adjustment event is currently occurring.*

During the STS-1 frame that follows the "Byte-Stuffing" event

The "I" bits (within the "pointer-word") will be set back to their normal value; and the contents of the H1 and H2 bytes will be incremented by "1".

If f1 > f2

If frequency f1 is greater than f2, then this means that the STS-1 data is being clocked into the "Slip Buffer" at a faster rate than is being clocked out. In this case, the "Slip Buffer" will start to fill up. Whenever this occurs, a typical strategy is to delete (e.g., negative-stuff) a byte from the Slip Buffer. The purpose of this "negative-stuffing" is to compensate for the frequency differences between f1 and f2; and to attempt to keep the "Slip Buffer" at a somewhat constant fill-level.

NOTE: *This byte, which is being "un-stuffed" does carry valuable information for the user (e.g., this byte is typically a payload byte). Therefore, whenever this negative stuffing occurs, two things must happen.*

a. The "negative-stuffed" byte must not be simply discarded. In other words, it must somehow also be transmitted to the remote PTE with the remainder of the SPE data.

b. The remote PTE must be notified of the occurrence of these "negative-stuffing" events. Further, the remote PTE must know where to obtain this "negative-stuffed" byte.

Negative-Stuffing and Pointer-Decrementing in a SONET Network

Whenever this "byte negative-stuffing" occurs then the following other things occur within the STS-1 data-stream.

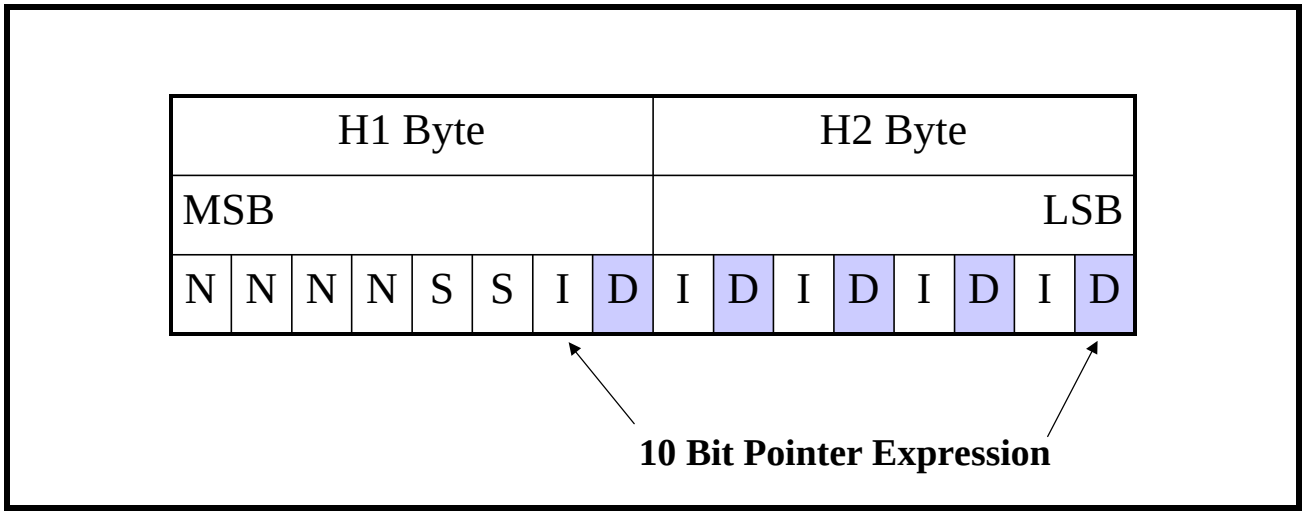
During the STS-1 frame that contains the "Negative Byte-Stuffing" Event

a. The "Negative-Stuffed" byte will be inserted into the H3 byte position. Whenever an SPE data byte is inserted into the H3 byte position (which is ordinarily an unused byte), the number of bytes that will exist between the H3 byte and the J1 byte within the very next SPE will be reduced by 1 byte. As a consequence, in this case, the J1 byte (and in-turn, the rest of the SPE) will now be "byte-shifted" towards the H3 byte position.

b. The "Transmitting" Network Element will notify the remote terminal of this "negative-stuff" event by inverting certain bits within the "pointer word" (within the H1 and H2 bytes) that are referred to as "D" bits.

Figure 46 presents an illustration of the bit format within the 16-bit word (consisting of the H1 and H2 bytes) with the "D" bits designated.

FIGURE 46. AN ILLUSTRATION OF THE BIT-FORMAT WITHIN THE 16-BIT WORD (CONSISTING OF THE H1 AND H2 BYTES) WITH THE "D" BITS DESIGNATED



NOTE: *At this time the "D" bits are inverted in order to denote that a "decrementing" pointer adjustment event is currently occurring.*

During the STS-1 frame that follows the "Negative Byte-Stuffing" Event

The "D" bits (within the pointer-word) will be set back to their normal value; and the contents of the H1 and H2 bytes will be decremented by one.

9.3.4 Why are we talking about Pointer Adjustments?

The overall SONET network consists of numerous "Synchronization Islands". As a consequence, whenever a SONET signal is being transmitted from one "Synchronization Island" to another; that SONET signal will undergo a "clock domain" change as it traverses the network. This clock domain change will result in periodic pointer-adjustments occurring within this SONET signal. Depending upon the direction of this "clock-domain" shift that the SONET signal experiences, there will either be periodic "incrementing" pointer-adjustment events or periodic "decrementing" pointer-adjustment events within this SONET signal.

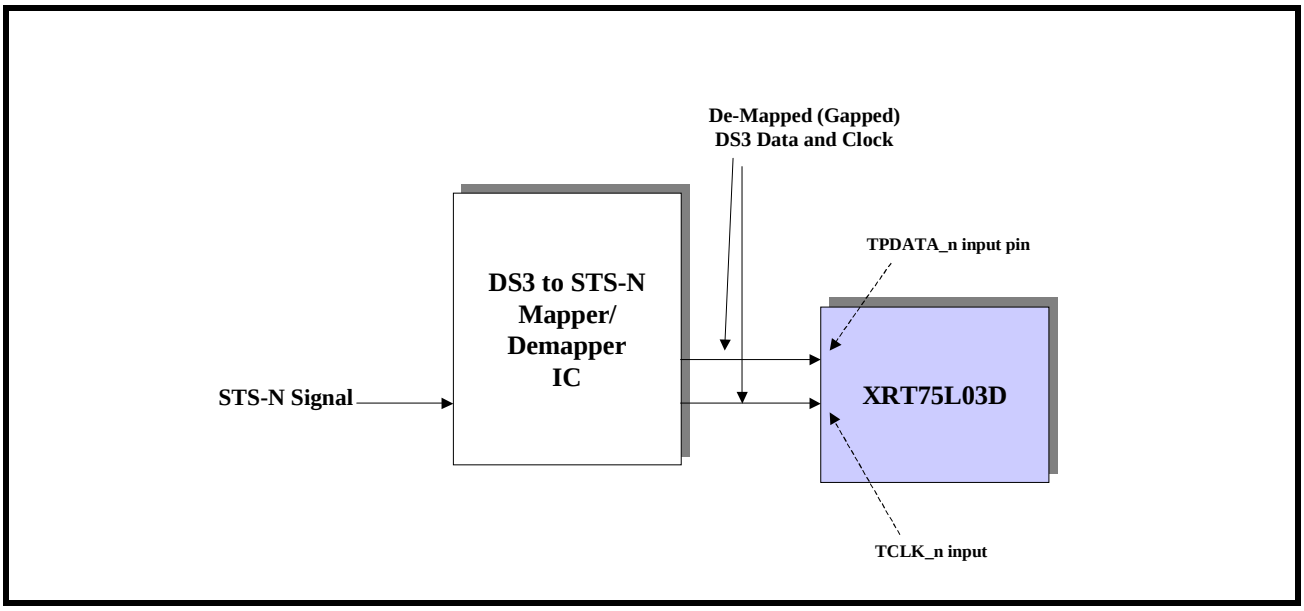
Regardless of whether a given SONET signal is experiencing incrementing or decrementing pointer adjustment events, each pointer adjustment event will result in an abrupt 8-bit shift in the position of the SPE within the STS-1 data-stream. If this STS-1 signal is transporting an "asynchronously-mapped" DS3 signal; then this 8-bit shift in the location of the SPE (within the STS-1 signal) will result in approximately 8UIpp of jitter within the asynchronously-mapped DS3 signal, as it is de-mapped from SONET. In “Section 9.5, A Review of the Category I Intrinsic Jitter Requirements (per Telcordia GR-253-CORE) for DS3 applications” on page 110 we will discuss the "Category I Intrinsic Jitter Requirements (for DS3 Applications) per Telcordia GR-253-CORE. However, for now we will simply state that this 8UIpp of intrinsic jitter far exceeds these "intrinsic jitter" requirements.

In summary, pointer-adjustments events are a "fact of life" within the SONET/SDH network. Further, pointer-adjustment events, within a SONET signal that is transporting an asynchronously-mapped DS3 signal, will impose a significant impact on the Intrinsic Jitter and Wander within that DS3 signal as it is de-mapped from SONET.

9.4 *Clock Gapping Jitter*

In most applications (in which the XRT75L03D will be used in a SONET De-Sync Application) the user will typically interface the XRT75L03D to a Mapper Device in the manner as presented below in Figure 47.

FIGURE 47. ILLUSTRATION OF THE TYPICAL APPLICATIONS FOR THE XRT75L03D IN A SONET DE-SYNC APPLICATION



In this application, the Mapper IC will have the responsibility of receiving an STS-N signal (from the SONET Network) and performing all of the following operations on this STS-N signal.

- Byte-de-interleaving this incoming STS-N signal into N STS-1 signals
- Terminating each of these STS-1 signals
- Extracting (or de-mapping) the DS3 signal(s) from the SPEs within each of these terminated STS-1 signals.

In this application, these Mapper devices can be thought of as multi-channel devices. For example, an STS-3 Mapper can be viewed as a 3-Channel DS3/STS-1 to STS-3 Mapper IC. Similarly, an STS-12 Mapper can be viewed as a 12-Channel DS3/STS-1 to STS-12 Mapper IC. Continuing on with this line of thought, if a Mapper IC is configured to receive an STS-N signal, and (from this STS-N signal) de-map and output N DS3 signals (towards the DS3 facility), then it will typically do so in the following manner.

- In many cases, the Mapper IC will output this DS3 signal, using both a "Data-Signal" and a "Clock-Signal". In many cases, the Mapper IC will output the contents of an entire STS-1 data-stream via the Data-Signal.
- However, as the Mapper IC output this STS-1 data-stream, it will typically supply clock pulses (via the Clock-Signal output) coincident to whenever a DS3 bit is being output via the Data-Signal. In this case, the Mapper IC will NOT supply a clock pulse coincident to when a TOH, POH, or any "non-DS3 data-bit" is being output via the "Data-Signal".

Now, since the Mapper IC will output the entire STS-1 data stream (via the Data-Signal), the output Clock-Signal will be of the form such that it has a period of 19.3ns (e.g., a 51.84MHz clock signal). However, the Mapper IC will still generate approximately 44,736,000 clock pulses during any given one second period. Hence, the clock signal that is output from the Mapper IC will be a horribly gapped 44.736MHz clock signal. One can view such a clock signal as being a very-jittery 44.736MHz clock signal. This jitter that exists within the "Clock-Signal" is referred to as "Clock-Gapping" Jitter. A more detailed discussion on how the user must handle this type of jitter is presented in “Section 9.8.2, Recommendations on Pre-Processing the Gapped Clocks (from the Mapper/ASIC Device) prior to routing this DS3 Clock and Data-Signals to the Transmit Inputs of the XRT75L03D” on page 121.

9.5 *A Review of the Category I Intrinsic Jitter Requirements (per Telcordia GR-253-CORE) for DS3 applications*

The "Category I Intrinsic Jitter Requirements" per Telcordia GR-253-CORE (for DS3 applications) mandates that the user perform a large series of tests against certain specified "Scenarios". These "Scenarios" and their corresponding requirements is summarized in Table 31, below.

TABLE 31: SUMMARY OF "CATEGORY I INTRINSIC JITTER REQUIREMENT PER TELCORDIA GR-253-CORE, FOR DS3 APPLICATIONS

SCENARIO DESCRIPTION	SCENARIO NUMBER	TELCORDIA GR-253-CORE CATEGORY I INTRINSIC JITTER REQUIREMENTS	COMMENTS
DS3 De-Mapping Jitter		0.4UI-pp	Includes effects of De-Mapping and Clock Gapping Jitter
Single Pointer Adjustment	A1	0.3UI-pp + Ao	Includes effects of Jitter from Clock-Gapping, De-Mapping and Pointer Adjustments.NOTE: Ao is the amount of intrinsic jitter that was measured during the "DS3 De-Mapping Jitter" phase of the Test.
Pointer Bursts	A2	1.3UI-pp	Includes effects of Jitter from Clock-Gapping, De-Mapping and Pointer Adjustments.
Phase Transients	A3	1.2UI-pp	Includes effects of Jitter from Clock-Gapping, De-Mapping and Pointer Adjustments.
87-3 Pattern	A4	1.0UI-pp	Includes effects of Jitter from Clock-Gapping, De-Mapping and Pointer Adjustments.
87-3 Add	A5	1.3UI-pp	Includes effects of Jitter from Clock-Gapping, De-Mapping and Pointer Adjustments.
87-3 Cancel	A5	1.3UI-pp	Includes effects of Jitter from Clock-Gapping, De-Mapping and Pointer Adjustments.

TABLE 31: SUMMARY OF "CATEGORY I INTRINSIC JITTER REQUIREMENT PER TELCORDIA GR-253-CORE, FOR DS3 APPLICATIONS

SCENARIO DESCRIPTION	SCENARIO NUMBER	TELCORDIA GR-253-CORE CATEGORY I INTRINSIC JITTER REQUIREMENTS	COMMENTS
Continuous Pattern	A4	1.0UI-pp	Includes effects of Jitter from Clock-Gapping, De-Mapping and Pointer Adjustments.
Continuous Add	A5	1.3UI-pp	Includes effects of Jitter from Clock-Gapping, De-Mapping and Pointer Adjustments.
Continuous Cancel	A5	1.3UI-pp	Includes effects of Jitter from Clock-Gapping, De-Mapping and Pointer Adjustments.

NOTE: *All of these intrinsic jitter measurements are to be performed using a band-pass filter of 10Hz to 400kHz.*

Each of the scenarios presented in Table 31, are briefly described below.

9.5.1 DS3 De-Mapping Jitter

DS3 De-Mapping Jitter is the amount of Intrinsic Jitter that will be measured within the "Line" or "Facility-side" DS3 signal, (after it has been de-mapped from a SONET signal) without the occurrence of "Pointer Adjustments" within the SONET signal.

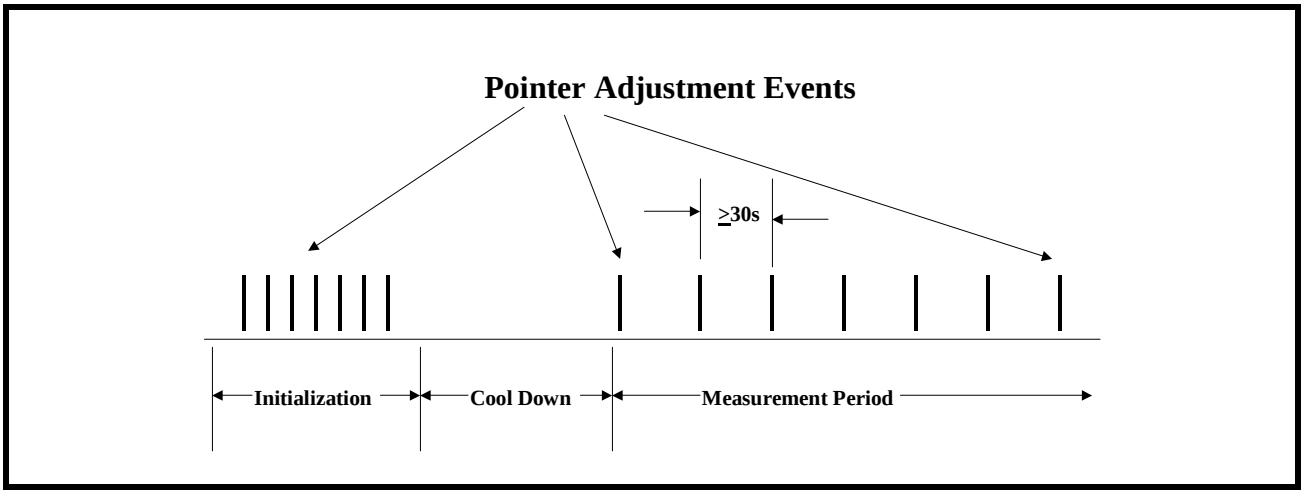
Telcordia GR-253-CORE requires that the "DS3 De-Mapping" Jitter be less than 0.4UI-pp, when measured over all possible combinations of DS3 and STS-1 frequency offsets.

9.5.2 Single Pointer Adjustment

Telcordia GR-253-CORE states that if each pointer adjustment (within a continuous stream of pointer adjustments) is separated from each other by a period of 30 seconds, or more; then they are sufficiently isolated to be considered "Single-Pointer Adjustments".

Figure 48 presents an illustration of the "Single Pointer Adjustment" Scenario.

FIGURE 48. ILLUSTRATION OF SINGLE POINTER ADJUSTMENT SCENARIO



Telcordia GR-253-CORE states that the Intrinsic Jitter that is measured (within the DS3 signal) that is ultimately de-mapped from a SONET signal that is experiencing "Single-Pointer Adjustment" events, must NOT exceed the value 0.3UI-pp + Ao.

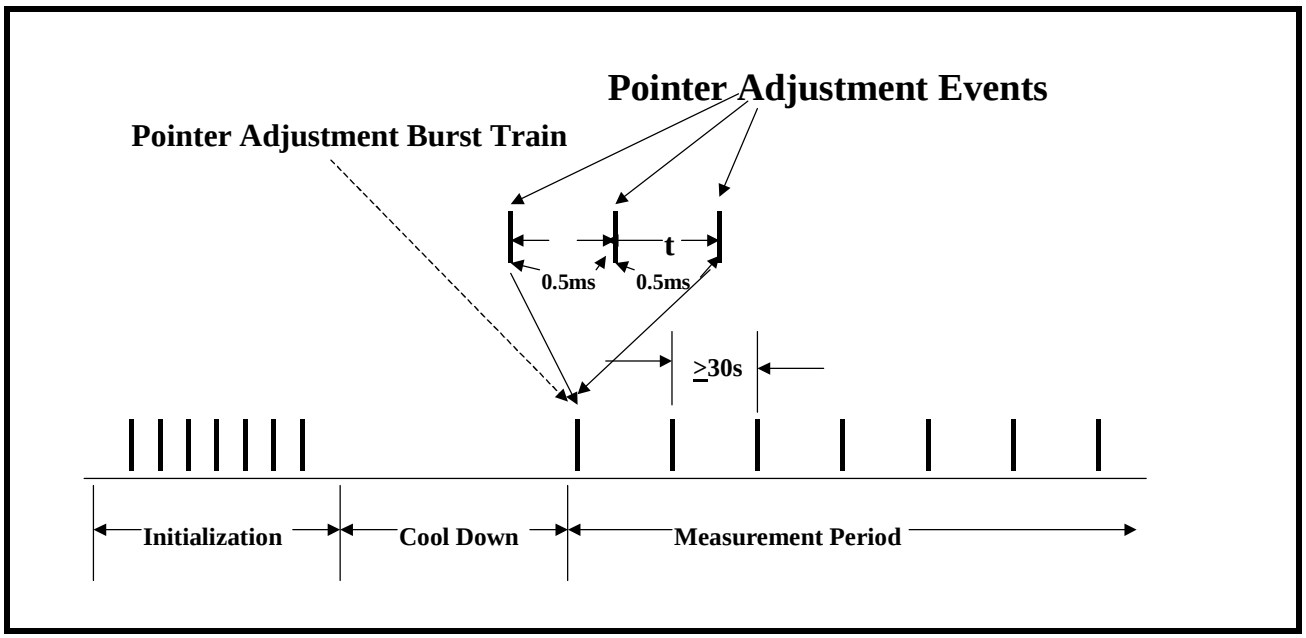
NOTES:

1. *Ao is the amount of Intrinsic Jitter that was measured during the "De-Mapping" Jitter portion of this test.*
2. *Testing must be performed for both Incrementing and Decrementing Pointer Adjustments.*

9.5.3 Pointer Burst

Figure 49 presents an illustration of the "Pointer Burst" Pointer Adjustment Scenario per Telcordia GR-253-CORE.

FIGURE 49. ILLUSTRATION OF BURST OF POINTER ADJUSTMENT SCENARIO

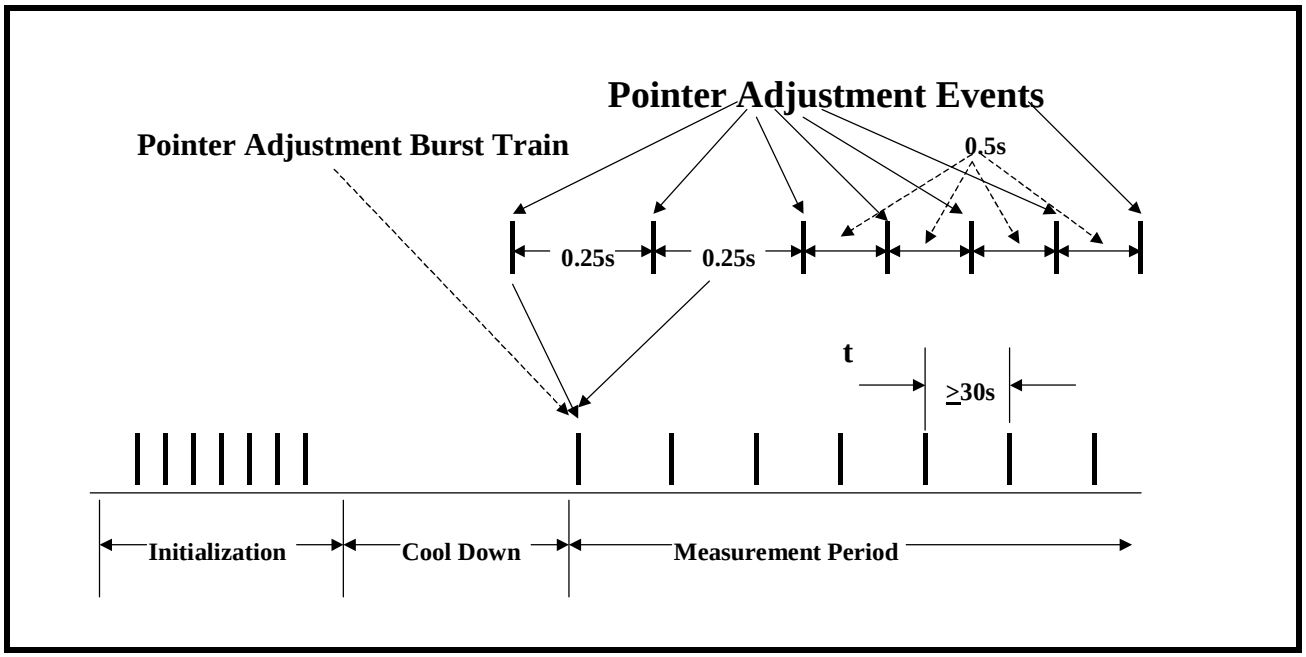


Telcordia GR-253-CORE mandates that the Intrinsic Jitter, within the DS3 signal that is de-mapped from a SONET signal, which is experiencing the "Burst of Pointer Adjustment" scenario, must NOT exceed 1.3UI-pp.

9.5.4 Phase Transients

Figure 50 presents an illustration of the "Phase Transients" Pointer Adjustment Scenario per Telcordia GR-253-CORE.

FIGURE 50. ILLUSTRATION OF "PHASE-TRANSIENT" POINTER ADJUSTMENT SCENARIO

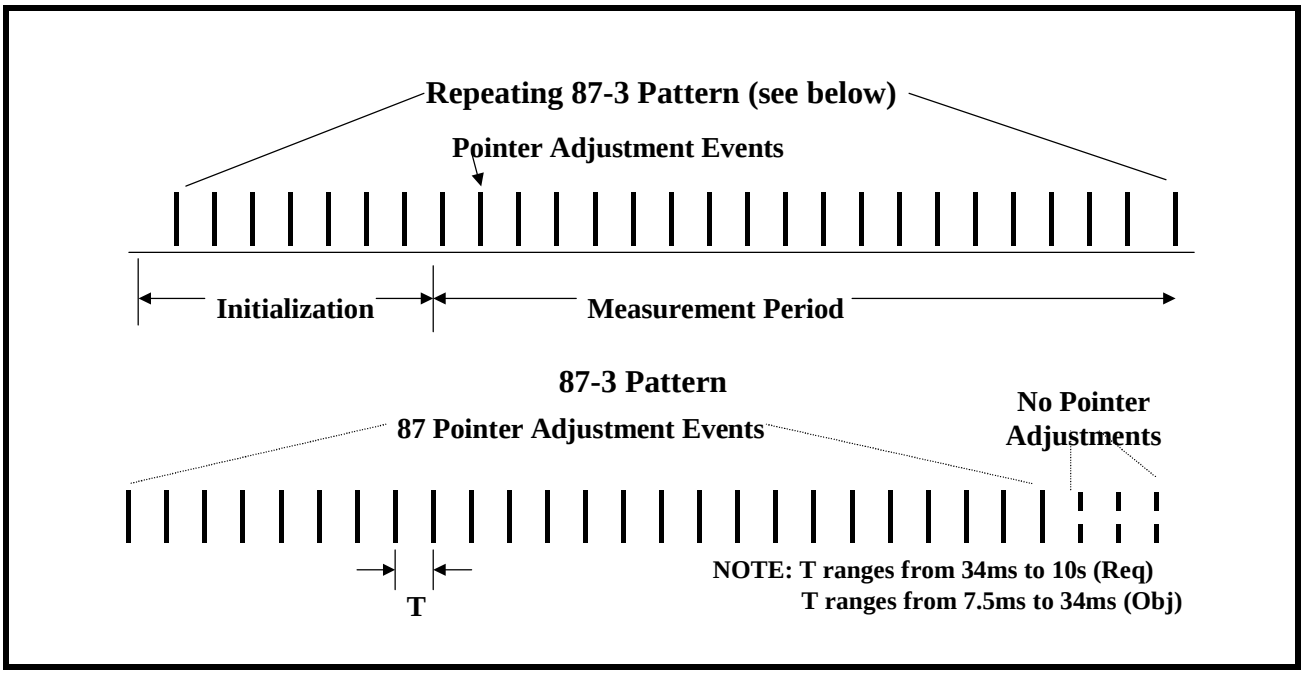


Telcordia GR-253-CORE mandates that the Intrinsic Jitter, within the DS3 signal that is de-mapped from a SONET signal, which is experiencing the "Phase Transient - Pointer Adjustment" scenario must NOT exceed 1.2UI-pp.

9.5.5 87-3 Pattern

Figure 51 presents an illustration of the "87-3 Continuous Pattern" Pointer Adjustment Scenario per Telcordia GR-253-CORE.

FIGURE 51. AN ILLUSTRATION OF THE 87-3 CONTINUOUS POINTER ADJUSTMENT PATTERN



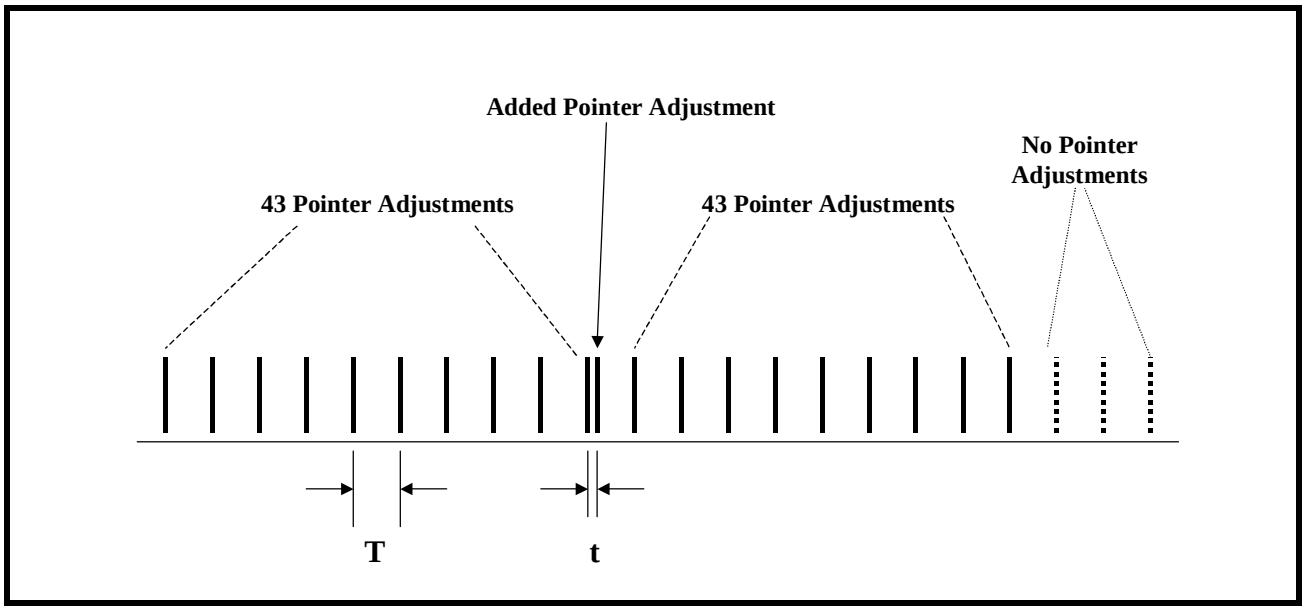
Telcordia GR-253-CORE defines an "87-3 Continuous" Pointer Adjustment pattern, as a repeating sequence of 90 pointer adjustment events. Within this 90 pointer adjustment event, 87 pointer adjustments are actually executed. The remaining 3 pointer adjustments are never executed. The spacing between individual pointer adjustment events (within this scenario) can range from 7.5ms to 10seconds.

Telcordia GR-253-CORE mandates that the Intrinsic Jitter, within the DS3 signal that is de-mapped from a SONET signal, which is experiencing the "87-3 Continuous" pattern of Pointer Adjustments, must not exceed 1.0UI-pp.

9.5.6 87-3 Add

Figure 52 presents an illustration of the "87-3 Add Pattern" Pointer Adjustment Scenario per Telcordia GR-253-CORE.

FIGURE 52. ILLUSTRATION OF THE 87-3 ADD POINTER ADJUSTMENT PATTERN



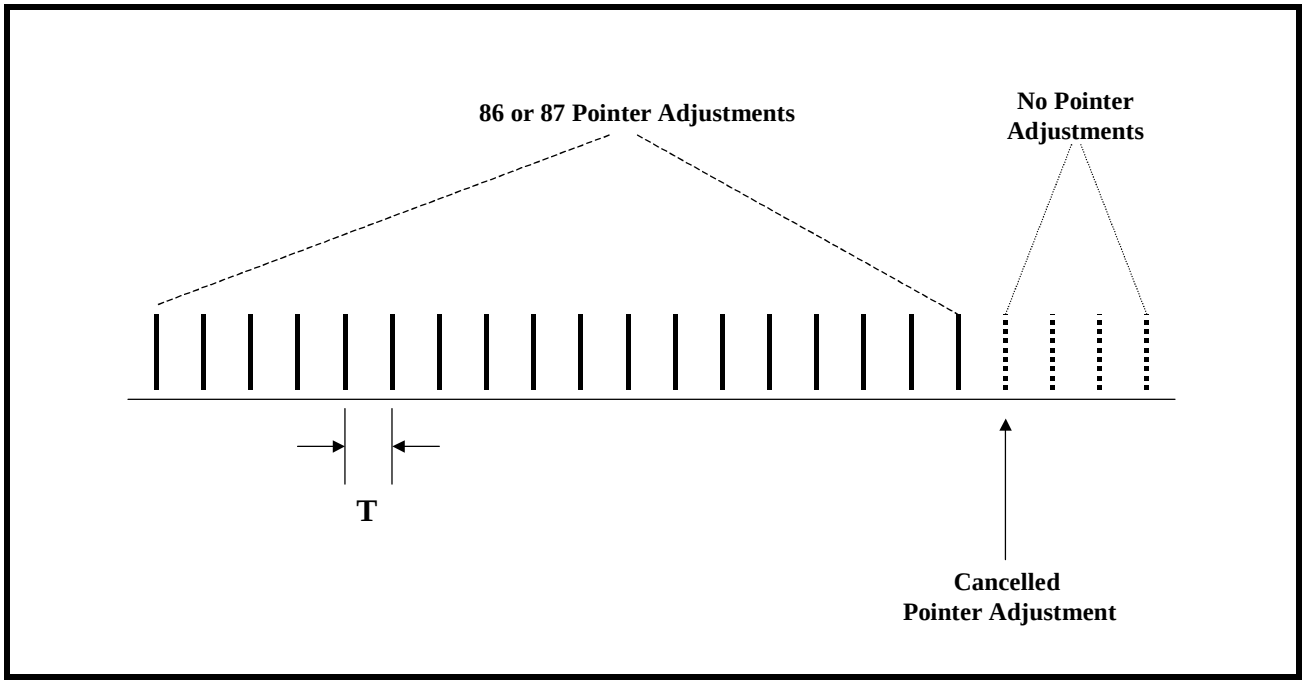
Telcordia GR-253-CORE defines an "87-3 Add" Pointer Adjustment, as the "87-3 Continuous" Pointer Adjustment pattern, with an additional pointer adjustment inserted, as shown above in Figure 52.

Telcordia GR-253-CORE mandates that the Intrinsic Jitter, within the DS3 signal that is de-mapped from a SONET signal, which is experiencing the "87-3 Add" pattern of Pointer Adjustments, must not exceed 1.3UI-pp.

9.5.7 87-3 Cancel

Figure 53 presents an illustration of the 87-3 Cancel Pattern Pointer Adjustment Scenario per Telcordia GR-253-CORE.

FIGURE 53. ILLUSTRATION OF 87-3 CANCEL POINTER ADJUSTMENT SCENARIO



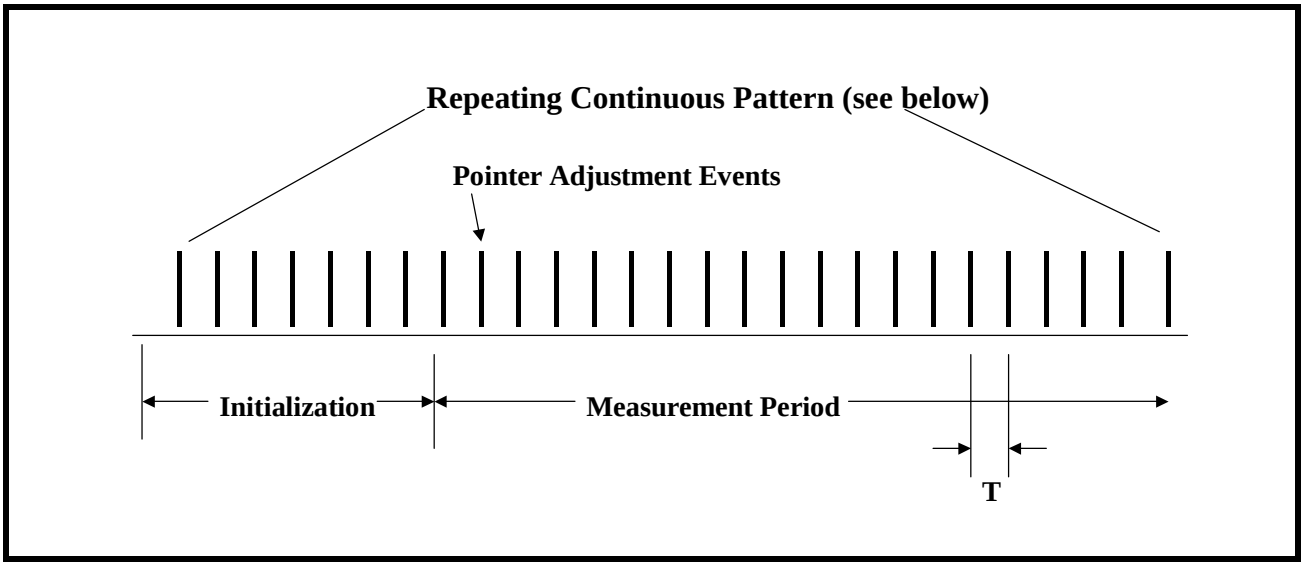
Telcordia GR-253-CORE defines an "87-3 Cancel" Pointer Adjustment, as the "87-3 Continuous" Pointer Adjustment pattern, with an additional pointer adjustment cancelled (or not executed), as shown above in Figure 53.

Telcordia GR-253-CORE mandates that the Intrinsic Jitter, within the DS3 signal that is de-mapped from a SONET signal, which is experiencing the "87-3 Cancel" pattern of Pointer Adjustments, must not exceed 1.3UI-pp.

9.5.8 Continuous Pattern

Figure 54 presents an illustration of the "Continuous" Pointer Adjustment Scenario per Telcordia GR-253-CORE.

FIGURE 54. ILLUSTRATION OF CONTINUOUS PERIODIC POINTER ADJUSTMENT SCENARIO

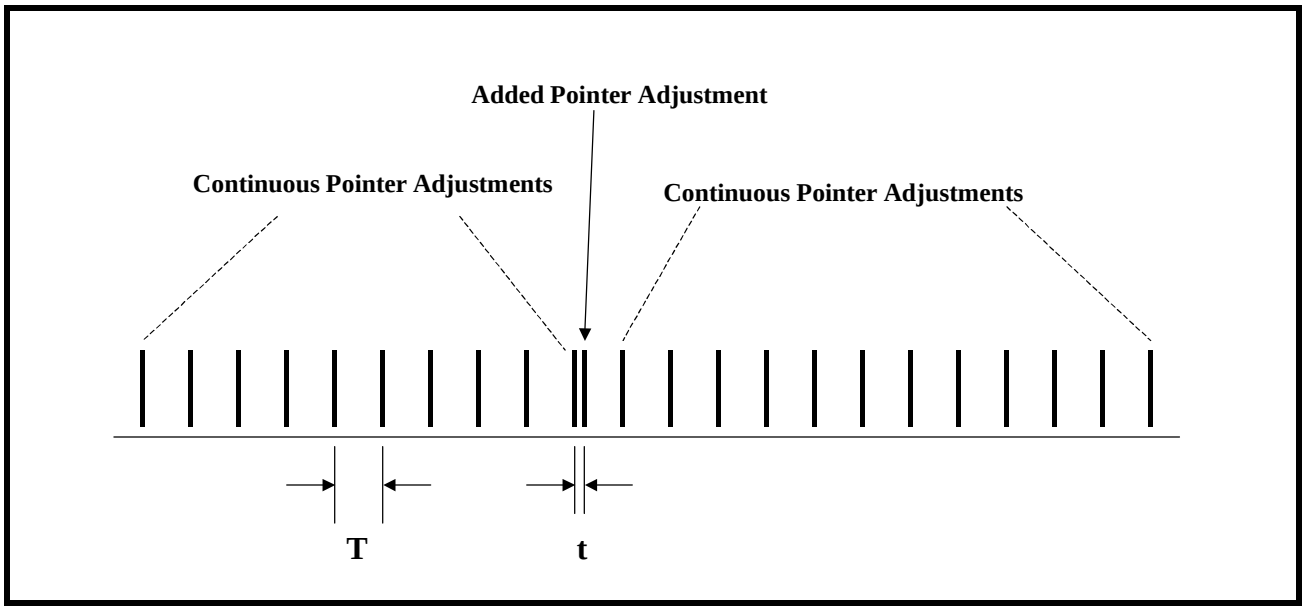


Telcordia GR-253-CORE mandates that the Intrinsic Jitter, within the DS3 signal that is de-mapped from a SONET signal, which is experiencing the "Continuous" pattern of Pointer Adjustments, must not exceed 1.0UI-pp. The spacing between individual pointer adjustments (within this scenario) can range from 7.5ms to 10s.

9.5.9 Continuous Add

Figure 55 presents an illustration of the "Continuous Add Pattern" Pointer Adjustment Scenario per Telcordia GR-253-CORE.

FIGURE 55. ILLUSTRATION OF CONTINUOUS-ADD POINTER ADJUSTMENT SCENARIO



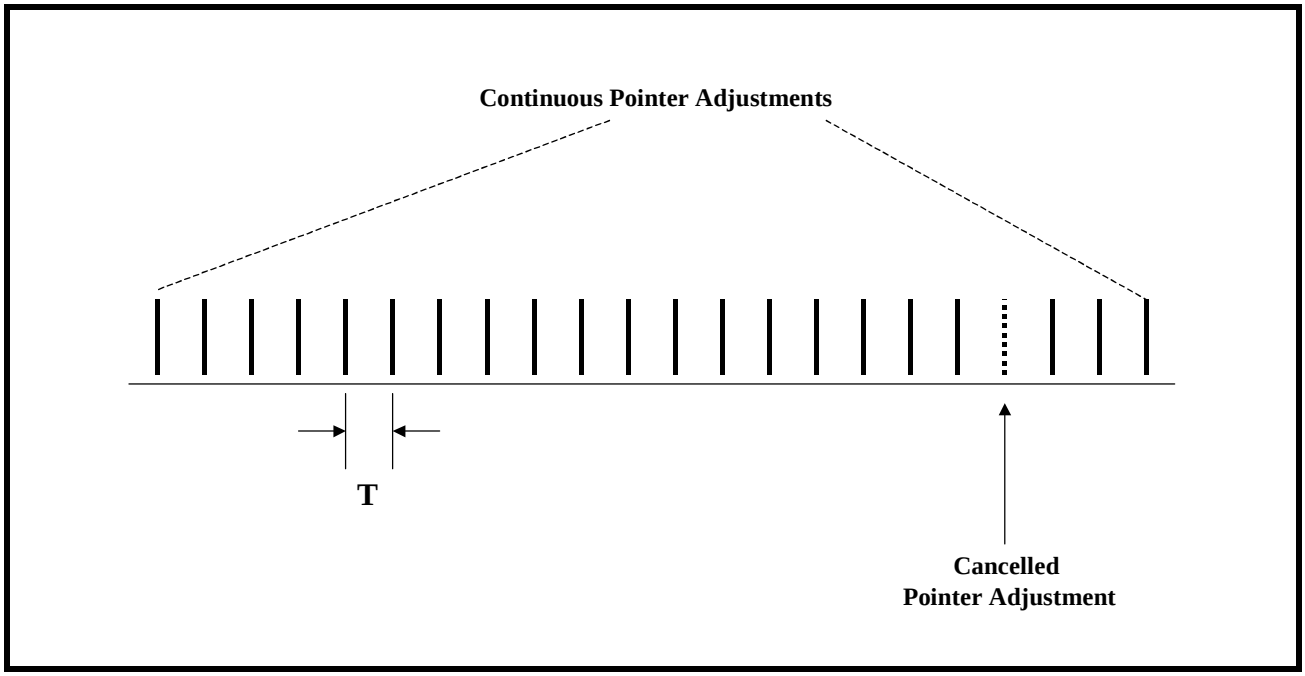
Telcordia GR-253-CORE defines an "Continuous Add" Pointer Adjustment, as the "Continuous" Pointer Adjustment pattern, with an additional pointer adjustment inserted, as shown above in Figure 55.

Telcordia GR-253-CORE mandates that the Intrinsic Jitter, within the DS3 signal that is de-mapped from a SONET signal, which is experiencing the "Continuous Add" pattern of Pointer Adjustments, must not exceed 1.3UI-pp.

9.5.10 Continuous Cancel

Figure 56 presents an illustration of the "Continuous Cancel Pattern" Pointer Adjustment Scenario per Telcordia GR-253-CORE.

FIGURE 56. ILLUSTRATION OF CONTINUOUS-CANCEL POINTER ADJUSTMENT SCENARIO



Telcordia GR-253-CORE defines a "Continuous Cancel" Pointer Adjustment, as the "Continuous" Pointer Adjustment pattern, with an additional pointer adjustment cancelled (or not executed), as shown above in Figure 56.

Telcordia GR-253-CORE mandates that the Intrinsic Jitter, within the DS3 signal that is de-mapped from a SONET signal, which is experiencing the "Continuous Cancel" pattern of Pointer Adjustments, must not exceed 1.3UI-pp.

9.6 *A Review of the DS3 Wander Requirements per ANSI T1.105.03b-1997.*

To be provided in the next revision of this data sheet.

9.7 *A Review of the Intrinsic Jitter and Wander Capabilities of the XRT75L03D in a typical system application*

The Intrinsic Jitter and Wander Test results are summarized in this section.

9.7.1 Intrinsic Jitter Test results

The Intrinsic Jitter Test results for the XRT75L03D in DS3 being de-mapped from SONET is summarized below in Table 2.

TABLE 32: SUMMARY OF "CATEGORY I INTRINSIC JITTER TEST RESULTS" FOR SONET/DS3 APPLICATIONS

SCENARIO DESCRIPTION	SCENARIO NUMBER	XRT75L03D INTRINSIC JITTER TEST RESULTS	TELCORDIA GR-253-CORE CATEGORY I INTRINSIC JITTER REQUIREMENTS
DS3 De-Mapping Jitter		0.13UI-pp	0.4UI-pp
Single Pointer Adjustment	A1	0.201UI-pp	0.43UI-pp (e.g. 0.13UI-pp + 0.3UI-pp)
Pointer Bursts	A2	0.582UI-pp	1.3UI-pp
Phase Transients	A3	0.526UI-pp	1.2UI-pp
87-3 Pattern	A4	0.790UI-pp	1.0UI-pp
87-3 Add	A5	0.926UI-pp	1.3UI-pp
87-3 Cancel	A5	0.885UI-pp	1.3UI-pp
Continuous Pattern	A4	0.497UI-pp	1.0UI-pp
Continuous Add	A5	0.598UI-pp	1.3UI-pp
Continuous Cancel	A5	0.589UI-pp	1.3UI-pp

NOTES:

1. *A detailed test report on our Test Procedures and Test Results is available and can be obtained by contacting your Exar Sales Representative.*
2. *These test results were obtained via the XRT75L03s mounted on our XRT94L43 12-Channel DS3/E3/STS-1 Mapper Evaluation Board.*
3. *These same results apply to SDH/AU-3 Mapping applications.*

9.7.2 Wander Measurement Test Results

Wander Measurement test results will be provided in the next revision of the XRT75L03D Data Sheet.

9.8 *Designing with the XRT75L03D*

In this section, we will discuss the following topics.

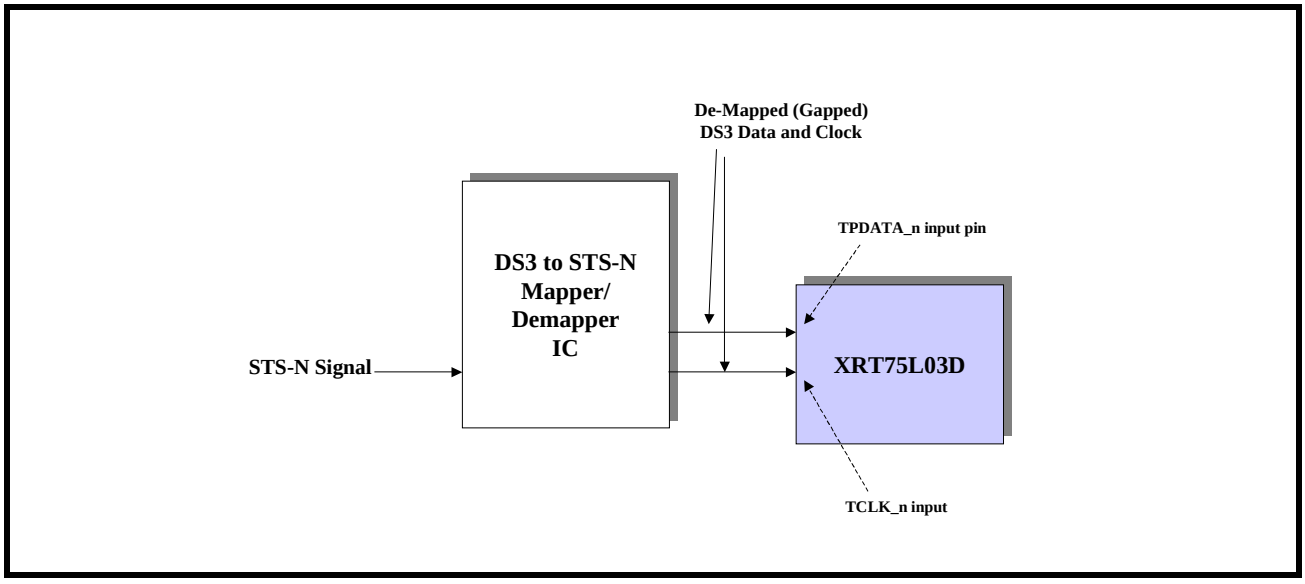
- How to design with and configure the XRT75L03D to permit a system to meet the above-mentioned Intrinsic Jitter and Wander requirements.
- How is the XRT75L03D able to meet the above-mentioned requirements?
- How does the XRT75L03D permits the user to comply with the SONET APS Recovery Time requirements of 50ms (per Telcordia GR-253-CORE)?
- How should one configure the XRT75L03D, if one needs to support "Daisy-Chain" Testing at the end Customer's site?

9.8.1 How to design and configure the XRT75L03D to permit a system to meet the above-mentioned Intrinsic Jitter and Wander requirements

As mentioned earlier, in most application (in which the XRT75L03D will be used in a SONET De-Sync Application) the user will typically interface the XRT75L03D to a Mapper device in the manner as presented below in Figure 57.

In this application, the Mapper has the responsibility of receiving a SONET STS-N/OC-N signal and extracting as many as N DS3 signals from this signal. As a given channel within the Mapper IC extracts out a given DS3 signal (from SONET) it will typically be applying a Clock and Data signal to the "Transmit Input" of the LIU IC. Figure 57 presents a simple illustration as to how one channel, within the XRT75L03D should be connected to the Mapper IC.

FIGURE 57. ILLUSTRATION OF THE XRT75L03D BEING CONNECTED TO A MAPPER IC FOR SONET DE-SYNC APPLICATIONS



As mentioned above, the Mapper IC will typically output a Clock and Data signal to the XRT75L03D. In many cases, the Mapper IC will output the contents of an entire STS-1 data-stream via the Data Signal to the XRT75L03D. However, the Mapper IC typically only supplies a clock pulse via the Clock Signal to the XRT75L03D coincident to whenever a DS3 bit is being output via the Data Signal. In this case, the Mapper IC would not supply a clock edge coincident to when a TOH, POH or any non-DS3 data-bit is being output via the Data-Signal.

Figure 57 indicates that the Data Signal from the Mapper device should be connected to the TPDATA_n input pin of the LIU IC and that the Clock Signal from the Mapper device should be connected to the TCLK_n input pin of the LIU IC.

In this application, the XRT75L03D has the following responsibilities.

- Using a particular clock edge within the "gapped" clock signal (from the Mapper IC) to sample and latch the value of each DS3 data-bit that is output from the Mapper IC.
- To (through the user of the Jitter Attenuator block) attenuate the jitter within this "DS3 data" and "clock signal" that is output from the Mapper IC.
- To convert this "smoothed" DS3 data and clock into industry-compliant DS3 pulses, and to output these pulses onto the line.

To configure the XRT75L03D to operate in the correct mode for this application, the user must execute the following configuration steps.

a. *Configure the XRT75L03D to operate in the DS3 Mode*

The user can configure a given channel (within the XRT75L03D) to operate in the DS3 Mode, by executing either of the following steps.

- **If the XRT75L03D has been configured to operate in the Host Mode**

The user can accomplish this by setting both Bits 2 (E3_n) and Bits 1 (STS-1/DS3*_n), within each of the "Channel Control Registers" to "0" as depicted below.

CHANNEL CONTROL REGISTER - CHANNEL 0 ADDRESS LOCATION = 0X06
CHANNEL 1 ADDRESS LOCATION = 0X0E
CHANNEL 2 ADDRESS LOCATION = 0X16

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		PRBS Enable Ch_n	RLB_n	LLB_n	E3_n	STS-1/$\overline{DS3}$_n	SR/$\overline{DR}$_n
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

- **If the XRT75L03D has been configured to operate in the Hardware Mode**

The user can accomplish this by pulling all of the following input pins "Low".

Pin 76 - E3_0

Pin 94 - E3_1

Pin 85 - E3_2

Pin 72 - STS-1/$\overline{DS3}$_0

Pin 98 - STS-1/$\overline{DS3}$_1

Pin 81 - STS-1/$\overline{DS3}$_2

b. *Configure the XRT75L03D to operate in the Single-Rail Mode*

Since the Mapper IC will typically output a single "Data Line" and a "Clock Line" for each DS3 signal that it demaps from the incoming STS-N signal, it is imperative to configure each channel within the XRT75L03D to operate in the Single Rail Mode.

The user can accomplish this by executing either of the following steps.

- **If the XRT75L03D has been configured to operate in the Host Mode**

The user can accomplish this by setting Bit 0 (SR/DR*), within the each of the "Channel Control" Registers to 1, as illustrated below.

CHANNEL CONTROL REGISTER - CHANNEL 0 ADDRESS LOCATION = 0X06

CHANNEL 1 ADDRESS LOCATION = 0X0E

CHANNEL 2 ADDRESS LOCATION = 0X16

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused		PRBS Enable Ch_n	RLB_n	LLB_n	E3_n	STS-1/ $\overline{DS3}$_n	SR/$\overline{DR}$_n
R/O	R/O	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	1

- **If the XRT75L03D has been configured to operate in the Hardware Mode**

Then the user should tie pin 65 (SR/DR*) to "High".

c. ***Configure each of the three channels within the XRT75L03D to operate in the SONET De-Sync Mode***

The user can accomplish this by executing either of the following steps.

- **If the XRT75L03D has been configured to operate in the Host Mode.**

Then the user should set Bit D2 (JA0) to "0" and Bit D0 (JA1) to "1", within the Jitter Attenuator Control Register, as depicted below.

JITTER ATTENUATOR CONTROL REGISTER - (CHANNEL 0 ADDRESS LOCATION = 0X07

CHANNEL 1 ADDRESS LOCATION = 0X0F

CHANNEL 2 ADDRESS LOCATION = 0X17

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			SONET APS Recovery Time DisableCh_n	JA RESET Ch_n	JA1 Ch_n	JA in Tx Path Ch_n	JA0 Ch_n
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	1

- **If the XRT75L03D has been configured to operate in the Hardware Mode**

Then the user should tie pin 44 (JA0) to a logic "HIGH" and pin 42 (JA1) to a logic "LOW".

Once the user accomplishes either of these steps, then the Jitter Attenuator (within the XRT75L03D) will be configured to operate with a very narrow bandwidth.

d. ***Configure the Jitter Attenuator (within each of three three channels) to operate in the Transmit Direction.***

The user can accomplish this by executing either the following steps.

- **If the XRT75L03D has been configured to operate in the Host Mode.**

Then the user should be Bit D1 (JATx/JARx*) to "1", within the Jitter Attenuator Control Register, as depicted below.

JITTER ATTENUATOR CONTROL REGISTER - CHANNEL 0 ADDRESS LOCATION = 0X07

CHANNEL 1 ADDRESS LOCATION = 0X0F

CHANNEL 2 ADDRESS LOCATION = 0X17

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			SONET APS Recovery Time DisableCh_n	JA RESET Ch_n	JA1 Ch_n	JA in Tx Path Ch_n	JA0 Ch_n
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	1	1

- **If the XRT75L03D has been configured to operate in the Hardware Mode.**

Then the user should tie pin 43 (JATx/JARx*) to "1".

e. *Enable the "SONET APS Recovery Time" Mode*

Finally, if the user intends to use the XRT75L03D in an Application that is required to reacquire proper SONET and DS3 traffic, prior within 50ms of an APS (Automatic Protection Switching) event (per Telcordia GR-253-CORE), then the user should set Bit 4 (SONET APS Recovery Time Disable), within the "Jitter Attenuator Control" Register, to "0" as depicted below.

JITTER ATTENUATOR CONTROL REGISTER - CHANNEL 0 ADDRESS LOCATION = 0X07

CHANNEL 1 ADDRESS LOCATION = 0X0F

CHANNEL 2 ADDRESS LOCATION = 0X17

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			SONET APS Recovery Time DisableCh_n	JA RESET Ch_n	JA1 Ch_n	JA in Tx Path Ch_n	JA0 Ch_n
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	1

NOTES:

1. *The ability to disable the "SONET APS Recovery Time" mode is only available if the XRT75L03D is operating in the Host Mode. If the XRT75L03D is operating in the "Hardware" Mode, then this "SONET APS Recovery Time Mode" feature will always be enabled.*
2. *The "SONET APS Recovery Time" mode will be discussed in greater detail in "Section 9.8.3, How does the XRT75L03D permit the user to comply with the SONET APS Recovery Time requirements of 50ms (per Telcordia GR-253-CORE)?" on page 126.*

9.8.2 Recommendations on Pre-Processing the Gapped Clocks (from the Mapper/ASIC Device) prior to routing this DS3 Clock and Data-Signals to the Transmit Inputs of the XRT75L03D

In order to minimize the effects of "Clock-Gapping" Jitter within the DS3 signal that is ultimately transmitted to the DS3 Line (or facility), we recommend that some "pre-processing" of the "Data-Signals" and "Clock-Signals" (which are output from the Mapper device) be implemented prior to routing these signals to the "Transmit Inputs" of the XRT75L03D.

9.8.2.1 *SOME NOTES PRIOR TO STARTING THIS DISCUSSION:*

Our simulation results indicate that Jitter Attenuator PLL (within the XRT75L03D LIU IC) will have no problem handling and processing the "Data-Signal" and "Clock-Signal" from a Mapper IC/ASIC if no pre-processing has been performed on these signals. In order words, our simulation results indicate that the Jitter Attenuator PLL (within the LIU IC) will have no problem handling the "worst-case" of 59 consecutive bits of no clock pulses in the "Clock-Signal (due to the Mapper IC processing the TOH bytes, an Incrementing Pointer-Adjustment-induced "stuffed-byte", the POH byte, and the two fixed-stuff bytes within the STS-1 SPE, etc), immediately followed be processing clusters of DS3 data-bits (as shown in Figure 37) and still comply with the "Category I Intrinsic Jitter Requirements per Telcordia GR-253-CORE for DS3 applications.

NOTE: *If this sort of "pre-processing" is already supported by the Mapper device that you are using, then no further action is required by the user.*

9.8.2.2 *OUR PRE-PROCESSING RECOMMENDATIONS*

For the time-being, we recommend that the customer implement the "pre-processing" of the DS3 "Data-Signal" and "Clock-Signal" as described below. Currently we are aware that some of the Mapper products on the Market do implement this exact "pre-processing" algorithm. However, if the customer is implementing their Mapper Design in an ASIC or FPGA solution, then we strongly recommend that the user implement the necessary logic design to realize the following recommendations.

Some time ago, we spent some time, studying (and then later testing our solution with) the PM5342 OC-3 to DS3 Mapper IC from PMC-Sierra. In particular, we wanted to understand the type of "DS3 Clock" and "Data" signal that this DS3 to OC-3 Mapper IC outputs.

During this effort, we learned the following.

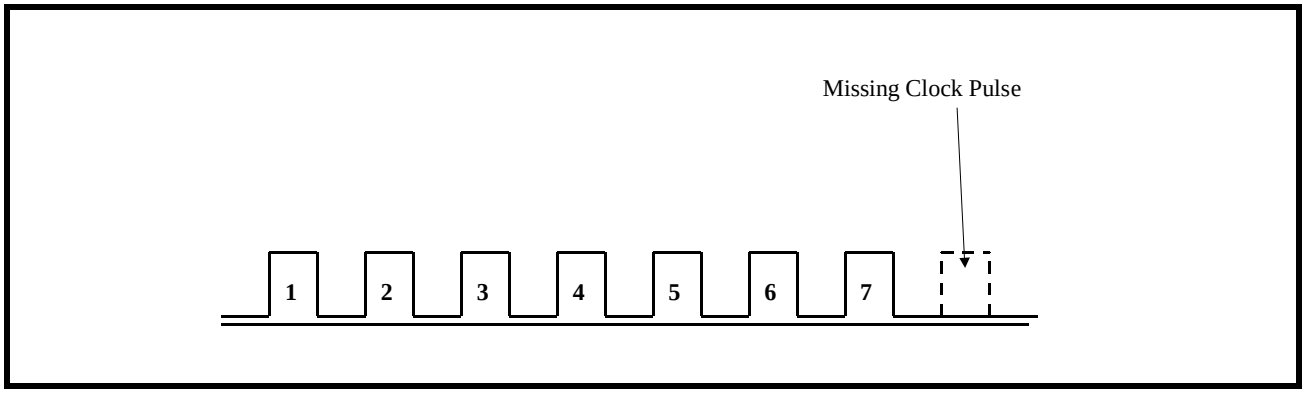
1. This "DS3 Clock" and "Data" signal, which is output from the Mapper IC consists of two major "repeating" patterns (which we will refer to as "MAJOR PATTERN A" and "MAJOR PATTERN B". The behavior of each of these patterns is presented below.

MAJOR PATTERN A

MAJOR PATTERN A consists of two "sub" or minor-patterns, (which we will refer to as "MINOR PATTERN P1 and P2).

MINOR PATTERN P1 consists of a string of seven (7) clock pulses, followed by a single gap (no clock pulse). An illustration of MINOR PATTERN P1 is presented below in Figure 58.

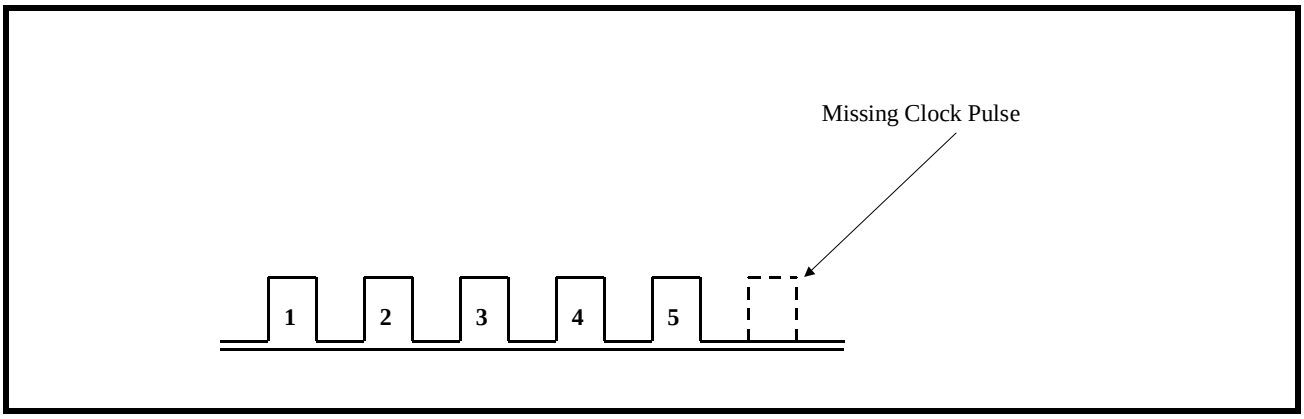
FIGURE 58. ILLUSTRATION OF MINOR PATTERN P1



It should be noted that each of these clock pulses has a period of approximately 19.3ns (or has an "instantaneously frequency of 51.84MHz).

MINOR Pattern P2 consists of string of five (5) clock pulses, which is also followed by a single gap (no clock pulse). An illustration of Pattern P2 is presented below in Figure 59.

FIGURE 59. ILLUSTRATION OF MINOR PATTERN P2



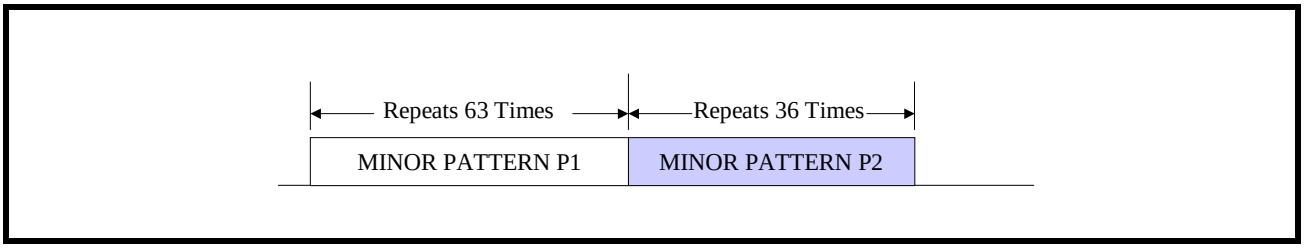
HOW MAJOR PATTERN A IS SYNTHESIZED

MAJOR PATTERN A is created (by the Mapper IC) by:

- Repeating MINOR PATTERN P1 (e.g., 7 clock pulses, followed by a gap) 63 times.
- Upon completion of the 63rd transmission of MINOR PATTERN P1, MINOR PATTERN P2 is transmitted repeatedly 36 times.

Figure 60 presents an illustration which depicts the procedure that is used to synthesize MAJOR PATTERN A

FIGURE 60. ILLUSTRATION OF PROCEDURE WHICH IS USED TO SYNTHESIZE MAJOR PATTERN A



Hence, MAJOR PATTERN A consists of "(63 x 7) + (36 x 5)" = 621 clock pulses. These 621 clock pulses were delivered over a period of "(63 x 8) + (36 x 6)" = 720 STS-1 (or 51.84MHz) clock periods.

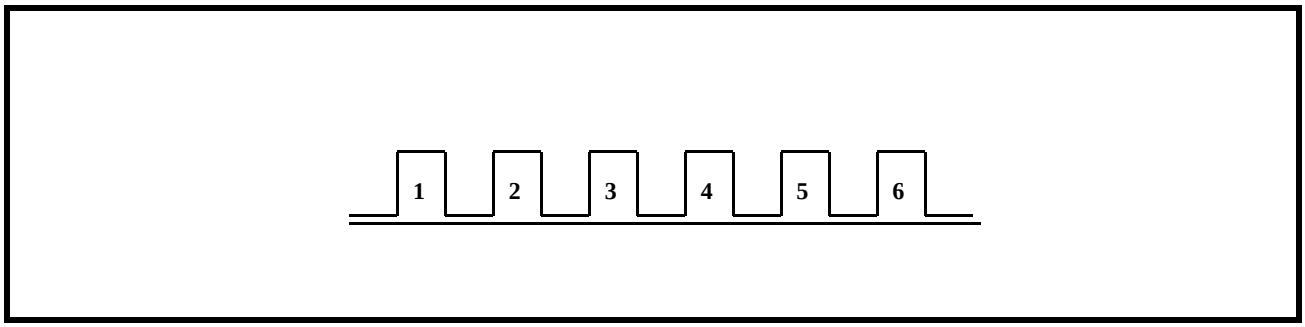
MAJOR PATTERN B

MAJOR PATTERN B consists of three sub or minor-patterns (which we will refer to as "MINOR PATTERNS P1, P2 and P3).

MINOR PATTERN P1, which is used to partially synthesize MAJOR PATTERN B, is exactly the same "MINOR PATTERN P1" as was presented above in Figure 30. Similarly, the MINOR PATTERN P2, which is also used to partially synthesize MAJOR PATTERN B, is exactly the same "MINOR PATTERN P2" as was presented in Figure 31.

MINOR PATTERN P3 (which has yet to be defined) consists of a string of six (6) clock pulses, which contains no gaps. An illustration of MINOR PATTERN P3 is presented below in Figure 61.

FIGURE 61. ILLUSTRATION OF MINOR PATTERN P3



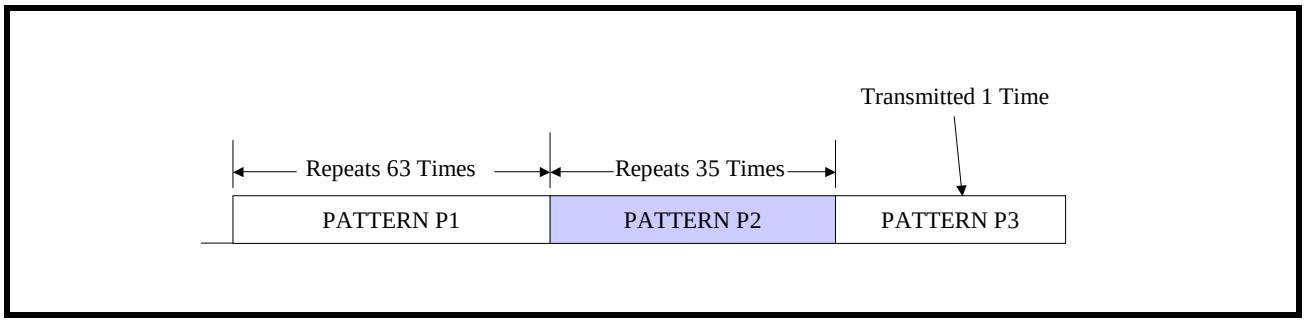
HOW MAJOR PATTERN B IS SYNTHESIZED

MAJOR PATTERN B is created (by the Mapper IC) by:

- Repeating MINOR PATTERN P1 (e.g., 7 clock pulses, followed by a gap) 63 times.
- Upon completion of the 63rd transmission of MINOR PATTERN P1, MINOR PATTERN P2 is transmitted repeatedly 36 times.
- pon completion of the 35th transmission of MINOR PATTERN P2, MINOR PATTERN P3 is transmitted once.

Figure 62 presents an illustration which depicts the procedure that is used to synthesize MAJOR PATTERN B.

FIGURE 62. ILLUSTRATION OF PROCEDURE WHICH IS USED TO SYNTHESIZE PATTERN B



Hence, MAJOR PATTERN B consists of "(63 x 7) + (35 x 5)" + 6 = 622 clock pulses.

These 622 clock pulses were delivered over a period of "(63 x 8) + (35 x 6) + 6 = 720 STS-1 (or 51.84MHz) clock periods.

PUTTING THE PATTERNS TOGETHER

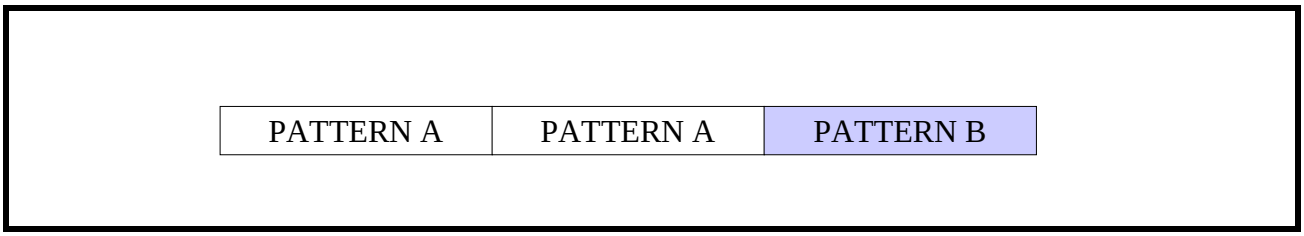
Finally, the DS3 to OC-N Mapper IC clock output is reproduced by doing the following.

- MAJOR PATTERN A is transmitted two times (repeatedly).
- After the second transmission of MAJOR PATTERN A, MAJOR PATTERN B is transmitted once.
- Then the whole process repeats.

Throughout the remainder of this document, we will refer to this particular pattern as the "SUPER PATTERN".

Figure 63 presents an illustration of this "SUPER PATTERN" which is output via the Mapper IC.

FIGURE 63. ILLUSTRATION OF THE SUPER PATTERN WHICH IS OUTPUT VIA THE "OC-N TO DS3" MAPPER IC



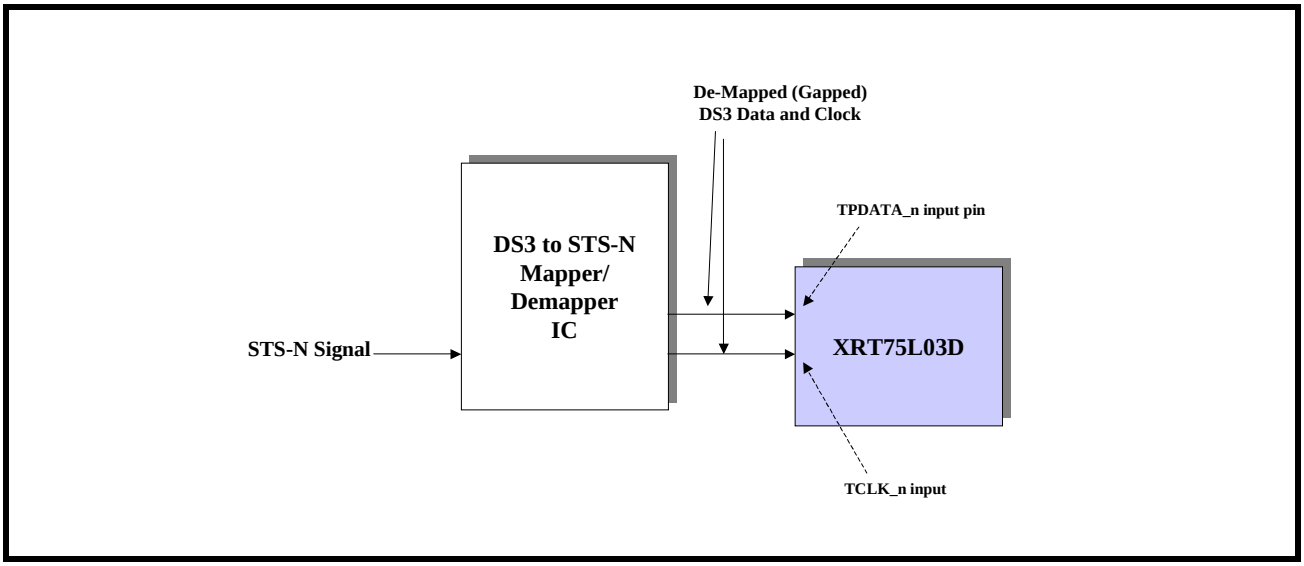
CROSS-CHECKING OUR DATA

- Each SUPER PATTERN consists of (621 + 621 + 622) = 1864 clock pulses.
- The total amount of time, which is required for the "DS3 to OC-N Mapper" IC to transmit this SUPER PATTERN is (720 + 720 + 720) = 2160 "STS-1" clock periods.
- This amount to a period of (2160/51.84MHz) = 41,667ns.
- In a period of 41, 667ns, the XRT75L03D (when configured to operate in the DS3 Mode), will output a total (41,667ns x 44,736,000) = 1864 uniformly spaced DS3 clock pulses.
- Hence, the number of clock pulses match.

APPLYING THE SUPER PATTERN TO THE XRT75L03D

Whenever the XRT75L03D is configured to operate in a "SONET De-Sync" application, the device will accept a continuous string of the above-defined SUPER PATTERN, via the TCLK input pin (along with the corresponding data). The channel within the XRT75L03D (which will be configured to operate in the "DS3" Mode) will output a DS3 line signal (to the DS3 facility) that complies with the "Category I Intrinsic Jitter Requirements - per Telcordia GR-253-CORE (for DS3 applications). This scheme is illustrated below in Figure 64.

FIGURE 64. SIMPLE ILLUSTRATION OF THE XRT75L03D BEING USED IN A SONET DE-SYNCHRONIZER" APPLICATION



According to this figure, the Jitter Attenuator will receive a very jitter DS3 or E3 signal (e.g., data and clock signals) from the Mapper device via the "Transmit System-side" input pins of the LIU IC.

9.8.3 How does the XRT75L03D permit the user to comply with the SONET APS Recovery Time requirements of 50ms (per Telcordia GR-253-CORE)?

Telcordia GR-253-CORE, Section 5.3.3.3 mandates that the "APS Completion" (or Recovery) time be 50ms or less. Many of our customers interpret this particular requirement as follows.

"From the instant that an APS is initiated on a high-speed SONET signal, all lower-speed SONET traffic (which is being transported via this "high-speed" SONET signal) must be fully restored within 50ms. Similarly, if the "high-speed" SONET signal is transporting some PDH signals (such as DS1 or DS3, etc.), then those entities that are responsible for acquiring and maintaining DS1 or DS3 frame synchronization (with these DS1 or DS3 data-streams that have been de-mapped from SONET) must have re-acquired DS1 or DS3 frame synchronization within 50ms" after APS has been initiated."

The XRT75L03D was designed such that the DS3 signals that it receives from a SONET Mapper device and processes will comply with the Category I Intrinsic Jitter requirements per Telcordia GR-253-CORE.

Reference 1 documents some APS Recovery Time testing, which was performed to verify that the Jitter Attenuator blocks (within the XRT75L03D) device that permit it to comply with the Category I Intrinsic Jitter Requirements (for DS3 Applications) per Telcordia GR-253-CORE, do not cause it to fail to comply with the "APS Completion Time" requirements per Section 5.3.3.3 of Telcordia GR-253-CORE. However, Table 3 presents a summary of some APS Recovery Time requirements that were documented within this test report.

Table 3,

TABLE 33: MEASURED APS RECOVERY TIME AS A FUNCTION OF DS3 PPM OFFSET

DS3 PPM OFFSET (PER W&G ANT-20SE)	MEASURED APS RECOVERY TIME (PER LOGIC ANALYZER)
-99 ppm	1.25ms
-40ppm	1.54ms
-30 ppm	1.34ms
-20 ppm	1.49ms
-10 ppm	1.30ms
0 ppm	1.89ms
+10 ppm	1.21ms
+20 ppm	1.64ms
+30 ppm	1.32ms
+40 ppm	1.25ms
+99 ppm	1.35ms

NOTE: *The APS Completion (or Recovery) time requirement is 50ms.*

Configuring the XRT75L03D to be able to comply with the SONET APS Recovery Time Requirements of 50ms

Quite simply, the user can configure a given Jitter Attenuator block (associated with a given channel) to (1) comply with the "APS Completion Time" requirements per Telcordia GR-253-CORE, and (2) also comply with the "Category I Intrinsic Jitter Requirements per Telcordia GR-253-CORE (for DS3 applications) by making sure that Bit 4 (SONET APS Recovery Time Disable Ch_n), within the Jitter Attenuator Control Register is set to "0" as depicted below.

JITTER ATTENUATOR CONTROL REGISTER - CHANNEL 0 ADDRESS LOCATION = 0X07

CHANNEL 1 ADDRESS LOCATION = 0X0F

CHANNEL 2 ADDRESS LOCATION = 0X17

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			SONET APS Recovery Time Disable Ch_n	JA RESET Ch_n	JA1 Ch_n	JA in Tx Path Ch_n	JA0 Ch_n
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	1	1

NOTE: *The user can only disable the "SONET APS Recovery Time Mode" if the XRT75L03D is operating in the Host Mode. If the user is operating the XRT75L03D in the Hardware Mode, then the user will have NO ability to disable the "SONET APS Recovery Time Mode" feature.*

9.8.4 How should one configure the XRT75L03D, if one needs to support "Daisy-Chain" Testing at the end Customer's site?

Daisy-Chain testing is emerging as a new requirements that many of our customers are imposing on our SONET Mapper and LIU products. Many System Designer/Manufacturers are finding out that whenever their end-customers that are evaluating and testing out their systems (in order to determine if they wish to move forward and start purchasing this equipment in volume) are routinely demanding that they be able to test out these systems with a single piece of test equipment. This means that the end-customer would like to take a single piece of DS3 or STS-1 test equipment and (with this test equipment) snake the DS3 or STS-1 traffic (that this test equipment will generate) through many or (preferably all) channels within the system. For example, we have had request from our customers that (on a system that supports OC-192) our silicon be able to support this DS3 or STS-1 traffic snaking through the 192 DS3 or STS-1 ports within this system.

After extensive testing, we have determined that the best approach to complying with test "Daisy-Chain" Testing requirements, is to configure the Jitter Attenuator blocks (within each of the Channels within the XRT75L03D) into the "32-Bit" Mode. The user can configure the Jitter Attenuator block (within a given channel of the XRT75L03D) to operate in this mode by settings in the table below.

JITTER ATTENUATOR CONTROL REGISTER - CHANNEL 0 ADDRESS LOCATION = 0X07

CHANNEL 1 ADDRESS LOCATION = 0X0F

CHANNEL 2 ADDRESS LOCATION = 0X17

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Unused			SONET APS Recovery Time Disable Ch_n	JA RESET Ch_n	JA1 Ch_n	JA in Tx Path Ch_n	JA0 Ch_n
R/O	R/O	R/O	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	1	1	0

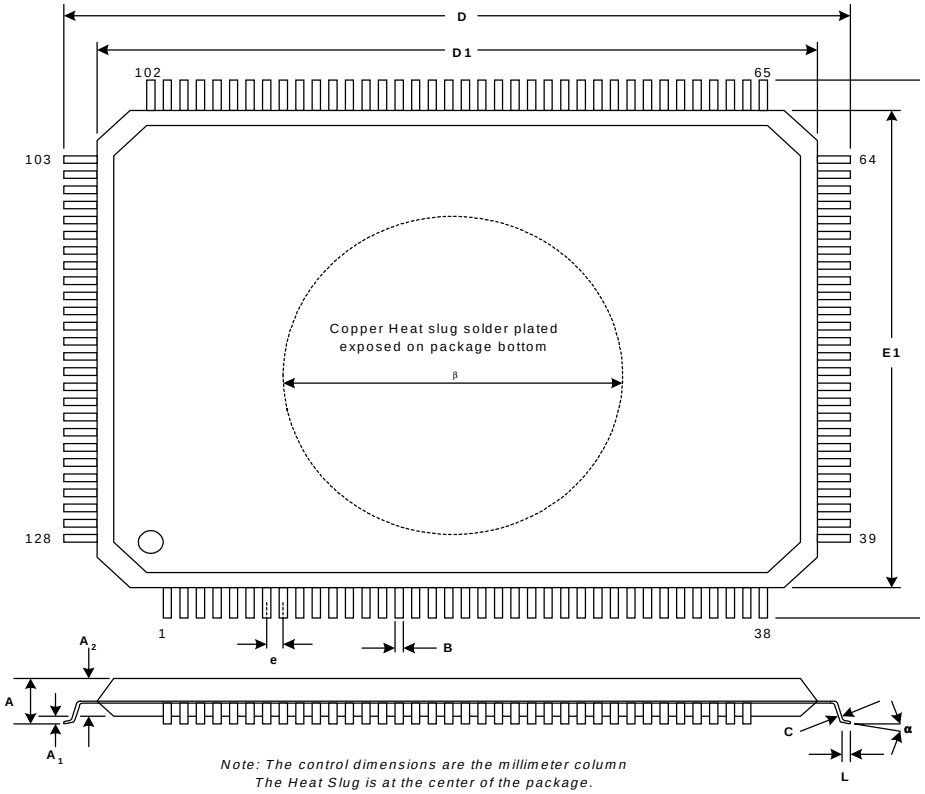
REFERENCES

1. TEST REPORT - AUTOMATIC PROTECTION SWITCHING (APS) RECOVERY TIME TESTING WITH THE XRT94L43 DS3/E3/STS-1 TO STS-12 MAPPER IC - Revision C Silicon

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT75L03DIV	14 x 20 mm 128 Pin LQFP	- 40°C to + 85°C

PACKAGE DIMENSIONS - 14X20 MM, 128 PIN PACKAGE



Note: The control dimensions are the millimeter column
The Heat Slug is at the center of the package.

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.055	0.063	1.40	1.60
A1	0.002	0.006	0.05	0.15
A2	0.053	0.057	1.35	1.45
B	0.007	0.011	0.17	0.27
C	0.004	0.008	0.09	0.20
D	0.858	0.874	21.80	22.20
D1	0.783	0.791	19.90	20.10
E	0.622	0.638	15.80	16.20
E1	0.547	0.555	13.90	14.10
e	0.020 BSC		0.50 BSC	
L	0.018	0.030	0.45	0.75
α	0°	7°	0°	7°
β	0.370	0.390	9.40	9.90

REVISIONS

REVISION	DATE	COMMENTS
1.0.0	June 2003	Initial issue

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