Single, Dual, and Quad Micropower, Low Drift, RRIO Operational Amplifiers

ISL28130, ISL28230, ISL28430

The ISL28130, ISL28230 and ISL28430 are single, dual and quad micropower, low offset drift operational amplifiers that are optimized for single and dual supply operation from 1.65V to 5.5V and ±0.825V to ±2.75V. Their low supply current of 20µA and rail-to-rail input range enable the ISL28130, ISL28230, ISL28430 to be an excellent general purpose op amp for a range of applications. The ISL28130, ISL28230 and ISL28430 are ideal for handheld devices that operate off 2 AA or single Li-ion batteries.

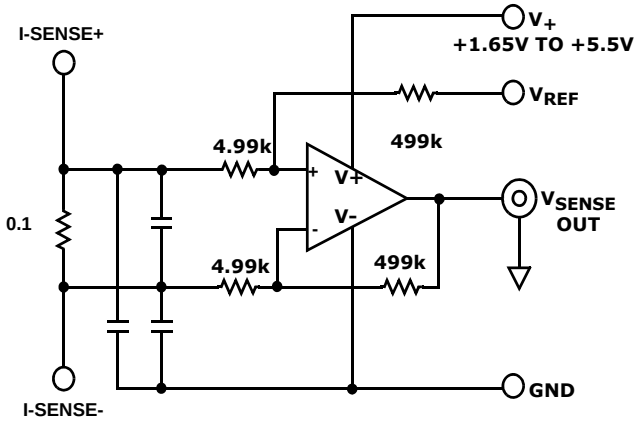
The ISL28130 is available in industry standard pinouts for 5 Ld SOT-23, 5 Ld SC70 and 8 Ld SOIC packages. The ISL28230 is available in industry standard pinouts for 8 Ld MSOP, 8Ld SOIC and 8 Ld DFN packages. The ISL28430 is available in 14 Ld TSSOP and 14 Ld SOIC packages. All devices operate over the temperature range of -40°C to +125°C.

Features

- Low Input Offset Voltage . . . . . 40µV, Max.
- Low Offset Drift . . . . . 150nV/°C, Max
- Input Bias Current . . . . . 250 pA, Max.
- Quiescent Current (Per Amplifier) . . . . . .20µA, Typ.
- Single Supply Range . . . . . +1.65V to +5.5V
- Dual Supply Range. . . . . ±0.825V to ±2.75V
- Low Noise (0.01Hz to 10Hz) . . . . . 1.1µV_{P-P}, Typ.
- Rail-to-Rail Inputs and Output

Applications

- Bi-Directional Current Sense
- Temperature Measurement
- Medical Equipment
- Electronic Weigh Scales
- Precision/Strain Gauge Sensor
- Precision Regulation
- Low Ohmic Current Sense
- High Gain Analog Front Ends



BI-DIRECTIONAL CURRENT SENSE AMPLIFIER

FIGURE 1. TYPICAL APPLICATION DIAGRAM

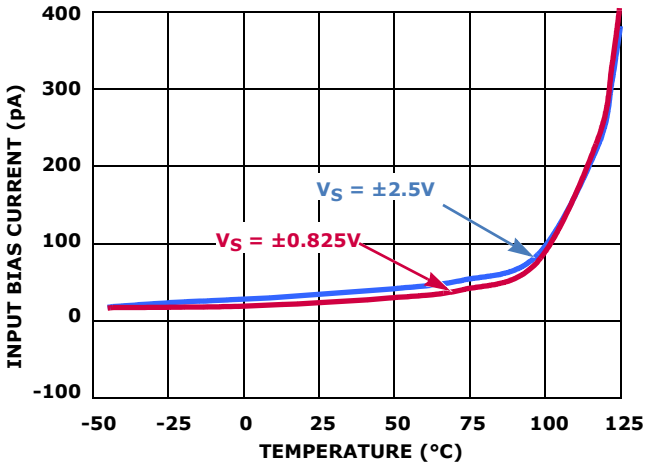


FIGURE 2. I_B vs TEMPERATURE

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Ordering Information

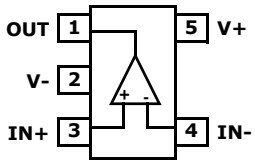
PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL28130CHZ-T7	BDPA (Note 4)	0 to +70	5 Ld SOT-23	P5.064A
ISL28130CHZ-T7A	BDPA (Note 4)	0 to +70	5 Ld SOT-23	P5.064A
Coming Soon ISL28130FHZ	TBD	-40 to +125	5 Ld SOT-23	P5.064A
ISL28130CEZ-T7	BLA (Note 4)	0 to +70	5 Ld SC70	P5.049
ISL28130CEZ-T7A	BLA (Note 4)	0 to +70	5 Ld SC70	P5.049
Coming Soon ISL28130FEZ	TBD	-40 to +125	5 Ld SC70	P5.049
Coming Soon ISL28130CBZ	28130 CBZ	0 to +70	8 Ld SOIC	M8.15E
Coming Soon ISL28130FBZ	TBD	-40 to +125	8 Ld SOIC	M8.15E
ISL28230CUZ	8230Z	0 to +70	8 Ld MSOP	M8.118A
Coming Soon ISL28230FUZ	TBD	-40 to +125	8 Ld MSOP	M8.118A
ISL28230CBZ	28230 CBZ	0 to +70	8 Ld SOIC	M8.15E
Coming Soon ISL28230FBZ	TBD	-40 to +125	8 Ld SOIC	M8.15E
ISL28230CRZ	230Z	0 to +70	8 Ld 3x3mm DFN	L8.3x3J
Coming Soon ISL28230FRZ	TBD	-40 to +125	8 Ld 3x3mm DFN	L8.3x3J
ISL28430CBZ	28430 CBZ	0 to +70	14 Ld SOIC	MDP0027
Coming Soon ISL28430FBZ	TBD	-40 to +125	14 Ld SOIC	MDP0027
ISL28430CVZ	28430 CVZ	0 to +70	14 Ld TSSOP	MDP0044
Coming Soon ISL28430FVZ	TBD	-40 to +125	14 Ld TSSOP	MDP0044

NOTES:

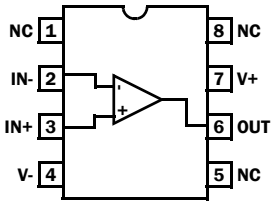
1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL28130, ISL28230, ISL28430. For more information on MSL please see techbrief TB363.
4. The part marking is located on the bottom of the part.

Pin Configurations

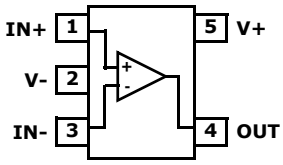
ISL28130
(5 LD SOT-23)
TOP VIEW



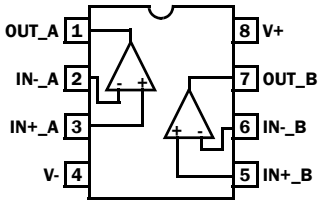
ISL28130
(8 LD SOIC)
TOP VIEW



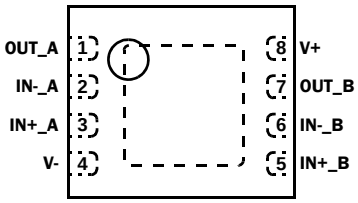
ISL28130
(5 LD SC70)
TOP VIEW



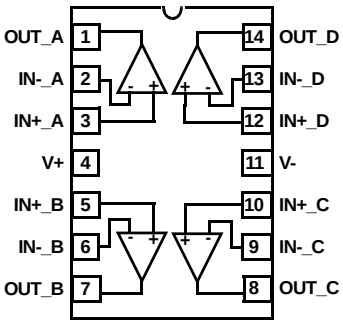
ISL28230
(8 LD MSOP, SOIC)
TOP VIEW



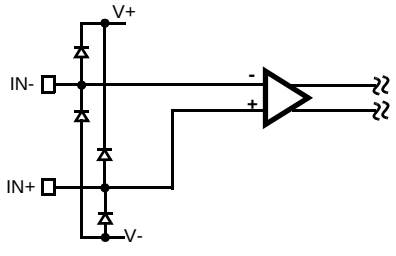
ISL28230
(8 LD DFN)
TOP VIEW



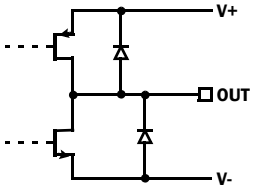
ISL28430
(14 LD TSSOP, SOIC)
TOP VIEW



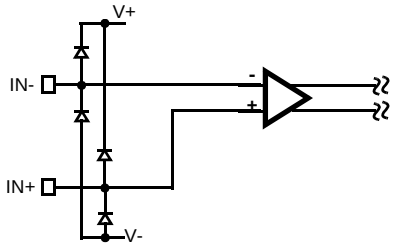
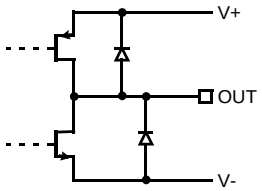
Pin Descriptions

ISL28130 (5 Ld SOT23)	ISL28130 (8 Ld SOIC)	ISL28130 (5 LD SC70)	PIN NAME	FUNCTION	EQUIVALENT CIRCUIT
3	3	1	IN+	Non-inverting input	 Circuit 1
2	4	2	V-	Negative supply	
4	2	3	IN-	Inverting input	(See “Circuit 1”)

Pin Descriptions (Continued)

ISL28130 (5 Ld SOT23)	ISL28130 (8 Ld SOIC)	ISL28130 (5 LD SC70)	PIN NAME	FUNCTION	EQUIVALENT CIRCUIT
1	6	4	OUT	Output	 Circuit 2
5	7	5	V+	Positive supply	
	1, 5, 8		NC	Not Connected – This pin is not electrically connected internally.	

Pin Descriptions

ISL28230 (8 Ld MSOP, SOIC, DFN)	ISL28430 (14 Ld TSSOP, SOIC)	PIN NAME	FUNCTION	EQUIVALENT CIRCUIT
3	3	IN+_A	Non-inverting input	 Circuit 1
5	5	IN+_B		
-	10	IN+_C		
-	12	IN+_D		
4	11	V-	Negative supply	
2	2	IN-_A	Inverting input	(See Circuit 1)
6	6	IN-_B		
-	9	IN-_C		
-	13	IN-_D		
1	1	OUT_A	Output	 Circuit 2
7	7	OUT_B		
-	8	OUT_C		
-	14	OUT_D		
8	4	V+	Positive supply	
PD	-	Paddle	Thermal Pad. Connect to most negative supply. DFN packages only.	

Absolute Maximum Ratings

Max Supply Voltage V+ to V- 6.5V
Max Voltage VIN to GND . . . . . (V- - 0.3V) to (V+ + 0.3V)V
Max Input Differential Voltage 6.5V
Max Input Current 20mA
Max Voltage VOUT to GND (10s) . . . . . ±3.0V
ESD Tolerance (ISL28130)
Human Body Model (Tested at JESD22-A114F) 3000V
Machine Model (Tested at JESD22-A115B) 200V
Charged Device Model (Tested at JESD22-C110D) 1500V
ESD Tolerance (ISL28230, ISL28430)
Human Body Model (Tested at JESD22-A114F) 4000V
Machine Model (Tested at JESD22-A115B) 400V
Charged Device Model (Tested at JESD22-C110D) 2000V
Latch-Up Passed Per JESD78B . . . . . +125°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
5 Ld SOT-23 (Notes 5, 7)	225	110
5 Ld SC70 (Notes 5, 7)	206	146
8 Ld SOIC (ISL28130) (Notes 5, 7)	135	95
8 Ld MSOP (Notes 5, 7)	180	65
8 Ld SOIC (ISL28230) (Notes 5, 7)	125	90
8 Ld DFN (Notes 6, 8)	53	12
14 Ld TSSOP (Notes 5, 7)	110	40
14 Ld SOIC (Notes 5, 7)	75	47

Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Temperature Range:
Full Grade Devices . . . . . -40°C to +125°C
Commercial Grade Devices . . . . . 0°C to +70°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

5. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
6. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
7. For θ_{JC}, the “case temp” location is taken at the package top center.
8. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications

V_+ = 5V, V_- = 0V, VCM = 2.5V, T_A = +25°C, R_L = 10kΩ, unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +125°C.**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
DC SPECIFICATIONS						
V_{OS}	Input Offset Voltage	Vs = 1.65V to 5.5V	-40	±5	40	µV
			-46.8	-	**46.8**	µV
TCV_{OS}	Input Offset Voltage Temperature Coefficient		**-150**	20	**150**	nV/°C
I_{OS}	Input Offset Current		-	-60	-	pA
TCI_{OS}	Input Offset Current Temperature Coefficient		-	0.11	-	pA/°C
I_B	Input Bias Current	T = 0°C to +70°C	-250	-	250	pA
			-700	-	**700**	pA
Common Mode Input Voltage Range		Guaranteed by CMRR	**-0.1**	-	**5.1**	V
CMRR	Common Mode Rejection Ratio	VCM = -0.1V to 5.1V	110	125	-	dB
			105	-	-	dB
PSRR	Power Supply Rejection Ratio	Vs = 2.0V to 5.5V	105	138	-	dB
			105	-	-	dB
V_{OH}	Output Voltage Swing, High		**4.950**	4.981	-	V
V_{OL}	Output Voltage Swing, Low		-	18	**50**	mV
A_{OL}	Open Loop Gain	R_L = 1MΩ	-	150	-	dB
V_+	Supply Voltage	Guaranteed by V_{OS}	**1.65**	-	**5.5**	V

Electrical Specifications V_+ = 5V, V_- = 0V, VCM = 2.5V, T_A = +25°C, R_L = 10kΩ, unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +125°C. (Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
I_S	Supply Current, Per Amplifier	R_L = OPEN	-	20	25	µA
			-	-	**35**	µA
I_{SC+}	Output Source Short Circuit Current	R_L = Short V-	-	15	-	mA
I_{SC-}	Output Sink Short Circuit Current	R_L = Short V+	-	-15	-	mA
AC SPECIFICATIONS						
GBWP	Gain Bandwidth Product	A_V = 100, R_F = 100kΩ, R_G = 1kΩ, R_L = 10kΩ to V_{CM}	-	400	-	kHz
e_N V_{P-P}	Peak-to-Peak Input Noise Voltage	f = 0.01Hz to 10Hz	-	1.1	-	$µV_{P-P}$
e_N	Input Noise Voltage Density	f = 1kHz	-	65	-	nV/√(Hz)
i_N	Input Noise Current Density	f = 1kHz	-	72	-	fA/√(Hz)
		f = 10Hz	-	80	-	fA/√(Hz)
C_{in}	Differential Input Capacitance	f = 1MHz	-	1.6	-	pF
	Common Mode Input Capacitance		-	1.12	-	pF
TRANSIENT RESPONSE						
SR	Positive Slew Rate	V_{OUT} = 1V to 4V, R_L = 10kΩ	-	0.2	-	V/µs
	Negative Slew Rate		-	0.1	-	V/µs
t_r, t_f, Small Signal	Rise Time, t_r 10% to 90%	A_V = +1, V_{OUT} = $0.1V_{P-P}$, R_F = 0Ω, R_L = 10kΩ, C_L = 1.2pF	-	1.1	-	µs
	Fall Time, t_f 10% to 90%		-	1.1	-	µs
t_r, t_f Large Signal	Rise Time, t_r 10% to 90%	A_V = +1, V_{OUT} = $2V_{P-P}$, R_F = 0Ω, R_L = 10kΩ, C_L = 1.2pF	-	20	-	µs
	Fall Time, t_f 10% to 90%		-	30	-	µs
t_s	Settling Time to 0.1%, $2V_{P-P}$ Step	A_V = +1, R_F = 0Ω, R_L = 10kΩ, C_L = 1.2pF	-	35	-	µs
$t_{recover}$	Output Overload Recovery Time, Recovery to 90% of Output Saturation	A_V = +2, R_F = 10kΩ, R_L = Open, C_L = 3.7pF	-	10.5	-	µs

NOTE:

9. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Typical Performance Curves

V+ = 5V, V- = 0V, V_{CM} = 2.5V, R_L = Open, T = +25°C, unless otherwise specified.

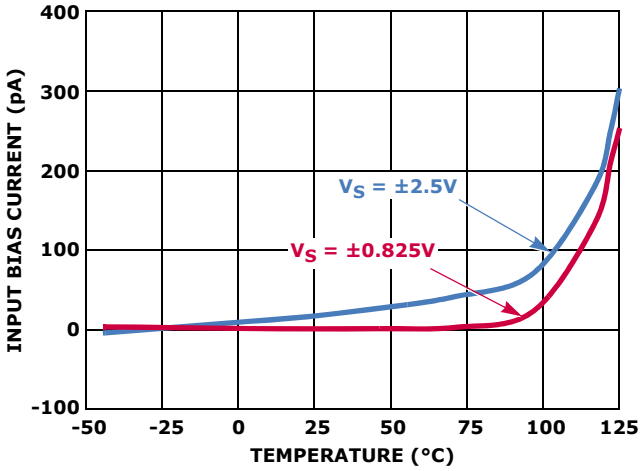


FIGURE 3. I_{B+} vs TEMPERATURE

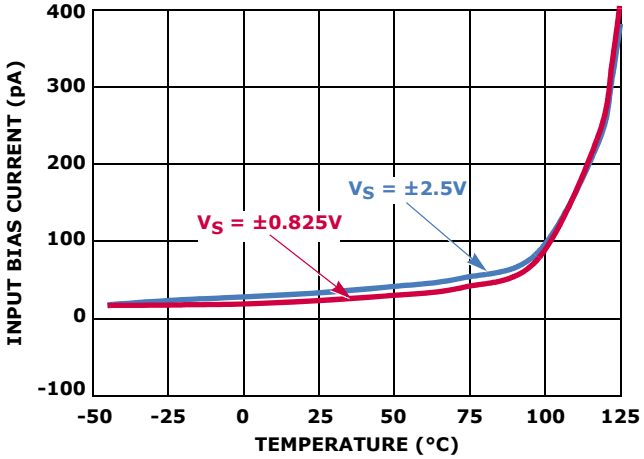


FIGURE 4. I_{B-} vs TEMPERATURE

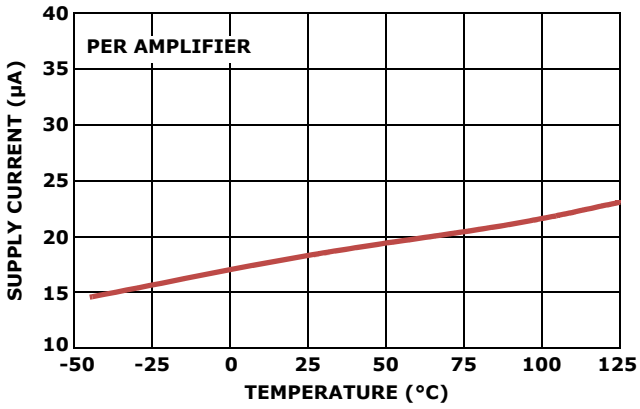


FIGURE 5. SUPPLY CURRENT vs TEMPERATURE, Vs = ±0.825V

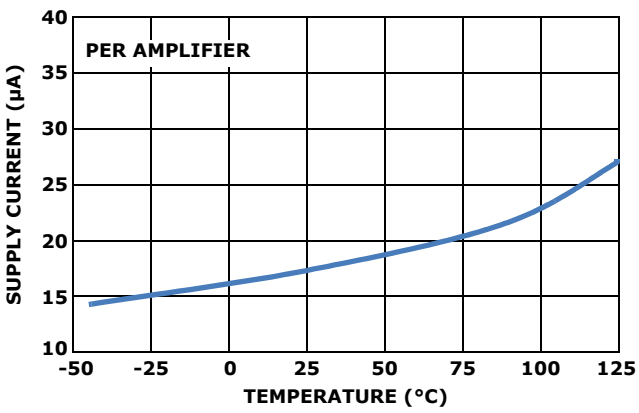


FIGURE 6. SUPPLY CURRENT vs TEMPERATURE, Vs = ±2.5V

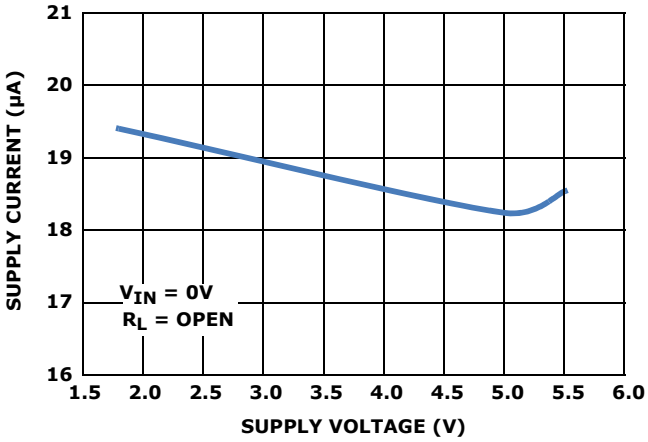


FIGURE 7. SUPPLY CURRENT vs SUPPLY VOLTAGE

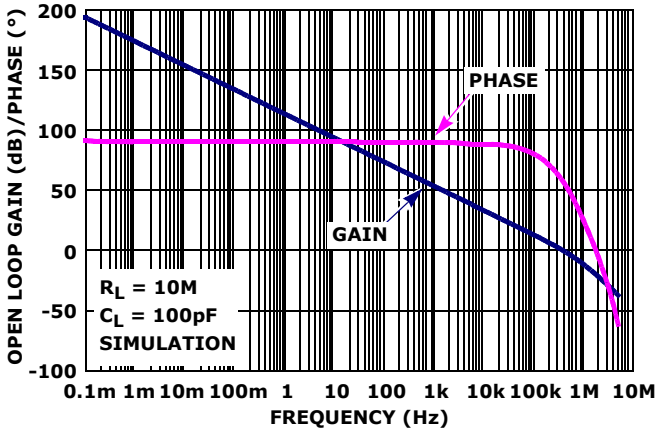


FIGURE 8. FREQUENCY RESPONSE vs OPEN LOOP GAIN, R_L = 10MΩ

Typical Performance Curves

V+ = 5V, V- = 0V, V_{CM} = 2.5V, R_L = Open, T = +25°C, unless otherwise specified. (Continued)

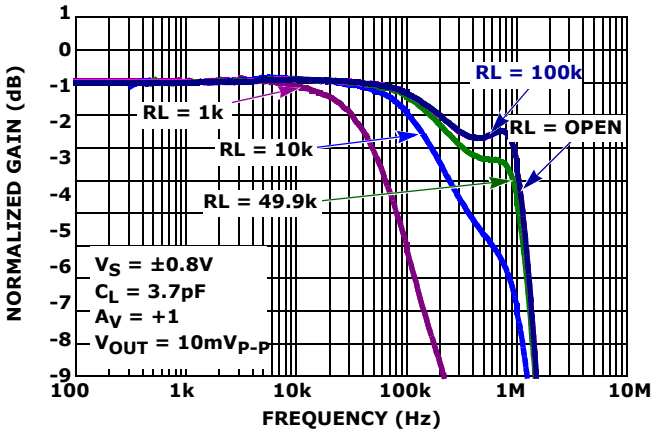


FIGURE 9. GAIN vs FREQUENCY vs R_L, V_S = ±0.8V

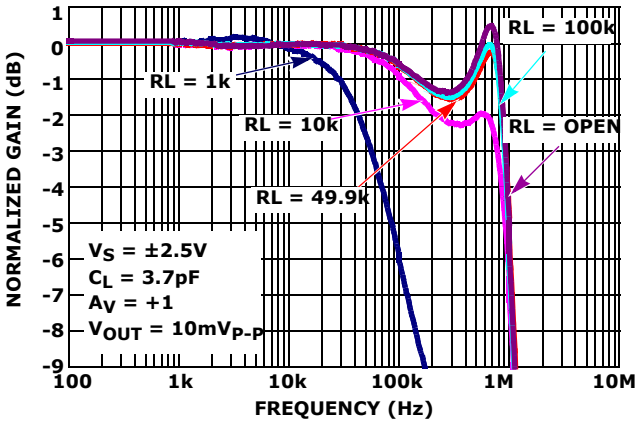


FIGURE 10. GAIN vs FREQUENCY vs R_L, V_S = ±2.5V

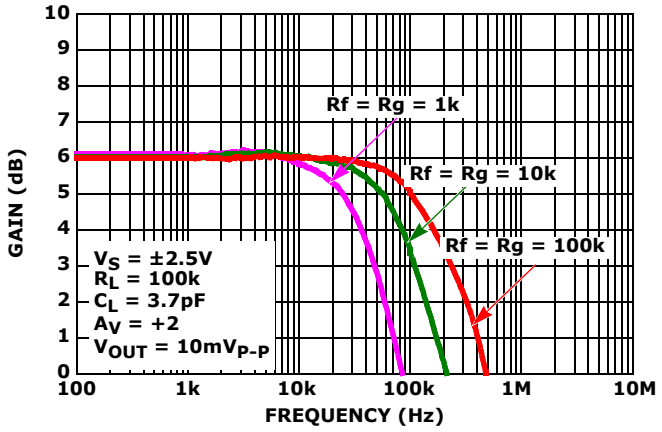


FIGURE 11. GAIN vs FREQUENCY vs FEEDBACK RESISTOR VALUES R_f/R_g

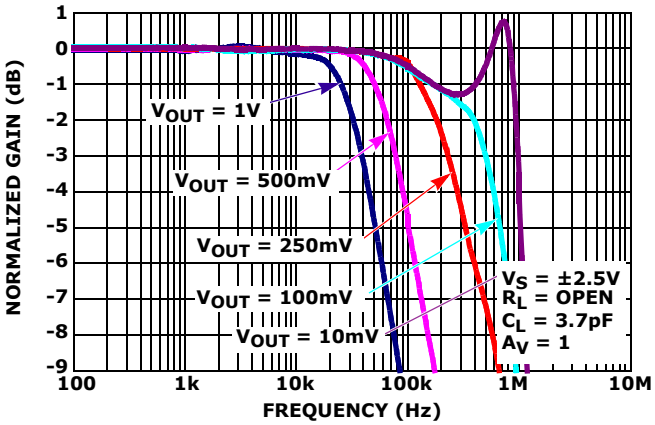


FIGURE 12. GAIN vs FREQUENCY vs V_{OUT}

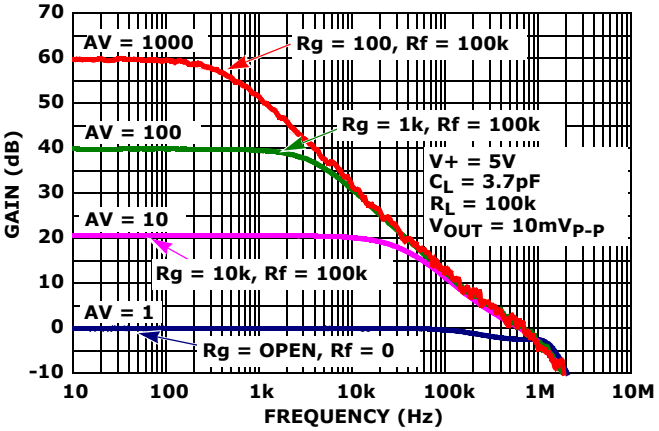


FIGURE 13. FREQUENCY RESPONSE vs CLOSED LOOP GAIN

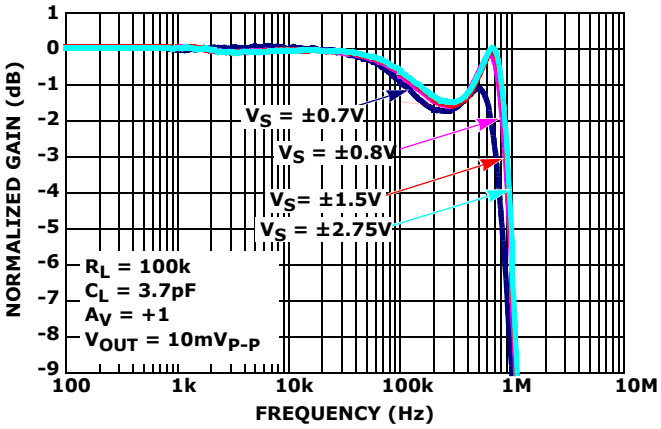


FIGURE 14. GAIN vs FREQUENCY vs SUPPLY VOLTAGE

Typical Performance Curves

V+ = 5V, V- = 0V, V_{CM} = 2.5V, R_L = Open, T = +25°C, unless otherwise specified. (Continued)

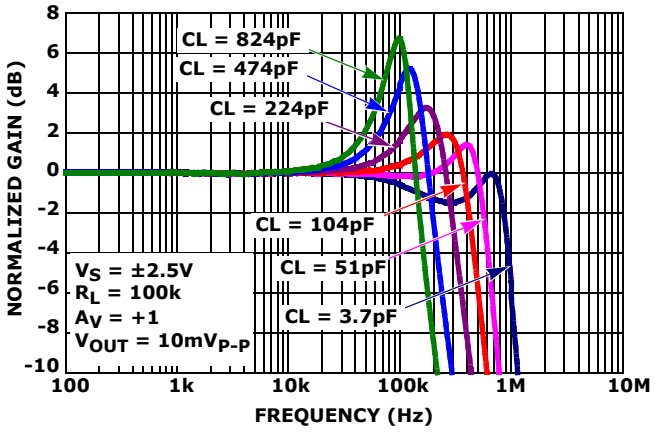


FIGURE 15. GAIN vs FREQUENCY vs C_L

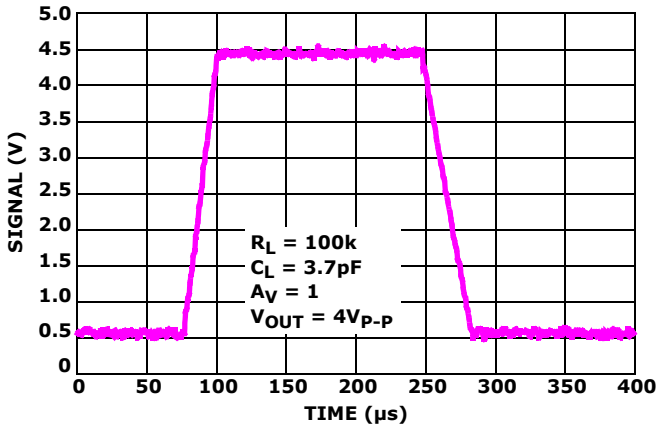


FIGURE 16. LARGE SIGNAL STEP RESPONSE (4V)

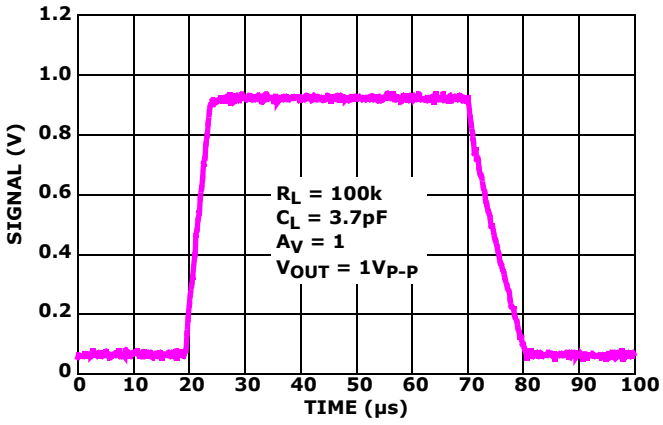


FIGURE 17. LARGE SIGNAL STEP RESPONSE (1V)

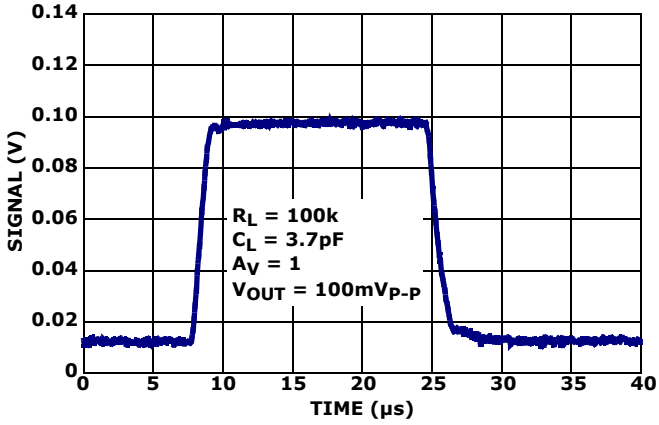


FIGURE 18. SMALL SIGNAL STEP RESPONSE (100mV)

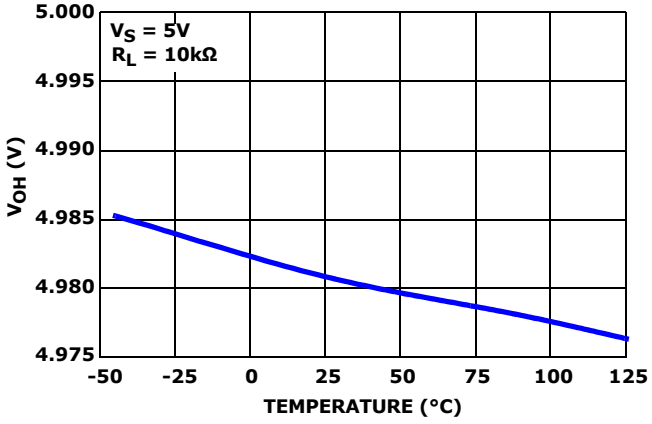


FIGURE 19. V_{OH} vs TEMPERATURE

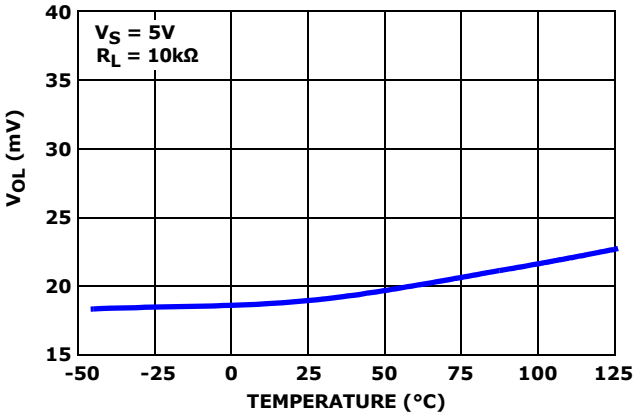


FIGURE 20. V_{OL} vs TEMPERATURE

Typical Performance Curves

V+ = 5V, V- = 0V, V_{CM} = 2.5V, R_L = Open, T = +25°C, unless otherwise specified. (Continued)

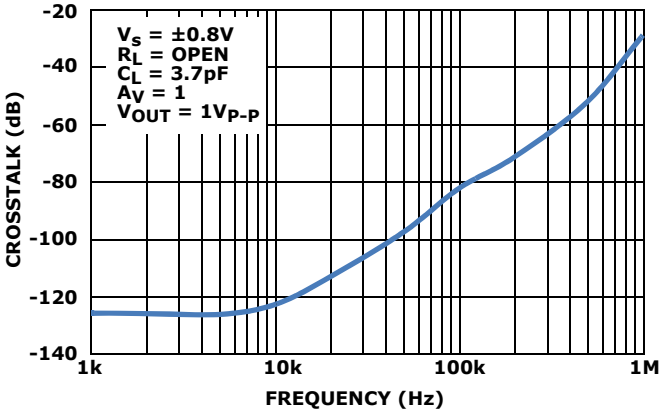


FIGURE 21. CROSSTALK vs FREQUENCY, V_S = ±0.8V

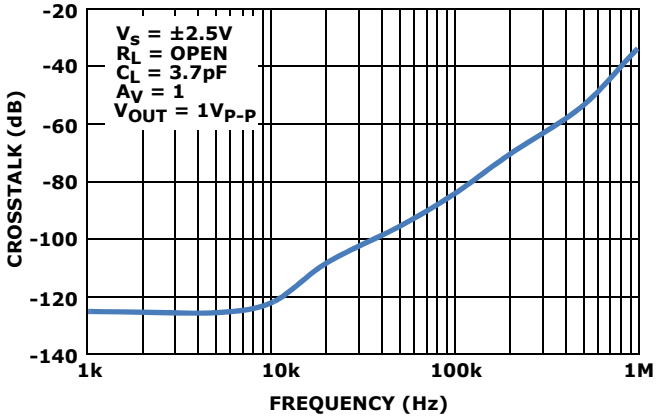


FIGURE 22. CROSSTALK vs FREQUENCY, V_S = ±2.5V

Applications Information

Functional Description

The ISL28130, ISL28230 and ISL28430 are low offset low drift operational amplifiers with a very high open loop gain (150dB) and rail-to-rail input/output. The ISL28130, ISL28230 and ISL28430 operate on a single supply range of 1.65V to 5.5V or dual supply range of ±0.825V to ±2.75V while consuming only 20µA of supply current per channel. The ISL28130, ISL28230 and ISL28430 has a 400kHz gain-bandwidth.

The high open loop gain, low offset voltage, high bandwidth and low 1/f noise make the ISL28130, ISL28230 and ISL28430 ideal for precision applications.

Rail-to-rail Input and Output (RRIO)

The RRIO CMOS amplifier uses parallel input PMOS and NMOS that enable the inputs to swing 100mV beyond either supply rail. The inverting and non-inverting inputs do not have back-to-back input clamp diodes and are capable of maintaining high input impedance at high differential input voltages. This is effective in eliminating output distortion caused by high slew-rate input signals.

The output stage uses common source connected PMOS and NMOS devices to achieve rail-to-rail output drive capability with 15mA current limit and the capability to swing to within 50mV of either rail while driving a 10kΩ load.

IN+ and IN- Protection

All input terminals have internal ESD protection diodes to both positive and negative supply rails, limiting the input voltage to within one diode beyond the supply rails. For applications where either input is expected to exceed the rails by 0.5V, an external series resistor must be used to ensure the input currents never exceed 20mA (see Figure 23).

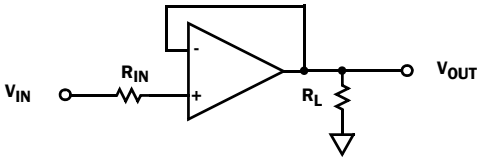


FIGURE 23. INPUT CURRENT LIMITING

Layout Guidelines for High Impedance Inputs

To achieve the maximum performance of the high input impedance and low offset voltage of the ISL28130, ISL28230 and ISL28430 amplifiers, care should be taken in the circuit board layout. The PC board surface must remain clean and free of moisture to avoid leakage currents between adjacent traces. Surface coating of the circuit board will reduce surface moisture and provide a humidity barrier, reducing parasitic resistance on the board.

High Gain, Precision DC-Coupled Amplifier

The circuit in Figure 24 implements a single-stage DC-coupled amplifier with an input DC sensitivity of under 100nV that is only possible using a low VOS amplifier with high open loop gain. High gain DC amplifiers operating from low voltage supplies are not practical using typical low offset precision op amps. For example, a typical precision amplifier in a gain of 10kV/V with a ±100µV V_{OS} and offset drift 0.5µV/°C of a low offset op amp would produce a DC error of >1V with an additional 5mV/°C of temperature dependent error making it difficult to resolve DC input voltage changes in the mV range.

The ±40µV max V_{OS} and 150nV/°C of temperature drift of the ISL28130, ISL28230, ISL28430 produces a temperature stable maximum DC output error of only ±400mV with a maximum output temperature drift of 1.5mV/°C. The additional benefit of a very low 1/f noise corner frequency and some feedback filtering enables DC voltages and voltage fluctuations well below 10µV to be easily detected with a simple single stage amplifier.

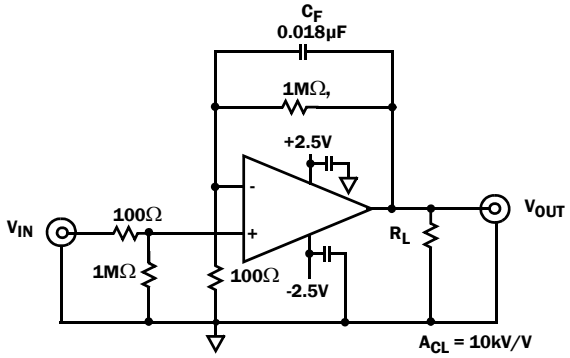


FIGURE 24. HIGH GAIN, PRECISION DC-COUPLED AMPLIFIER

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
12/7/10	FN7623.1	Corrected Thermals for DFN package in “Tja from 125 to 53, “Tjc from 90 to 12”
12/3/10		Removed Part Markings from Full temp grade parts and changed to TBD until availability is validated.
12/2/10		–Updated copyright to legal's suggested verbiage on page 1. -Updated front page text to add DFN packaging and extended temp range -40°C to +125°C -Removed previous Ib vs Temp plot and added new -40°C to +125°C Ib vs Temp plot on front page. -Updated ordering information table by adding a full temp range option to all parts and temp range column. Also added in DFN part to ordering table. All full temp parts are stamped Coming Soon. Parts ISL28130CHZ-T7, ISL28130CHZ-T7A and ISL28130CEZ-T7, ISL28130CEZ-T7A shown they are Tape and reel only parts. -Added in DFN package to Pin Configurations table. -Added in -40°C to +125°C temp range under Operating Conditions page 5. -Added the testing standards performance information to the ESD ratings in Abs Max Table -Added new Input Bias Current Ib spec of 700pA MIN/MAX in Electrical Spec table for -40°C to +125°C temp range -Revised Note 9 for Electrical Spec table as: "Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design." -Updated all curves in the datasheet with 0°C to +70°C temp range to -40°C to +125°C temp range. -Added DFN package L8.3x3J outline drawing to the end of datasheet.
10/19/10		On page 6 changed “Supply Current, Per Amplifier” from a typical of 18µA to 20µA to comply with front page.
8/17/10	FN7623.0	Initial Release

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

*For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL28130, ISL28230 , ISL28430.

To report errors or suggestions for this datasheet, please go to www.intersil.com/askourstaff

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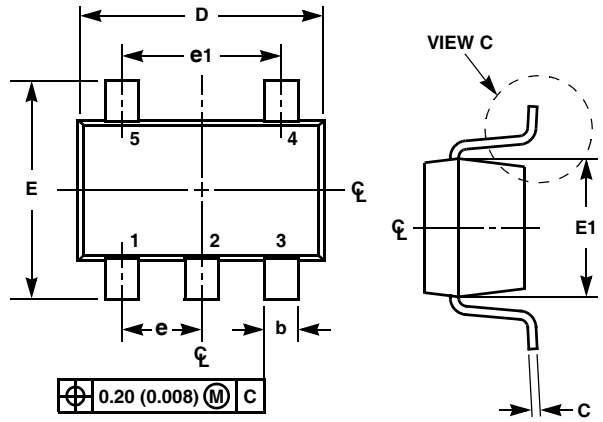
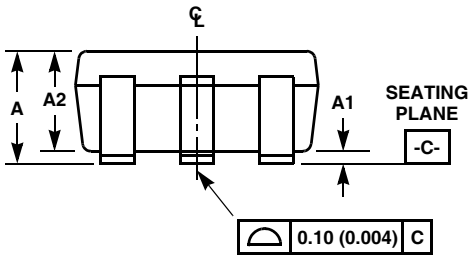
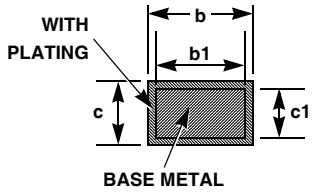
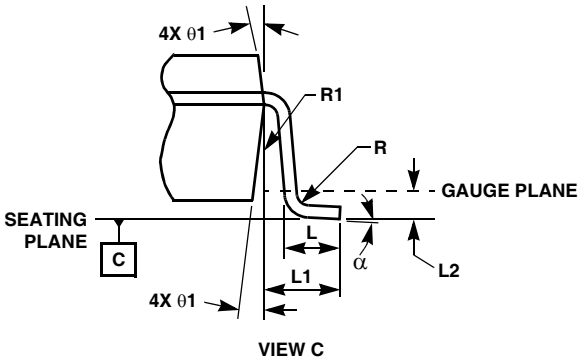
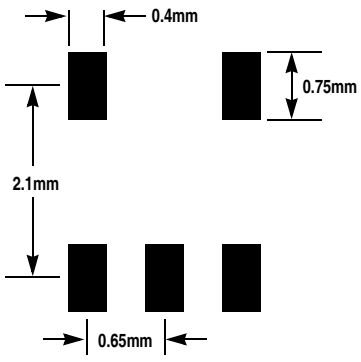
Small Outline Transistor Plastic Packages (SC70-5)











TYPICAL RECOMMENDED LAND PATTERN

P5.049

5 LEAD SMALL OUTLINE TRANSISTOR PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.031	0.043	0.80	1.10	-
A1	0.000	0.004	0.00	0.10	-
A2	0.031	0.039	0.80	1.00	-
b	0.006	0.012	0.15	0.30	-
b1	0.006	0.010	0.15	0.25	
c	0.003	0.009	0.08	0.22	6
c1	0.003	0.009	0.08	0.20	6
D	0.073	0.085	1.85	2.15	3
E	0.071	0.094	1.80	2.40	-
E1	0.045	0.053	1.15	1.35	3
e	0.0256 Ref		0.65 Ref		-
e1	0.0512 Ref		1.30 Ref		-
L	0.010	0.018	0.26	0.46	4
L1	0.017 Ref.		0.420 Ref.		-
L2	0.006 BSC		0.15 BSC		
α	0^o	8^o	0^o	8^o	-
N	5		5		5
R	0.004	-	0.10	-	
R1	0.004	0.010	0.15	0.25	

Rev. 3 7/07

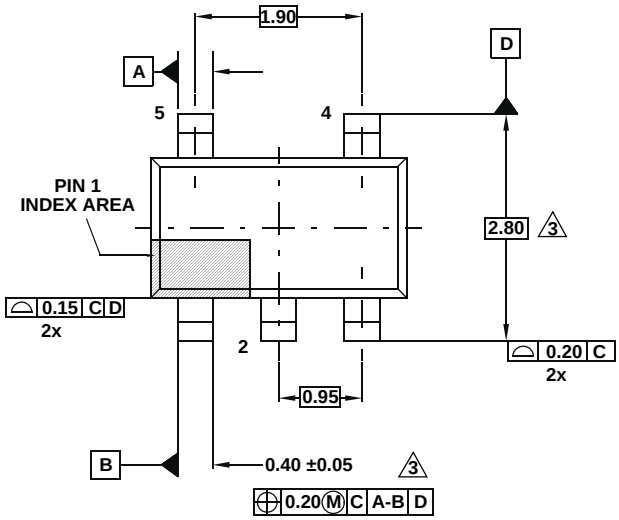
NOTES:

1. Dimensioning and tolerances per ASME Y14.5M-1994.
2. Package conforms to EIAJ SC70 and JEDEC MO-203AA.
3. Dimensions D and E1 are exclusive of mold flash, protrusions, or gate burrs.
4. Footlength L measured at reference to gauge plane.
5. “N” is the number of terminal positions.
6. These Dimensions apply to the flat section of the lead between 0.08mm and 0.15mm from the lead tip.
7. Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only.

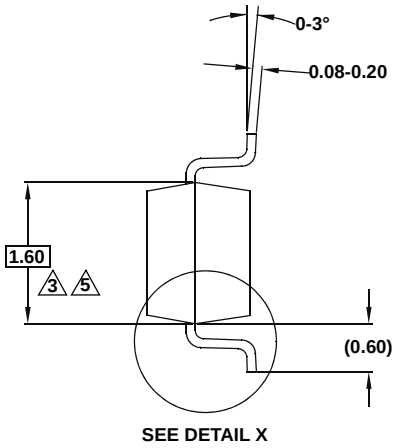
Package Outline Drawing

P5.064A

5 LEAD SMALL OUTLINE TRANSISTOR PLASTIC PACKAGE
Rev 0, 2/10

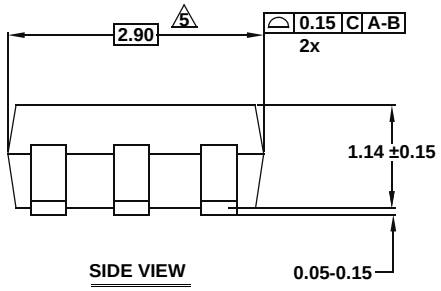


TOP VIEW

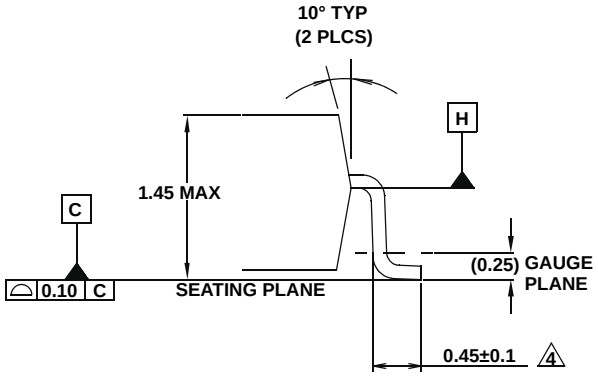


SEE DETAIL X

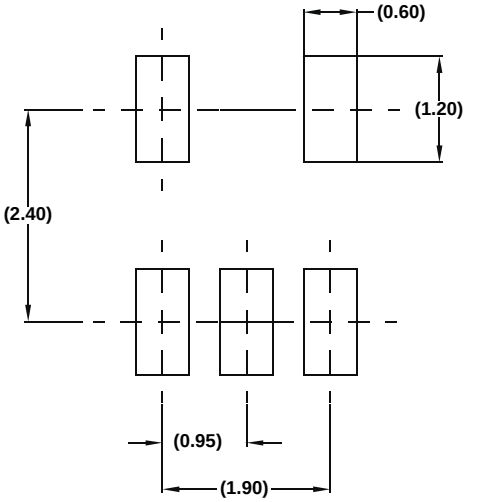
END VIEW



SIDE VIEW



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

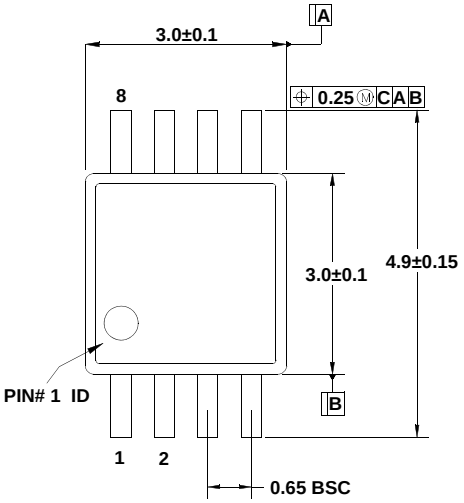
1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
3. Dimension is exclusive of mold flash, protrusions or gate burrs.
4. Foot length is measured at reference to guage plane.
5. This dimension is measured at Datum “H”.
6. Package conforms to JEDEC MO-178AA.

Package Outline Drawing

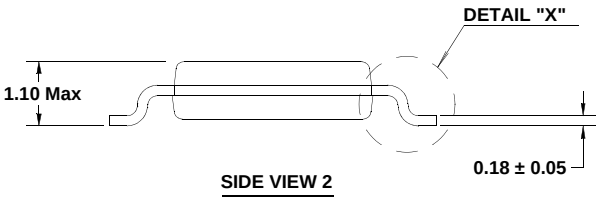
M8.118A

8 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE (MSOP)

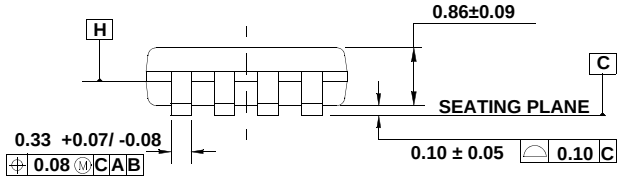
Rev 0, 9/09



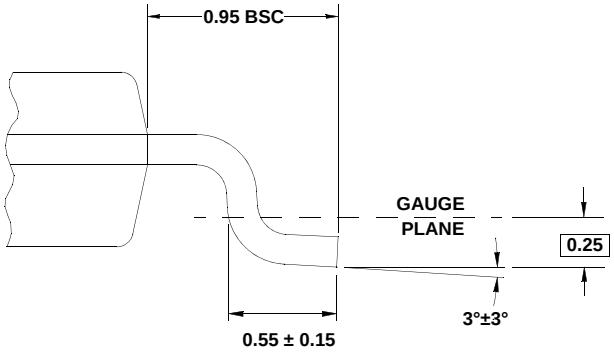
TOP VIEW



SIDE VIEW 2



SIDE VIEW 1



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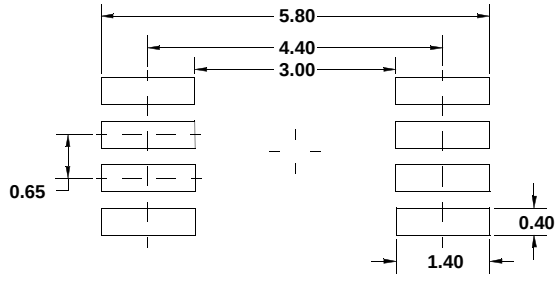
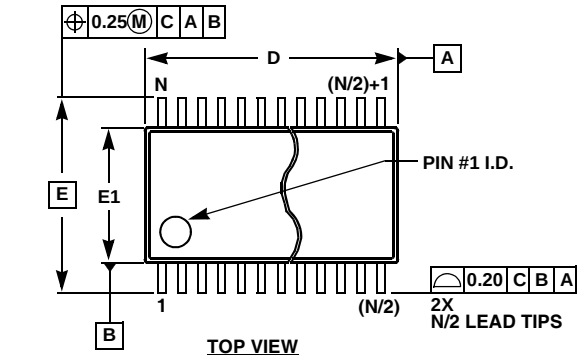


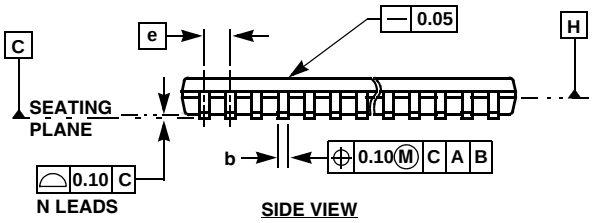
TYPICAL RECOMMENDED LAND PATTERN

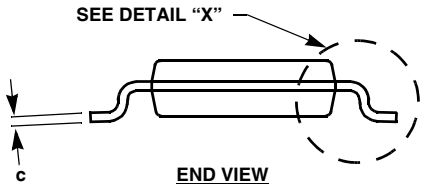
NOTES:

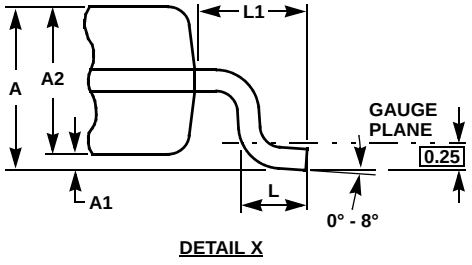
1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-AA and AMSE Y14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.25mm max per side are not included.
5. Dimensions “D” and “E1” are measured at Datum Plane “H”.
6. This replaces existing drawing # MDP0043 MSOP 8L.

Thin Shrink Small Outline Package Family (TSSOP)









MDP0044

THIN SHRINK SMALL OUTLINE PACKAGE FAMILY

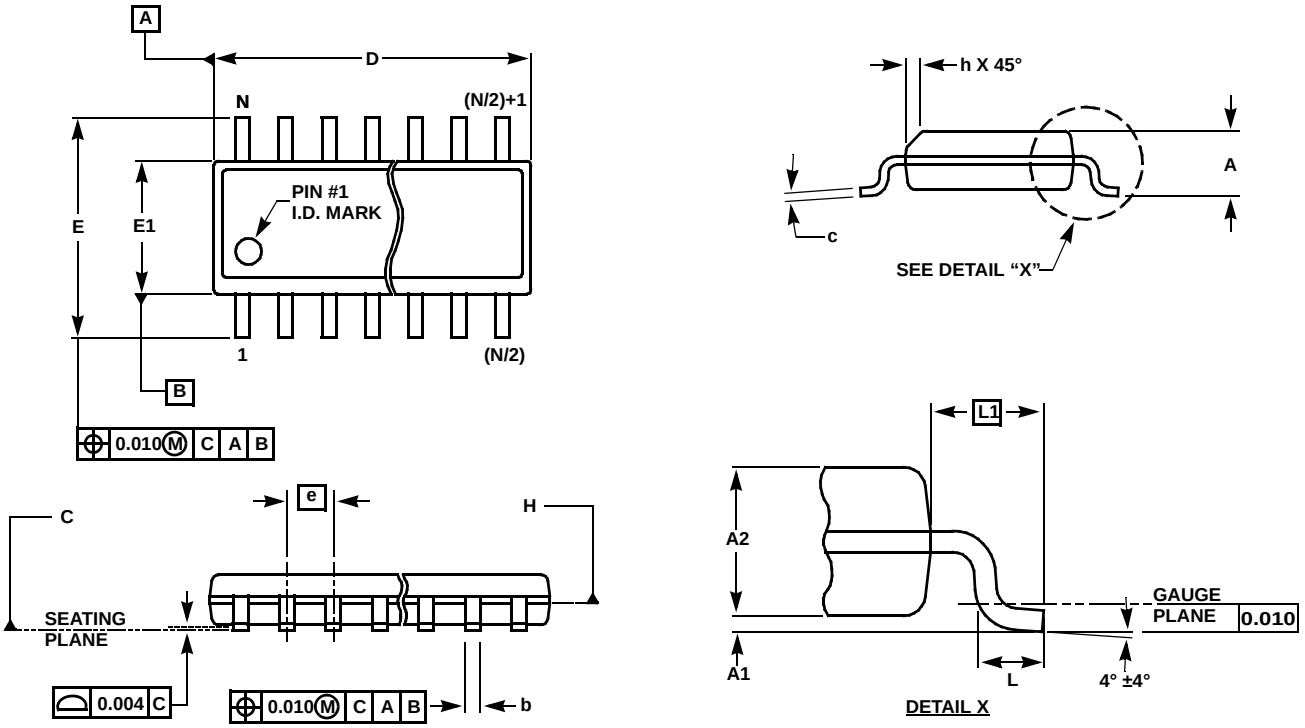
SYMBOL	MILLIMETERS					TOLERANCE
	14 LD	16 LD	20 LD	24 LD	28 LD	
A	1.20	1.20	1.20	1.20	1.20	Max
A1	0.10	0.10	0.10	0.10	0.10	±0.05
A2	0.90	0.90	0.90	0.90	0.90	±0.05
b	0.25	0.25	0.25	0.25	0.25	+0.05/-0.06
c	0.15	0.15	0.15	0.15	0.15	+0.05/-0.06
D	5.00	5.00	6.50	7.80	9.70	±0.10
E	6.40	6.40	6.40	6.40	6.40	Basic
E1	4.40	4.40	4.40	4.40	4.40	±0.10
e	0.65	0.65	0.65	0.65	0.65	Basic
L	0.60	0.60	0.60	0.60	0.60	±0.15
L1	1.00	1.00	1.00	1.00	1.00	Reference

Rev. F 2/07

NOTES:

1. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
2. Dimension “E1” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm per side.
3. Dimensions “D” and “E1” are measured at dAtum Plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.

Small Outline Package Family (SO)



MDP0027

SMALL OUTLINE PACKAGE FAMILY (SO)

SYMBOL	INCHES							TOLERANCE	NOTES
	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)		
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX	-
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	±0.003	-
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	±0.002	-
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	±0.003	-
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	±0.001	-
D	0.193	0.341	0.390	0.406	0.504	0.606	0.704	±0.004	1, 3
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	±0.008	-
E1	0.154	0.154	0.154	0.295	0.295	0.295	0.295	±0.004	2, 3
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic	-
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	±0.009	-
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic	-
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference	-
N	8	14	16	16	20	24	28	Reference	-

Rev. M 2/07

NOTES:

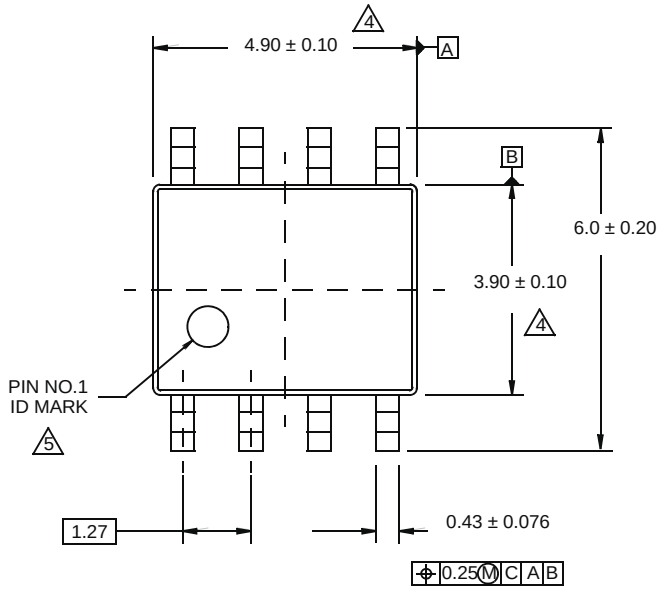
1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994

Package Outline Drawing

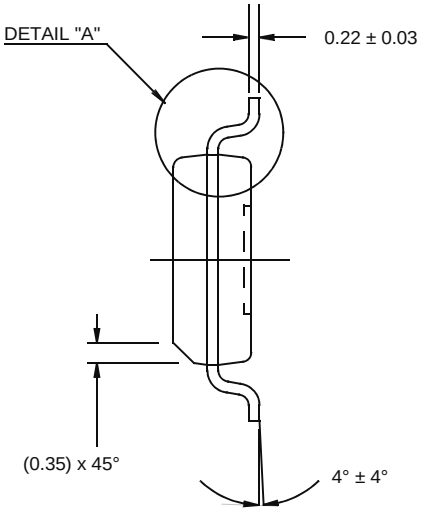
M8.15E

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

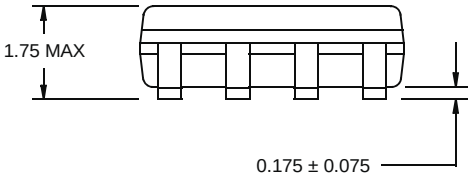
Rev 0, 08/09



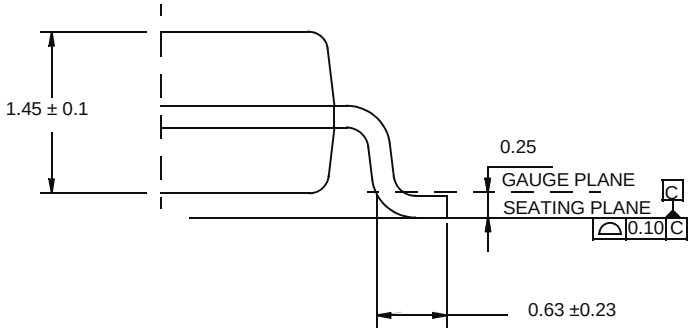
TOP VIEW



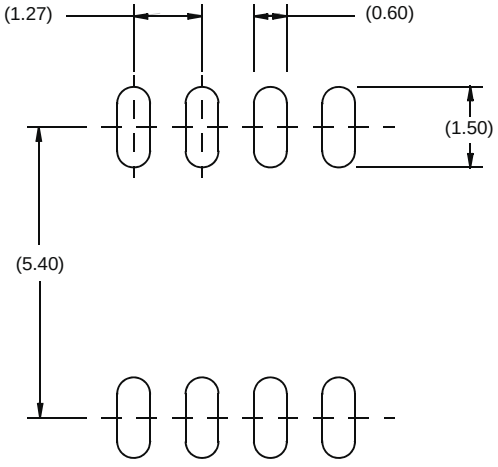
SIDE VIEW “B”



SIDE VIEW “A”



DETAIL "A"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

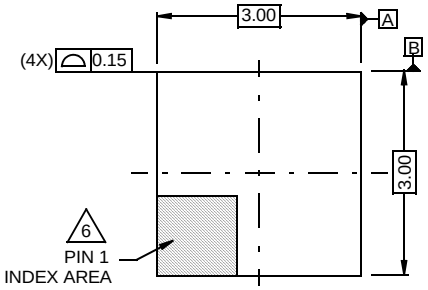
1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension does not include interlead flash or protrusions.
   Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 identifier may be either a mold or mark feature.
6. Reference to JEDEC MS-012.

Package Outline Drawing

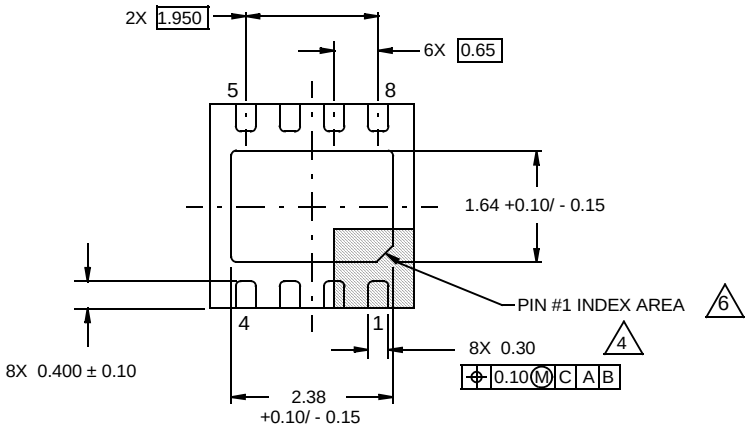
L8.3x3J

8 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE

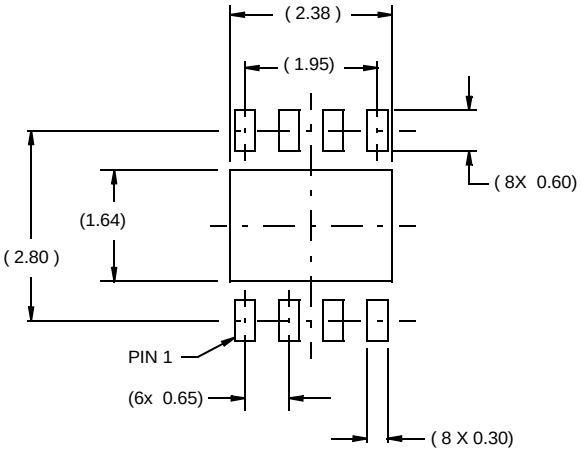
Rev 0 9/09



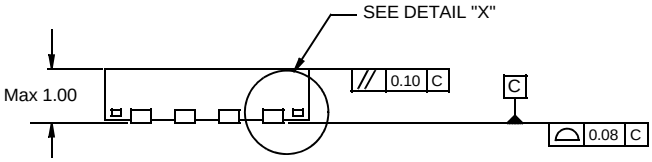
TOP VIEW



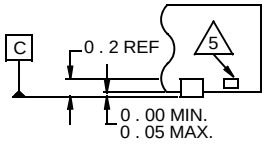
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.