AMMP-6421

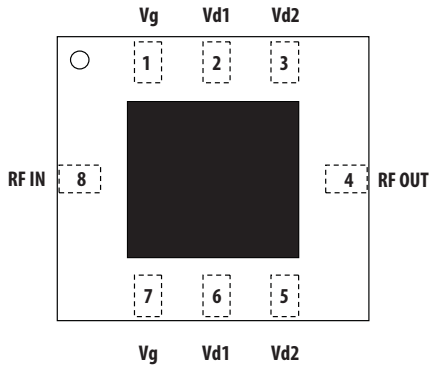
13-16 GHz 1W Power Amplifier in SMT Package

Data Sheet

Description

The AMMP-6421 MMIC is a 1W power amplifier in a surface mount package designed for use in transmitters that operate at frequencies between 13GHz and 16GHz. Between 13GHz and 16GHz, it provides 29 dBm of output power (P-1dB) and 26dB of small-signal gain. This power amplifier is optimized for linear operation with an output third order intercept point (OIP3) of +36dBm. The AMMC-6421 is manufactured with Avago's unique enhancement mode 0.25µm GaAs PHEMT process that eliminates the need for negative DC biasing.

Package Diagram



Features

- 5x5mm SMT package
- One-watt saturated output power
- 50 Ω match on input and output

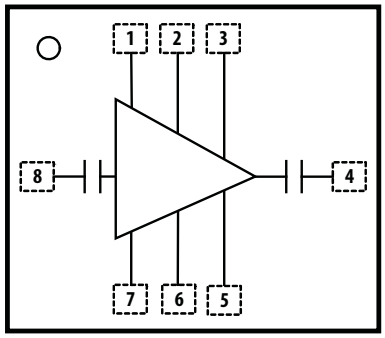
Typical Specifications (Vd=5V, Idsq=0.6A)

- Frequency range 13 to 16 GHz
- Small signal Gain of 26dB
- Output power @P-1 of 29dBm (Typ.)
- Input/Output return-loss of -6dB/-8dB

Applications

- Microwave Radio systems
- Satellite VSAT, Up/Down Link
- LMDS & Pt-Pt mmW Long Haul
- Broadband Wireless Access (including 802.16 and 802.20 WiMax)
- WLL and MMDS loops

Functional Block Diagram



Pin	Function
1	Vg
2	Vd1
3	Vd2
4	RF_OUT
5	Vd2
6	Vd1
7	Vg
8	RF_IN

RoHS-Exemption

Please refer to hazardous substances table on page 10.

Attention: Observe precautions for handling electrostatic sensitive devices.
ESD Machine Model (Class A) = 50 V
ESD Human Body Model (Class 0) = 200 V
Refer to Avago Application Note A004R: Electrostatic Discharge, Damage and Control.

Note: MSL Rating = Level 2A

Electrical Specifications

1. Small/Large -signal data measured in a fully de-embedded test fixture form TA = 25°C.
2. Pre-assembly into package performance verified 100% on wafer.
3. This final package part performance is verified by a functional test correlated to actual performance at one or more frequencies.
4. Specifications are derived from measurements in a 50 Ω test environment. Aspects of the amplifier performance may be improved over a more narrow bandwidth by application of additional conjugate, linearity, or low noise (Γopt) matching.
5. The Gain at P1dB tested at 13, 14.5 and 16 GHz guaranteed with measurement accuracy +/-1dB for Gain, +/-1.2dB for P1dB at 13 GHz and +/-1.5dB for P1dB at 14.5 GHz and 16 GHz.
6. NF is measure on-wafer. Additional bond wires (-0.2nH) at Input could improve NF at some frequencies.

Table 1. RF Electrical Characteristics

TA=25°C, Vd=5.0V, Idq=0.6mA, Vg= +0.5V, Zo=50 Ω

	13GHz			14.5GHz			16GHz				
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Comment**
Small Signal Gain, Gain	24	26	30	22	26	28	24	26	30	dB	
Output Power at 1dBGain Compression, P1dB	27	29		26	29		25	29		dBm	
Output Power at 3dBGain Compression, P3dB		30			30			30		dBm	
Output Third Order Intercept Point, OIP3; Point Δf= 2 MHz; Pout = +10 dBm, SCL		36			36			36		dBm	
Min Reverse Isolation, Isolation		45			45			45		dB	
Input Return Loss, Rlin		6			6			6		dB	
Output Return Loss, RLout		8			8			8		dB	

Table 2. Recommended Operating Range

1. Ambient operational temperature TA = 25°C unless otherwise noted.
2. Channel-to-backside Thermal Resistance (Tchannel (Tc) = 34°C) as measured using infrared microscopy. Thermal Resistance at backside temperature (Tb) = 25°C calculated from measured data.

Description	**Min.**	**Typical**	**Max.**	**Unit**	**Comments**
Drain Supply Current, Id		600		mA	Vd = 5V, Vg set for typical Id(q) Typical
Gate Supply Voltage, Vg		0.5		V	Id(q) = 600mA

Table 3. Thermal Properties

Parameter	Test Conditions	Value
Thermal Resistance (channel to backside), θjc	Ambient operational temperature TA = 25°C	θjc = 17 °C/W
Channel Temperature, Tch		Tch = 136 °C

Note:

1. Assume SnPb soldering to an evaluation RF board at 85°C base plate temperatures. Worst case for the channel temperature is under the quiescent operation. At saturated output power, DC power consumption rises to 5 W with 1.43 W RF power delivered to load. Power dissipation is 3.57 W and the temperature rise in the channel is 33.6°C. In this condition, the base plate temperature must be remained below 94.3°C to maintain maximum operating channel temperature below 155°C.

Absolute Minimum and Maximum Ratings

Table 4. Minimum and Maximum Ratings

Description	Min.	Max.	Unit	Comments
Drain Supply Voltage, Vd		6	V	
Gate Supply Voltage, Vg		1	V	
Power Dissipation, Pd [2,3]		8	W	
RF CW Input Power, Pin [2]		23	dBm	CW
Channel Temperature, Tch, max [4,5]		+150	°C	
Storage Case Temperature, Tstg	-65	+150	°C	
Maximum Assembly Temperature, Tmax		260	°C	30 second maximum

Notes:

1. Operation in excess of any one of these conditions may result in permanent damage to this device.
2. Combinations of supply voltage, drain current, input power, and output power shall not exceed PD.
3. When operate at this condition with a base plate temperature of 85°C, the median time to failure (MTTF) is significantly reduced.
4. These ratings apply to each individual FET
5. The operating channel temperature will directly affect the device MTTF. For maximum life, it is recommended that junction temperatures be maintained at the lowest possible levels.

AMMP-6421 Typical Performances

(Data obtained from 3.5-mm connector based test fixture, and this data is including connecter loss, and board loss.)

(T_A = 25°C, V_d = 5 V, $I_{d(q)}$ = 600 mA, Z_{in} = Z_{out} = 50 Ω)

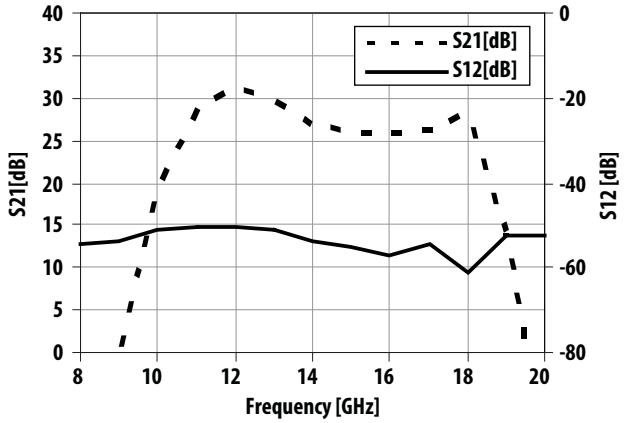


Figure 1. Typical Gain and Reverse Isolation

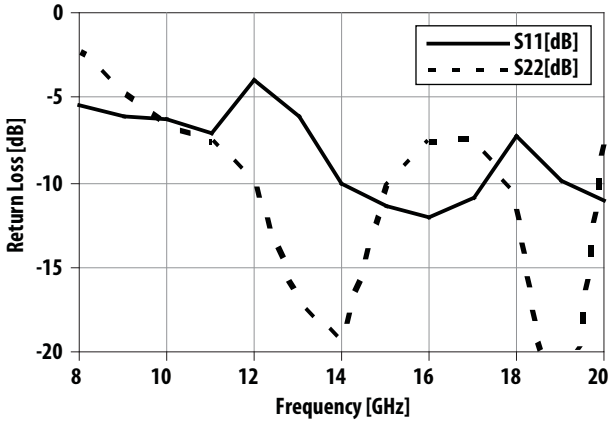


Figure 2. Typical Return Loss (Input and Output)

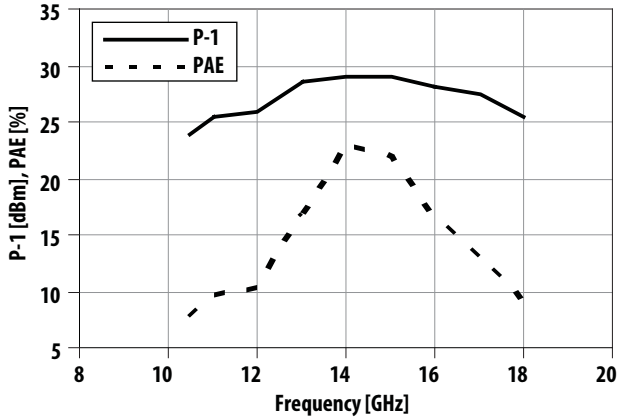


Figure 3. Typical Output Power (@P-1) and PAE and Frequency

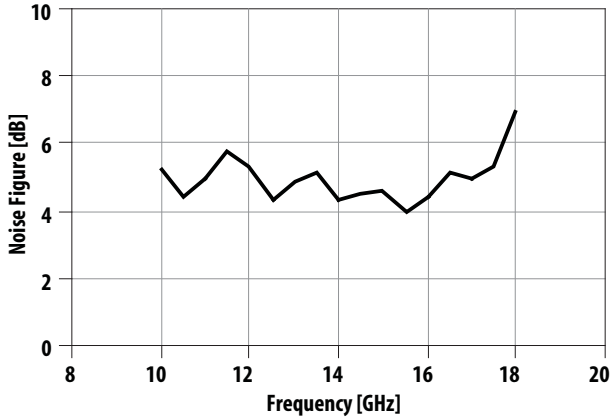


Figure 4. Typical Noise Figure

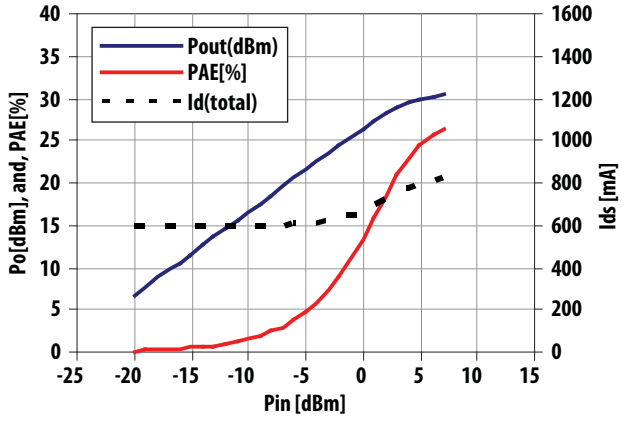


Figure 5. Typical Output Power, PAE, and Total Drain Current versus Input Power at 14GHz

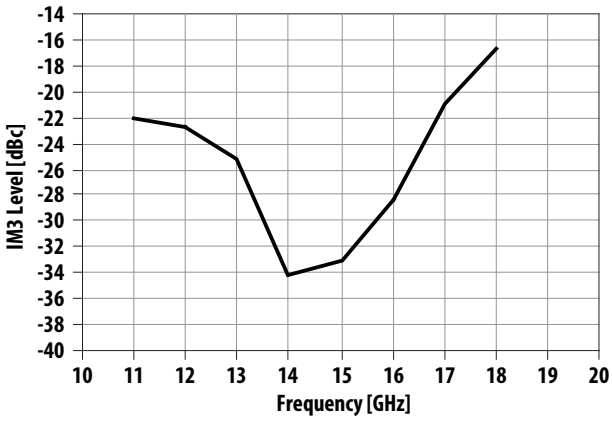


Figure 6. Typical IM3 level vs. Frequency at +20dBm output single carrier level (SCL)

Typical Performance (continued)

(Data obtained from 3.5-mm connector based test fixture, and this data is including connecter loss, and board loss.)

(T_A = 25°C, V_d = 5 V, $I_{d(q)}$ = 600 mA, Z_{in} = Z_{out} = 50 Ω)

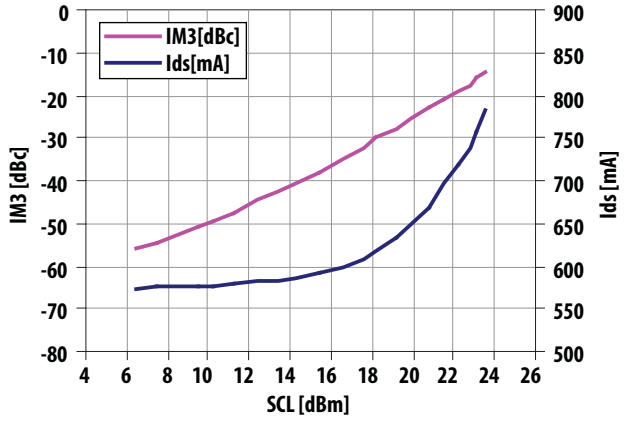


Figure 7. Typical IM3 level and Ids vs. single carrier output level at 13GHz

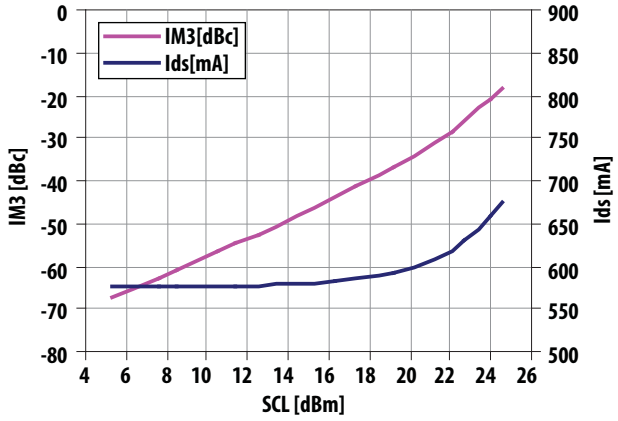


Figure 8. Typical IM3 level and Ids vs. single carrier output level at 14GHz

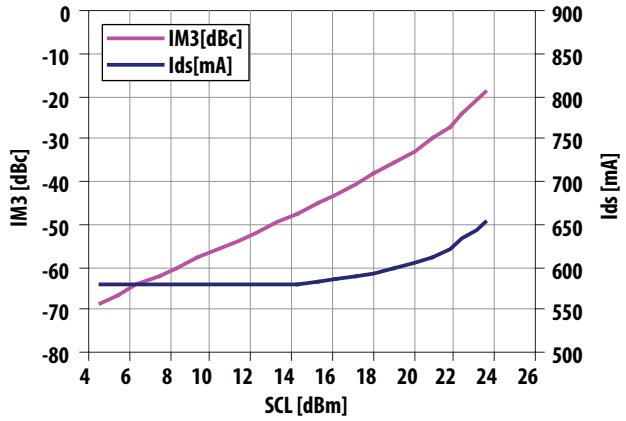


Figure 9. Typical IM3 level and Ids vs. single carrier output level at 15GHz

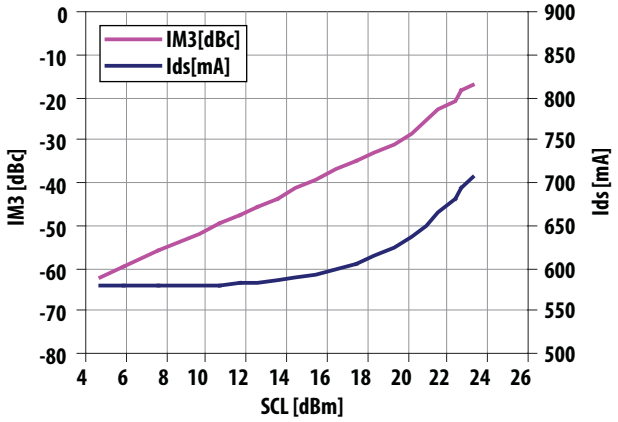


Figure 10. Typical IM3 level and Ids vs. single carrier output level at 16GHz

AMMP-6421 Typical over temperature dependencies

(T_A = 25°C, V_d =5 V, $I_{d(q)}$ = 600 mA, Z_{in} = Z_{out} = 50 Ω)

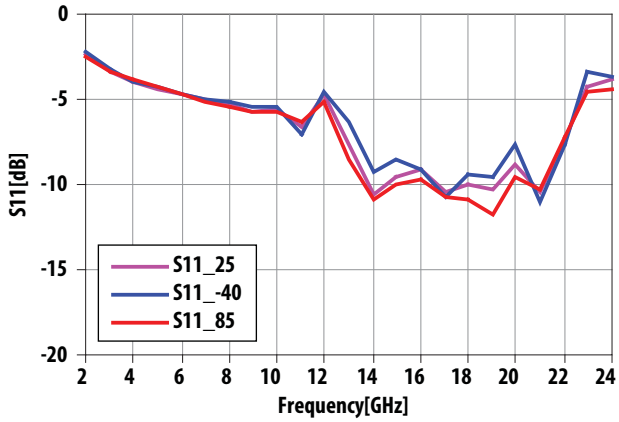


Figure 11. Typical S11 over temperature

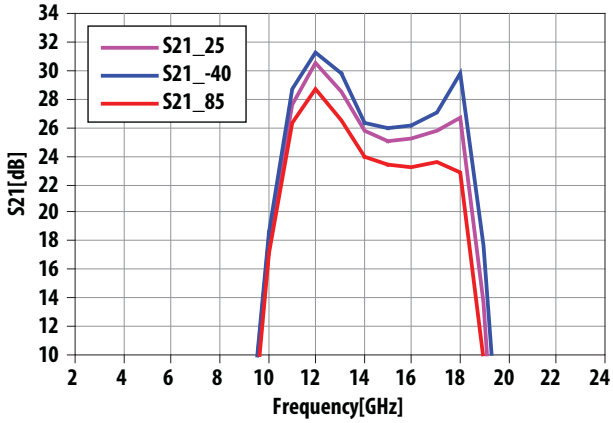


Figure 12. Typical Gain over temperature

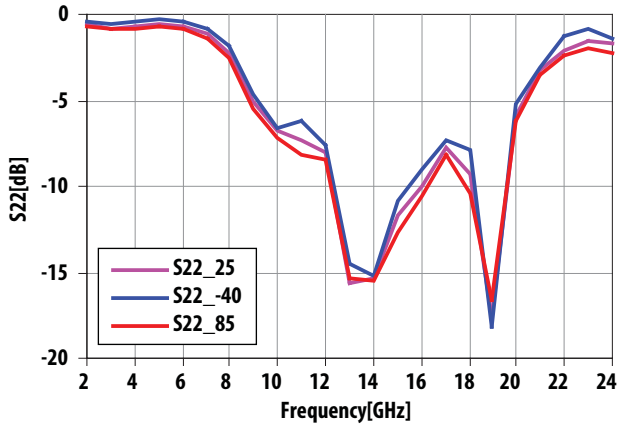


Figure 13. Typical S22 over temperature

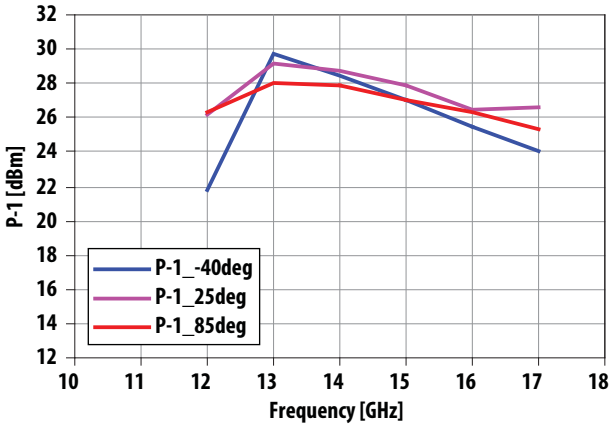


Figure 14. Typical P1 over temperature

Typical Scattering Parameters [1]

(T_A = 25°C, V_d =5 V, I_D = 600 mA, Z_{in} = Z_{out} = 50 Ω)

Freq	S11			S21			S12			S22		
[GHz]	dB	Mag	Phase	dB	Mag	Phase	dB	Mag	Phase	dB	Mag	Phase
1	3.22	1.45	-20.80	-20.82	0.09	-5.05	-35.45	1.69E-02	-113.80	3.60	1.51	158.04
2	0.82	1.10	-15.77	-22.80	0.07	-4.50	-37.48	1.34E-02	-113.80	1.56	1.20	149.01
3	-2.32	0.77	-6.21	-25.37	0.05	-3.56	-40.14	9.84E-03	-113.79	-0.64	0.93	134.19
4	-6.32	0.48	15.98	-29.01	0.04	-1.66	-43.99	6.32E-03	-113.79	-2.32	0.77	110.63
5	-8.24	0.39	64.29	-35.36	0.02	4.37	-51.09	2.79E-03	-113.77	-2.22	0.77	81.97
6	-4.75	0.58	102.83	-48.21	0.00	110.97	-62.67	7.35E-04	66.08	-0.44	0.95	59.24
7	-5.12	0.55	104.57	-45.45	0.01	84.47	-47.30	4.32E-03	-48.35	-0.32	0.96	40.55
8	-6.93	0.45	92.88	-19.99	0.10	111.07	-50.95	2.83E-03	175.39	-1.81	0.81	12.86
9	-7.57	0.42	69.98	2.91	1.40	16.33	-51.57	2.64E-03	147.20	-5.10	0.56	-24.21
10	-7.03	0.45	42.82	20.60	10.71	-119.19	-54.32	1.92E-03	146.44	-6.63	0.47	-33.47
11	-5.63	0.52	16.27	29.64	30.33	70.21	-56.65	1.47E-03	134.01	-5.09	0.56	-70.24
12	-5.04	0.56	5.80	30.63	34.01	-75.22	-56.90	1.43E-03	166.70	-8.25	0.39	-77.87
13	-4.07	0.63	-26.92	30.60	33.87	146.03	-57.11	1.39E-03	114.49	-8.88	0.36	-86.72
14	-8.53	0.37	-26.01	26.99	22.35	36.29	-61.39	8.52E-04	-39.90	-23.11	0.07	-40.24
15	-9.63	0.33	-32.05	25.98	19.91	-61.13	-56.95	1.42E-03	-163.33	-10.16	0.31	5.61
16	-8.89	0.36	-56.38	26.58	21.33	-172.51	-50.29	3.06E-03	-170.11	-6.59	0.47	-16.17
17	-10.61	0.29	-91.07	26.33	20.74	70.84	-70.34	3.04E-04	168.60	-8.98	0.36	-56.63
18	-5.44	0.53	-95.08	29.14	28.64	-92.98	-59.79	1.03E-03	-82.15	-12.98	0.22	-101.09
19	-6.01	0.50	-140.38	11.72	3.85	62.18	-47.74	4.10E-03	-43.64	-15.86	0.16	89.98
20	-9.54	0.33	169.29	-12.96	0.22	-10.58	-39.20	1.10E-02	-120.94	-5.92	0.51	-18.40
21	-15.70	0.16	64.10	-21.08	0.09	-129.11	-40.97	8.94E-03	-167.68	-2.35	0.76	-65.21
22	-5.81	0.51	27.18	-39.66	1.04E-02	150.93	-43.70	6.53E-03	159.88	-1.14	0.88	-90.95
23	-2.67	0.73	-6.68	-39.83	1.02E-02	104.74	-47.51	4.21E-03	105.92	-1.22	0.87	-107.37
24	-3.07	0.70	-31.53	-43.85	6.42E-03	-11.62	-53.42	2.13E-03	17.26	-1.23	0.87	-117.13
25	-4.30	0.61	-56.50	-44.41	6.02E-03	-98.07	-51.89	2.54E-03	-63.98	-1.12	0.88	-132.87
26	-5.42	0.54	-89.90	-50.60	2.95E-03	43.80	-46.85	4.55E-03	-67.11	-0.55	0.94	-148.59
27	-4.92	0.57	-125.50	-40.26	9.70E-03	-129.43	-41.20	8.71E-03	-101.52	-0.60	0.93	-168.10
28	-4.52	0.59	-148.37	-35.86	1.61E-02	-138.94	-41.27	8.64E-03	-164.60	-0.86	0.91	176.85
29	-4.56	0.59	-156.26	-40.91	9.01E-03	172.66	-44.67	5.84E-03	159.25	-0.47	0.95	167.80
30	-4.57	0.59	-151.19	-64.26	6.12E-04	40.57	-53.94	2.01E-03	89.72	-0.32	0.96	163.09
31	-5.29	0.54	-144.53	-44.94	5.66E-03	-107.38	-55.80	1.62E-03	-161.00	-0.43	0.95	154.34

Note:
1. Reference planes for this data are at the package RF I/O edges.

Biasing and Operation

The recommended quiescent DC bias condition for optimum efficiency, performance and reliability is Vd=5 volts with Vg (+0.5V typ.) set to give Id(q)=600 mA. Minor improvements in performance are possible depending on the application. The drain bias voltage range is 3 to 5V and the quiescent drain current biasing range is 400mA to 650mA. A single DC gate supply connected to Vg will bias all the amplifier stages. Muting can be accomplished by setting Vg to zero.

A simplified schematic for the MMIC die in the package is shown in Figure 15. The MMIC die contains ESD and over voltage protection diodes for Vg, Vd1, and Vd2. ESD diodes protect all possible ESD or over voltage damages among Vg to ground, Vg to Vd1, Vg to Vd2, Vd1 to ground and Vd2 to ground. The typical forward current versus voltage for 11 diodes connected in series is shown in Figure 16. The RF input and output are DC blocked internally.

Under the recommended DC quiescent biasing condition at Vds=5V, Ids=600mA, Vgg=+0.5V, typical gate terminal current is approximately 0.02mA. If an active biasing technique is selected for the AMMP6421 MMIC PA DC biasing, the active biasing circuit must have more than 10-times higher internal current that the gate terminal current.

The AMMP6421 can be biased either single positive DC biasing or dual positive supply operation as shown in Figure 17(a) and (b).

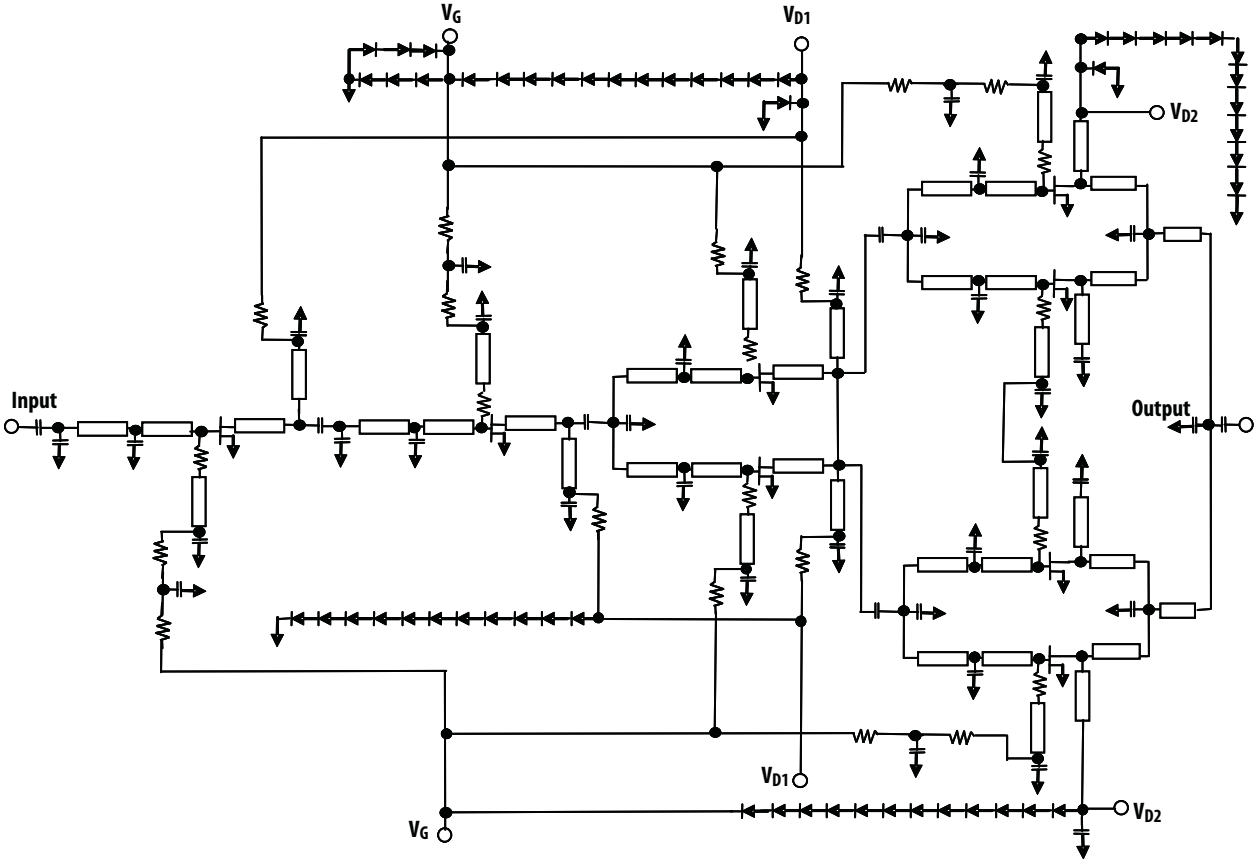


Figure 15. Simplified schematic for the MMIC die in the package

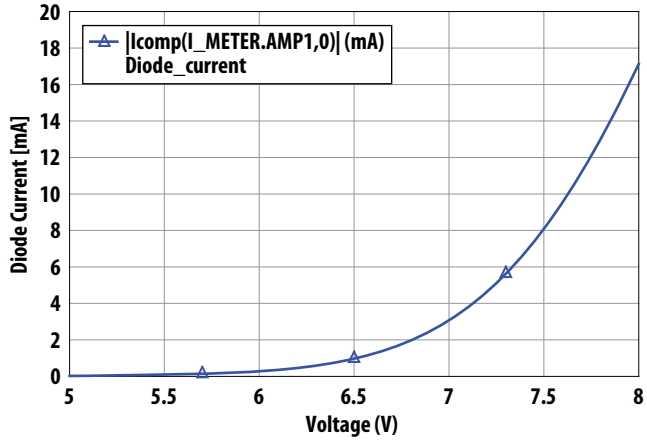
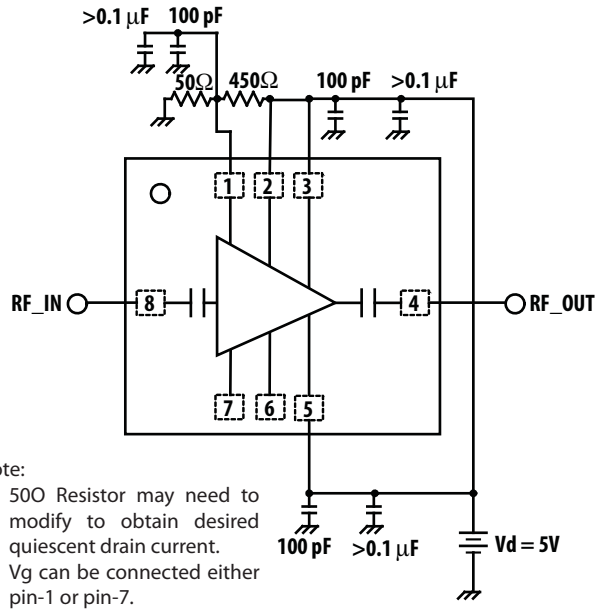
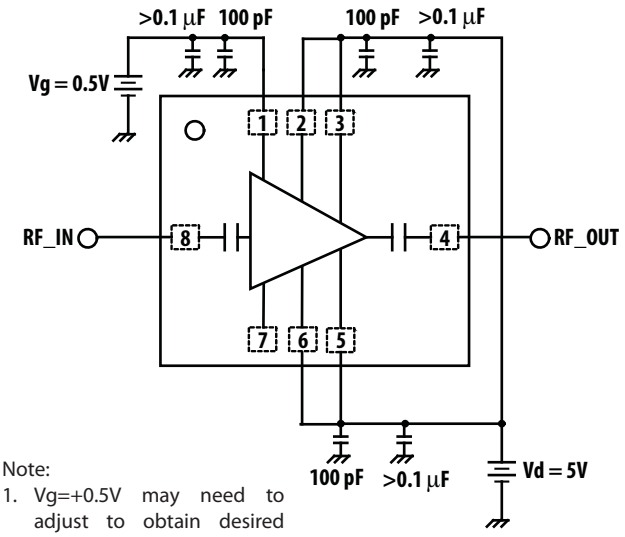


Figure 16. Typical ESD diode current versus diode voltage for 11-connected diodes in series



Note:
1. 50O Resistor may need to modify to obtain desired quiescent drain current.
2. Vg can be connected either pin-1 or pin-7.
3. Vd1 can be connected either pin-2 or pin-6.
4. Vd2 must be connected both sides (pin-3 and pin-5).

(a) Single positive bias operation



Note:
1. Vg=+0.5V may need to adjust to obtain desired quiescent drain current.
2. Vg can be connected to either pin-1 or pin-7.
3. Vd1 can be connected to either pin-2 or pin-6.
4. Vd2 must be connected to both sides (pin-3 and pin-5).

(b) Dual positive bias operation

Figure 17. AMMP-6421 Schematic and recommended assemble example

Package Dimension, PCB Layout and Tape and Reel information

Please refer to Avago Technologies Application Note 5521, AMxP-xxxx production Assembly Process (Land Pattern B).

AMMP-64xx Part Number Ordering Information

Part Number	Devices Per Container	Container
AMMP-6421-BLKG	10	Antistatic bag
AMMP-6421-TR1G	100	7″ Reel
AMMP-6421-TR2G	500	7″ Reel

Names and Contents of the Toxic and Hazardous Substances or Elements in the Products
产品中有毒有害物质或元素的名称及含量

Part Name 部件名称	Toxic and Hazardous Substances or Elements 有毒有害物质或元素					
	Lead (Pb) 铅 (Pb)	Mercury (Hg) 汞 （Hg ）	Cadmium (Cd) 镉 （Cd ）	Hexavalent (Cr(VI)) 六价铬（Cr(VI) ）	Polybrominated biphenyl (PBB) 多溴联苯（PBB ）	Polybrominated diphenylether (PBDE) 多溴二苯醚（PBDE ）
100pF capacitor	×	O	O	O	O	O

O: indicates that the content of the toxic and hazardous substance in all the homogeneous materials of the part is below the concentration limit requirement as described in SJ/T 11363-2006.
×: indicates that the content of the toxic and hazardous substance in at least one homogeneous material of the part exceeds the concentration limit requirement as described in SJ/T 11363-2006.
(The enterprise may further explain the technical reasons for the “x” indicated portion in the table in accordance with the actual situations.)

O：表示该有毒有害物质在该部件所有均质材料中的含量均在 SJ/T 11363-2006 标准规定的限量要求以下。
×：表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 SJ/T 11363-2006 标准规定的限量要求。
（企业可在此处，根据实际情况对上表中打“×” 的技术原因进行进一步说明。）

Note: EU RoHS compliant under exemption clause of “lead in electronic ceramic parts (e.g. piezoelectronic devices)”

For product information and a complete list of distributors, please go to our web site: **www.avagotech.com**

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