ISL54406

Stereo Click and Pop Eliminator with Audio Muting

FN6578
Rev 1.00
July 14, 2010

The ISL54406 is a Dual SPST (Single Pole/Single Throw) switch that provides a very low distortion audio path for a stereo headphone or high impedance line-in load. This path can be interrupted to provide >110dB of off-isolation for signal muting purposes into 32Ω or high impedance loads such as consumer entertainment system line-inputs, MP3 docking systems for powered speaker or automotive entertainment system in-line or cassette interfaces. Recovery from muting is instant even with very large DC blocking capacitors.

The ISL54406 also has comprehensive Click and Pop elimination measures to prevent these artifacts from occurring in the load due to system power-up/power-down, codec enable/disable, headphone hot plug in, and audio muting on/off situations. The Click and Pop elimination is effective into low and high impedance loads and requires no external timing components to deal with DC blocking capacitors placed between the single supply codec and the load.

The ISL54406 is available in a 10 Ld TDFN (3mmx3mm) or a tiny 10 Ld µTQFN (1.8mmx1.4mm) ultra-thin package. It operates over a temperature range of -40 to +85°C.

Features

- Single Supply Operation (V_{DD}) . . . +2.7V to +5.0V
- Negative Signal Swing Capability. . . . . -1.5V
- Low THD
  - THD+N at 1mW into 32Ω Load . . . . . <0.02%
- Click and Pop Elimination . . . . . >60dB
- Audio Muting . . . . . >110dB
- Low Power Consumption . . . . 21µW with 3V supply
- Low Power Shutdown Mode
- 1.8V Logic Compatible
- Available in 10 Ld TDFN (3mmx3mm) or tiny 10 Ld (1.8mmx1.4mm) µTQFN Package
- Pb-Free (RoHS Compliant)

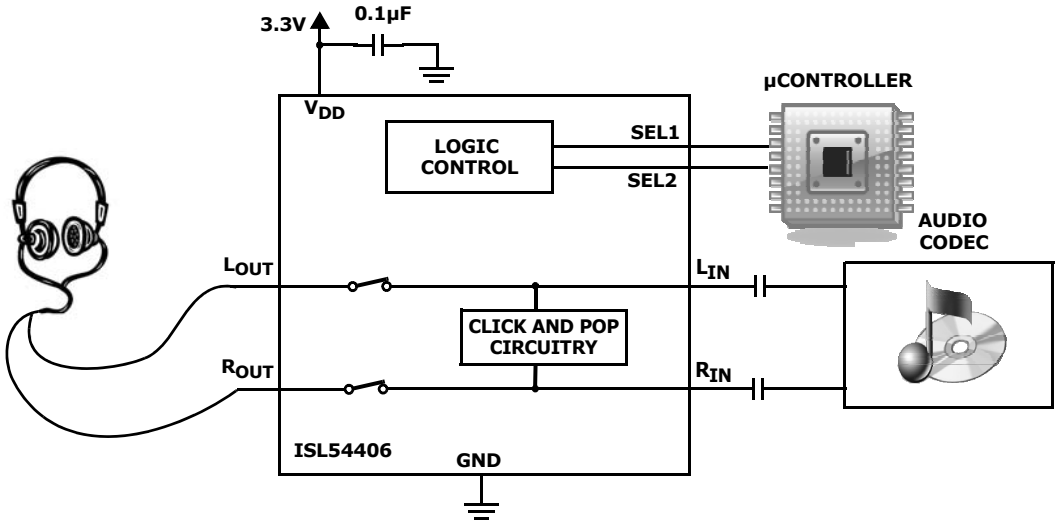
Applications

- Consumer Entertainment Systems
- MP3 and other Personal Media Players
- Cellular/Mobile Phones
- PDA's
- Audio Switching and Muting

Related Literature* (see page 14)

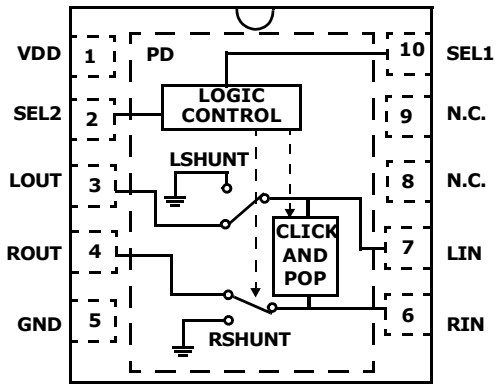
- Technical Brief TB363 "Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)".
- Application Note AN1368 "ISL54406EVAL1Z Evaluation Board User's Manual"

Application Block Diagram

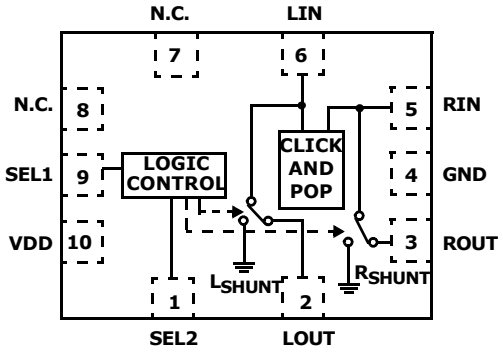


Pin Configurations (Note 1)

ISL54406
(10 Ld 3x3 TDFN)
TOP VIEW



ISL54406
(10 Ld 1.8x1.4 µTQFN)
TOP VIEW



NOTE:

1. ISL54406 Switches Shown for SEL1 = Logic “1” and SEL2 = Logic “1”.

Truth Table

ISL54406					
SEL2	**SEL1**	**L_{IN}/ R_{IN}**	**L_{SHUNT}/ R_{SHUNT}**	**CLICK AND POP**	**MODE**
0	0	OFF	OFF	Inactive	Shutdown
0	1	OFF	ON	Active	Click and Pop
1	0	OFF	ON	Inactive	Mute
1	1	ON	OFF	Inactive	Audio

SEL1 and SEL2: Logic “0” when ≤ 0.5V, Logic “1” when ≥ 1.4V

Pin Descriptions

ISL54406			
TDFN	**µTQFN**	**NAME**	**FUNCTION**
1	10	V_{DD}	Power Supply
2	1	SEL2	Logic Control 2
3	2	LOUT	Audio Left Output
4	3	ROUT	Audio Right Output
5	4	GND	IC Ground Connection
6	5	RIN	Audio Right Input
7	6	LIN	Audio Left Input
8, 9	7, 8	N.C.	No Connection
10	9	SEL1	Logic Control 1
PD	-	PD	Thermal Pad. Tie to Ground or Float

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL54406IRUZ-T (Notes 2, 3)	6	-40 to +85	10 Ld 1.8x1.4 µTQFN	L10.1.8x1.4A
ISL54406IRTZ (Note 4)	4406	-40 to +85	10 Ld 3x3 TDFN	L10.3x3A
ISL54406IRTZ-T (Notes 2, 4)	4406	-40 to +85	10 Ld 3x3 TDFN	L10.3x3A
ISL54406EVAL1Z	Evaluation Board			

NOTES:

2. Please refer to TB347 for details on reel specifications.
3. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
4. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
5. For Moisture Sensitivity Level (MSL), please see device information page for ISL54406. For more information on MSL please see techbrief TB363.

Absolute Maximum Ratings

V_{DD} to GND . . . . . -0.3 to 5.5V
Input Voltages
L_{IN}, R_{IN} (Note 6) . . . . . -2V to ((V_{DD}) + 0.3V)
SEL1 (Note 6) . . . . . -0.3V to ((V_{DD}) + 0.3V)
SEL2 (Note 6) . . . . . -0.3 to ((V_{DD}) + 0.3V)
Output Voltages
L_{OUT}, R_{OUT} (Note 6) . . . . . -2V to ((V_{DD}) + 0.3V)
Continuous Current . . . . . ±150mA
Peak Current
(Pulsed 1ms, 10% Duty Cycle, Max) . . . . . ±300mA
ESD Rating:
Human Body Model . . . . . >5kV
Machine Model . . . . . >300V
Charged Device Model . . . . . >1.5kV
Latch-up Tested per JEDEC; Class II Level A . . . . . at +85°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
10 Ld µTQFN (Note 7, 8)	160	105
10 Ld TDFN (Notes 9, 10)	55	18

Maximum Junction Temperature (Plastic Package) . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Temperature Range . . . . . -40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

6. Signals on LIN, RIN, LOUT, ROUT, SEL1, and SEL2 exceeding V_{DD} or GND by specified amount are clamped. Limit current to maximum current ratings.
7. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
8. For θ_{JC}, the “case temp” location is taken at the package top center.
9. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
10. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications - 2.7V to 3.6V Supply

Test Conditions: V_{DD} = +3.0V, GND = 0V, V_{SELx_H} = 1.4V, V_{SELx_L} = 0.5V, (Notes 11), Unless Otherwise Specified
Boldface limits apply over the operating temperature range, -40°C to +85°C.

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 12, 13)	TYP	MAX (Notes 12, 13)	UNITS
ANALOG SWITCH CHARACTERISTICS						
Analog Input Signal Range, V_{ANALOG}	V_{DD} = 3.3V, V_{SEL2} = 1.4V, V_{SEL1} = 1.4V	Full	**-1.5**	-	**1.5**	V
ON-Resistance, r_{ON}	V_{DD} = 3.0V, V_{SEL2} = 1.4V, V_{SEL1} = 1.4V I_{XOUT} = 40mA, V_{LIN} or V_{RIN} = -0.85V to 0.85V, (See Figure 2, Note 16)	+25	-	2.5	2.8	Ω
		Full	-	-	**4.0**	Ω
r_{ON} Flatness, $r_{FLAT(ON)}$	V_{DD} = 3.0V, V_{SEL2} = 1.4V, V_{SEL1} = 1.4V I_{XOUT} = 40mA, V_{LIN} or V_{RIN} = -0.85V to 0.85V, (Notes 14, 16)	+25	-	2	-	mΩ
		Full	-	-		mΩ
r_{ON} Matching Between Channels, Δr_{ON}	V_{DD} = 3.0V, V_{SEL2} = 1.4V, V_{SEL1} = 1.4V I_{XOUT} = 40mA, V_{LIN} or V_{RIN} = Voltage at max r_{ON} over signal range of -0.85V to 0.85V, (Note 15, 16)	+25	-	0.09	0.25	Ω
		Full	-	-	**0.35**	Ω
Discharge Pull-Down Resistance, R_L, R_R	V_{DD} = 3.6V, V_{SEL2} = 1.4V, V_{SEL1}= 1.4V , V_{ROUT} or V_{LOUT} = -0.85V, 0.85V. Measure current through the discharge pull down resistor and calculate resistance value.	+25	-	240	-	kΩ
Click and Pop Discharge Resistance	V_{DD} = 3.0V, V_{SEL2} = 0V, V_{SEL1}= 1.4V, V_{INL} or V_{INR} = -0.85V, 0.85V. Measure current through the Click and Pop discharge resistance and calculate resistance value.	+25	-	35	-	Ω

Electrical Specifications - 2.7V to 3.6V Supply Test Conditions: V_{DD} = +3.0V, GND = 0V, V_{SELx_H} = 1.4V, V_{SELx_L} = 0.5V, (Notes 11), Unless Otherwise Specified **(Continued) Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 12, 13)	TYP	MAX (Notes 12, 13)	UNITS
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V_{DD} = 2.7V, V_{SEL1} = 2.7V, R_L = 50Ω, C_L = 10pF, (See Figure 1)	+25	-	5	-	µs
Turn-OFF Time, t_{OFF}	V_{DD} = 2.7V, V_{SEL1} = 2.7V, R_L = 50Ω, C_L = 10pF, (See Figure 1)	+25	-	45	-	ns
OFF-Isolation, Mute Mode	V_{DD} = 3.0V, V_{SEL2} = 0V, V_{SEL1} = 3.0V, V_{LIN} or V_{RIN} = 0.707V_{RMS}, R_L = 32Ω, f = 20Hz to 20kHz, (See Figure 3).	+25	-	110	-	dB
	V_{DD} = 3.0V, V_{SEL2} = 0V, V_{SEL1} = 3.0V, V_{LIN} or V_{RIN} = 0.707V_{RMS}, R_L = 20kΩ, f = 20Hz to 20kHz, (See Figure 3).	+25	-	110	-	dB
Crosstalk R_{IN} to L_{OUT}, L_{IN} to R_{OUT}	V_{DD} = 3.0V, V_{SEL2} = 3.0V, V_{SEL1} = 3.0V, R_L = 32Ω, f = 20Hz to 20kHz, V_{LIN} or V_{RIN} = 0.707V_{RMS} ($2V_{P-P}$), (See Figure 4)	+25	-	-90	-	dB
Total Harmonic Distortion	V_{DD} = 3.0V, f = 20Hz to 20kHz, V_{SEL2} = 3.0V, V_{SEL1} = 3.0V, V_{LIN} or V_{RIN} = 0.36V_{RMS} ($1V_{P-P}$), R_L = 32Ω	+25	-	0.03	-	%
	V_{DD} = 3.0V, f = 20Hz to 20kHz, V_{SEL2} = 3.0V, V_{SEL1} = 3.0V, V_{LIN} or V_{RIN} = 0.707V_{RMS} ($2V_{P-P}$), R_L = 32Ω	+25	-	0.06	-	%
Click and Pop Reduction (Note 17)	V_{DD} = 3.0V, V_{SEL1} = 3.0V, V_{SEL2} = 0V to 3.0V DC step, R_L = 20kΩ, V_{INL} or V_{INR} = 0VDC to 1.5VDC step (see Figure 6)	+25	-	>60	-	dB
	V_{DD} = 3.0V, V_{SEL1} = 3.0V, V_{SEL2} = 0V to 3.0V DC step, R_L = 32Ω, V_{INL} or V_{INR} = 0VDC to 1.5VDC step (see Figure 6)	+25	-	>70	-	dB
POWER SUPPLY CHARACTERISTICS						
Power Supply Range, V_{DD}		Full	**2.7**		**3.6**	V
Positive Supply Current, I_{DD}	V_{DD} = 3.6V, V_{SEL2} = 1.4V, V_{SEL1} = 1.4V	+25	-	7	10	µA
		Full	-	-	**15**	µA
Shutdown Current, I_{SHDN}	V_{DD} = 3.6V, V_{SEL2} = Float, V_{SEL1} = Float	25	-	-	**50**	nA
DIGITAL INPUT CHARACTERISTICS						
SELx Voltage Low, V_{SELx_L}	V_{DD} = 2.7V to 3.6V	Full	-	-	**0.5**	V
SELx Voltage High, V_{SELx_H}	V_{DD} = 2.7V to 3.6V	Full	**1.4**	-	-	V
Input Low Current, I_{SEL2L}, I_{SEL1L}	V_{DD} = 3.6V, V_{SEL2} = 0V or Float, V_{SEL1} = 0V or Float	Full	**-20**	2	**20**	nA

Electrical Specifications - 2.7V to 3.6V Supply Test Conditions: V_{DD} = +3.0V, GND = 0V, V_{SELx_H} = 1.4V, V_{SELx_L} = 0.5V, (Notes 11), Unless Otherwise Specified **(Continued) Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 12, 13)	TYP	MAX (Notes 12, 13)	UNITS
Input High Current, I_{SEL2H}, I_{SEL1H}	V_{DD} = 3.6V, V_{SEL2} = 3.6V, V_{SEL1} = 3.6V	Full	**-2**	1	**2**	µA
SEL1 Pull-Down Resistor, R_{SEL1}	V_{DD} = 3.6V, V_{SEL2} = 3.6V, V_{SEL1} = 0V	Full	-	4	-	MΩ
SEL2 Pull-Down Resistor, R_{SEL2}	V_{DD} = 3.6V, V_{SEL2} = 0V, V_{SEL1} = 3.6V	Full	-	4	-	MΩ

NOTES:

11. V_{SELx} = Input voltage to perform proper function.
12. The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
13. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
14. Flatness is defined as the difference between maximum and minimum value of ON-resistance over the specified analog signal range.
15. r_{ON} matching between channels is calculated by subtracting the channel with the highest max r_{ON} value from the channel with lowest max r_{ON} value.
16. Limits established by characterization and are not production tested.
17. Click and Pop Reduction specifications are limited by test equipment.

Test Circuits and Waveforms

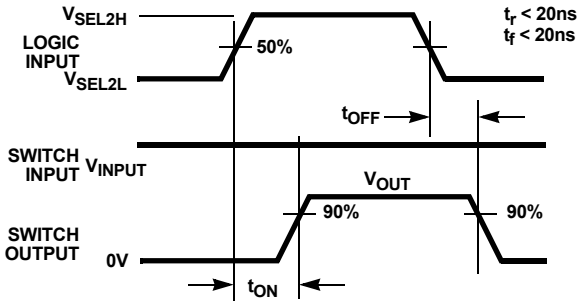
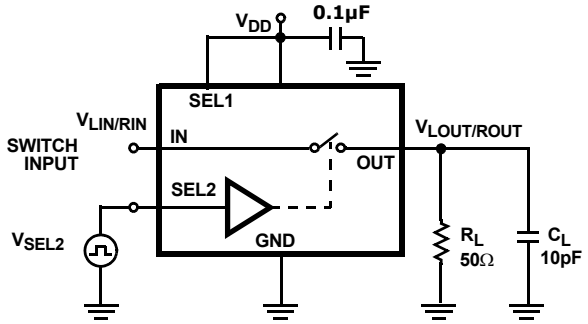


FIGURE 1A. MEASUREMENT POINTS



Repeat test for all switches. C_L includes fixture and stray capacitance.

$$V_{OUT} = V_{(INPUT)} \frac{R_L}{R_L + r_{ON}}$$

FIGURE 1B. TEST CIRCUIT

FIGURE 1. SWITCHING TIMES

Test Circuits and Waveforms (Continued)

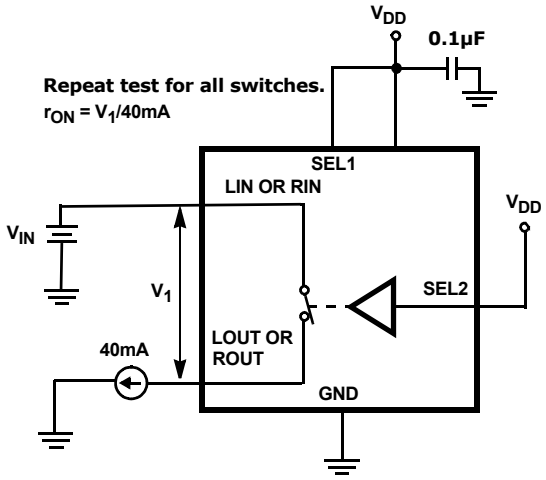


FIGURE 2. r_{ON} TEST CIRCUIT

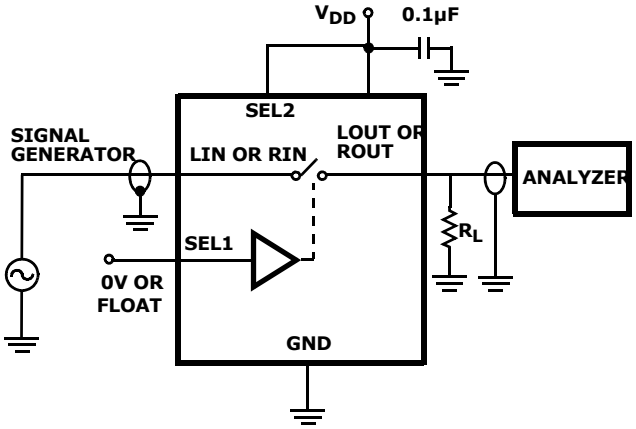


FIGURE 3. OFF ISOLATION CIRCUIT

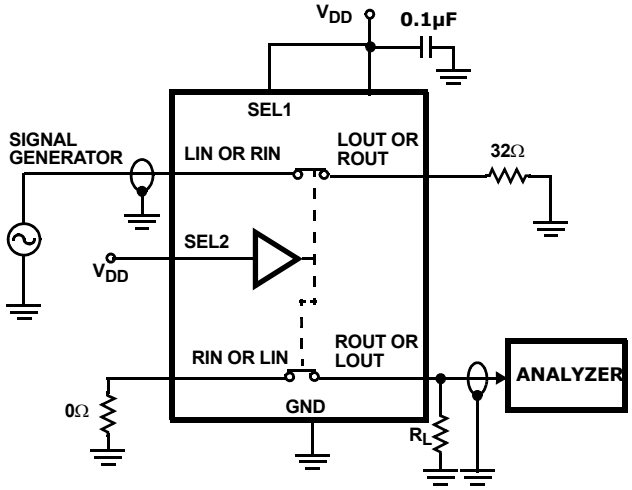
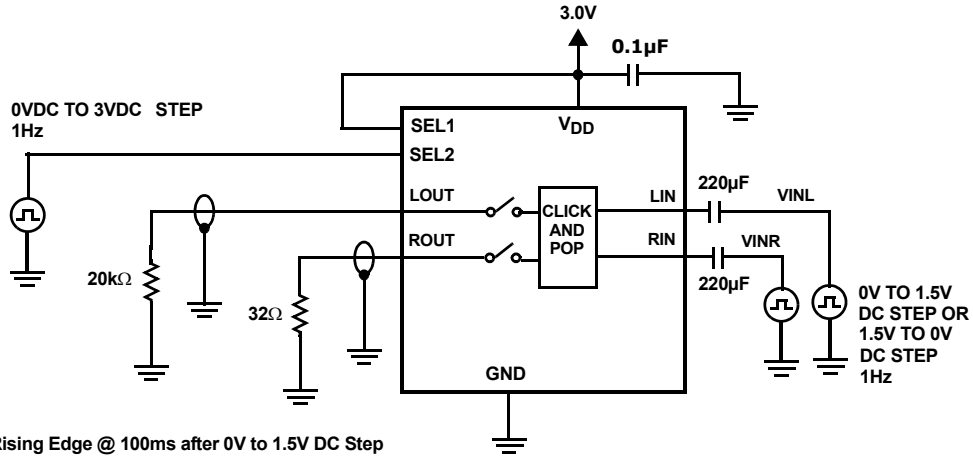


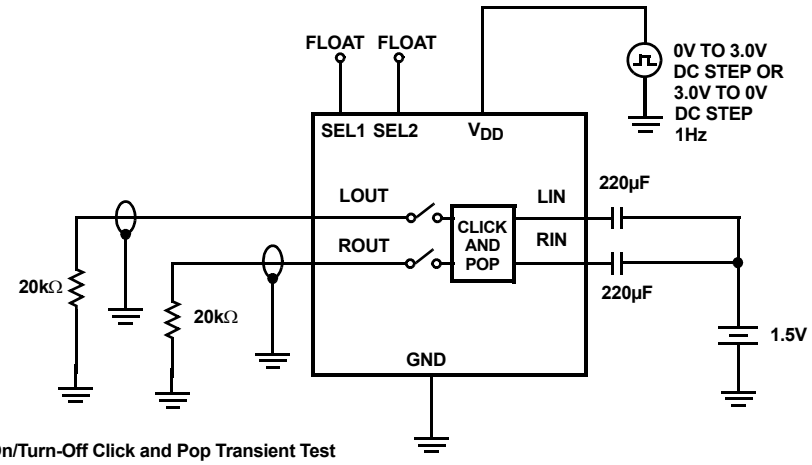
FIGURE 4. CROSSTALK TEST CIRCUIT



SEL2 Waveform: Rising Edge @ 100ms after 0V to 1.5V DC Step
Falling Edge @ 100ms before 1.5V to 0V DC Step
*See Figures 18 and 19

FIGURE 5. CLICK AND POP TEST CIRCUIT #1

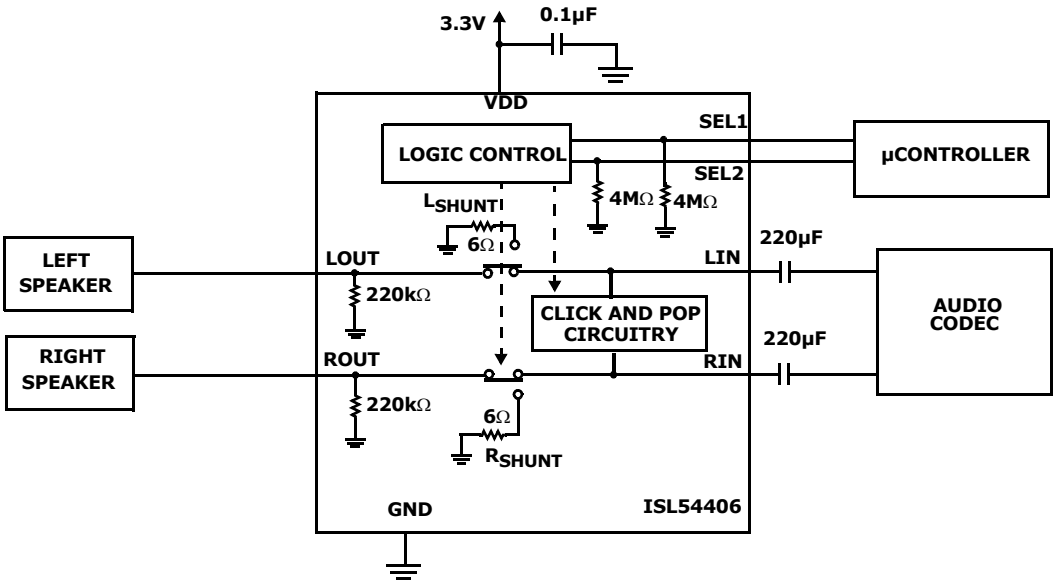
Test Circuits and Waveforms (Continued)



Power Supply Turn-On/Turn-Off Click and Pop Transient Test
*See Figure 17

FIGURE 6. CLICK AND POP TEST CIRCUIT #2

Application Block Diagram



Detailed Description

The ISL54406 device is a dual single pole-single throw (SPST) analog switch that operates from a single DC power supply in the range of +2.7V to +5V. It was designed to function as a transient suppressor to eliminate Click and Pop noise on headphones. It comes in a 10 Ld (3mmx3mm) TDFN or a tiny 10 Ld (1.8mmx1.4mm) µTQFN package for use in MP3 players, PDAs, cellphones, and other personal media players.

The part consist of a pair of 2.5Ω audio switches. The audio switches can accept signals that swing below ground by as much as -1.5V. They were designed to pass audio left and right stereo signals that are ground referenced with minimal distortion.

The ISL54406 was specifically designed for MP3 players, personal media players and cellphone applications that require but do not have Click and Pop elimination. See “Application Block Diagram” on page 9.

The ISL54406 contains logic control pins SEL1 and SEL2 that will determine the state of the switch. See the “Truth Table” on page 2 for a description of each state. A detailed description of the audio switches are provided in the section that follows.

Audio Switches

The two 2.5Ω audio switches (L, R) are designed to pass signals that swing 1.5V above and below ground. Crosstalk between the audio switches is -90dB over the audio band. These switches have excellent off-isolation of 110dB over the audio bandwidth with a 32Ω load.

Over a signal range of ±1V (0.707V_{RMS}) with V_{DD} > 2.7V, these switches have an extremely low r_{ON} resistance variation (0.03Ω). They can pass ground referenced audio signals with very low distortion (<0.04% THD+N) when delivering 4mW into a 32Ω headphone speaker load. See Figures 10, 11, 12 and 13 for THD+N performance curves.

The audio drivers should be connected at the LIN and RIN side of the switch and the speaker loads should be connected at the LOUT and ROUT side of the switch for proper Click and Pop elimination. The switches have Click and Pop circuitry on the LIN and RIN side that is activated when the SEL1 pin is driven High and SEL2 pin is driven Low. The audio switches are turned OFF in this state. The ISL54406 should be put in this mode before powering down or powering up of the audio source drivers. The high off-isolation of the audio switches along with the Click and Pop circuitry will prevent the transients generated during power-up and power-down of the audio source from getting through to the headphones, thus eliminating Click and Pop noise in the headphones. The audio switches are turned ON and the Click and Pop circuitry disabled whenever SEL1 and SEL2 is driven High.

ISL54406 Operation

The discussion that follows will describe using the ISL54406 in the “Application Block Diagram” on page 9.

LOGIC CONTROL

The state of the ISL54406 device is determined by the logic level at the SEL1 and SEL2 pins. The part has four states or modes of operation. The Audio Playback Mode, Audio Mute Mode, Click and Pop Mode, and Shutdown Mode. Refer to “Truth Table” on page 2 for the logic state of each mode of operation. The SEL1 and SEL2 pins are internally pulled low through 4MΩ resistors to ground and can be left floating to pull the logic pins Low.

Logic Control Voltage Levels:

SEL1 and SEL2 = Logic “0” (Low) when ≤ 0.5V or Floating.
SEL1 and SEL2 = Logic “1” (High) when ≥ 1.4V

Audio Playback Mode

If the SEL1 and SEL2 pins are Logic “1”, the device will be in the Audio Playback mode. In Audio Playback mode the LIN (left) and RIN (right) 2.5Ω audio switches are connected to LOUT and ROUT respectively, and the audio Click and Pop circuitry is inactive (high impedance). When headphones are connected to the LOUT and ROUT outputs of the ISL54406, the audio source drives the headphones with low distortion audio.

Audio Mute Mode

If SEL1 is Logic “0” and SEL2 is Logic “1”, the device will be in the Audio Mute Mode. In Audio Mute Mode the audio switches are OFF (high impedance), the audio Click and Pop shunt circuitry is OFF (high impedance), and the LOUT and ROUT pins are shorted through 6Ω resistors to ground. Off Isolation performance in Audio Mute Mode gives a 110 dB signal reduction across a 32Ω load when driving with a 0.707V_{RMS} signal at the switch input.

Click and Pop Mode

Note: Click and Pop Mode should not be used for audio muting applications. In Click and Pop Mode, a low impedance (35Ω) path to ground at the LIN/RIN inputs will degrade Off Isolation performance (see Figure 14).

If SEL1 is Logic “1” and SEL2 is Logic “0”, the device will go into Click and Pop Mode. This mode is optimal when powering up or down the audio sources. In Click and Pop Mode the audio in-line 2.5Ω switches are OFF (high impedance). The LOUT and ROUT pins are shorted through 6Ω resistors to ground and the LIN and RIN are shunted through 35Ω resistors to ground (Click and Pop circuitry is active).

Before powering down or powering up of the audio source drivers, the ISL54406 should be put in the Click and Pop Mode. In Click and Pop Mode, transients generated at the LIN and RIN pins due to a DC step voltage at the audio drivers will not pass through the ISL54406 audio switches, preventing Click and Pop noise to the load.

Shutdown Mode

If SEL1 and SEL2 pins are Logic “0”, the device will enter a low powered Shutdown (SHDN) Mode. In SHDN, the audio switches are OFF, the 6Ω path is high impedance, the Click and Pop circuitry is inactive, and the device will draw a typical supply current of 5nA.

Note: When the logic inputs are floated, the ISL54406 will automatically be placed in SHDN mode due to the internal 4MΩ pull down resistors on the logic pins.

Note: In Shutdown Mode, the Off-Isolation of the audio switch degrades in performance compared to Audio Mute Mode. In SHDN, the negative charge pumps that permit the signal to swing below ground are turned off to reduce power consumption, thus any negative signal swing at the LIN and RIN will appear at the LOUT and ROUT pins. The device should not be placed into SHDN when the source is still active or for high Off-Isolation performance.

CLICK AND POP OPERATION

Single supply audio sources are biased at a DC offset that generates transients during power on/off of the source. This DC transient is coupled into the load through a blocking capacitor (see “Application Block Diagram” on page 9). When the source is off and suddenly turned on with a DC offset, the capacitor will develop a voltage across it that is equal to the DC offset. If the switch is in Audio mode when this occurs, a transient discharge will occur in the speaker, generating a Click and Pop noise.

Proper elimination of Click and Pop transients requires that the ISL54406 be placed in Click and Pop Mode before the audio source is turned on or off. This allows any transients generated by the source to be discharged through the Click and Pop circuitry first. With a typical DC blocking capacitor of 220µF and the Click and Pop circuitry designed to have a resistance of 35Ω, allowing a 100ms dead-time for discharging a transient before placing the switch in Audio mode will eliminate the DC transient generated by the blocking capacitor.

Note: The ISL54406 should not be brought into Audio Playback Mode directly from Shutdown Mode and vice versa. A DC transient may occur at the LOUT/ROUT pins when brought from Shutdown directly to Audio Playback mode. The recommended procedure is to place the ISL54406 into Mute mode for at least 100ms when entering or leaving Audio Playback mode.

Power supply considerations

The power supply connected at V_{DD} and GND provides power to the ISL54406 part. In a typical application V_{DD} will be in the range of +2.7V to +5.0V and will be connected to the battery or LDO of the MP3 player or cellphone. A 0.1µF local decoupling capacitor should be placed near the V_{DD} pin of the IC to eliminate power supply transients.

Before power-up and power-down of the ISL54406 part, the SEL1 and SEL2 logic control pins should be driven to Logic “0” or left floating. In a high impedance state, 4MΩ internal pull down resistors on the SEL1 and SEL2 pins will set the ISL54406 logic pins to “0”. This will put the switch in the SHDN state which turns all switches OFF and deactivates the Click and Pop circuitry which will minimize power supply currents and increase battery life.

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified

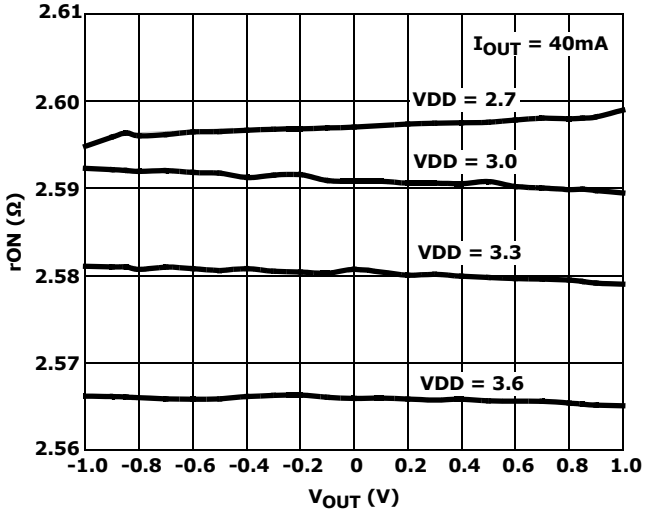


FIGURE 7. ON-RESISTANCE vs SWITCH VOLTAGE vs SUPPLY VOLTAGE

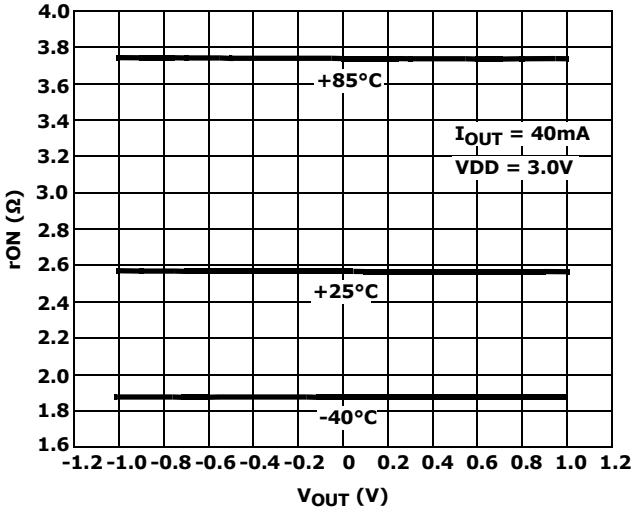


FIGURE 8. ON-RESISTANCE vs SWITCH VOLTAGE vs TEMPERATURE

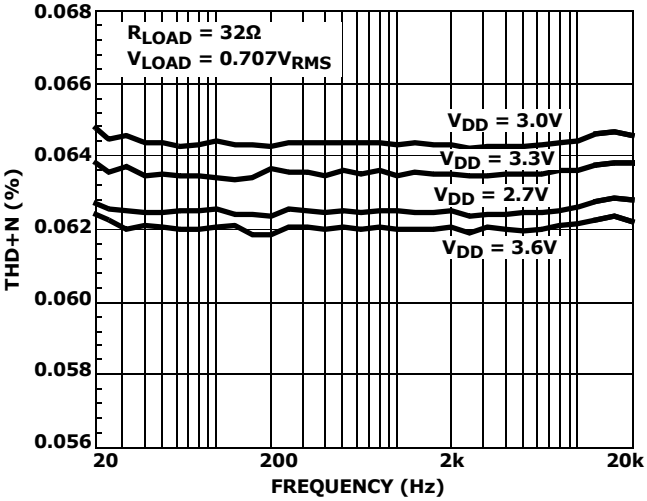


FIGURE 9. THD+N vs SUPPLY VOLTAGE vs FREQUENCY

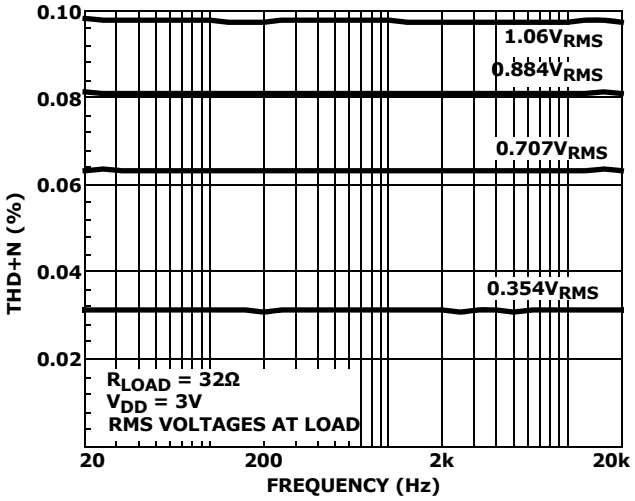


FIGURE 10. THD+N vs SIGNAL LEVELS vs FREQUENCY

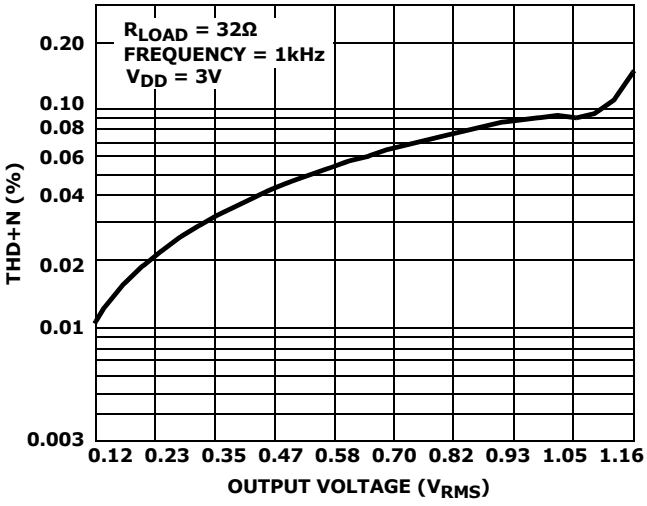


FIGURE 11. THD+N vs OUTPUT VOLTAGE

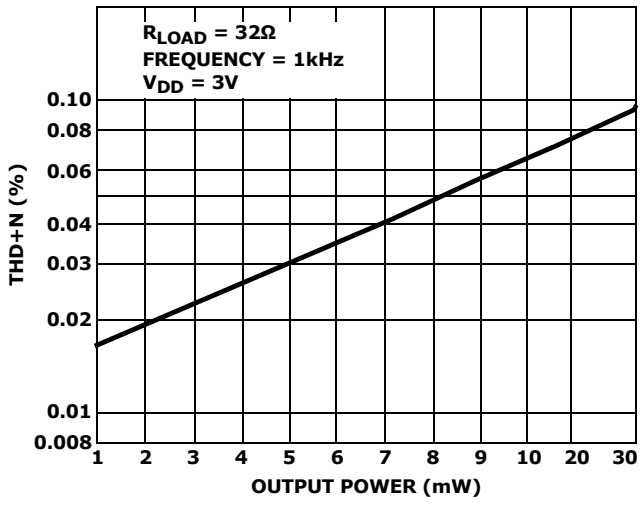


FIGURE 12. THD+N vs OUTPUT POWER

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified **(Continued)**

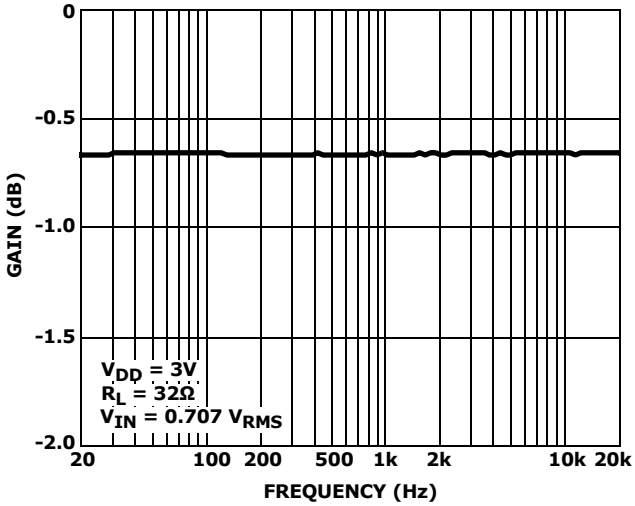


FIGURE 13. INSERTION LOSS

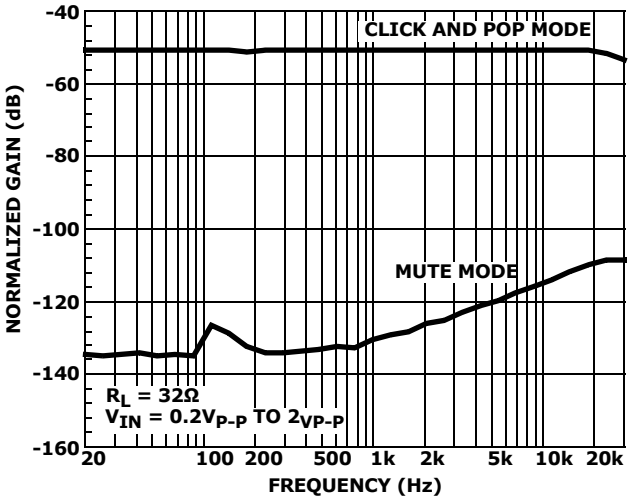


FIGURE 14. OFF-ISOLATION

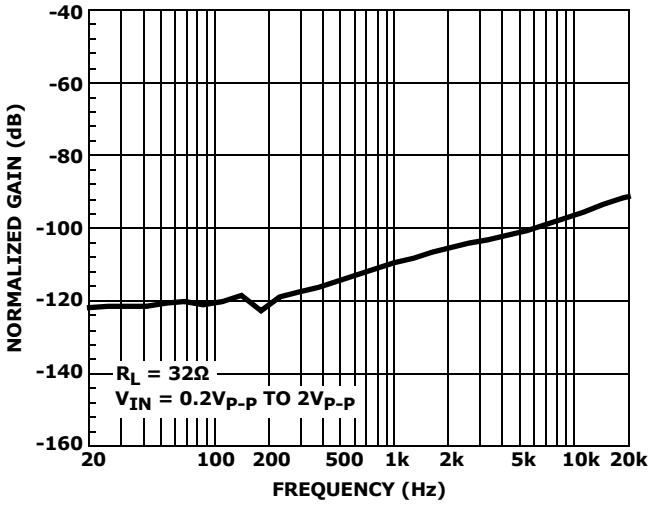


FIGURE 15. CROSSTALK

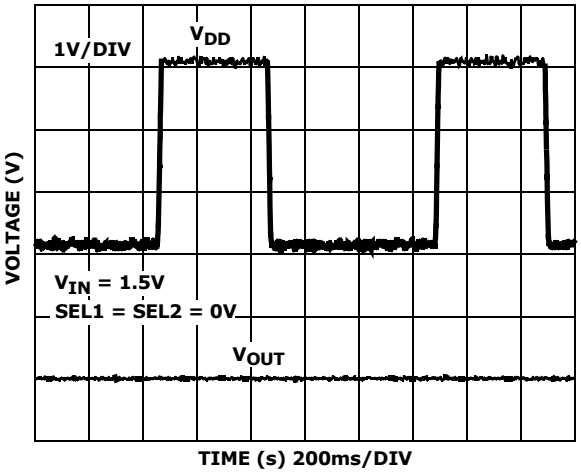


FIGURE 16. POWER-UP/POWER-DOWN CLICK AND POP TRANSIENT

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified **(Continued)**

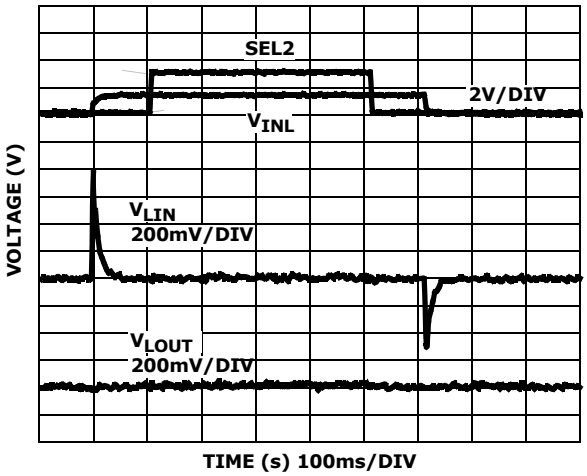


FIGURE 17. 20kΩ CLICK AND POP REDUCTION

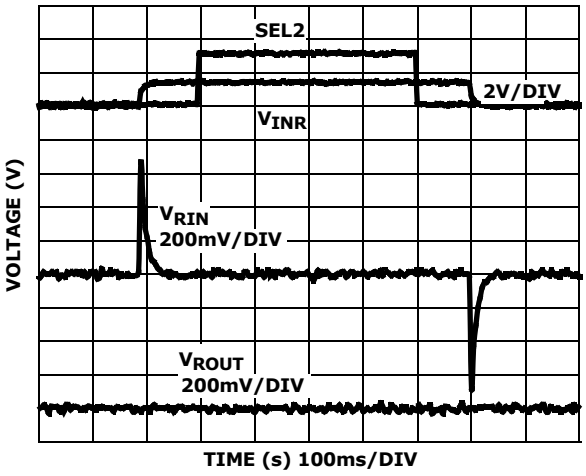


FIGURE 18. 32Ω CLICK AND POP REDUCTION

Die Characteristics

SUBSTRATE AND TDFN THERMAL PAD POTENTIAL (POWERED UP):

GND

TRANSISTOR COUNT:

98

PROCESS:

Submicron CMOS

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
06/4/10	FN6578.1	On page 3, added evaluation board part number to “Ordering Information” table. On page 4 in “Thermal Information”, changed µTQFN theta JC value from 62 to 105. Added Notes 7 and 8 to reference uTQFN package. On page 5, changed “Shutdown Current, ISHDN” limit from 5nA to 50nA. Converted to new Intersil template. Changes include: Added Note 5 to “Ordering Information” on page 3. “Pin Descriptions” on page 2, updated to show the thermal pad. “Absolute Maximum Ratings” on page 4, added latch-up level. Added boldface limits text in conditions of Spec Table and bolded Min and Max over-temp Limits Updated Over-temp Note to meet standard verbiage Added “Products” on page 14. Added “Revision History” on page 14.
5/28/08	FN6578.0	Initial Release

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

*For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL54406

To report errors or suggestions for this datasheet, please go to www.intersil.com/askourstaff

FITs are available from our website at
http://rel.intersil.com/reports/search.php

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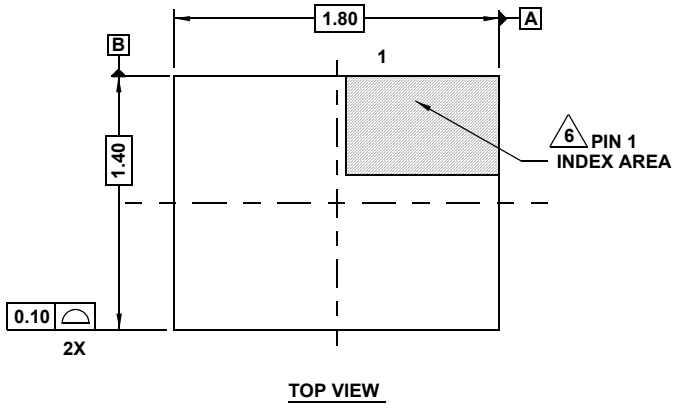
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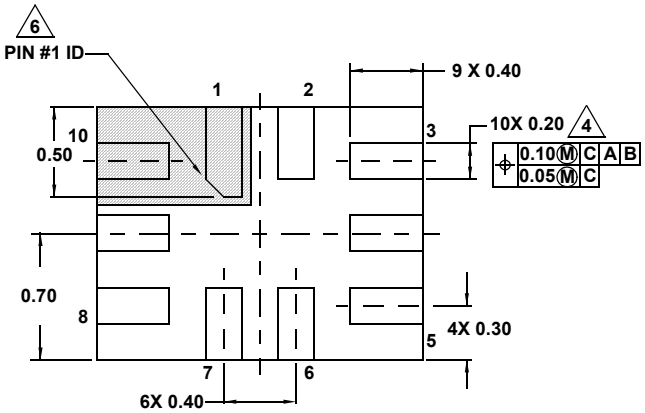
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L10.1.8x1.4A

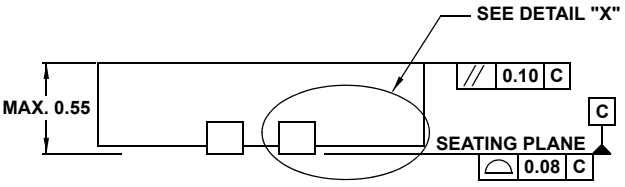
10 LEAD ULTRA THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 5, 3/10



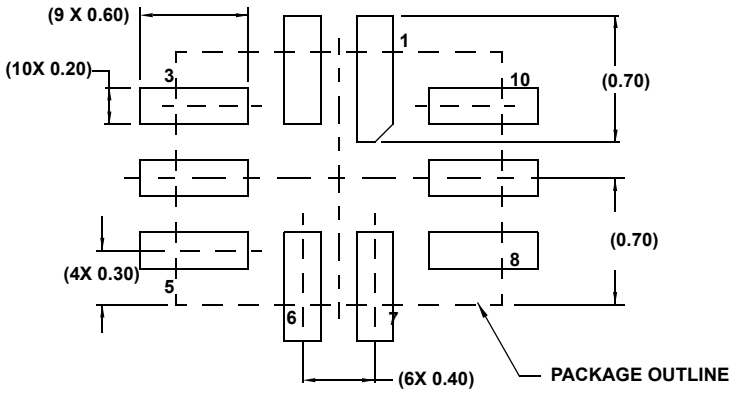
TOP VIEW



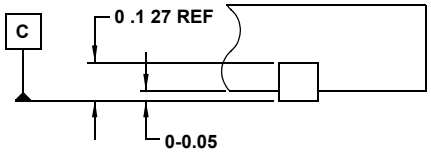
BOTTOM VIEW



SIDE VIEW



TYPICAL RECOMMENDED LAND PATTERN

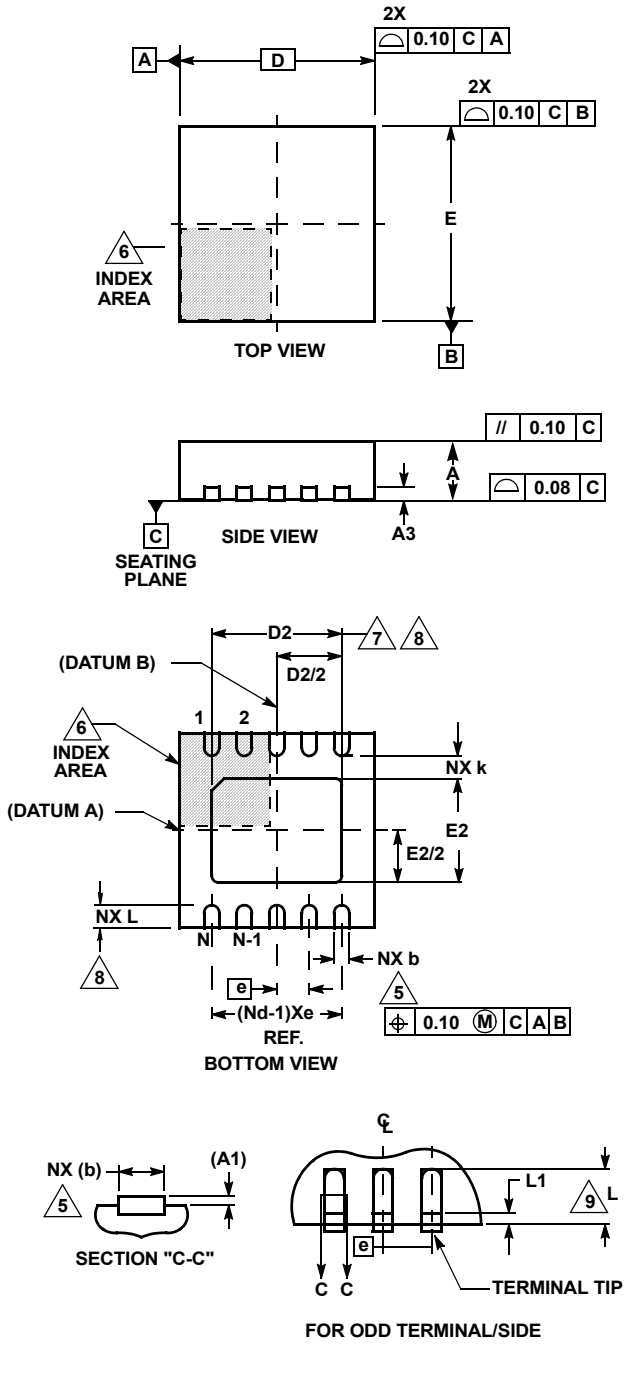


DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. JEDEC reference MO-255.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

Thin Dual Flat No-Lead Plastic Package (TDFN)



L10.3x3A

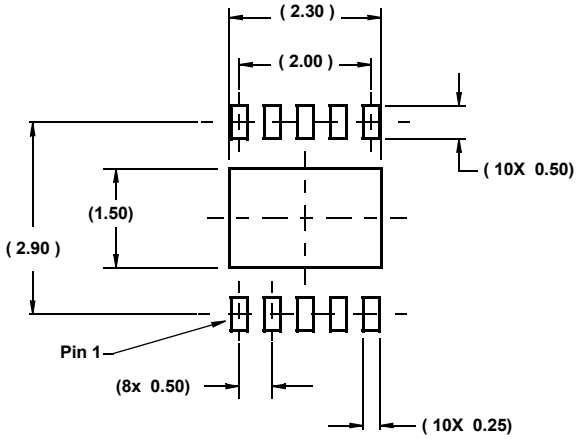
10 LEAD THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.70	0.75	0.80	-
A1	-	-	0.05	-
A3		0.20 REF		-
b	0.20	0.25	0.30	5, 8
D	2.95	3.0	3.05	-
D2	2.25	2.30	2.35	7, 8
E	2.95	3.0	3.05	-
E2	1.45	1.50	1.55	7, 8
e		0.50 BSC		-
k	0.25	-	-	-
L	0.25	0.30	0.35	8
N		10		2
Nd		5		3

Rev. 4 8/09

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd refers to the number of terminals on D.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Compliant to JEDEC MO-229-WEED-3 except for D2 dimensions.



TYPICAL RECOMMENDED LAND PATTERN