MIC4600

28V Half-Bridge MOSFET Driver

Features

- Adjustable Dead Time Circuitry
- Anti-Shoot-Through Protection
- Internal LDO for Single Supply Operation
- Input Voltage Range: 4.5V to 28V
- Fast Propagation Delay: 20 ns
- Up to 1.5 MHz Operation
- Low Voltage Logic Level Inputs for µC or FPGA Driven Power Solutions
- Independent Inputs for Low and High-Side Drivers
- 2Ω Gate Drive Capable of Driving 3000 pF Load with 15 ns Rise and Fall Times
- Low 450 µA Typical Quiescent Current
- 3 mm x 3 mm VQFN Package
- –40°C to +125°C Junction Temperature Range

Applications

- Distributed Power Systems
- Communications/Networking Infrastructure
- Set-Top Boxes, Gateways, and Routers
- Printers and Scanners
- µP and FPGA Controlled DC-DC Regulators

General Description

The MIC4600 is a 28V half-bridge MOSFET driver targeted for cost-sensitive applications that require high performance such as set-top boxes, gateways, routers, computing peripherals, telecom, and networking equipment.

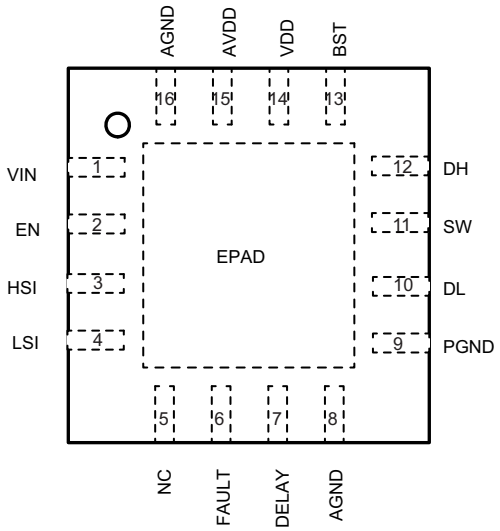
The MIC4600 operates over a supply range of 4.5V to 28V. It has an internal linear regulator that provides a regulated 5V to power the MOSFET gate drive and operates up to 1.5 MHz switching frequency.

The MIC4600 uses an adjustable dead time circuit to prevent shoot-through in the external high and low-side MOSFETs.

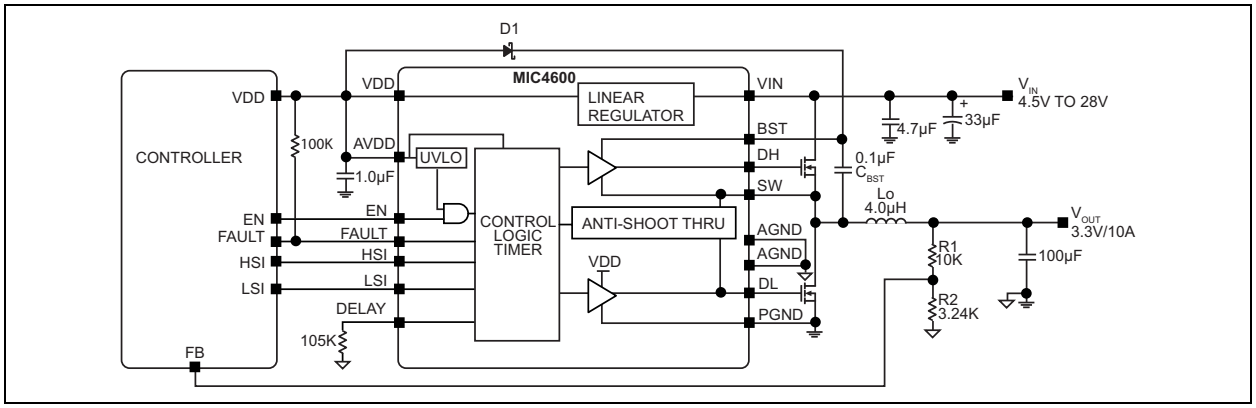
The MIC4600 is available in a small 3 mm x 3 mm VQFN package with a junction temperature range of –40°C to +125°C.

Package Type

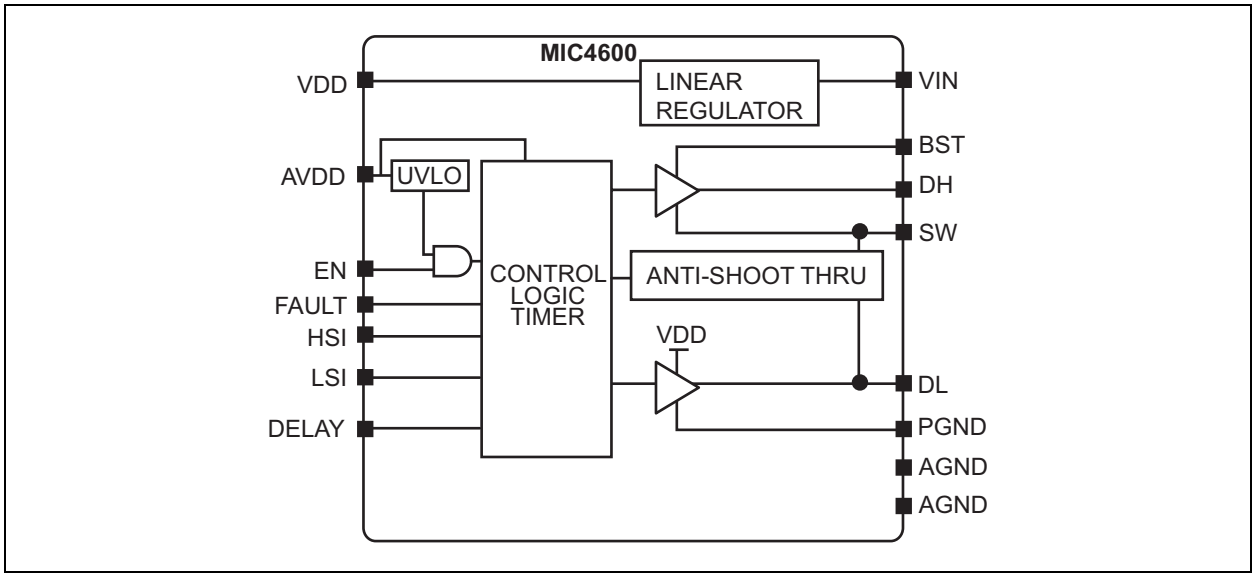
MIC4600
3 mm x 3 mm VQFN
(Top View)



Typical Application Circuit



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

V_{IN} to PGND ..... –0.3V to +29V
V_{DD} to PGND ..... –0.3V to +6V
V_{SW} to PGND ..... –0.3V to (V_{IN} + 0.3V)
V_{BST} to V_{SW} ..... –0.3V to +6V
V_{BST} to PGND ..... –0.3V to +34V
V_{HSI}, V_{LSI} to PGND ..... –0.3V to (V_{DD} + 0.3V)
V_{FAULT} to AGND ..... –0.3V to +6V
V_{EN} to PGND ..... –0.3V to (V_{IN} + 0.3V)
PGND to AGND ..... –0.3V to +0.3V
ESD Protection on All Pins ..... ±1.5 kV HBM

Operating Ratings ††

Supply Voltage (V_{IN}) ..... +4.5V to +28V
VDD Supply Voltage (V_{DD}) ..... +4.5V to +5.5V
Enable Input (V_{EN}) ..... 0V to V_{IN}
Maximum Power Dissipation ..... Note 1

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† Notice: The device is not guaranteed to function outside its operating ratings.

Note 1: $P_{D(MAX)} = (T_{J(MAX)} – T_A)/\theta_{JA}$, where θ_{JA} depends upon the printed circuit layout. See “Applications Information.”

ELECTRICAL CHARACTERISTICS

Electrical Characteristics: $V_{IN} = V_{EN} = 12V$, $V_{BST} – V_{SW} = 5V$; $T_A = +25°C$, $C_{VIN} = C_{VDD} = 1\ \mu F$ unless noted. **Bold** values indicate $–40°C \le T_J \le +125°C$. Specification for packaged product only.

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Power Supply Input						
Input Voltage Range	V_{IN}	4.5	—	28	V	—
Quiescent Supply Current		—	450	750	µA	HSI = V_{DD}, LSI = 0V, R_{DELAY} = 124 kΩ, non-switching
Shutdown Supply Current		—	9	20	µA	V_{EN} = 0V
V_{DD} Supply Voltage						
V_{DD} Output Voltage		**4.8**	5	**5.4**	V	V_{IN} = 7V to 26V, I_{DD} = 25 mA
V_{DD} UVLO Threshold		**3.6**	4.0	**4.4**	V	V_{DD} Rising
V_{DD} UVLO Hysteresis		—	400	—	mV	—
Dropout Voltage ($V_{IN} – V_{DD}$)		—	380	—	mV	I_{DD} = 25 mA, V_{IN}= 5V
V_{DD} Load Regulation		—	1.23	—	%	I_{DD} = 0 mA to 25 mA
Enable Control						
EN Logic Threshold		**0.65**	1.25	**1.4**	V	Rising
EN Hysteresis		—	200	—	mV	—

Note 1: Specified for packaged product only.

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: $V_{IN} = V_{EN} = 12V$, $V_{BST} – V_{SW} = 5V$; $T_A = +25°C$, $C_{VIN} = C_{VDD} = 1\ \mu F$ unless noted. **Bold** values indicate $–40°C \le T_J \le +125°C$. Specification for packaged product only.

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
EN Input Bias Current		—	—	**2**	µA	V_{EN} = 12V
Fault						
Fault Overtemperature		—	150	—	°C	T_J rising
Overtemperature Hysteresis		—	23	—	°C	—
FAULT Logic Level Low		—	0.125	**0.2**	V	I_{FAULT} = 5 mA
FAULT Pin Leakage Current		—	0.01	**0.1**	µA	V_{FAULT} = 5.5V
Input Control						
HSI Logic Level High		**1.4**	—	—	V	—
HSI Logic Level Low		—	—	**0.65**	V	—
HSI Bias Current		—	0.01	**0.1**	µA	V_{HSI} = 5V
LSI Logic Level High		**1.4**	—	—	V	—
LSI Logic Level Low		—	—	**0.65**	V	—
LSI Bias Current		—	0.01	**0.1**	µA	V_{LSI} = 5V
Timing						
Dead Time		—	18.7	—	ns	R_{DELAY} = 105 kΩ
Switching Frequency Range		—	—	1.5	MHz	—
Minimum Allowable Pulse Width		—	32	—	ns	—
Rise Time (DH, DL)	t_r	—	15	—	ns	C_{LOAD} = 3 nF, 10%V_{DD} to 90%V_{DD}
Fall Time (DH,DL)	t_f	—	13.5	—	ns	C_{LOAD} = 3 nF, 10%V_{DD} to 90%V_{DD}
Propagation Delay, Rising HSI to DH		—	26	—	ns	GND to 10%xV_{DD}
Propagation Delay, Rising LSI to DL		—	18	—	ns	GND to 10%xV_{DD}
Propagation Delay, Falling HSI to DH		—	55	—	ns	V_{DD} to 90%xV_{DD}
Propagation Delay, Falling LSI to DL		—	14	—	ns	V_{DD} to 90%xV_{DD}
MOSFET Drivers						
DH $R_{DS(ON)}$, High		—	2	3	Ω	I_{DH} = 20 mA
DH $R_{DS(ON)}$, Low		—	1.5	3	Ω	I_{DH} = –20 mA
DL $R_{DS(ON)}$, High		—	2	3	Ω	I_{DL} = 20 mA
DL $R_{DS(ON)}$, Low		—	1	2	Ω	I_{DL} = –20 mA

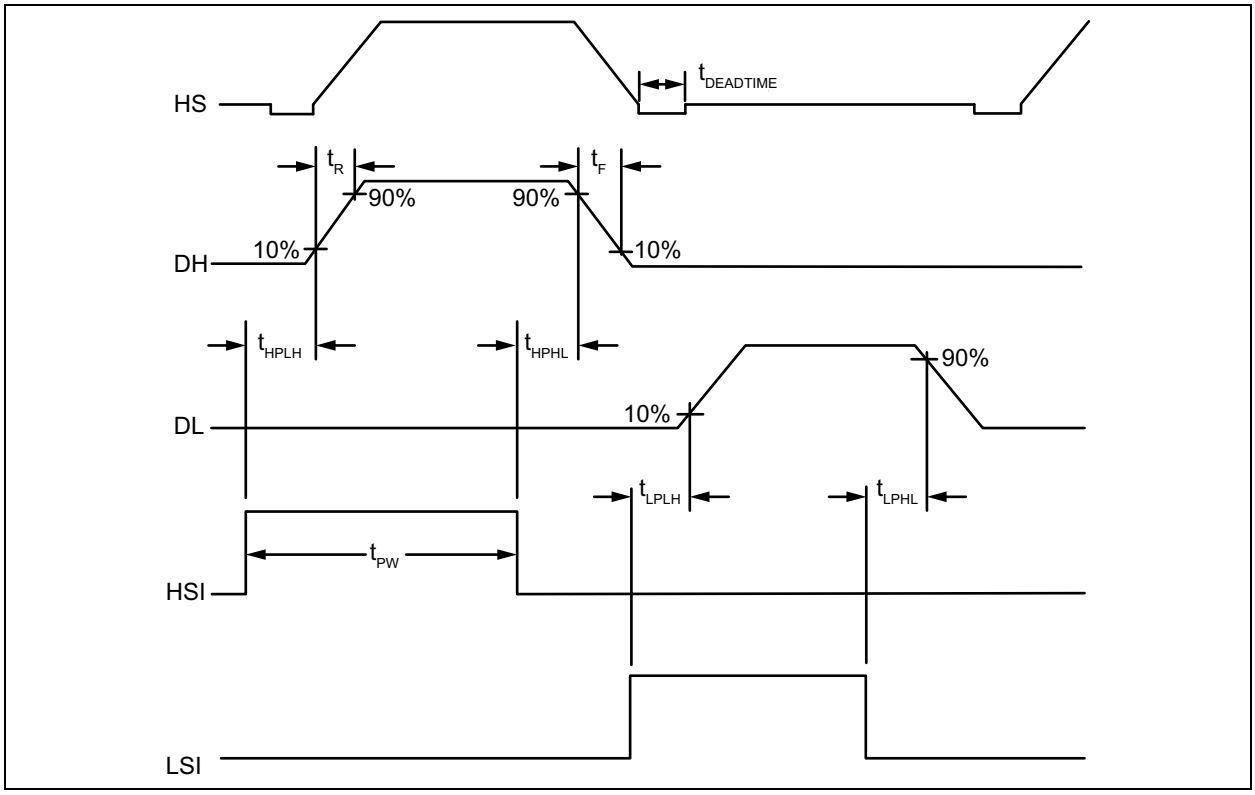
Note 1: Specified for packaged product only.

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Maximum Junction Temperature	T_J	—	—	+150	°C	—
Lead Temperature	—	—	—	+260	°C	Soldering, 10 sec.
Junction Operating Temperature	T_J	–40	—	+125	°C	—
Storage Temperature Range	—	–65	—	+150	°C	—
Package Thermal Resistance						
Thermal Resistance, 3x3 QFN-16Ld	θ_{JA}	—	59	—	°C/W	—

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

Timing Diagram



2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Unless otherwise indicated, V_{IN} = 12V.

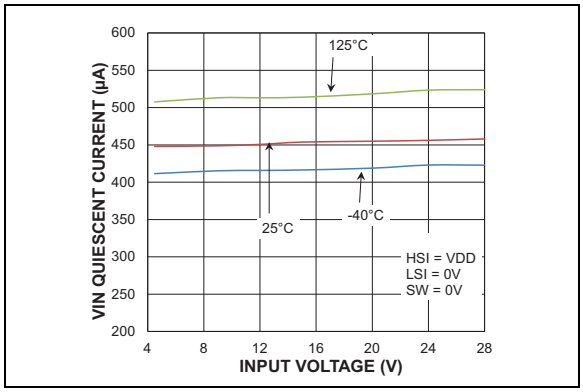


FIGURE 2-1: *VIN Quiescent Current vs. Input Voltage.*

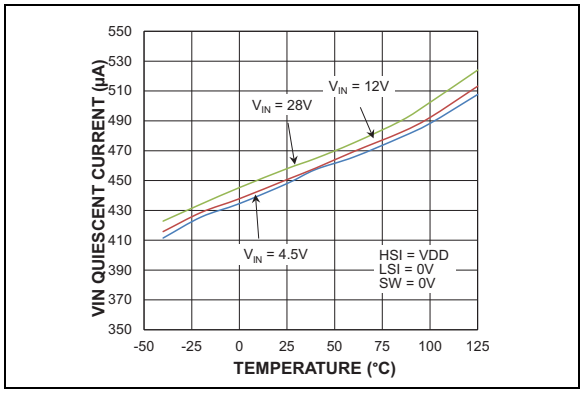


FIGURE 2-2: *VIN Quiescent Current vs. Temperature.*

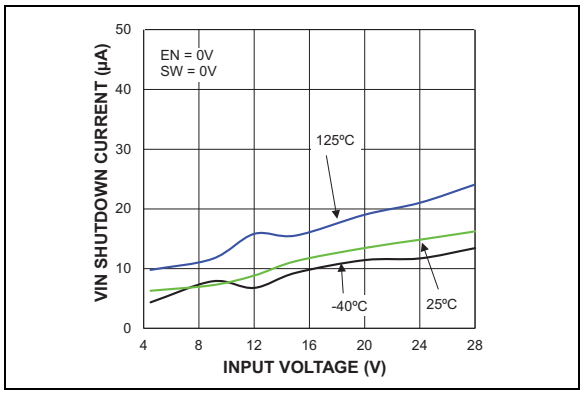


FIGURE 2-3: *VIN Shutdown Current vs. Input Voltage.*

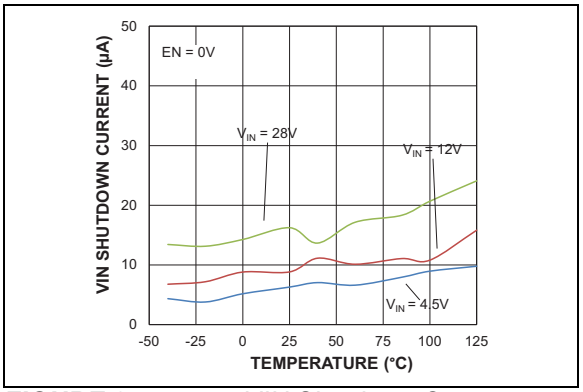


FIGURE 2-4: *VIN Shutdown Current vs. Temperature.*

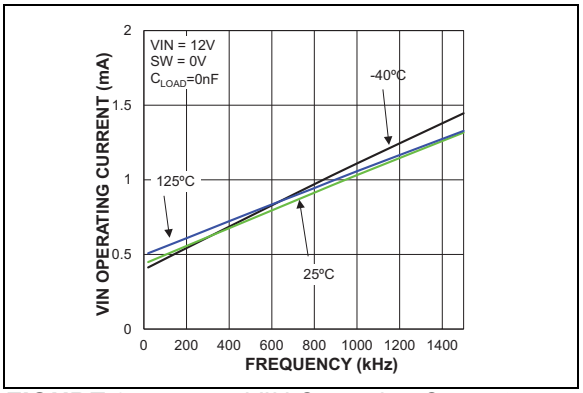


FIGURE 2-5: *VIN Operating Current vs. Frequency.*

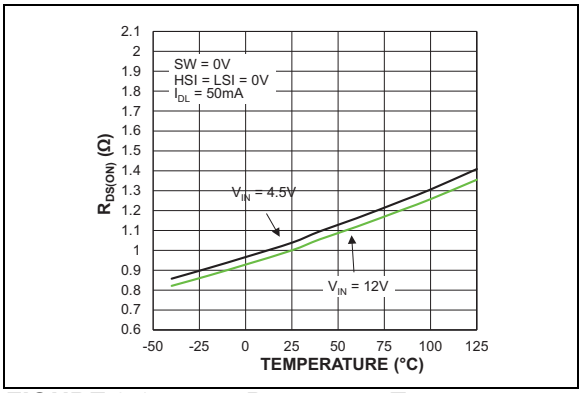


FIGURE 2-6: *$R_{DS(ON)}$ vs. Temperature.*

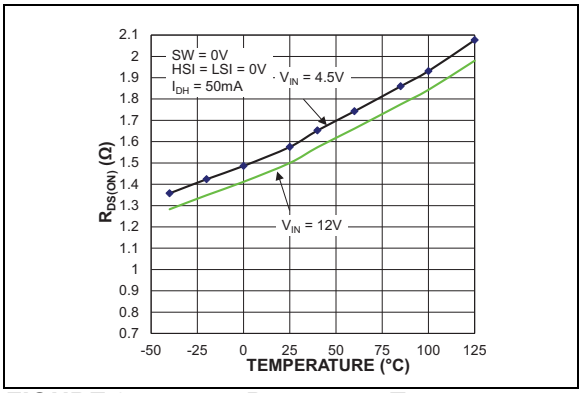


FIGURE 2-7: *$R_{DS(ON)}$ vs. Temperature.*

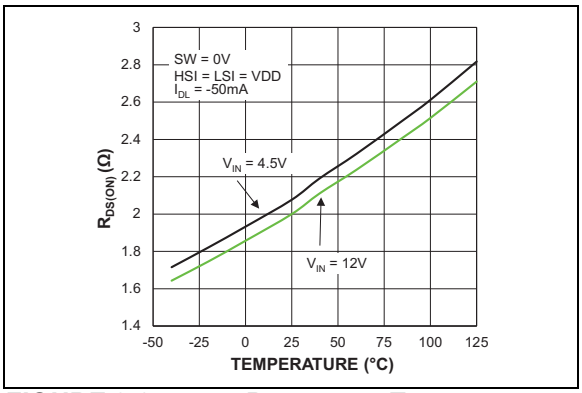


FIGURE 2-8: *$R_{DS(ON)}$ vs. Temperature.*

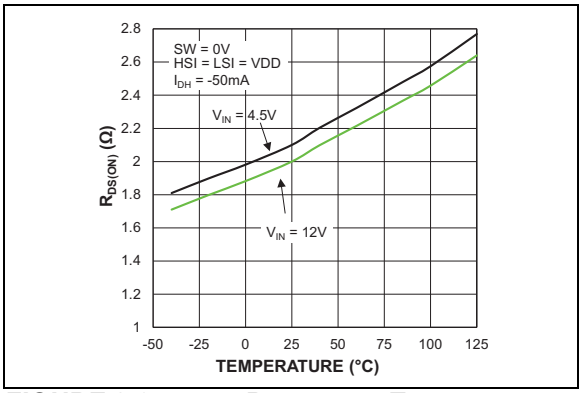


FIGURE 2-9: *$R_{DS(ON)}$ vs. Temperature.*

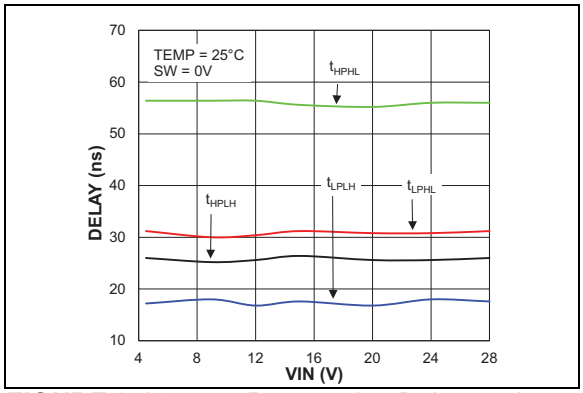


FIGURE 2-10: *Propagation Delay vs. Input Voltage.*

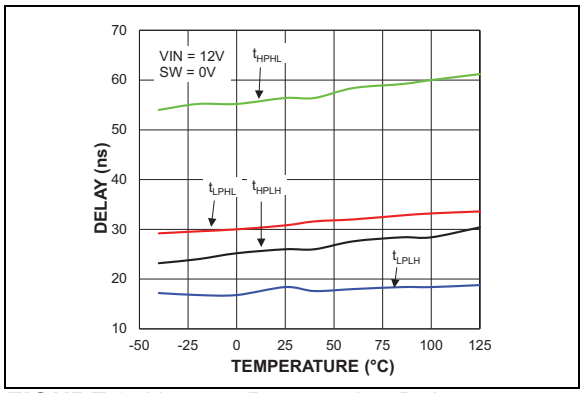


FIGURE 2-11: *Propagation Delay vs. Temperature.*

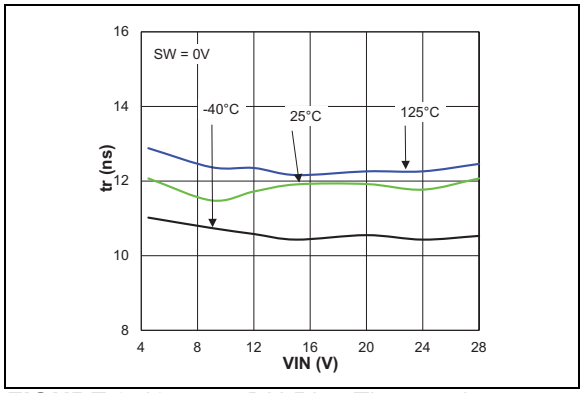


FIGURE 2-12: *DH Rise Time vs. Input Voltage.*

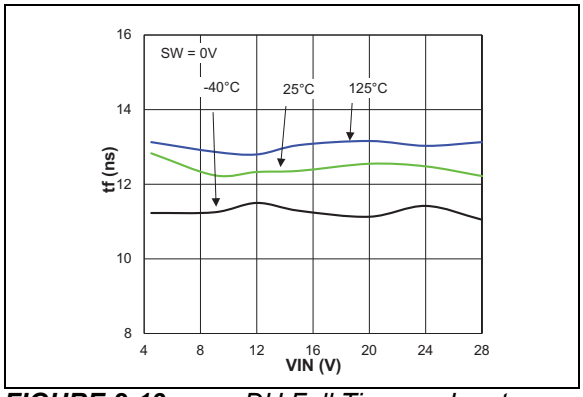


FIGURE 2-13: *DH Fall Time vs. Input Voltage.*

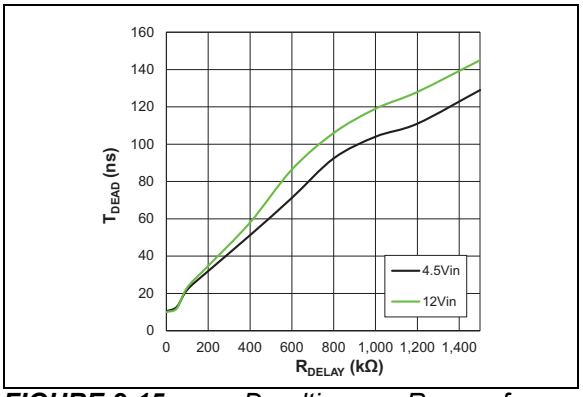


FIGURE 2-15: *Deadtime vs. R_{DELAY} for DH↓ to DL↑.*

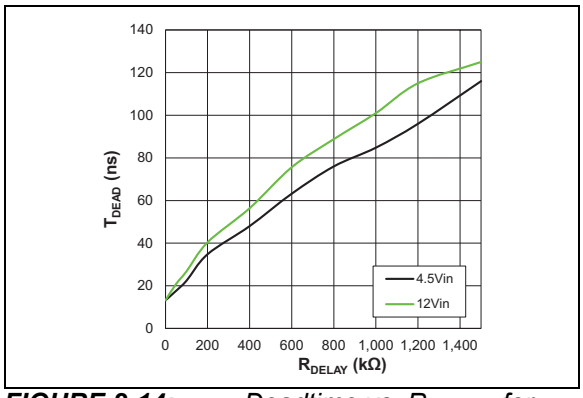


FIGURE 2-14: *Deadtime vs. R_{DELAY} for DL↓ to DH↑.*

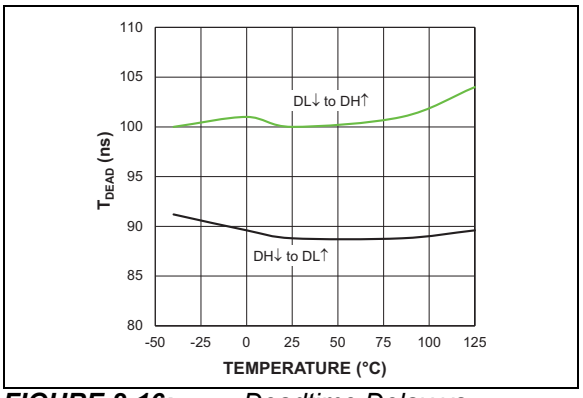


FIGURE 2-16: *Deadtime Delay vs. Temperature.*

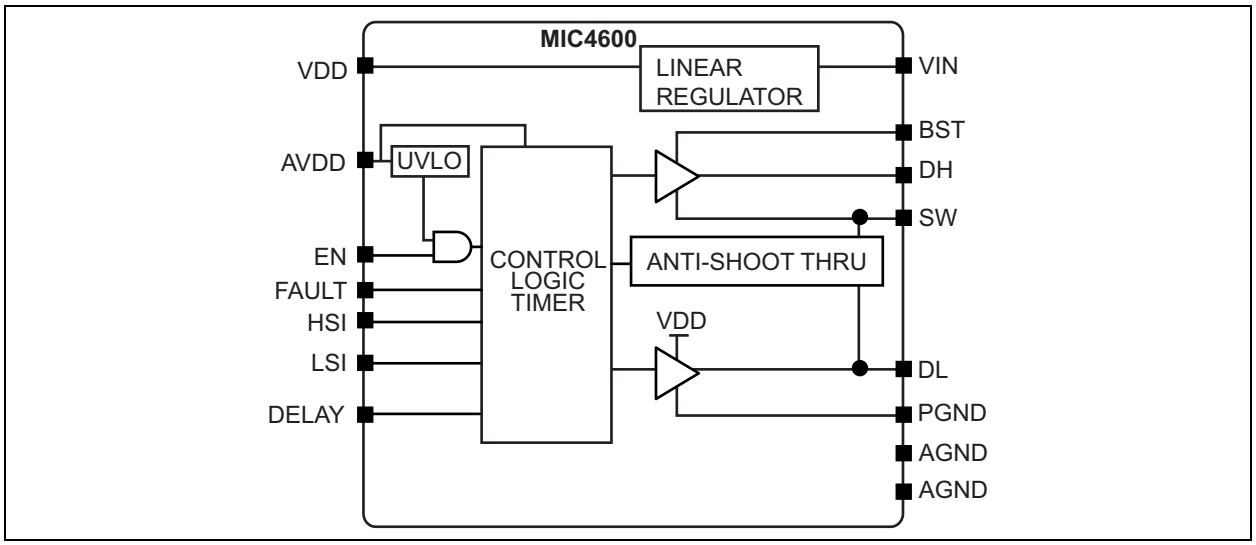
3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	VIN	VIN Supply (Input): Input supply to the internal LDO. The V_{IN} operating voltage range is from 4.5V to 28V. Connect a decoupling capacitor between this pin and PGND.
2	EN	Enable (Input): A logic level high allows normal operation. A logic level low on this pin shuts down the drive in a low quiescent current state. The EN pin must not be left floating.
3	HSI	High-side input (input): A logic level input that controls the high-side gate drive.
4	LSI	Low-side input (input): A logic level input that controls the low-side gate drive.
5	NC	No Connect. Not internally connected.
6	FAULT	FAULT (Output). The active-low, open-drain output pulls low during an overtemperature fault. A resistor to VDD is needed to pull this signal high.
7	DELAY	Delay (Output). Connect a resistor from this pin to ground to adjust the dead time (break before make).
8, 16	AGND	Analog ground. AGND must be connected directly to the ground planes. Do not route the AGND pin to the PGND Pad on the top layer.
9	PGND	Power Ground. PGND is the ground path for the MIC4600 output drivers. The PGND pin should be connected to the source of low-side N-Channel MOSFET and the negative terminals of decoupling capacitors.
10	DL	Drive Low (Output). Low-side MOSFET gate driver.
11	SW	Switch Node (Output): Internal connection for the high-side MOSFET source and low-side MOSFET drain. Due to the high speed switching on this pin, the SW pin should be routed away from sensitive nodes.
12	DH	Drive High (Output). High-side MOSFET gate driver.
13	BST	Boost (output): Bootstrapped voltage to the high-side N-channel MOSFET driver. Connect a Schottky diode between the VDD pin and the BST pin. Connect a boost capacitor between the BST pin and the SW pin.
14	VDD	5V Internal Linear Regulator (Output): VDD supplies the power MOSFET gate drive supply voltage. VDD is created by internal LDO from VIN. When V_{IN} < +5.5V, VDD should be tied to the VIN pin. A 2.2 µF ceramic capacitor from the VDD pin to ground plane on PCB is required for stability.
15	AVDD	5V Analog Input (Input): AVDD is the supply for the internal driver logic and control circuitry. Connect the VDD output to the AVDD pin.
EPAD	ePad	Exposed thermal pad. Connect to the ground plane for optimum thermal performance.

4.0 FUNCTIONAL DESCRIPTION



The MIC4600 is a 28V half-bridge MOSFET driver with integrated LDO. It is designed to independently drive both high-side and low-side N-Channel MOSFETs. The LDO eliminates the need for a second V_{DD} supply voltage by generating the gate drive voltage from the input supply. The MIC4600 offers a wide 4.5V to 28V operating supply range. Refer to the diagram above.

The high and low-side drivers contain an input buffer with hysteresis and an output buffer. The high-side output buffer includes a high-speed level-shifting circuit that is referenced to the HS pin. An external diode is used to supply V_{DD} to the bootstrap circuit that provides the drive voltage for the high-side output.

4.1 Startup and UVLO

The UVLO circuit monitors V_{DD} and inhibits both drivers in a low state when the supply voltage is below the UVLO threshold. Hysteresis in the UVLO circuit prevents noise and circuit impedance from causing chatter during turn-on.

4.2 Enable Input

A logic high on the enable pin (EN) allows normal operation to occur. Conversely, when a logic low is applied on the enable pin, the high and low-side driver outputs turn-off and the driver enters a low supply current shutdown mode. Do not leave floating.

4.3 Dead-Time Delay

Shoot-through occurs in a half-bridge or synchronous buck topology when both the high and low-side MOSFETs conduct at the same time. This condition is caused by driver propagation delay variation and MOSFET turn on/off times. Shoot-through causes an increase in MOSFET power dissipation, circuit noise, and interference with power circuit operation. A resistor on the DELAY pin sets the break-before-make delay time between the high- and low-side MOSFETs. See the Applications section for additional information.

4.4 Input Stage

Both the HSI and LSI pins are referenced to the AGND pin. The voltage state of the input signal does not change the quiescent current draw of the driver.

The MIC4600 has a TTL-compatible input range and can be used with input signals with amplitude less than or equal to the V_{DD} voltage. A small amount of hysteresis improves the noise immunity of the driver inputs.

4.5 Low-Side Driver

Figure 4-1 shows a block diagram of the low-side driver. The low-side driver is designed to drive a ground (PGND pin) referenced N-channel MOSFET. The low-side gate drive voltage equals V_{DD}, which is typically 5V.

A low driver impedance allows the external MOSFET to be turned on and off quickly. The rail-to-rail drive capability of the output ensures a low $R_{DS(ON)}$ from the external MOSFET.

A high level applied to the LSI pin causes the upper driver MOSFET to turn on and V_{DD} voltage is applied to the gate of the external MOSFET. A low level on the LSI pin turns off the upper driver and turns on the low-side driver to ground the gate of the external MOSFET.

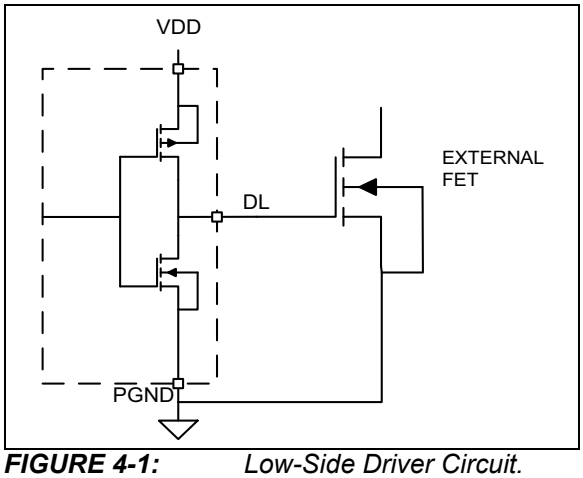


FIGURE 4-1: *Low-Side Driver Circuit.*

4.6 High-Side Driver and Bootstrap Circuit

A block diagram of the high-side driver and bootstrap circuit is shown in Figure 4-2. This driver is designed to drive a floating N-channel MOSFET, whose source terminal is referenced to the SW pin. The output voltage of the DH pin equals V_{DD} minus the external bootstrap diode forward voltage drop. The high-side gate drive voltage is typically 4.5V.

A low-power, high-speed, level-shifting circuit isolates the low side (AGND pin) referenced circuitry from the high-side (SW pin) referenced driver. Power to the high-side driver is supplied by the bootstrap circuit.

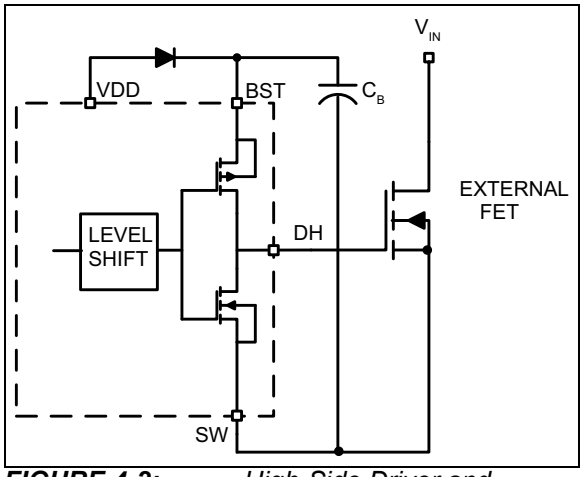


FIGURE 4-2: *High-Side Driver and Bootstrap Circuit.*

The bootstrap circuit consists of an external diode and external capacitor, C_B. In a typical application, such as the synchronous buck converter shown in Figure 4-3, the SW pin is at ground potential while the low-side MOSFET is on. During this time, the diode allows capacitor C_B to charge up to $V_{DD} – V_F$ (where V_F is the forward voltage drop of the diode). After the low-side MOSFET is turned off and the DH pin goes high, the voltage across capacitor C_B is applied to the gate of the upper external MOSFET. As the upper MOSFET turns on, voltage on the SW pin rises with the source of the high-side MOSFET until it reaches V_{IN}. As the SW and BST pins rise, the diode is reverse biased preventing capacitor C_B from discharging.

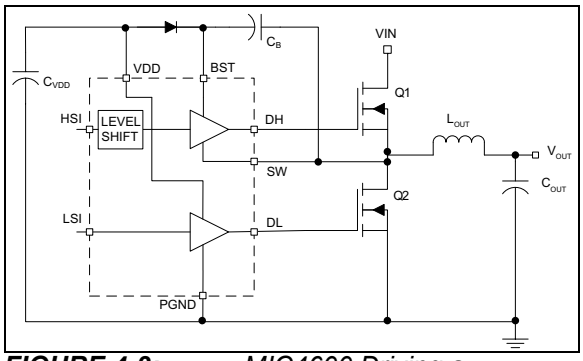


FIGURE 4-3: *MIC4600 Driving a Synchronous Buck Converter.*

4.7 Overtemperature Indicator

If the die exceeds the high temperature threshold (Fault Overtemperature), the FAULT pin is asserted low, while the outputs remain unchanged and still follow the inputs. The low level on the Fault pin simply indicates the need for thermal management, potentially requiring the inputs to be pulled low, and the FAULT pin is deasserted, when the die temperature cools below the lower threshold, set by the circuit's hysteresis. If resumed operation results in reheating of the die above the high threshold, another shutdown cycle occurs.

As long as ENABLE is high and V_{IN} is greater than +5.5V, the internal LDO remains on even when the FAULT pin is asserted low.

4.8 Fault Pin

The FAULT signal is an N-channel open-drain output, which is asserted low when the MIC4600 enters an overtemperature condition.

5.0 APPLICATION INFORMATION

5.1 Adjustable Dead Time

Dead-time control prevents shoot-through current from flowing through the external power MOSFETs during switching transitions. The delay allows enough time for the high-side driver to turn off before the low-side driver turns on. It also prevents the high-side driver from turning on before the low-side driver has turned off.

The dead time between the high- and low-side MOSFETs can be adjusted with a resistor on the DELAY pin. The dead time can be approximated with the formula below. See the Typical Performance Curves for a more precise determination of R_{DELAY} vs. t_{DEAD}.

EQUATION 5-1:

$$t_{DEAD} = 12 \times 10^{-9} + R_{DELAY} \times 0.9 \times 10^{-10}$$

Where:
t_{DEAD} = The break-before-make delay between the high-side and low-side gate drive signals.
R_{DELAY} = The DELAY pin resistance in kΩ.

5.2 Other Timing Considerations

Make sure the input signal pulse width is greater than the minimum specified pulse width. An input signal that is less than the minimum pulse width may result in no output pulse or an output pulse whose width is significantly less than the input.

The maximum duty cycle (ratio of high-side on-time to switching period) is controlled by the minimum pulse width of the low-side and by the time required for the C_B capacitor to charge during the off-time. Adequate time must be allowed for the C_B capacitor to charge up before the high-side driver is turned on.

5.3 Single Input Operation

Both outputs can be controlled from a single input signal by pulling the LSI input high to V_{DD} and applying the input signal to the HSI pin. In this configuration, the dead-time between the DH and DL transitions is set by the resistor value connected to the DELAY pin.

When the HSI pin goes from a low to a high, the DL pin goes low and the DH pin goes high after the dead time delay. When the HSI pin changes from a high to a low, the DH pin goes low. After the delay time, the DL pin goes high.

5.4 Bootstrap Diode and Capacitor

The gate drive voltage of the high-side driver equals the V_{DD} voltage minus the voltage drop across the bootstrap diode. A Schottky diode is recommended due to the lower forward voltage drop.

Power dissipation in the bootstrap diode can be calculated using the following equations. The average current drawn by repeated charging of the high-side MOSFET is calculated by:

EQUATION 5-2:

$$I_{F(AVE)} = Q_{GATE} \times f_S$$

Where:
Q_{GATE} = Total gate charge at V_{DD}.
f_S = Gate drive switching frequency.

The average power dissipated by the forward voltage drop of the diode equals:

EQUATION 5-3:

$$Pdiode_{FWD} = I_{F(AVE)} \times V_F$$

Where:
V_F = Diode forward voltage drop.

The value of V_F should be taken at the peak current through the diode; however, this current is difficult to calculate because of differences in source impedances. The peak current can either be measured or the value of V_F at the average current can be used, which will yield a good approximation of diode power dissipation.

The voltage on the bootstrap capacitor drops each time it delivers charge to turn on the MOSFET. The voltage drop depends on the gate charge required by the MOSFET. Most MOSFET specifications specify gate charge versus V_{GS} voltage. Based on this information and a suggested capacitor voltage drop of less than 0.1V, the minimum value of bootstrap capacitance is:

EQUATION 5-4:

$$C_B \geq \frac{Q_{GATE}}{\Delta V_{BST}}$$

Where:
Q_{GATE} = Total gate charge at V_{DD}.
ΔV_{BST} = Voltage drop at the BST pin.

5.5 Power Dissipation Considerations

Power dissipation in the driver can be separated into two areas:

- Quiescent current dissipation
- Internal driver dissipation

5.6 Quiescent Current Power Dissipation

Power is dissipated in the MIC4600 even if nothing is being driven. The quiescent current is drawn by the bias for the internal circuitry and the level shifting circuitry. The quiescent current is proportional to operating frequency. The typical characteristic graphs show how quiescent current varies with switching frequency.

The power dissipated due to quiescent current is calculated by:

EQUATION 5-5:

$$P_{DISS\_IQ} = V_{DD} \times I_{DD}$$

5.7 Gate Driver Power Dissipation

Power dissipation in the output driver stage is mainly caused by charging and discharging the gate to source and gate to drain capacitance of the external MOSFET. Figure 5-1 shows a simplified equivalent circuit of the MIC4600 driving an external high-side MOSFET.

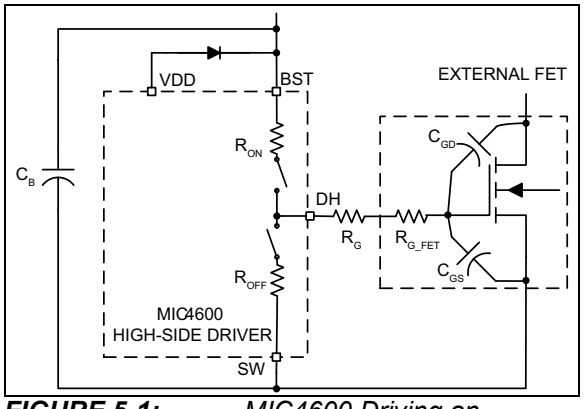


FIGURE 5-1: *MIC4600 Driving an External MOSFET.*

5.7.1 DISSIPATION DURING THE EXTERNAL MOSFET TURN-ON

Energy from capacitor C_B is used to charge up the input capacitance of the MOSFET (C_{GD} and C_{GS}). The energy delivered to the MOSFET is dissipated in the three resistive components, R_{ON}, R_G, and R_{G_FET}. R_{ON} is the on-resistance of the upper driver MOSFET in the MIC4600. R_G is the series resistor (if any) between the driver IC and the MOSFET. R_{G_FET} is the gate resistance of the MOSFET. R_{G_FET} is usually listed in the power MOSFET's specifications. The ESR of capacitor C_B and the resistance of the connecting etch can be ignored because they are much less than R_{ON} and R_{G_FET}.

The effective capacitances of C_{GD} and C_{GS} are difficult to calculate because they vary non-linearly with Id, V_{GS}, and V_{DS}. Fortunately, most power MOSFET specifications include a typical graph of total gate charge vs. V_{GS}. Figure 5-2 is a typical gate charge curve for a power MOSFET. This chart shows that for a gate voltage of 4.5V, the MOSFET gate is charged up to 25 nC of total gate charge. The energy dissipated by the resistive components of the gate drive circuit during turn-on is calculated as noted in Equation 5-6.

EQUATION 5-6:

$$E = \frac{1}{2} \times C_{ISS} \times V_{GS}^{2}$$

but

$$Q = C \times V$$

so

$$E = \frac{1}{2} \times Q_G \times V_{GS}$$

Where:
C_{ISS} = Total gate capacitance of the MOSFET.

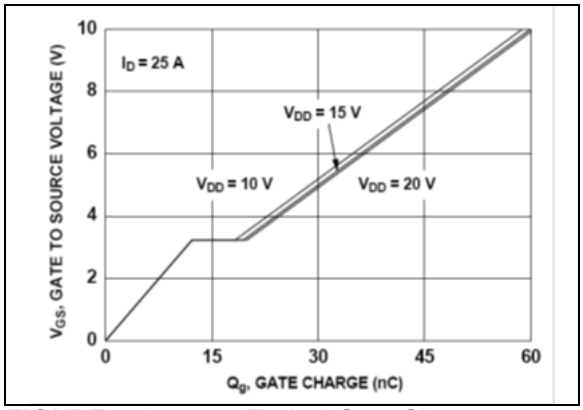


FIGURE 5-2: *Typical Gate Charge vs. V_{GS}.*

The same energy is dissipated by R_{OFF}, R_G, and R_{G_FET} when the driver IC turns the MOSFET off. Assuming R_{ON} is approximately equal to R_{OFF}, the total energy and power dissipated by the resistive drive elements is illustrated in Equation 5-7:

EQUATION 5-7:

$$E_{DRIVER} = Q_G \times V_{GS}$$

and

$$P_{DRIVER} = Q_G \times V_{GS} \times f_S$$

Where:
E_{DRIVER} = Energy dissipated per switching cycle.
P_{DRIVER} = Power dissipated per switching cycle.
Q_G = Total gate charge at V_{GS}.
V_{GS} = Gate to source voltage on the MOSFET.
f_S = Switching frequency of the gate drive circuit.

The power dissipated inside the driver is equal to the ratio of R_{ON} and R_{OFF} to the external resistive losses in R_G and R_{G_FET}. Letting R_{ON} = R_{OFF}, the power dissipated in the MIC4600 due to driving the external MOSFET is illustrated in Equation 5-8:

EQUATION 5-8:

$$P_{DISSDRIVER} = P_{DRIVER} \times \frac{R_{ON}}{R_{ON} + R_G + R_{G\_FET}}$$

5.8 Total Power Dissipation and Thermal Considerations

Total power dissipation in the MIC4600 is equal to the power dissipation caused by driving the external MOSFETs and the quiescent current.

EQUATION 5-9:

$$P_{DISSTOTAL} = P_{DISSIQ} + P_{DISSDRIVE}$$

The die temperature can be calculated after the total power dissipation is known, as in Equation 5-10:

EQUATION 5-10:

$$T_J = T_A + P_{DISSTOTAL} \times \theta_{JA}$$

Where:
T_A = Maximum ambient temperature.
T_J = Junction temperature.
$P_{DISSTOTAL}$ = Power dissipation of the MIC4600.
θ_{JA} = Thermal resistance from junction to ambient air.

5.9 Decoupling and Bootstrap Capacitor Selection

Decoupling capacitors are required for both the low-side (VDD) and high-side (BST) supply pins. These capacitors supply the charge necessary to drive the external MOSFETs and also minimize the voltage ripple on these pins. The capacitor from BST to SW has two functions: it provides decoupling for the high-side driver and is the supply voltage to the high-side circuit while the external MOSFET is on. Ceramic capacitors are recommended because of their low impedance and small size. Z5U type ceramic capacitor dielectrics are not recommended because of the large change in capacitance overtemperature and voltage. A minimum value of 0.1 µF is required for each of the capacitors, regardless of the MOSFETs being driven. Larger MOSFETs may require larger capacitance values for proper operation.

Placement of the decoupling capacitors is critical. The bypass capacitor for VDD should be placed as close as possible between the VDD and PGND pins. The bypass capacitor (C_B) for the BST supply pin must be located as close as possible between the BST and SW pins. The etch connections must be short, wide, and direct. The use of a ground plane to minimize connection impedance is recommended (refer to the following section for more information).

5.10 Grounding, Component Placement, and Circuit Layout

Nanosecond switching speeds and ampere peak currents in and around the MIC4600 drivers require proper placement and trace routing of all components. Improper placement may cause degraded noise immunity, false switching, excessive ringing, or circuit latch-up.

Figure 5-3 shows the critical current paths when the driver outputs go high and turn on the external MOSFETs. It also helps demonstrate the need for a low impedance ground plane. Charge needed to turn-on the MOSFET gates comes from the decoupling

capacitors C_{VDD} and C_B. Current in the low-side gate driver flows from C_{VDD} through the internal driver, into the MOSFET gate, and out the source. The return connection back to the decoupling capacitor is made through the ground plane. Any inductance or resistance in the ground return path causes a voltage spike or ringing to appear on the source of the MOSFET. This voltage works against the gate drive voltage and can either slow down or turn off the MOSFET during the period when it should be turned on.

Current in the high-side driver is sourced from capacitor C_B and flows into the BST pin and out the DH pin, into the gate of the high side MOSFET. The return path for the current is from the source of the MOSFET and back to capacitor C_B. The high-side circuit return path usually does not have a low-impedance ground plane so the etch connections in this critical path should be short and wide to minimize parasitic inductance. As with the low-side circuit, impedance between the MOSFET source and the decoupling capacitor causes negative voltage feedback that fights the turn-on of the MOSFET.

It is important to note that capacitor C_B must be placed close to the BST and SW pins. This capacitor not only provides all the energy for turn-on but it must also keep HB pin noise and ripple low for proper operation of the high-side drive circuitry.

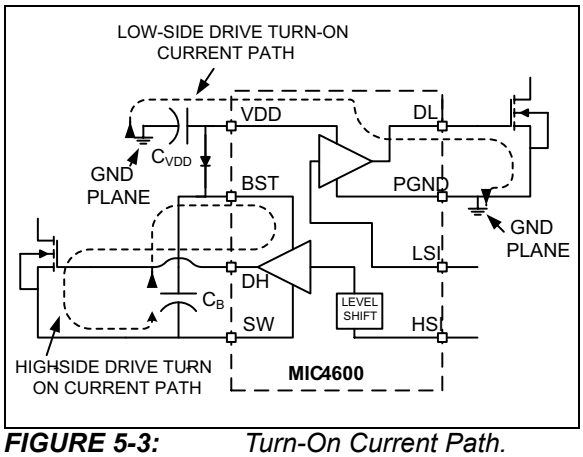


FIGURE 5-3: *Turn-On Current Path.*

Figure 5-4 shows the critical current paths when the driver outputs go low and turn off the external MOSFETs. Short, low-impedance connections are important during turn-off for the same reasons given in the turn-on explanation. Current flowing through the internal diode replenishes charge in the bootstrap capacitor, C_{BST}.

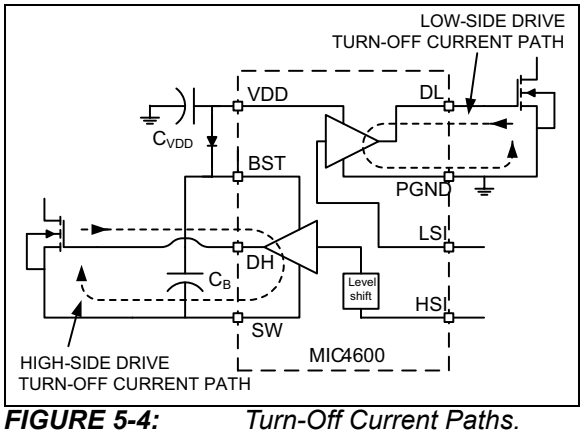


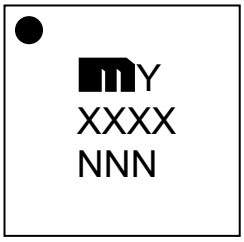
FIGURE 5-4: *Turn-Off Current Paths.*

Use a ground plane to minimize parasitic inductance and impedance of the return paths. The MIC4600 is capable of greater than 1A peak currents and any impedance between the MIC4600, the decoupling capacitors, and the external MOSFET will degrade the performance of the driver.

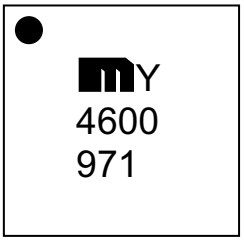
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

16-Lead QFN*



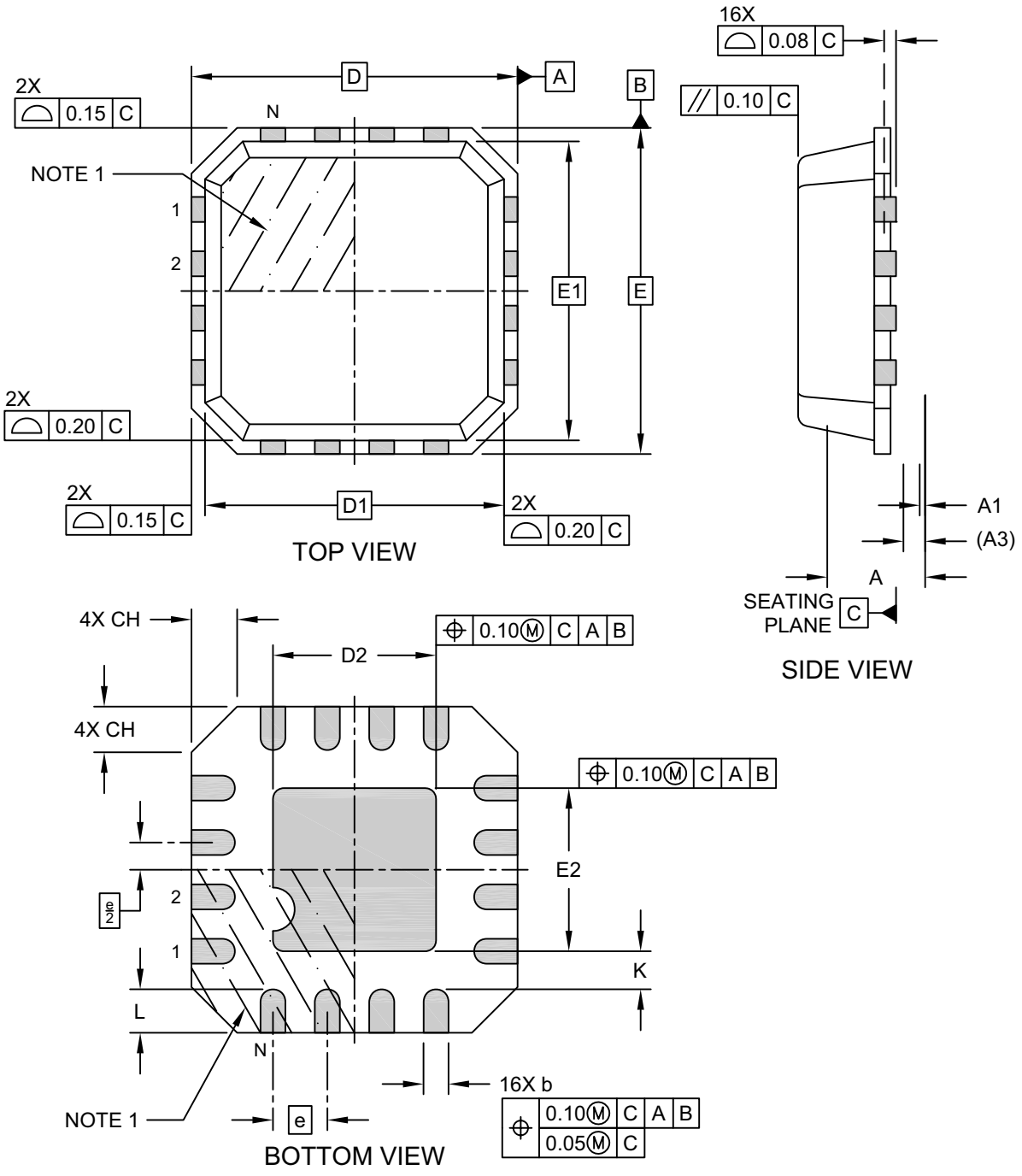
Example



Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar (_) and/or Overbar (¯) symbol may not be to scale.	

16-Lead Ultra Thin Plastic Quad Flat, No Lead Package (NCA) - 3x3x1.0 mm Body [VQFN]

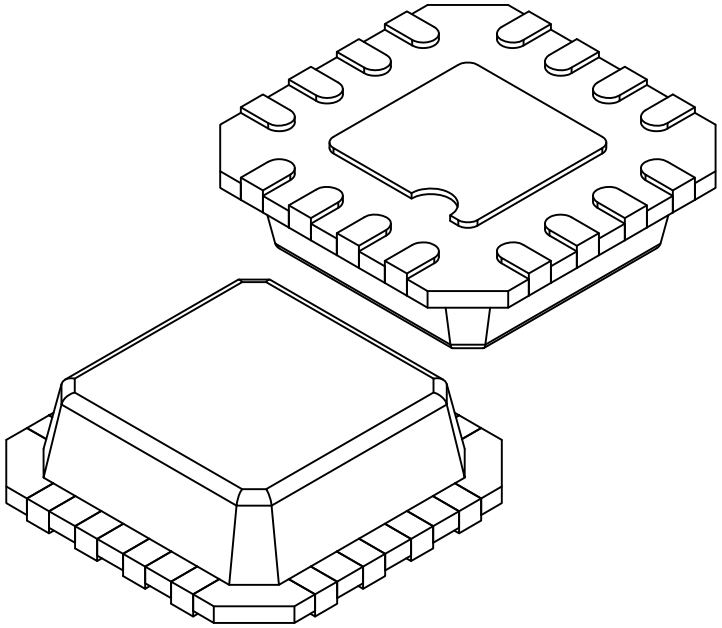
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-1103-NCA Rev A Sheet 1 of 2

16-Lead Ultra Thin Plastic Quad Flat, No Lead Package (NCA) - 3x3x1.0 mm Body [VQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		16	
Pitch	e		0.50 BSC	
Overall Height	A	0.85	-	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Length	D		3.00 BSC	
Mold Cap Length	D1		2.75 BSC	
Exposed Pad Length	D2	1.35	1.50	1.65
Overall Width	E		3.00 BSC	
Mold Cap Width	E1		2.75 BSC	
Exposed Pad Width	E2	1.35	1.50	1.65
Body Corner Chamfer	CH	0.24	0.42	0.60
Terminal Width	b	0.16	0.23	0.28
Terminal Length	L	0.10	0.40	0.50
Terminal-to-Exposed-Pad	K	0.20	-	-

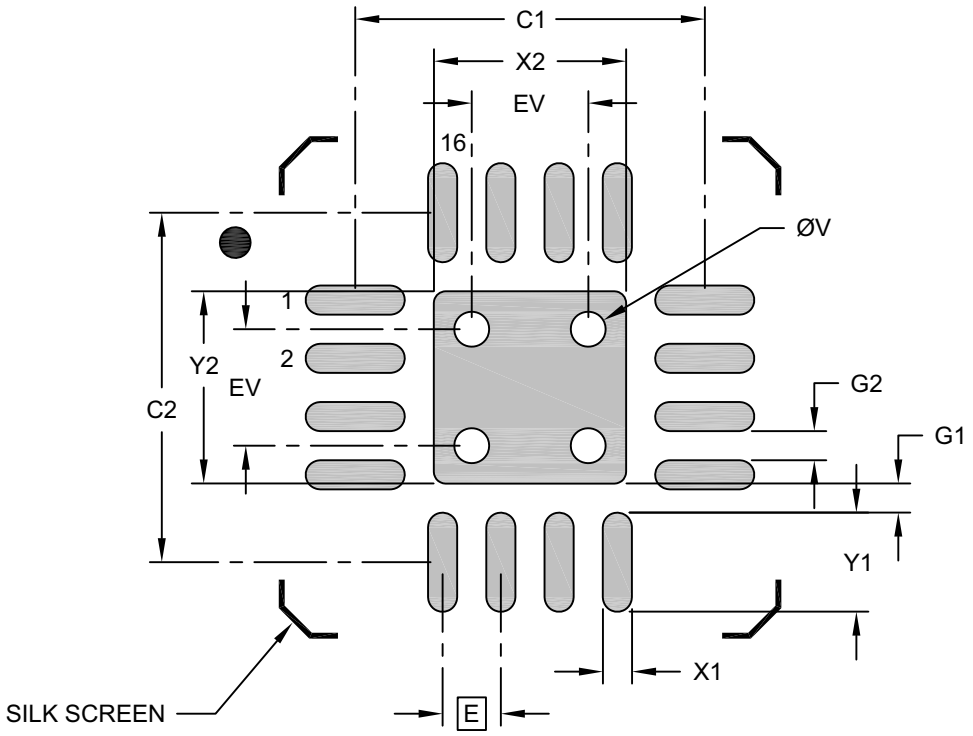
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is punch singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1103-NCA Rev A Sheet 1 of 2

16-Lead Ultra Thin Plastic Quad Flat, No Lead Package (NCA) - 3x3x1.0 mm Body [VQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			1.65
Optional Center Pad Length	Y2			1.65
Contact Pad Spacing	C1		3.00	
Contact Pad Spacing	C2		3.00	
Contact Pad Width (x16)	X1			0.25
Contact Pad Length (x16)	Y1			0.85
Contact Pad to Center Pad (x16)	G1	0.25		
Contact Pad to Contact Pad (X12)	G2	0.25		
Thermal Via Diameter	V		0.30	
Thermal Via Pitch	EV		1.00	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-1103-NCA Rev A

NOTES:

APPENDIX A: REVISION HISTORY

Revision B (November 2020)

The following is the list of modifications:

- Updates to the Electrical Characteristics table.
- Updated **Section 4.7 "Over-Temperature Indicator"** and **Section 4.8 "Fault Pin"**.

Revision A (July 2016)

- Converted Micrel document MIC4600 to Microchip data sheet template DS20005584A.
- •Minor text changes throughout.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	X	XX	—	XX
Device	Temperature Range	Package		Media Type

Device:	MIC4600:	28V Half-Bridge MOSFET Driver	
Temperature Range:	Y	=	–40°C to +125°C (RoHS Compliant)
Package:	NCA	=	16-Lead 3x3 VQFN
Media Type:	T5	=	500/Reel
	TR	=	5000/Reel

Examples:

a) MIC4600YML-T5: 28V Half-Bridge MOSFET Driver, Two independent TTL inputs, –40°C to +125°C Temp. Range, RoHS Compliant, 16LD 3x3 VQFN, 500/Reel

b) MIC4600YML-TR: 28V Half-Bridge MOSFET Driver, Two independent TTL inputs, –40°C to +125°C Temp. Range, RoHS Compliant, 16LD 3x3 VQFN, 5000/Reel

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