Power Loss Protection with 6A eFuse

BENEFITS and FEATURES

Wide 2.7-to-18V Operating Input Range
24V Max Input Blocking Voltage
Adjustable Bus Voltage Start-Up Slew Rate for In-rush Current Control
Configurable Input power Failure Level
Programmable up to 10A Input Current Limit
Programmable 5V to 36V Boost Storage Voltage
36V@6A Synchronous Buck Supports 100% Duty Cycle
Programmable up to 1.13MHz Buck Operating Frequency for Small Inductor Size
Undetectable Transition from Input Supply to Capacitor Bank Power
Compatible with Different Types of Storage Caps: Super Caps, Electrolytic, Tantalum, POSCAP etc.
ADC Monitoring of Critical Signals
Autonomous Health Monitoring for Detection of Earlier Storage Capacitor Failures
Configurable Interrupts to Inform Host for any Faults/Status Change
eFuse, Boost, and Buck UV/OV/OC Protection
Thermal Alert and Protection
Thermal Enhanced FCQFN 5x5-28 package

APPLICATIONS

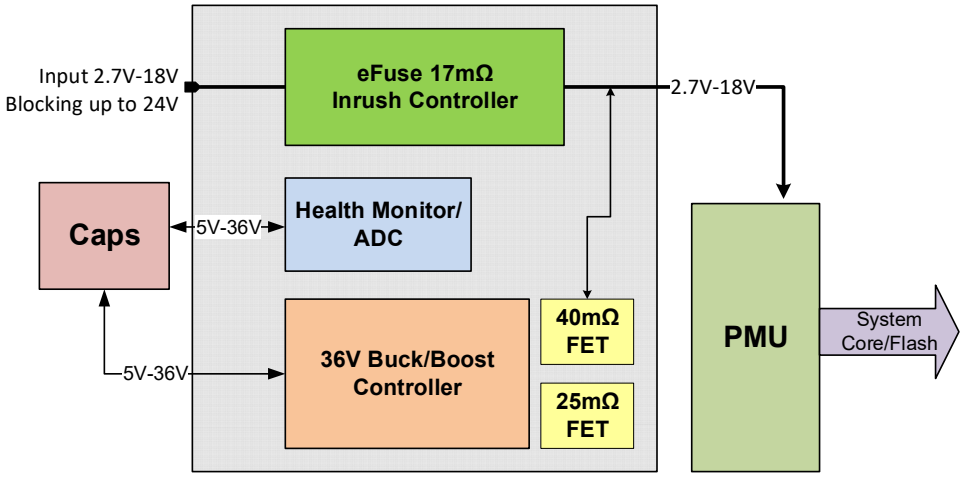
- Solid State Drives
- Industrial Applications
- Backup Power
- Hot Plug Devices

GENERAL DESCRIPTION

The ACT4910 device is a highly integrated power loss protection IC. It provides backup storage power in the event of an input power failure. A built-in boost converter provides high voltage energy storage to minimize storage capacitor size requirements. The built-in buck converter regulates the storage voltage to a fixed output voltage. It contains internal, back-to-back eFuse FETs to provide bi-directional input to output isolation. The IC also provides hot swap and inrush current control.

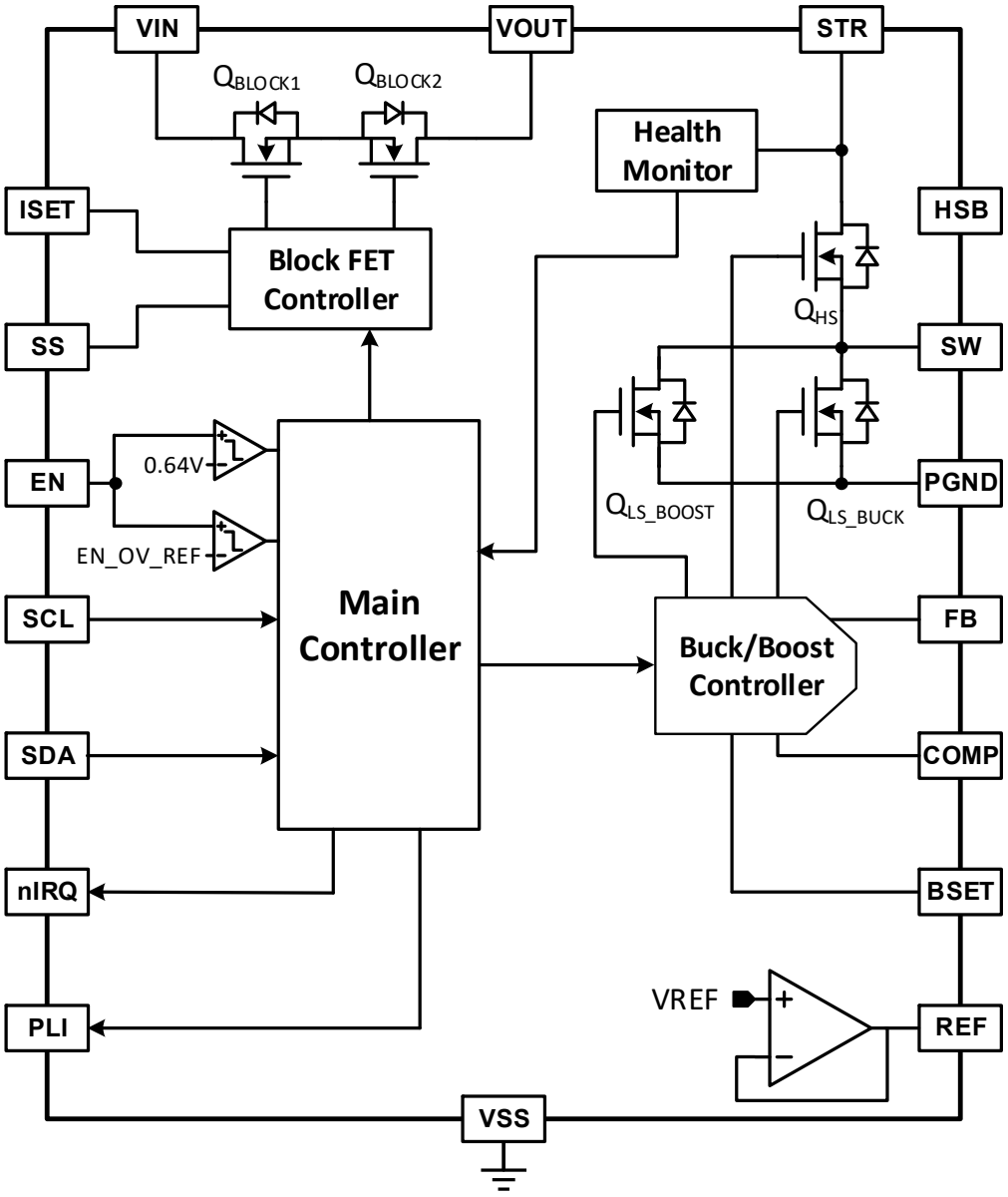
The ACT4910 is very flexible and can easily be configured with I²C and external components. It features programmable storage capacitor voltage to optimize the storage capacitor sizing and system run time. The internal ADC and health monitoring provide an extra layer of protection and improve system reliability and early capacitor failure notification. It automatically checks the storage capacitor health and notifies the user when the energy in the storage caps is not sufficient for backup power. The ADC also measures the input voltage, output voltage, storage voltage, eFuse current, and die temperature. The built-in synchronous buck converter maximizes energy transfer from the storage caps to the system.

ACT4910 provides an I²C bus interface to allow MCU control and monitoring. There are supervisor monitors for the input voltage, output voltage, and storage voltage. It is available with the thermal enhanced QFN 5x5 28 pins package.



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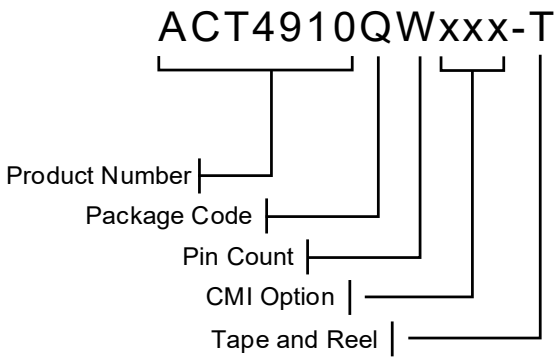
FUNCTIONAL BLOCK DIAGRAM



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ORDERING INFORMATION

PART NUMBER	Input Voltage	Storage Voltage	Fsw	PLI Function	7 Bit I²C Address	PACKAGE
ACT4910QW121-T	12V	28V	1130kHz	PLI & VOUT OK	0x5Ah	FCQFN5x5-28
ACT4910QW122-T	12V	36V	900kHz	PLI & VOUT OK	0x5Ah	FCQFN5x5-28



Note 1: Standard product options are identified in this table. Contact factory for custom options, minimum order quantity required.

Note 2: All Active-Semi components are RoHS Compliant and with Pb-free plating unless specified differently. The term Pb-free means semiconductor products that are in compliance with current RoHS (Restriction of Hazardous Substances) standards.

Note 3: Package Code designator “Q” represents QFN

Note 4: Pin Count designator “W” represents 28 pins

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PIN CONFIGURATION

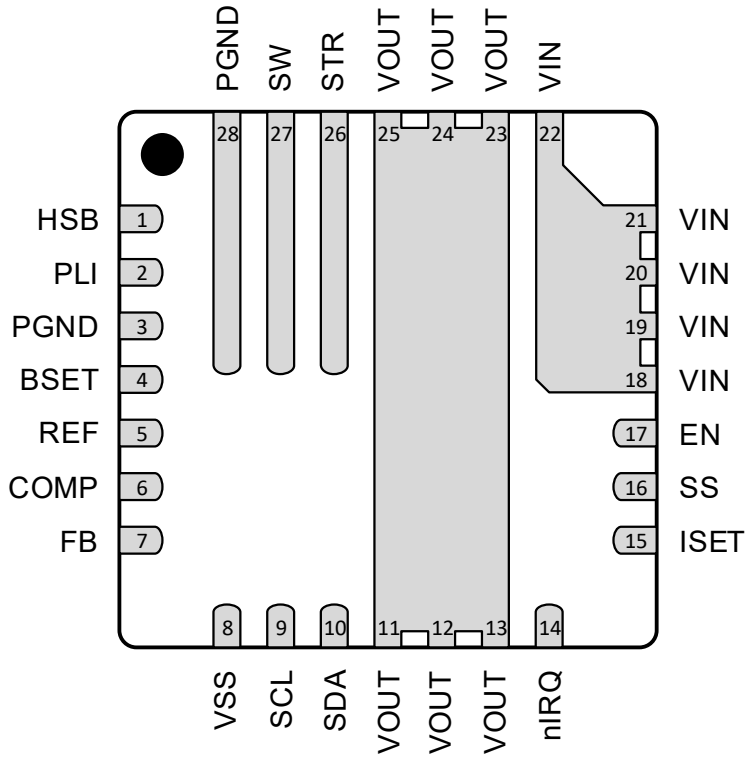


Figure 1: Pin Configuration – Top View – QFN5x5-28

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PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	HSB	High Side Bias, Boot-strap pin. This provides power to the internal high-side MOSFET gate driver circuitry. Connect a 47nF capacitor from HSB pin to SW pin
2	PLI	Power Loss Indicator Open-Drain Output. PLI goes low to indicate loss of input power. Can also be configured as a storage voltage monitor or an output voltage monitor. PLI is referenced to VSS.
3, 28	PGND	Power Ground. Connect to large ground plane on PCB
4	BSET	Sets the storage capacitor voltage. Place a resistor from BSET to VSS to set the desired voltage.
5	REF	Internal Bias Voltage Output. Connect a 1μF capacitor between REF and VSS.
6	COMP	Compensation input pin for the buck converter.
7	FB	Output Voltage Feedback. Kelvin connect FB to the output capacitor.
8	VSS	Analog Ground. Kelvin connect VSS to the PGND plane.
9	SCL	I^2C Clock Input. Needs an external pull up resistor.
10	SDA	I^2C Data Input and Output. Needs an external pull up resistor.
11,12,13,23, 24, 25	VOUT	Output for by-pass mode, in-rush, and eFuse functionality. Connect VOUT to the system load.
14	nIRQ	Interrupt Open-Drain Output. nIRQ goes low to indicate a fault condition. nIRQ is referenced to VSS.
15	ISET	Input and Output Current Limit pin. ISET can also indicate the load current through the eFuse. Connect a resistor from ISET to VSS to set the current limit.
16	SS	Soft Start Input. Place a capacitor from SS to VSS to control the eFuse startup voltage slew rate.
17	EN	Enable Input. A dual comparator on EN measures the input voltage to determine if it is under, voltage, over voltage, or within normal operating limits. Connect a resistive voltage divider between VIN, EN, and VSS to set the EN_UV and EN_UV thresholds. The EN_UV threshold is 0.64V. The EN_OV threshold is typically 0.92V, but can be modified by the IC's CMI.
18,19, 20, 21, 22	VIN	Power Supply Input. Input to the eFuse. Connect a 0.1μF capacitor between VIN and PGND as close to the IC as possible.
26	STR	Storage Capacitor Input. Connect the storage capacitors to STR. STR requires a minimum capacitor of 100μF to PGND.
27	SW	Switching Pin. This is the boost converter switch node and the buck converter switch node. Connect the inductor to SW.

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ABSOLUTE MAXIMUM RATINGS

PARAMETER	VALUE	UNIT
FB, SS, ISET, REF, SDA, SCL, EN, BSET, nIRQ to VSS	-0.3 to 6	V
VIN, VOUT to PGND (ACT4910)	-0.3 to 24	V
HSB to SW	-0.3 to 6	V
SW to PGND	-0.3 to STR+ 0.3	V
PLI to VSS	-0.3 to 24	V
STR to PGND	-0.3 to 40	V
VSS to PGND	-0.3 to + 0.3	V
ESD Rating (human body model), all pins	2	kV
Junction to Ambient Thermal Resistance, dependent on board layout	16.8	°C /W
Operating Ambient Temperature Range (T_A)	-40 to 105	°C
Operating Junction Temperature (TJ), (note 1)	-40 to 125	°C
Storage Temperature	-40 to 150	°C
Lead Temperature (Soldering 10s)	300	°C

Note1: Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods may affect device reliability.

Note2: Measured on Active-Semi Evaluation Kit

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SYSTEM CHARACTERISTICS

(VIN = 12V, T_A = 25°C, unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Input Supply					
Input Supply Voltage Range	VIN	2.7		18	V
Input Supply Power On Reset (Internal)	VIN Rising		2.53		V
Input Supply Power On Reset Hysteresis (Internal POR)	VIN Falling		90		mV
Input Supply Over Voltage Lock Out (OVLO)			20		V
Input Under Voltage Lock Out (UVLO)	VIN Rising (Boost/eFuse Enabled)		2.65	2.7	V
Input UVLO Hysteresis	VIN Falling		50		mV
Input Operation Current	eFuse Enabled and Soft start completed Buck/Storage Regulator Disabled ADC Disabled Storage Health Check Disabled			3	mA
	eFuse Enabled and Soft start completed Buck/Storage Regulator Disabled ADC Enabled Storage Health Check Disabled			5.5	mA
Input Current (Shutdown)	V_{EN}=0V		470		µA
Thermal					
Thermal Warning	Sets nIRQ		120		°C
Thermal Shutdown – Disables buck and boost			145		°C
Thermal Shutdown – Disables eFuse			155		°C
Thermal Comparators Hysteresis			15		°C
SET Thresholds					
BSET Current Source	BSET = 1.0V (25°C)	19.6	20	20.4	µA
BSET Current Source Temperature Coefficient	BSET = 1.0V (25°C – 125°C)		0.011		%/°C
STR Thresholds					
Input Under Voltage Lock Out (STR_UVLO)	STR Falling		3.6		V
Input Under Voltage Lock Out (STR_UVLO)	STR Rising		4.0		V

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PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Open Drain Outputs					
Switch Maximum Voltage Range (nIRQ,PG_STR, SDA)		0		5	V
Switch resistance (nIRQ,PG_STR, SDA)	Sinking Current 500μA			100	Ω
Enable Thresholds					
Under Voltage Reference	UV REF after POR release (-40°C ~ 125°C)	0.63	0.64	0.65	V
Overvoltage Reference Programmable Range	OV REF after POR release		0.92		V
EN Deglitch Time	EN UV Rising or OV Falling (0ms turn-on delay)		1		ms
Hysteresis for Reference			17		mV

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INTERNAL BUCK REGULATOR

(VIN = 12V, T_A = 25°C, unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Input Voltage Range		4.2		36	V
Typical Output Voltage			3.3		V
Programmable Output Voltage Range	Using external resistor divider	1.8		18	V
Standby Supply Current	V_{OUT} = 103%, Regulator Enabled, No Load, not switching			500	µA
Feedback Voltage			1.2		V
Output Voltage Accuracy	V_{OUT} = 12V, I_{OUT} = 2A (PWM mode)	-1%	V_{NOM}	1%	V
Output Voltage Accuracy	V_{OUT} = 12V, I_{OUT} = 1mA (PFM mode)	-1%	V_{NOM}	1%	V
Line Regulation	V_{OUT} = 12V V_{IN} = 5.5V to 12V, PWM Regulation		0.02		%/V
Load Regulation	V_{OUT} = 12V PWM Regulation		0.04		%/A
Power Good Threshold	V_{OUT} Rising	90.5	93	95.5	$\%V_{NOM}$
Power Good Hysteresis	V_{OUT} Falling		3		$\%V_{NOM}$
Overvoltage Fault Threshold	V_{OUT} Rising	107	110	113	$\%V_{NOM}$
Overvoltage Fault Hysteresis	V_{OUT} Falling		2		$\%V_{NOM}$
Programmable Switching Frequency Range		320		1130	kHz
Current Limit, Cycle-by-Cycle	BK_CLIM = 00 BK_CLIM = 01 BK_CLIM = 10 BK_CLIM = 11		5.0 6.0 7.0 9.0		A
Current Limit, Cycle-by-Cycle Tolerance	At default BK_CLIM	-10%		+10%	
	At other set points	-15%		+15%	
Current Limit, Shutdown	Above BK_CLIM	+15%	+22.5%	+30%	
High Side On-Resistance	I_{SW} = -3A, V_{STR} = 12V		45		mΩ
Low Side On-Resistance	I_{SW} = 3A, V_{STR} = 12V		28		mΩ
SW Leakage Current	V_{STR} = 12V, V_{SW} = 0 or 5.5V			1	µA

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INTERNAL EFUSE

(VIN = 12V, T_A = 25°C, unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Normal Mode					
Operating Voltage Range		2.7		18	V
eFuse On-Resistance	I_{SW} = -2A, VIN= 3.3V, 5V, and 12V, T_J = 25°C		17		mΩ
	I_{SW} = -2A, VIN= 3.3V, 5V, and 12V, T_J = 100°C		24.5		mΩ
Programmable eFuse Current Limit Range	VIN = 12V, Configured using ISET pin, Triggers nIRQ Pin	1		10	A
	VIN = 3.3V, Configured using ISET pin, Triggers nIRQ Pin	1		7	A
Internal Path Current Regulation Accuracy	V_{ISET}		1		V
ISET Monitor Current Ratio	ISET current divided by eFuse current		1/50,000		
eFuse Overcurrent Detection Deglitch			10		µs
eFuse Overcurrent Current Shutdown			11		A
Current Limit Restart Time			100		ms
eFuse Soft start	C_{SS} = 10nF	5.94	6.6	7.26	mV/us

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STORAGE BOOST REGULATOR

(VIN = 12V, T_A = 25°C, unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Storage Boost Converter					
Operating Voltage Range		2.7		36	V
Programmable Output Voltage Range		5.0		36	V
Peak switching Current	BST _CLIM = 00 BST _CLIM = 01 BST _CLIM = 10 BST _CLIM = 11		250 650 950 1500		mA
Standby Supply Current	V_{STR} = 103%, Regulator Enabled, not switching		25	40	µA
Output Voltage Accuracy	V_{STR} = 28V, I_{OUT} = 15mA (continuous PWM mode)	-3%	V_{NOM}	3%	V
Power Good Threshold	V_{STR} Rising		95		%V_{NOM}
Power Good Hysteresis	V_{STR} Falling	2	5		%V_{NOM}
Overvoltage Fault Threshold	V_{STR} Rising		110		%V_{NOM}
Overvoltage Fault Hysteresis	V_{STR} Falling		3		%V_{NOM}
Minimum On-Time			50		ns
Low Side FET On-Resistance	I_{SW} = 325mA		300		mΩ

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HEALTH MONITOR

(VIN = 12V, T_A = 25°C, unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Health Monitor					
Operating Voltage Range		4.2		40	V
Sink Current Source		9	10	11	mA
Programmable Health Monitor Current Sink Timer Range		2		1280	ms
Programmable Storage Voltage Threshold Range	Configurable 0.2% steps	95		98	%
ADC Monitoring					
Operating Voltage Range		3		20	V
Supply Current	Enabled		2	5	mA
Total Error	5V scale and 8 bit range			0.5	LSB
Conversion Time	Total time for all channels			100	ms
Full Scale Input Range		-2.5		2.5	V
Input Resistance			10		kΩ
Input Capacitance			5		pF

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I²C INTERFACE ELECTRICAL CHARACTERISTICS

(VIN = 5V, T_A = 25°C, unless otherwise specified.)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SCL, SDA Input Low	V_{IO} = 1.8V			0.6	V
SCL, SDA Input High	V_{IO} = 1.8V	1.2			V
SDA Leakage Current	SDA=5V			1	µA
SDA Output Low	I_{OL} = 5mA			0.35	V
SCL Clock Frequency, f_{SCL}		0		1000	kHz
SCL Low Period, t_{LOW}		0.5			µs
SCL High Period, t_{HIGH}		0.26			µs
SDA Data Setup Time, t_{SU}		50			ns
SDA Data Hold Time, t_{HD}	(Note1)	0			ns
Start Setup Time, t_{ST}	For Start Condition	260			ns
Stop Setup Time, t_{SP}	For Stop Condition	260			ns
Capacitance on SCL or SDA Pin				10	pF
SDA Rise Time SDA, T_r	Device requirement			120	ns
SDA Fall Time SDA, T_f	Device requirement			120	ns
Pulse Width of spikes must be suppressed on SCL and SDA		0		50	ns

Note1: Comply with I²C timings for 1MHz operation - “Fast Mode Plus”.
Note2: No internal timeout for I²C operations, however, I²C communication state machine will be reset when entering UV/POR State.
Note3: This is an I²C system specification only. Rise and fall time of SCL & SDA not controlled by the device.
Note4: Device Address is factory configurable to 7’h1A, 7’h3A, 7’h5A.

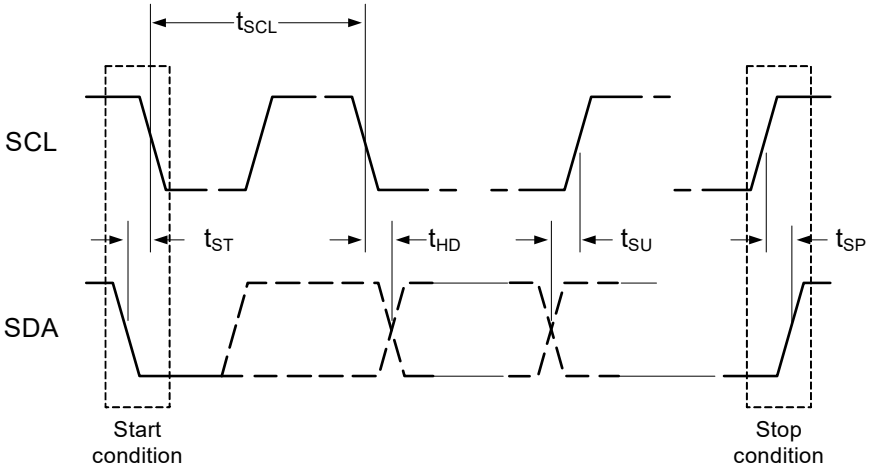


Figure 2: I²C Data Transfer

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FUNCTIONAL DESCRIPTION

General

ACT4910 provides protection, control, and supplemental storage for power failure prevention systems. This functionality goes by many names: Power Loss Protection (PLP), Power Loss Imminent (PLI) and Power Failure Protection (PFP). It provides a system with additional run time after a power failure to all the system to save critical data before shutting down. Typical applications include solid state disk drives (SSD) and servers. In normal operation when input power is good, the IC connects the input to the output through the eFuse. This powers the system load from the system input power. If an input voltage fault occurs, the IC disconnects the input from the output and enters supplement mode, where output power comes from the high voltage storage capacitor power. The internal buck converter efficiently converts the storage voltage down to the regulated output voltage. All startup, storage capacitor charging, and switching between normal and supplement mode operation is autonomous and does not require user intervention.

During start up, the ACT4910 limits the output voltage dV/dt to minimize system level inrush currents. After softstart is complete, the IC charges the storage capacitors with the internal boost converter. The IC automatically recharges the storage capacitors as needed. The IC contains extensive protection circuitry to protect against input voltage overvoltage and undervoltage, output voltage overload and short circuit, degraded storage capacitors, and thermal overload.

The IC communicates with the host processor via I2C and GPIOs. The nIRQ pin indicates general faults which can be read by the host processor via I2C. A dedicated power failure pin, PLI, automatically and immediately goes low to indicate a power loss condition. This gives the system advanced warning to complete all active tasks and shutdown. See the Pin Function section for additional PLI pin functionality.

The ACT4910 is highly flexible and contains many I2C configurable functions. The IC's default functionality is defined by its default CMI (Code Matrix Index), but much of this functionality can be changed via I2C. I2C functionality includes storage voltage setting, OV and UV fault thresholds, switching frequencies, ADC control and automatic fault thresholds, PLI pin functionality, health check settings, and current limits. The CMI Options section shows the default settings for each available CMI option. Contact sales@active-semi.com for additional information about other configurations.

I²C Serial Interface

To ensure compatibility with a wide range of systems, the ACT4910 uses standard I²C commands. The ACT4910 operates as a slave device, and can be factory configured to one of three 7-bit slave addresses. The 7-bit slave address is followed by an eighth bit, which indicates whether the transaction is a read-operation or a write-operation. Refer to each specific CMI for the IC's slave address

7-Bit Slave Address		8-Bit Write Address	8-Bit Read Address
0x1Ah	001 1010b	0x34h	0x35h
0x3Ah	011 1010b	0x74h	0x75h
0x5Ah	101 1010b	0xB4h	0xB5h

The I²C packet processing state machine does not have a timeout function, however, any time the I²C state machine receives a start bit command, it immediately resets the packet processing, even if it is in the middle of a valid packet. The I²C functionality is operational in all states except RESET.

I²C commands are communicated using the SCL and SDA pins. SCL is the I²C serial clock input. SDA is the data input and output. SDA is open drain and must have a pull-up resistor. Signals on these pins must meet timing requirements in the Electrical Characteristics Table.

I²C Registers

The ACT4910 contains an array of internal registers that contain the IC's basic instructions for setting up the IC configuration, output voltages, sequencing, fault thresholds, fault masks, etc. These registers are what give the IC its operating flexibility. The two types of registers are described below.

Basic Volatile – These are R/W (Read and Write) and RO (Read only). After the IC is powered, the user can modify the R/W register values to change IC functionality. Changes in functionality include things like masking certain faults. The RO registers communicate IC status such as fault conditions. Any changes to these registers are lost when power is recycled. The default values are fixed and cannot be changed by the factory or the end user.

Basic Non-Volatile – These are R/W and RO. After the IC is powered, the user can modify the R/W register values to change IC functionality. Changes in functionality include things like output voltage settings,

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startup delay time, and current limit thresholds. Any changes to these registers are lost when power is recycled. The default values can be modified at the factory to optimize IC functionality for specific applications. Please consult sales@active-semi.com for custom options and minimum order quantities.

When modifying only certain bits within a register, take care to not inadvertently change other bits. Inadvertently changing register contents can lead to unexpected device behavior.

State Machine

ACT4910 contains an internal state machine with seven internal states: UV/POR, SOFT-START, NORMAL, HEALTH CHECK, SUPPLEMENT, SHUTDOWN1, and SHUTDOWN2.

UV/POR State

The IC enters the UV/POR state on power up. It also enters UV/POR from SUPPLEMENT state in the following conditions:

1. When the input voltage drops below the EN_UV threshold.
2. When the storage capacitor voltage drops below 3.6V.
3. When the buck converter output voltage goes OV or UV.

The user may force the IC into UV/POR by writing a 1 into the FORCE_PWROFF bit, register 0x0Ah, bit 0. When entering UV/POR from power up, all registers reset to their default state. The registers retain their existing values when the IC enters from SUPPLEMENT state or from SHUTDOWN2 EFUSE. The IC transitions to the SOFT-START state when EN pin is above 0.64V and the input voltage is above UVLO.

SOFTSTART State

In the SOFTSTART state, the IC slowly turns on the eFuse to minimize inrush currents. The output voltage dV/dt ramp rate is controlled by the SS pin. The SS pin directly controls the maximum output voltage dV/dt while the ILIM pin indirectly controls it by limiting the current into the output capacitance. The IC stays in the SOFTSTART state until VIN-VOUT < 200mV and a 10ms timer times out. Note that the output voltage may be fully charged up to VIN even though the IC in still in the SOFTSTART state. The storage caps charge up to the output voltage in this state.

NORMAL State

The NORMAL state is the normal operating state after startup with no faults. The eFuse is fully on, VOUT = VIN, and the IC provides full operating current. Note that the IC charges the storage capacitors to their programmed value at the beginning of NORMAL state.

HEALTH CHECK State

The HEALTH CHECK state can be considered a sub-state of NORMAL. The IC operates identical to the NORMAL state with the addition of activating the circuitry that check the storage capacitor health. The IC automatically enters HEALTH STATE every four minutes. The user may also manually enter this state by writing a 1 into the FORCE_HLTHCHK bit which is bit 1 in register 0x0Ah. This bit automatically resets to 0 after the health check routine completes. The IC automatically exits HEALTH CHECK and enters SUPPLEMENT state in a fault condition.

SUPPLEMENT State

The IC enters SUPPLEMENT state when it detects a fault condition. It opens the eFuse to bi-directionally disconnect the input from the output. It automatically turn on the buck converter to power the output from the storage capacitors. The following five conditions move the IC into SUPPLEMENT state.

1. EN voltage below UV threshold
2. EN voltage above the OV threshold
3. Input voltage above the OV threshold
4. eFuse current above the OC threshold
5. VIN – VOUT > 560mV

SHUTDOWN1 State

SHUTDOWN1 protects against over temperature (145 °C), internal LDO failure, or boot capacitor failure. The eFuse remains on and continues to provide power to the output, but the boost converter is disabled. The ADC remains on and I^2C functionality is still operational. The IC transitions to SHUTDOWN2 state if the die temperature increases to 155°C. If transitions back to the NORMAL state if the fault conditions go away.

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SHUTDOWN2 State

SHUTDOWN2 disables all IC functionality to protect against extreme over temperature conditions above 155°C. This includes shutting off the eFuse. I²C functionality not available in this state. The IC transitions to SOFT-START when the junction temperature drops and there is no overcurrent fault. Figure 3 shows the ACT4910 State Diagram. Table 1 shows which functions are enabled in each state. Note that the current operating state can be determined by reading the I²C register bits CURRENT_STATE in register 0x00h.

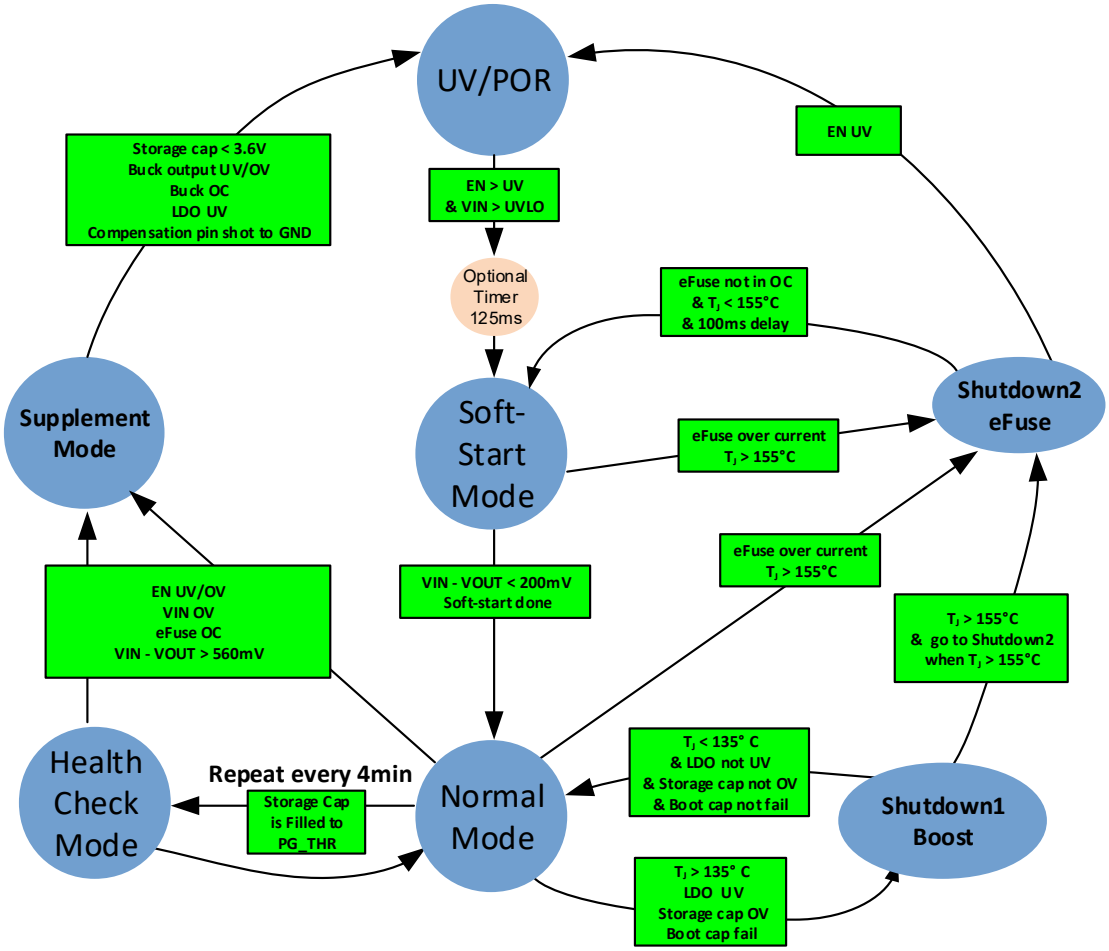


Figure 3: State Machine Diagram

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States	eFuse	Boost	Buck	ADC	V_{REF}
UV/POR	Disabled	Disabled	Disabled	Disabled	Disabled
SOFT-START	Enabled	Disabled	Disabled	Disabled	Enabled
NORMAL	Enabled	Enabled	Disabled	Enabled	Enabled
HEALT CHECK	Enabled	Enabled	Disabled	Enabled	Enabled
SUPPLEMENT	Disabled	Disabled	Enabled	Enabled	Enabled
SHUTDOWN1	Enabled	Disabled	Disabled	Enabled	Enabled
SHUTDOWN2	Disabled	Disabled	Disabled	Disabled	Disabled

Table 1: Enabled Functions in Different States

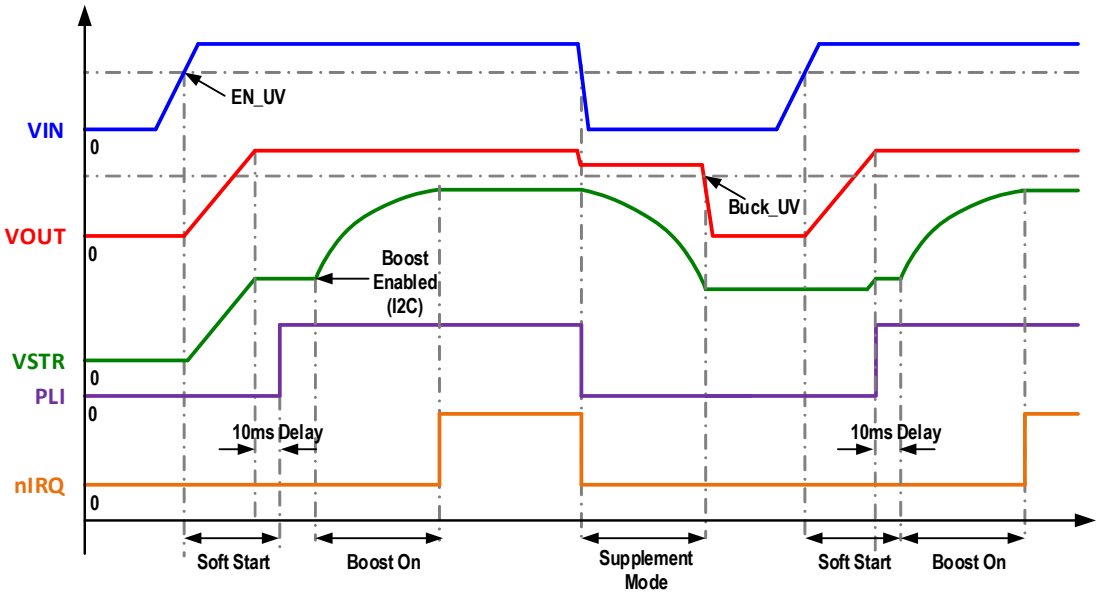


Figure 4: Operation states

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Pin Functions

VIN

VIN is the input the eFuse. Connect a 0.1uF ceramic capacitor between VIN and PGND. VIN is directly connected to VOUT in normal operation. The eFuse disconnects VIN from VOUT when the IC enters supplement mode.

EN

The EN pin is the ACT4910 enable input used to turn the eFuse on or off. It provides both overvoltage and undervoltage protection thresholds. The EN pin contains a precision comparator with hysteresis. It can be directly driven from a digital input to turn the eFuse on and off. The EN pin can also be used with a resistor divider from VIN to VSS to program an eFuse startup voltage higher than the IC's UVLO value. The EN pin also contains an overvoltage comparator. The eFuse turns on when the input EN pin goes above the EN_UV_REF threshold. Once the eFuse is on, it turns off and enters supplement mode if the EN pin goes above the EN_OV_REF threshold or below the EN_UV_REF threshold.

The EN pin should not be left floating. It can be driven from standard logic signals greater than EN_UV_REF. It can also be driven with open-drain logic to provide. When driving it with an open-drain, ensure that the pullup voltage is not higher than the EN_OV_REF setting.

EN_UV_REF is fixed at 0.64V. However, the EN_OV_REF can be programmed by I²C bits EN_OV_REF [2:0]. The default EN_OV_REF voltage is set by the IC's CMI.

Table 2: Over Voltage Reference Settings

EN_OV_REF[2:0]	OV Threshold (V)
000	Disabled
001	0.82
010	0.92
011	1.00
100	1.08
101	1.16
110	1.24
111	1.32

STR

STR is the output to the storage capacitor bank. In normal operation the internal boost converter charges the storage capacitors through the STR pin. When the IC enters supplement mode, the internal buck converter uses the STR pin as its input to power the system. The STR pin typically has a 22uF or greater ceramic capacitor. See the Buck Converter section for more information.

IRQ—Interrupt

ACT4910 has an interrupt pin to inform the host of any fault conditions. In general, any IC function with a status bit asserts nIRQ if the status changes. The status changes can be masked by setting the corresponding register bits. If nIRQ is asserted low, the fault must be read before the IC deasserts nIRQ. If the fault remains after reading the status bits, nIRQ remains asserted.

The below status changes will set the IRQ:

- Input overvoltage, undervoltage
- Thermal warning, thermal shutdown
- eFuse VIN to VOUT over limits
- eFuse current warning and limit
- Storage capacitor overvoltage, undervoltage
- Supplemental mode active
- Buck operation faults
- Buck undervoltage shutdown
- REF LDO undervoltage
- ADC data is ready
- ADC beyond set limits

nIRQ is an open-drain output and should be pulled up to an appropriate supply voltage with a 10kΩ or greater pull-up resistor.

SCL, SDA

SCL and SDA are the I²C clock and data pins to the IC They have standard I²C functionality. They are open-drain outputs and each require a pull-up resistor. The pull-up resistor is typically tied to the system's uP IO pins. The pullup voltage can range from 1.8V to 5.0V.

REF

The REF pin is an internal bias voltage output pin. Connect a 1µF capacitor between REF and VSS. Do not apply an external load to the REF pin.

BSET

BSET sets the boost converter output voltage. The output voltage is a function of both a resistor connected between BSET and VSS as well as internal I²C register

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settings. See the Storage Boost Converter section for more information.

ISET

ISET sets the eFuse current limit with a resistor connected to VSS. See the eFuse section for more information.

SS

The SS pin uses a capacitor to VSS to control the eFuse softstart timing. See the eFuse section for more information.

PGND

The PGND pin is the buck and boost converters' power ground. The internal FETs connect directly to the PGND pins. The power supply input and output capacitors should connect to the PGND pins.

COMP

COMP is the output of a transconductance amplifier that is used to compensate the internal buck converter. The compensation components, which are typically a standard type-2 compensation should be grounded to the VSS pin. See the Application section for more information on compensating the internal buck converter.

PLI

The PLI pin has four possible functions which are set by the internal I^2C registers.

Power Loss Indicator function. Set register bits PLI_FUNC_SEL[1:0] in 0x19h to 00 to configure PLI for this function. With this setting, PLI goes high after softstart and stays high in normal operation. PLI immediately goes low when the IC enters supplement mode. This setting is used to let the system uP know that power loss is imminent.

PG_STR function. Set PLI_FUNC_SEL = 01 to configure PLI for this function. With this setting, PLI starts low during softstart and then goes high when the storage capacitor voltage is in regulation. It goes low if the storage voltage drops below 95% of its programmed output voltage.

VOUT_READY function. Set PLI_FUNC_SEL = 10 to configure PLI for this function. With this setting, PLI starts low during softstart and then goes high when the IC exits the softstart mode and goes into normal operation. The IC exits softstart ~10ms after the programmed softstart time ends.

PLI_VOUT_READY function. Set PLI_FUNC_SEL = 11 to configure PLI for this function. With this setting, PLI performs a dual function. It starts out as the VOUT_READY function at turn-on. After PLI goes from low to high after softstart, it then acts as the Power Loss Indicator function.

The PLI pin is an open-drain output and is 24V compliant.

FB

The FB pin is used to regulate the buck converter output voltage when the IC is in supplement mode.

HSB

HSB provides power to the internal high-side MOSFET gate driver circuitry. Connect a 47nF capacitor from HSB pin to SW pin.

SW

SW is the switch node for the internal buck and boost converters.

VOUT

VOUT is the output of the eFuse and connects to the system load. VOUT powers the boost converter when it charges up the storage capacitors. It is the output of the buck converter when the IC is in supplement mode. The eFuse connects VOUT to VIN in normal operation, and it disconnects it in supplement mode.

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EFUSE

General Description

The ACT4910 eFuse is an "electronic" fuse that disconnects the input from the output. It has considerable advantages over mechanical fuses because it has adjustable current thresholds and it resets after the fault condition is gone. The eFuse consists of two back-to-back MOSFETS to provide bi-directional protection. This provides protection against both input and output short circuit conditions by preventing current flow in both directions. Hot swap functionality is provided by the eFuse softstart function and current limiting circuitry. This prevents large inrush currents from pulling down the input voltage. The eFuse also provides protection against high input voltage transients up to 24V by opening when the input voltage goes above the programmed threshold.

The eFuse turns off in the following conditions.

1. EN voltage below UV threshold
2. EN voltage above the OV threshold
3. Input voltage above the OV threshold
4. eFuse current above the OC threshold
5. VIN – VOUT > 560mV

Current Limit Setting

A resistor connected between the ISET pin and VSS program the ACT4910 eFuse inrush and maximum DC current limits. The input current limit is linearly proportional to the resistor value on the ISET pin. The following equation calculates the correct resistor value to get the desired current limit threshold.

$$R_{ILIM} = \frac{50000}{I_{ILIM}} \qquad \text{Equation (1)}$$

Where R_{ILIM} is the current limit resistor in ohms and I_{ILIM} is the desired current limit threshold in Amperes. Figure 5 shows the current limit setting vs R_{ILIM} value.

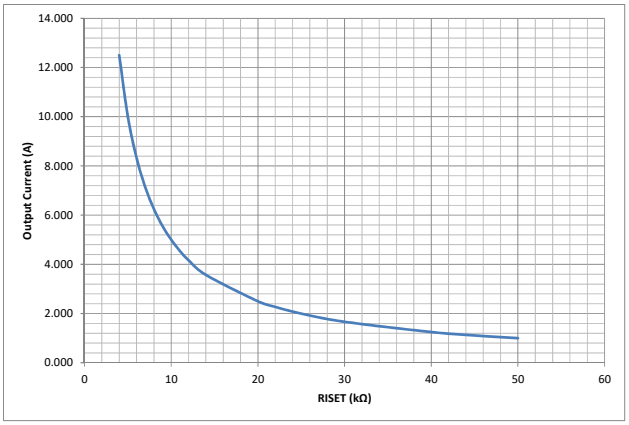


Figure 5: Current Limit Threshold vs R_{ILIM}

Note that the eFuse current can be measured using the ILIM pin. If eFuse current is measured via the ILIM pin, the measurement circuit must have a high impedance input to minimize errors. The current flowing out of ILIM is 1/50000 of the current through the eFuse. The following equation calculates the eFuse current when measured via the ILIM pin.

$$I_{eFuse} = \frac{V_{ILIM} * 50000}{R_{ILIM}} \qquad \text{Equation (2)}$$

Where R_{ILIM} is the current limit resistor in ohms and V_{ILIM} is the voltage on the ILIM pin in volts.

When the eFuse reaches the current limit threshold, it clamps the output current. If the load tries to draw additional current, the eFuse opens.

Soft-Start

The SS pin controls the eFuse start-up. The SS pin drives a constant 5μA internal current source into the external soft-start capacitor to provide a linear ramping voltage at the SS pin. The output voltage linearly ramps with the SS pin voltage, resulting in a well-controlled linear softstart ramp on VOUT, regardless of the load conditions. The following equation calculates the required soft-start capacitance.

$$C_{SS}(nF) = \frac{65 \times T_{SS}(mS)}{V_{OUT}(V)} \qquad \text{Equation 2}$$

Where the T_{SS} is the soft-start time in ms and V_{OUT} is the output voltage.

The softstart current must be less than 90% of the programmed eFuse current limit. If the softstart current is greater than 90% of the eFuse current limit, the IC enters the SHUTDOWN2 state, turns off the eFuse, and

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then retries to softstart again. The following equation calculates the minimum allowable softstart time.

$$T_{SS_min}(ms) = \frac{C_{OUT}(mF) * V_{OUT}}{0.9 * I_{ILIM}(A)} \qquad \textit{Equation 3}$$

Where C_{OUT} is the sum of the output capacitance and storage capacitance in mF, V_{OUT} is the output voltage in volts, and I_{ILIM} is the eFuse current limit in Amperes programmed by the ILIM resistor.

Buck Converter

General Description

The ACT4910 contains current-mode, synchronous PWM step-down converter that achieves peak efficiencies of 95%. The buck converter minimizes noise in sensitive applications and allows the use of small external components. It is highly flexible with external component selection and can be reconfigured via I²C registers. External components set the output voltage and compensation while I²C registers set the switching frequency and current limit. The buck converter operates in fixed frequency PWM mode. Its switching frequency is programmable between 320kHz to 1130 kHz via the I²C register BK_FREQ[2:0] which allows the system to be optimized for different applications. Its current limit is adjustable between 5A to 9A, allowing for further system optimization. The output voltage is externally programmable between 1.8V and 18V.

The buck converter generates a regulated output voltage at the VOUT pin from the storage capacitors when the IC enters supplement mode. This provides the backup power when the system experiences fault conditions. After the IC exits the SOFTSTART state, the buck converter is enabled but remains turned off. It automatically turns on when the IC enters supplement mode, and remains on until the storage capacitors discharge to 3.6V.

Frequency Setting

Higher switching frequencies result in smaller solution sizes at the cost of slightly lower efficiency. Lower switching frequencies result in larger solution sizes with higher efficiency. The maximum allowable switching frequency for any given design is limited by the following equation.

$$F_{sw_max} < \frac{V_{OUT}}{V_{STR} * 180ns} \qquad \text{Equation 3}$$

Where F_{SW_max} is the maximum allowable frequency, V_{STR} is the storage voltage, and V_{OUT} is the output voltage during supplement mode.

Output Voltage Setting

The buck converter output voltage is programmed by an external resistor divider connected between the VOUT pin and VSS, with the center tap connected to the FB pin. The buck output voltage can be set above, below, or equal to the input voltage supplement threshold. When the input voltage drops below this threshold, the IC enters supplement mode and regulates the output to the programmed buck voltage. Although the buck converter immediately starts up when the IC enters supplement mode, the output voltage still has a small, but finite drop in output voltage between the time the eFuse turns off and the buck converter is fully on. This voltage drop should be considered when setting the output voltage. The following equation calculates the correct resistor values to set the desired output voltage.

$$R1 = \mathrm{R2} * \left(\frac{V_{\mathrm{OUT}}}{V_{\mathrm{FB}}} - 1\right) \qquad \text{Equation 4}$$

Where R1 is the top feedback resistor, R2 is the bottom feedback resistor, VOUT is the desired output voltage, and VFB is the fixed 1.2V reference voltage on the FB pin. Choose R2 in the range of 10kohm. Smaller resistor values are acceptable, but larger values will affect voltage accuracy due to bias currents into the FB pin.

Protection

The buck converter has several protection mechanisms to insure safe operation. It stops operation when input voltage from storage cap reaches STR_UVLO (3.6V) or when the output voltage drops below the power good threshold which is fixed at 93% of the output setpoint. It also stops operating when the output voltage is above the over voltage threshold which is fixed at 110% of the output voltage setpoint. The output undervoltage protection can be masked by the I²C register bit Mask_BK_UV REG0x38 [0].

The buck converter provides overcurrent and short circuit protection. Overcurrent protection is achieved with cycle-by-cycle current limiting. The peak current threshold is set between 5A and 9A by the BK_CLIM bits. If the peak current reaches the programmed threshold, the IC turns off the power FET. This condition typically results in shutdown due to an output voltage UV condition due to the shortened switching cycle.

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Table 3: Buck Current Limit

BK_CLIM[1:0]	ILIMSET (A)
00	5.0
01	6.0
10	7.0
11	9.0

A short circuit condition that results in the peak switch current being 122.5% of BK_CLIM immediately shuts down the supply and asserts nIRQ low. A buck overcurrent, undervoltage, or overvoltage condition moves the IC into the UV/POR state.

Compensation

The Buck regulator utilizes type 2 external compensation placed on the COMP pin. Contact the factory for compensation details.

Input Capacitor Selection

The STR pin is the input voltage to the buck converter. It requires a dedicated high quality, low-ESR, ceramic input capacitor that is optimally placed to minimize the power routing. For optimal PCB layout considerations, 1206 or 1210 sized input capacitors are recommended. A 22uF capacitor is typically suitable, but the actual value is application dependent. The input capacitor can be increased without limit. Choose the input capacitor value to keep the input voltage ripple less than 50mV

$$C_{IN} = Iout * \frac{\frac{V_{OUT}}{V_{STR}} * \left(1 - \frac{V_{OUT}}{V_{STR}}\right)}{F_{SW} * V_{ripple}} \quad \text{Equation 5}$$

Where Iout is the maximum eFuse load current in Amperes, V_{STR} is the maximum storage voltage, F_{SW} is the switching frequency, and V_{ripple} is the maximum allowable ripple voltage on the input of the buck converter. Note that the storage capacitor values should not be considered when calculating the input voltage ripple because they are not typically designed for high frequency functionality.

Be sure to consider the input capacitor's DC bias effects. A capacitor's actual capacitance is strongly affected by its DC bias characteristics. The input capacitor is typically an X5R, X7R, or similar dielectric. Use of Y5U, Z5U, or similar dielectrics is not recommended. Input capacitor placement is critical for proper operation. The buck's input capacitor must be placed as close to the IC as possible. The traces from STR to the capacitor and from the capacitor to PGND should as short and wide as possible.

Inductor Selection

The Buck regulator utilizes current-mode control and a proprietary internal compensation scheme to simultaneously simplify external component selection and optimize transient performance over their full operating range. These ACT4910 is optimized for operation with 1uH to 3.3uH inductors. Choose an inductor with a low DC-resistance, and avoid inductor saturation by choosing inductors with DC ratings that exceed the maximum output current by at least 30%. Due to the requirement for the buck converter to start up as quickly as possible, the inductor should be designed to give a maximum ripple current, ΔI_L, of 50% to 60% of the maximum output current. The following equation calculates the recommended inductor value.

$$L = \frac{\left(1 - \frac{V_{OUT}}{V_{STR}}\right) * V_{OUT}}{F_{SW} * \Delta I_L} \quad \text{Equation 6}$$

Where L is the inductor value in μH, V_{OUT} is the output voltage, V_{STR} is the maximum storage voltage, F_{SW} is the switching frequency in Hz, and ΔI_L is the desired ripple current in Amperes.

Output Capacitor Selection

The buck converter is designed to take advantage of the benefits of ceramic capacitors, namely small size and very-low ESR. The buck converter is designed to operate with 44μF output capacitor over most of its operating ranges, although more capacitance may be desired depending on the duty cycle and load step requirements. Choose a ripple voltage that is approximately 1% of the output voltage setpoint. Note that the output capacitance must be placed at the output of the buck converter. Additional downstream capacitance will be placed at the loads, but this capacitance should not be considered when calculating the buck output capacitance. However, the downstream capacitance should be considered when compensating the power supply. The following equation calculates the output voltage ripple as a function of output capacitance. Note that the worst case ripple voltage occurs at the beginning of supplement mode when the storage capacitors are fully charged.

$$C_{OUT} = \frac{\Delta I_L}{8 * F_{SW} * V_{ripple}} \quad \text{Equation 7}$$

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Where V_{ripple} is the desired output ripple voltage, F_{SW} is the switching frequency in Hz, and ΔI_L is the maximum ripple current in Amperes.

As with the input capacitor selection, use X5R or X7R dielectrics and be sure to consider the capacitor's DC bias effects.

Storage Boost Converter

General Description

The ACT4910 contains an integrated peak current-mode, synchronous boost converter. It minimizes system level costs by using the same components as the buck converter. The peak current is adjustable between 250mA and 950mA, allowing for system optimization. The output voltage is adjustable between 5V and 36V via I²C registers and an external resistor. The peak current-mode control topology eliminates the need for compensation. The boost automatically charges up the storage capacitors from the input voltage so they are ready to provide backup power in the event of a system fault.

Startup

The boost converter automatically starts when the IC exits the SOFTSTART state. Note that the IC exits the SOFTSTART state 10ms after the output voltage is within 200mV of the input voltage.

When the storage voltage reaches regulation, the boost enters standby mode and monitors the storage voltage. It automatically turns back on and "tops off" the storage capacitors when the storage voltage drops below 95% of the programmed voltage. The boost converter automatically turns off if it is "topping off" the storage capacitors when the IC enters supplement mode.

The average input current when the boost charges the storage capacitors is approximately ½ of the peak switching current. The peak switch current is programed by register BST_CLIM[1:0].

Table 4: Boost Peak Current Settings

BST_CLIM[1:0]	(mA)
00	250
01	650
10	950
11	1500

Operating Mode

The boost converter operates in peak current mode, non-fixed frequency mode. The power FET stays on until its current reaches programmed peak current. It then turns off until the inductor current drops to 0A, at which time it turns on again.

Storage Capacitor Voltage Setting

The buck converter output voltage is set by either the I²C register BSTVSET[4:0], or a combination the register and a resistor placed between the BSET pin to VSS.

When using only the BSTVSET[4:0] leave the BSET pin floating. Table 5 shows the programmed storage voltage. The default value is determined by the IC's specific CMI option.

Table5: Storage Capacitor Voltage Settings with BSET Pin Open

BSTVSET[3:0]	BSTVSET[4]	
	0	1
0000	5V	21V
0001	5.6V	22V
0010	7V	23V
0011	8V	24V
0100	9V	25V
0101	10V	26V
0110	11V	27V
0111	12V	28V
1000	13V	29V
1001	14V	30V
1010	15V	31V
1011	16V	32V
1100	17V	33V
1101	18V	34V
1110	19V	35V
1111	20V	36V

Using both the BSTVSET[4:0] register and an external resistor provides additional output voltage resolution. In this configuration, the following equation calculates the output voltage.

$$V_{STR} = V_{BSTVSET} * \frac{R_{BSET}}{75k\Omega} \qquad \text{Equation 8}$$

Where $V_{BSTVSET}$ is the voltage set by the BSTVSET register in Table 5 and R_{BSET} is the resistor on the BSET pin in ohms.

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As an example, with BSTVSET[4:0] = 10111 (sets $V_{BSTVSET}$ = 28V) and R_{BSET} = 34.2kΩ, V_{STR} = 12.8V. Note that R_{BSET} should be set between 20kΩ and 75kΩ. Setting R_{BSET} below 20kΩ gives the same result as using a 20kΩ resistor. Setting R_{BSET} above 75kΩ gives the same result as using a 75kΩ resistor. Using R_{BSET} outside the range is acceptable and does not damage the IC.

Input Capacitor Selection

There are no special considerations for the boost converter input capacitor. The IC topology uses the buck converter output capacitor for the boost input capacitor. Proper selection of the buck converter output capacitor automatically results in an acceptable boost converter input capacitor.

Output Inductor Selection

There are no special considerations for the boost converter inductor. The IC topology uses the buck converter inductor for the boost converter inductor. Proper selection of the buck converter output capacitor automatically results in an acceptable boost converter input capacitor.

Output Capacitor Selection

The IC topology uses the buck converter input capacitor for the boost converter output capacitor. Note that the storage capacitors are also included in the boost converter output capacitors. Proper selection of the buck converter input capacitor typically results in an acceptable boost converter output capacitor. The boost output capacitor has two criteria. The first is that it must consist of at least 10µF of high quality X5R or X7R ceramic capacitance placed directly between the STR pin and PGND. The second criteria is that the sum of the ceramic capacitor and storage capacitors must be greater than 100µF. There is no requirement for the additional capacitance dielectric material. This provides flexibility for the storage capacitors, which allows the use of super capacitors, electrolytic, polymer, Tantalum, ceramic, or any capacitors in the design.

Output Voltage UVLO Setting

The storage capacitor power good signal indicates that the STR voltage is above the UVLO threshold. The UVLO threshold is shared with the storage capacitor health check, and is set by the I²C register HMON_THR [3:0]. The default value is determined by the IC's specific CMI option.

Table 6: Storage Capacitor PG Threshold

HMON_THR[2:0]	HMON_THR[3]	
	0	1
000	95.0%	96.6%
001	95.2%	96.8%
010	95.4%	97.0%
011	95.6%	97.2%
100	95.8%	97.4%
101	96.0%	97.6%
110	96.2%	97.8%
111	96.4%	98.0%

Storage Capacitor Health Monitor

General Description

The ACT4910 has an internal health monitor for the storage capacitors. It applies a constant current sink to the capacitors and monitors the voltage drop. If the voltage drops below a predetermined threshold, the IC asserts nIRQ to indicate that the storage capacitance has dropped below the allowable threshold. Health monitoring is completely autonomous, but can also be manually initiated by the system uP. Health monitoring can also be configured so that it is only a manual operation so it can be triggered on demand to avoid any critical system operations. The health monitor parameters are adjustable via I²C registers to allow flexibility for different capacitor values.

Health Monitor Algorithm

The health check algorithm sinks 10mA into the STR pin for a time determined by I²C register HMON_TSET. It then sinks 50mA for 200us. It monitors the voltage on the STR pin, and if the voltage drops more than the percentage set by I²C register HMON_THR, it asserts nIRQ low and sets the fault bit. The IC's specific CMI option sets the default HMON_TSET and HMON_THR settings. After the HMON_TSET time, the boost turns back on to recharge the storage capacitor.

The health check function can be enabled and disabled by the DIS_HEALTH_CHK bit (0x1Fh [5]). It also can be forced to perform a one-shot health check by the FORCE_HLTHCHK bit (0x0Ah [1]). Forcing a single health check is valid even when the DIS_HEALTH_CHK bit =1. If set in continuous mode, the IC performs a health check every 4 minutes. This timing can be configured for every 8 minutes or 16 minutes by bits SCALE_HCHK _2X and SCALE_HCHK _4X in register 0x27h [1:0].

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The ACT4910 allows for very flexible health checking routines by allowing the system to manually enable the 10mA discharge current by setting the EN_STR10mASINK bit = 1. In this situation, the system manually turns the discharge current on and off. The storage capacitor voltage threshold is still determined by the HMON_THR register. This function is useful for checking extremely large capacitor values which need very long discharge times.

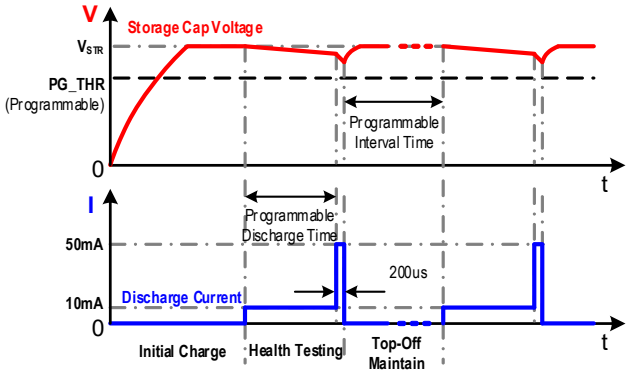


Figure 6: Storage Voltage at Different Stages

The register HMON_TSET [3:0] sets the health check discharge time as shown in Table 7. This also allows the use of the ADC to check the slope of the discharge and calculate the capacitance.

Table 7: Health Check Discharge Time

HMON_TSET[2:0]	HMON_TSET[3] (ms)	
	0	**1**
000	2	384
001	4	512
010	8	640
011	16	768
100	32	896
101	64	1024
110	128	1152
111	256	1280

ADC Monitoring

General Description

The ACT4910 contains a built-in analog to digital converter, ADC, which can be used to monitor five system level parameters. These include input voltage, output voltage, storage capacitor voltage, eFuse current, and die temperature. It is a single 8 bit delta-sigma ADC that uses an analog input multiplexer to select one of six channels for the A/D conversion. The resulting digital results are stored in six digital registers. A six to one multiplexer connects one of the ADC output registers to the user accessible register map.

ADC Configuration

The ACT4910 ADC is configured through the I²C interface. It is enabled and disabled by the EN_ADC register bit. The ADC has two conversion modes, manual single-shot conversion and automatic polling conversion.

Single-Shot Conversion

Configure the IC for single-shot conversion mode by setting the following I²C bits in register 0x08h

ADC_ONE_SHOT = 1.
ADC_CH_SCAN = 0
EN_ADCBUF = 1

In single shot mode, the user defines the input channel to be converted and then manually initiates the ADC conversion. I²C bits ADC_CH_CONV [2:0] in register 0x08h select the input channel to be converted. ADC_CH_READ [2:0] selects the ADC channel to be read. These should be set to the same channel. The user initiates an ADC read by writing a 1 into EN_ADC in register 0x08h. When ADC conversion is complete, the ADC_DATA_READY bit (register 0x07h [7]) is set to 1, nIRQ is asserted low, and EN_ADC automatically changes back to 0. The uP can then read the status bits to find that the ADC conversion is complete. The ADC data are stored in ADC_DOUT [13:6] in register 0x05h. nIRQ stays asserted low and the ADC_READY_BIT stays equal to 1 until the ADC data is read. Reading the ADC data automatically deasserts nIRQ. To initiate another ADC conversion for the same channel, set EN_ADC=1. To initiate an ADC conversion for another channel, change ADC_CH_CONV and ADC_CH_READ to the appropriate channel and then set EN_ADC=1.

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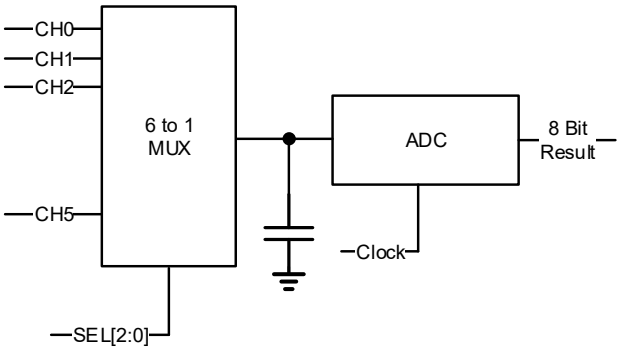


Figure 7: ADC Block Diagram

Automatic Polling Conversion

Configure the IC for automatic polling conversion mode by setting the following I²C bits in register 0x08h

ADC_ONE_SHOT = 0
ADC_CH_SCAN = 1
EN_ADCBUF = 1

Start the automatic polling by changing EN_ADC to 1. When in automatic polling mode, the ADC continuously changes the MUX inputs to read all input channels. The ADC continually overwrites the data in the output register. After all channels have been converted, the ADC_DATA_READY bit is set to 1. Note that nIRQ is not asserted low in Automatic Polling mode. Ensure that ADC data is valid and ready by reading the ADC_DATA_READY before reading ADC data. After the ADC_DATA_READY bit is set to 1, the user defines the channel to be read with the ADC_CH_CONV [2:0] bits in register 0x08h. Change ADC_CH_CONV to read additional channels.

Table 8: ADC Channels

Channel	Channel Description	ADC_CH_CONV[2:0]	ADC_CH_READ[2:0]	Value
CH0	Input Current	000	000	IIN = (DOUT-128)*1.221/RILIM (A)
CH1	Input Voltage	001	001	VIN = (DOUT-128)*0.392 (V)
CH2	Storage Cap Voltage	010	010	VSTR = (DOUT-128)*0.392 (V)
CH3	Output Voltage	011	011	VOUT = (DOUT-128)*0.392 (V)
CH4	Die Temperature	100	100	Temp = 6.125*DOUT-1053.75 (deg C)
CH5	GND	101	101	

Autonomous ADC Supervisory Function

The ACT4910 can be configured to automatically measure any or all of the five system level parameters and then then automatically notify the system if one of the parameters falls out of its specified range. This check is performed automatically, without any external circuit components. The ACT4910 implements this using internal digital undervoltage and overvoltage comparators for all five ADC channels. Table 9 shows each ADC channel's undervoltage and overvoltage registers. When in automatic polling mode, if an ADC conversion result is below the undervoltage threshold or above the overvoltage threshold, the IC asserts nIRQ low. The uP can then read the status register 0x04h to determine which parameter is out of range. nIRQ can be masked by setting the ADC_OUTRNG_IRQ_MASK bit. The default thresholds are determined by each ICs CMI, but can be changed at any time after startup. Disable a channel's supervisory function by programming the undervoltage register value to 0x00h and the overvoltage register to 0xFFh.

Table 9: ADC Thresholds Registers

	Undervoltage Threshold Register	Overvoltage Threshold Register
Input Current	0x0Ch	0x14h
Input Voltage	0x0Dh	0x15h
Storage Cap Voltage	0x0Eh	0x16h
Output Voltage	0x0Fh	0x17h
Die Temperature	0x10h	0x18h

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PC board layout guidance

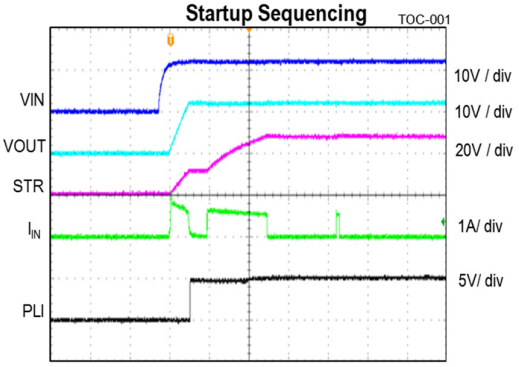
Proper parts placement and PCB layout are critical to the operation of switching power supplies. Follow the following layout guidelines when designing the ACT4910 PCB. Refer to the Active-Semi ACT4910 Evaluation Kits for layout examples

1. Place the buck input capacitors as close as possible to the IC. Connect the input capacitors directly between STR and PGND pins on the top layer. Routing these traces on the top layer eliminates the need for vias.
2. Minimize the switch node trace length between the SW pin and the inductor. Optimal switch node routing is to run the trace between the input capacitor's pads. Using 1206 or larger sized input capacitors is recommended. Avoid routing sensitive analog signals near these high frequency, high dV/dt traces.
3. The Buck output capacitors should be placed by the inductor and connected directly to the inductor and ground plane with short and wide traces. The output capacitor ground should make a short connection to the input capacitor ground. If required, use multiple vias.
4. The FB pin should be Kelvin connected to the output capacitor through the shortest possible route, while keeping sufficient distance from switching node to prevent noise injection. The IC regulates the output voltage to this Kelvin connection.
5. Connect the PGND and VSS ground pins must be electrically connected together. The VSS ground plane should be isolated from the rest of the PCB power ground.
6. Remember that all open drain outputs need pull-up resistors.
7. Connect the exposed pad directly to the top layer ground plane. Connect the top layer ground plane to both internal ground planes and the PCB backside ground plane with thermal vias. Provide ground plane routing on multiple layers to allow the IC's heat to flow into the PCB and then spread radially from the IC. Avoid cutting the ground planes or adding vias that restrict the radial flow of heat.

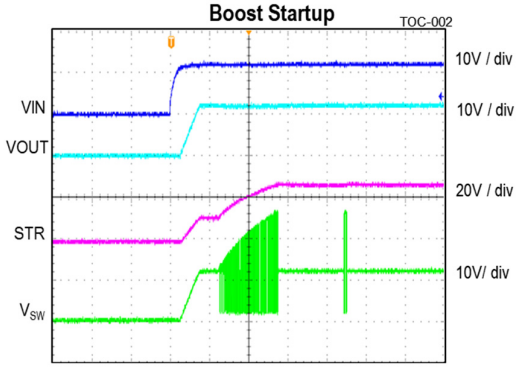
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Typical Operating Characteristics

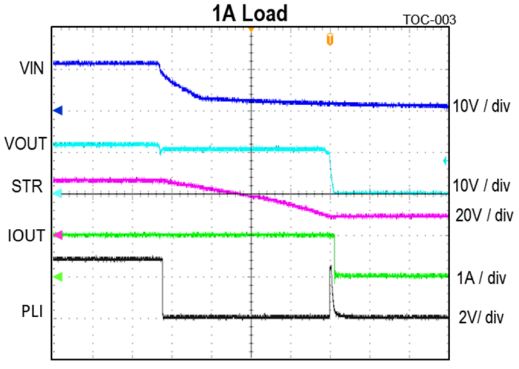
CMI 121
Startup Sequencing
TOC-001



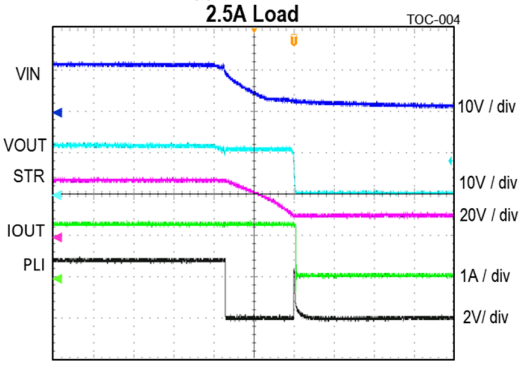
CMI 121
Boost Startup
TOC-002



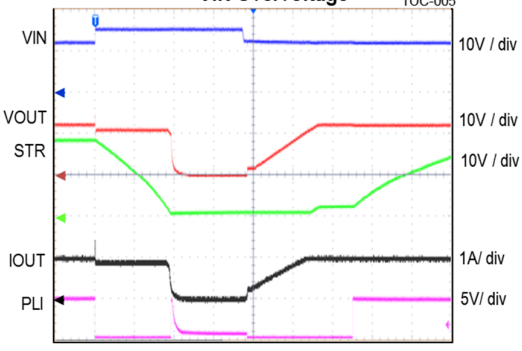
CMI 121
Supplement Mode
1A Load
TOC-003



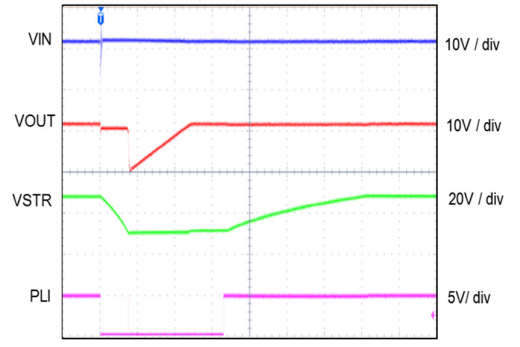
CMI 121
Supplement Mode
2.5A Load
TOC-004



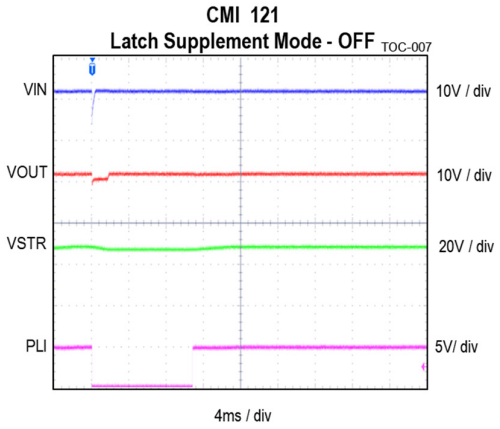
CMI 121
Supplement Mode
VIN Overvoltage
TOC-005

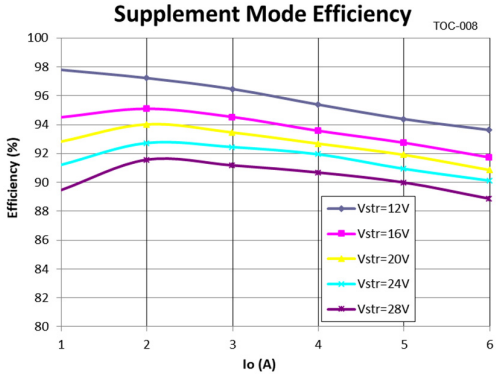


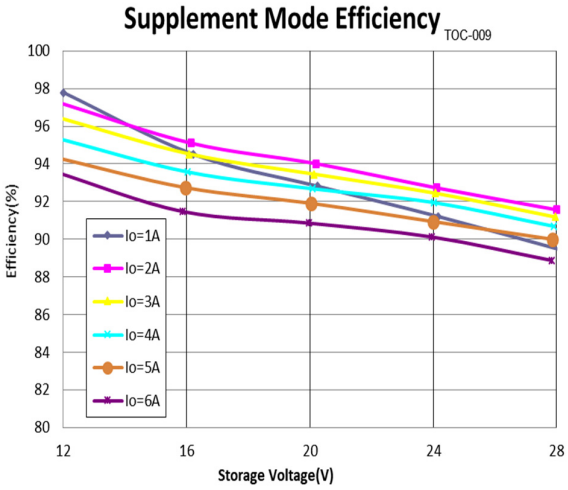
CMI 121
Latch Supplement Mode - ON
TOC-006

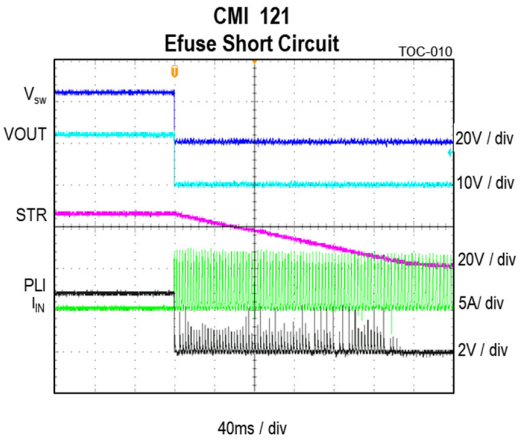


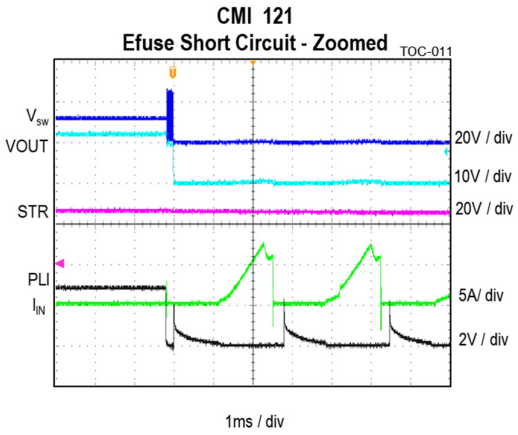
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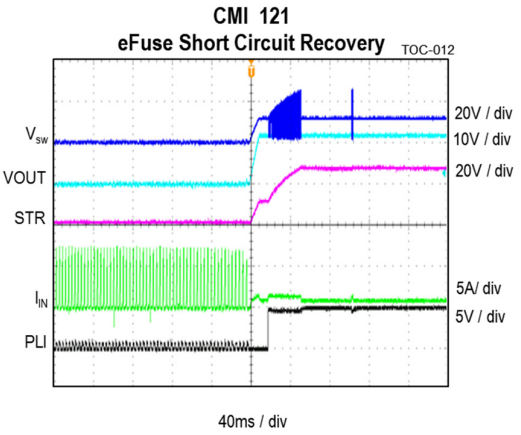






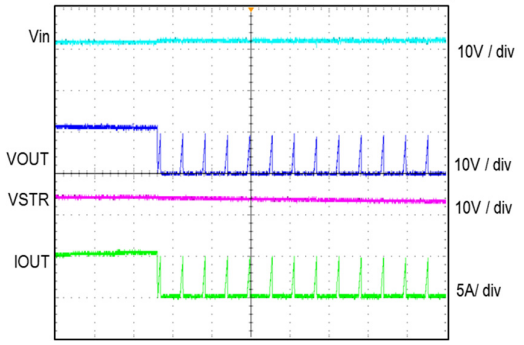




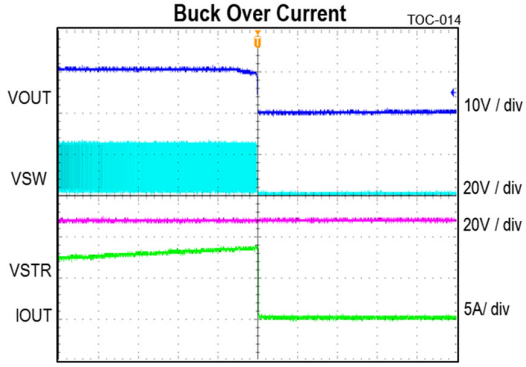


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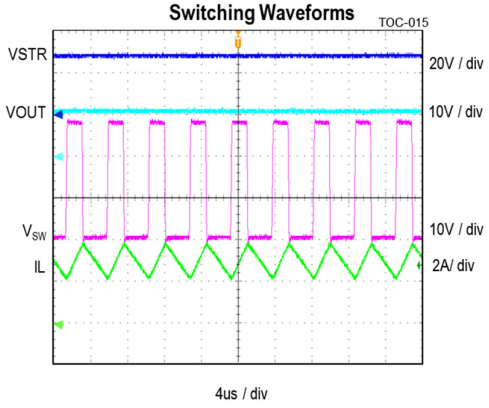
CMI 121
Efuse Over Current
TOC-013



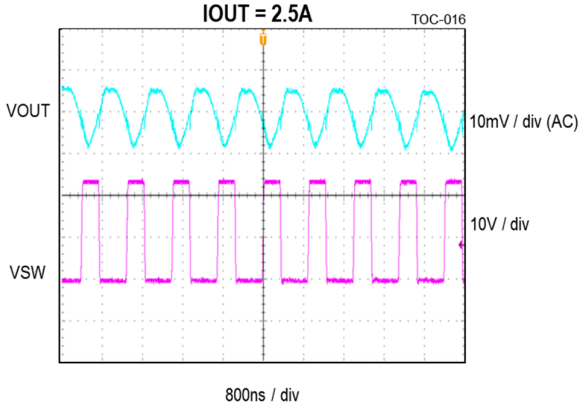
CMI 121
Buck Over Current
TOC-014



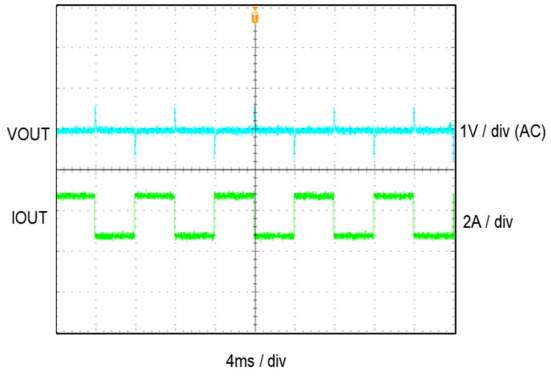
CMI 121
Switching Waveforms
TOC-015



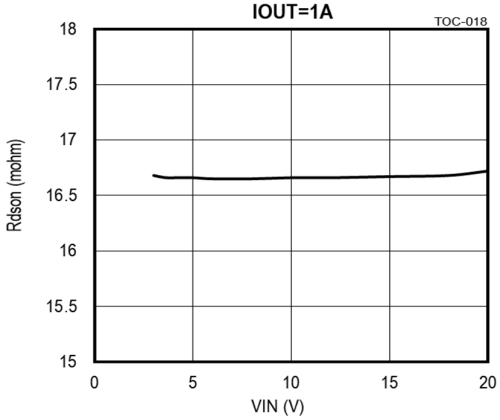
CMI 121
Output Ripple
IOUT = 2.5A
TOC-016



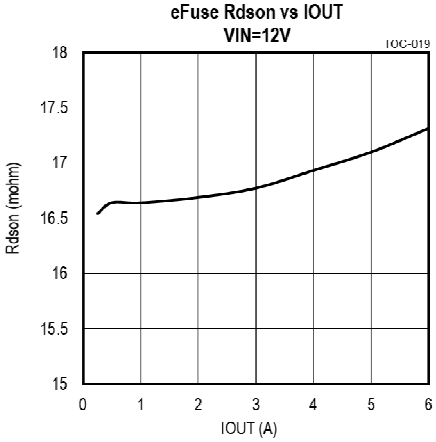
CMI 121
Buck Load Transient
TOC-017



eFuse Rdson vs VIN
IOUT=1A
TOC-018



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CMI OPTIONS

This section provides the basic default configuration settings for each available ACT4910 CMI option. Refer to each option's application note for the comprehensive list of default settings

CMI 121: ACT4910QW121

CMI 121 is designed for standard 12V applications. CMI 121 default settings are appropriate for most typical applications. It provides the fastest buck switching frequency for the smallest solution sizes. Table 10 shows the default register settings.

Table 10: CMI 121 Default Register Settings

Function	Value	Register	Register Settings
PLI Pin Function	PLI & VOUT OK	0x19h	PLI_FUNC_SEL[1:0] = 11
Health Monitor Time	32ms	0x1Fh	HMON_TSET[3:0] = 0100
Health Monitor Threshold	96%	0x20h	HMON_THR[3:0] = 0101
Enable Overvoltage Reference	0.92V	0x20h	EN_OV_REF[2:0] = 010
Startup Delay	0ms	0x20h	EN_STARTDELAY = 0
Latch Supplement Mode	Yes	0x21h	EN_LATCH_SPLMNT = 1
Boost Current Limit	950mA	0x21h	BST_CLIM[1:0] = 10
Boost Voltage	28V	0x21h	BST_VSET[4:0] = 10111
Buck Peak Current Limit	9A	0x26h	BK_CLIM[1:0] = 11
Buck Switching Frequency	1130kHz	0x28h	BK_FREQ[2:0] = 111

I2C Address

The CMI 121 7-bit I2C address is 0x5Ah. This results in 0xB4h for a write address and 0xB5h for a read address.

Device ID

The CMI 121 Device ID (register 0x3Bh) = 0x02h. This can be used to distinguish between different CMI versions.

Autonomous ADC Supervisory Function

The autonomous ADC supervisory function is disabled by default. All undervoltage register value are set to 0x00h and all overvoltage register values are set to 0xFFh.

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CMI 122: ACT4910QW122

CMI 121 is designed for standard 12V applications. CMI 121 default settings are appropriate for most typical applications. It provides the 900kHz buck switching frequency to compromise size and efficiency. The default storage voltage is 36V which allows for maximum capacitor energy storage. Placing a resistor between BSET and VSS can program the default storage voltage to a lower value. Table 11 shows the default register settings.

Table 11: CMI 122 Default Register Settings

Function	Value	Register	Register Settings
PLI Pin Function	PLI & VOUT OK	0x19h	PLI_FUNC_SEL[1:0] = 11
Health Monitor Time	32ms	0x1Fh	HMON_TSET[3:0] = 0100
Health Monitor Threshold	97.2%	0x20h	HMON_THR[3:0] = 1011
Enable Overvoltage Reference	0.92V	0x20h	EN_OV_REF[2:0] = 010
Startup Delay	0ms	0x20h	EN_STARTDELAY = 0
Latch Supplement Mode	Yes	0x21h	EN_LATCH_SPLMNT = 1
Boost Current Limit	950mA	0x21h	BST_CLIM[1:0] = 10
Boost Voltage	36V	0x21h	BST_VSET[4:0] = 11111
Buck Peak Current Limit	9A	0x26h	BK_CLIM[1:0] = 11
Buck Switching Frequency	900kHz	0x28h	BK_FREQ[2:0] = 110

I2C Address

The CMI 122 7-bit I2C address is 0x5Ah. This results in 0xB4h for a write address and 0xB5h for a read address.

Device ID

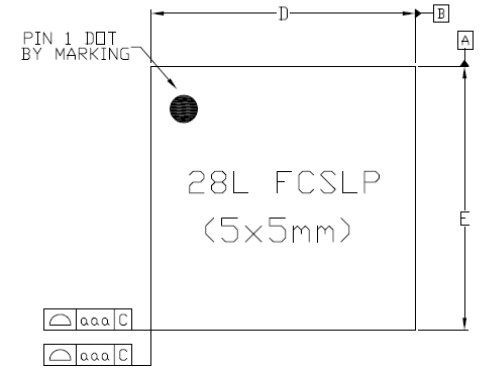
The CMI 122 Device ID (register 0x3Bh) = 0x03h. This can be used to distinguish between different CMI versions.

Autonomous ADC Supervisory Function

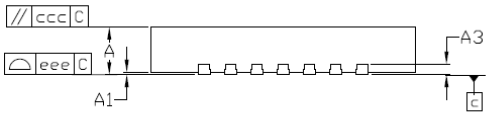
The autonomous ADC supervisory function is disabled by default. All undervoltage register value are set to 0x00h and all overvoltage register values are set to 0xFFh.

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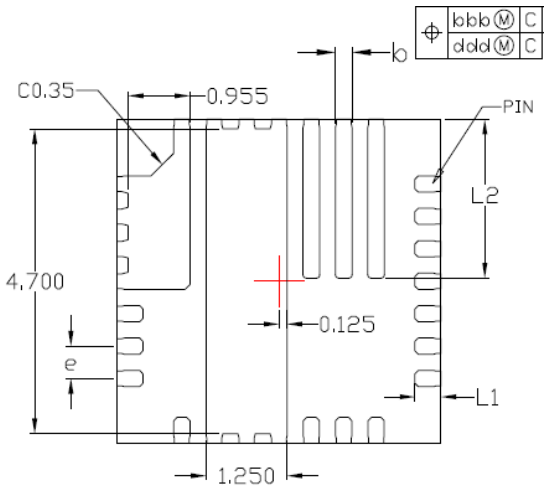
PACKAGE OUTLINE AND DIMENSIONS QFN5X5-28



TOP VIEW



SIDE VIEW



BOTTOM VIEW

Dimensional Ref.			
REF.	Min.	Nom.	Max.
A	0.800	0.850	0.900
A1	---	---	0.050
A3	0.203 Ref.		
D	4.950	0.500	5.050
E	4.950	0.500	5.050
--		--	
b	0.200	0.250	0.300
e	0.500 BSC		
L1	0.350	0.400	0.450
L2	2.400	2.450	2.500
Tol. of Form&Position			
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		

See Active Semi Application note AN-104, QFN PCB Layout Guidelines for more information on generating the ACT4910 land pattern.

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