Filterless High Efficiency Mono 3 W Class-D Audio Amplifier

SSM2311

FEATURES

Filterless Class-D amplifier with Σ-Δ modulation
No sync necessary when using multiple Analog Devices, Inc., Class-D amplifiers
3 W into 3 Ω load and 1.4 W into 8 Ω load at 5.0 V supply with less than 10% total harmonic distortion (THD)
90% efficiency at 5.0 V, 1.4 W into 8 Ω speaker
Better than 98 dB signal-to-noise ratio (SNR)
Single-supply operation from 2.5 V to 5.5 V
20 nA ultralow shutdown current
Short-circuit and thermal protection
Available in 9-ball, 1.5 mm × 1.5 mm WLCSP
Pop-and-click suppression
Built-in resistors reduce board component count
Default fixed 18 dB or user-adjustable gain setting

APPLICATIONS

Mobile phones
MP3 players
Portable gaming
Portable electronics
Educational toys

GENERAL DESCRIPTION

The SSM2311 is a fully integrated, high efficiency, Class-D audio amplifier. It is designed to maximize performance for mobile phone applications. The application circuit requires a minimum of external components and operates from a single 2.5 V to 5.5 V supply. It is capable of delivering 3 W of continuous output power with less than 1% THD + N driving a 3 Ω load from a 5.0 V supply.

The SSM2311 features a high efficiency, low noise modulation scheme that does not require any external LC output filters. The modulation continues to provide high efficiency even at low output power. It operates with 90% efficiency at 1.4 W into 8 Ω or 85% efficiency at 3 W into 3 Ω from a 5.0 V supply and has an SNR that is better than 98 dB. Spread-spectrum pulse density modulation is used to provide lower EMI-radiated emissions compared with other Class-D architectures.

The SSM2311 has a micropower shutdown mode with a typical shutdown current of 20 nA. Shutdown is enabled by applying a logic low to the $\overline{SD}$ pin.

The device also includes pop-and-click suppression circuitry. This minimizes voltage glitches at the output during turn-on and turn-off, thus reducing audible noise on activation and deactivation.

The fully differential input of the SSM2311 provides excellent rejection of common-mode noise on the input. Input coupling capacitors can be omitted if the dc input common-mode voltage is approximately $V_{DD}/2$.

The default gain of SSM2311 is 18 dB, but users can reduce the gain by using a pair of external resistors (see the Gain section).

The SSM2311 is specified over the industrial temperature range (−40°C to +85°C). It has built-in thermal shutdown and output short-circuit protection. It is available in a 9-ball, 1.5 mm × 1.5 mm wafer level chip scale package (WLCSP).

FUNCTIONAL BLOCK DIAGRAM

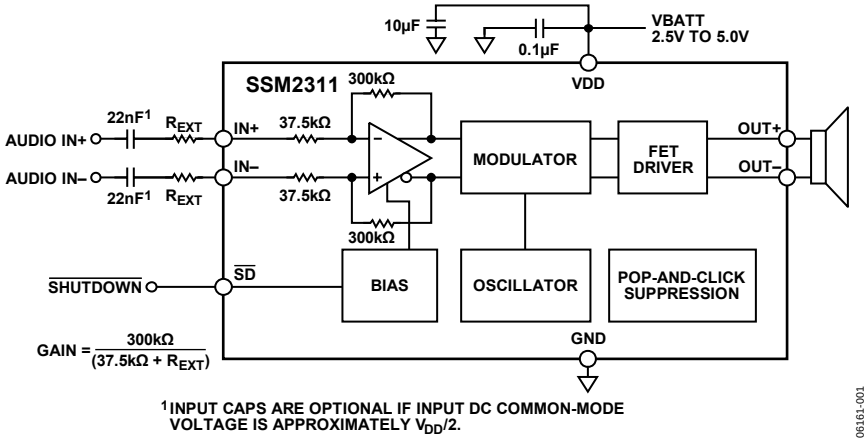


Figure 1.

Rev. 0
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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.461.3113 **©2008 Analog Devices, Inc. All rights reserved.**

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REVISION HISTORY

1/08—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 5.0 V, T_A = 25°C, R_L = 8 Ω, unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DEVICE CHARACTERISTICS						
Output Power	P_O	R_L = 8 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, V_{DD} = 5.0 V		1.2		W
		R_L = 8 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, V_{DD} = 3.6 V		0.615		W
		R_L = 8 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, V_{DD} = 5.0 V		1.53		W
		R_L = 8 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, V_{DD} = 3.6 V		0.77		W
		R_L = 4 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, V_{DD} = 5.0 V		2		W
		R_L = 4 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, V_{DD} = 3.6 V		1.4		W
		R_L = 4 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, V_{DD} = 5.0 V		2.3		W
		R_L = 4 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, V_{DD} = 3.6 V		1.6		W
		R_L = 3 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, V_{DD} = 5.0 V		3		W
		R_L = 3 Ω, THD = 1%, f = 1 kHz, 20 kHz BW, V_{DD} = 3.6 V		1.8		W
		R_L = 3 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, V_{DD} = 5.0 V		3.3		W
		R_L = 3 Ω, THD = 10%, f = 1 kHz, 20 kHz BW, V_{DD} = 3.6 V		2.5		W
Efficiency	η	P_{OUT} = 1.4 W, 8 Ω, V_{DD} = 5.0 V		89		%
Total Harmonic Distortion + Noise	THD + N	P_O = 3 W into 3 Ω, f = 1 kHz, V_{DD} = 5.0 V		0.5		%
		P_O = 1 W into 8 Ω, f = 1 kHz, V_{DD} = 5.0 V		0.2		%
Input Common-Mode Voltage Range	V_{CM}		1.0		V_{DD} − 1.0	V
Common-Mode Rejection Ratio	$CMRR_{GSM}$	V_{CM} = 2.5 V ± 100 mV at 217 Hz input referred		60		dB
Average Switching Frequency	f_{SW}			800		kHz
Differential Output Offset Voltage	V_{OOS}	G = 18 dB		2.0	12.0	mV
POWER SUPPLY						
Supply Voltage Range	V_{DD}	Guaranteed from PSRR test	2.5		5.0	V
Power Supply Rejection Ratio	PSRR	V_{DD} = 2.5 V to 5.0 V, dc input floating/ground	70	85		dB
	$PSRR_{GSM}$	V_{RIPPLE} = 100 mV at 217 Hz, inputs ac GND, C_{IN} = 0.1 µF		60		dB
Supply Current	I_{SY}	V_{IN} = 0 V, no load, V_{DD} = 5.0 V		5.5		mA
		V_{IN} = 0 V, no load, V_{DD} = 3.6 V		4.5		mA
		V_{IN} = 0 V, no load, V_{DD} = 2.5 V		4.0		mA
Shutdown Current	I_{SD}	$\overline{SD}$ = GND		20		nA
GAIN CONTROL						
Closed-Loop Gain	Av			18		dB
Differential Input Impedance	Z_{IN}	$\overline{SD}$ = VDD		37.5		kΩ
SHUTDOWN CONTROL						
Input Voltage High	V_{IH}	I_{SY} ≥ 1 mA		1.2		V
Input Voltage Low	V_{IL}	I_{SY} ≤ 300 nA		0.5		V
Turn-On Time	t_{WU}	$\overline{SD}$ rising edge from GND to V_{DD}		30		ms
Turn-Off Time	t_{SD}	$\overline{SD}$ falling edge from V_{DD} to GND		5		µs
Output Impedance	Z_{OUT}	$\overline{SD}$ = GND		>100		kΩ
NOISE PERFORMANCE						
Output Voltage Noise	e_n	V_{DD} = 3.6 V, f = 20 Hz to 20 kHz, inputs are ac grounded, A_V = 18 dB, A weighting		35		µV
Signal-to-Noise Ratio	SNR	P_{OUT} = 1.4 W, R_L = 8 Ω		98		dB

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings apply at 25°C, unless otherwise noted.

Table 2.

Parameter	Rating
Supply Voltage	6 V
Input Voltage	V_{DD}
Common-Mode Input Voltage	V_{DD}
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Junction Temperature Range	−65°C to +165°C
Lead Temperature (Soldering, 60 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	PCB	θ_{JA}	θ_{JB}	Unit
9-Ball, 1.5 mm × 1.5 mm WLCSP	1S0P[1]	162	38.5	°C/W
	2S0P[1]	76	21	°C/W

[1] Referencing the JEDEC thermal standard.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

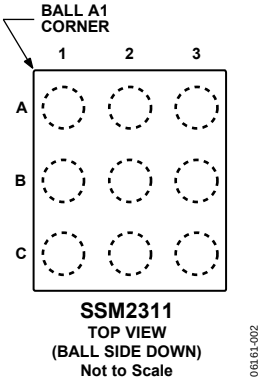


Figure 2. SSM2311 WLCSP Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
2C	$\overline{SD}$	Shutdown Input. Active low digital input.
1A	IN+	Noninverting Input.
1C	IN–	Inverting Input.
3C	OUT–	Inverting Output.
1B	VDD	Power Supply.
2A, 3B	GND	Ground.
3A	OUT+	Noninverting Output.
2B	PVDD	Power Supply.

TYPICAL PERFORMANCE CHARACTERISTICS

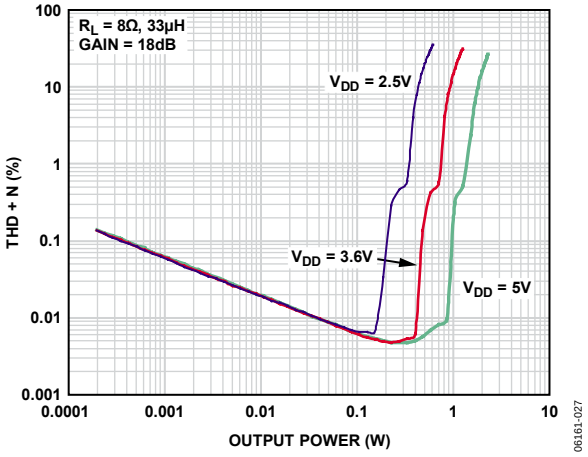


Figure 3. THD + N vs. Output Power into 8 Ω, A_V = 18 dB

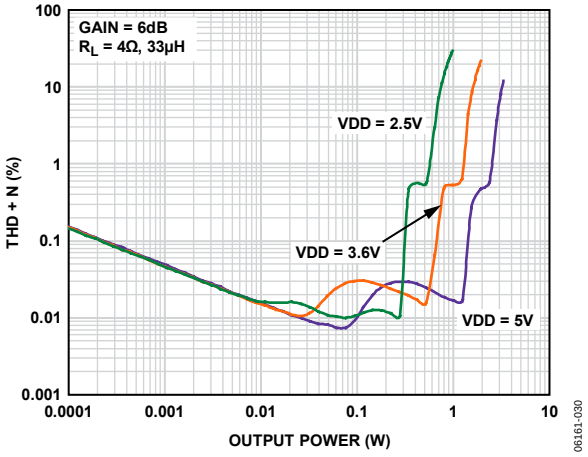


Figure 6. THD + N vs. Output Power into 4 Ω, A_V = 6 dB

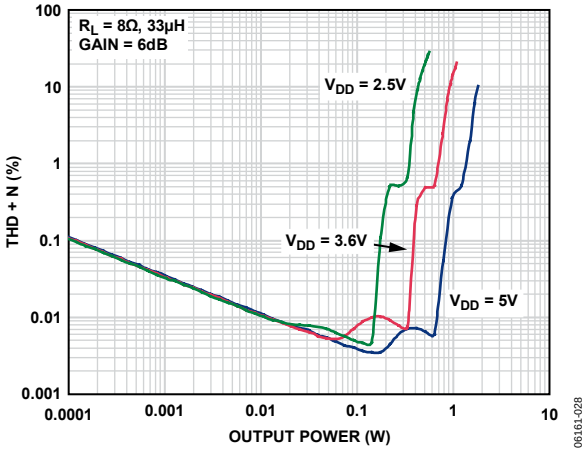


Figure 4. THD + N vs. Output Power into 8 Ω, A_V = 6 dB

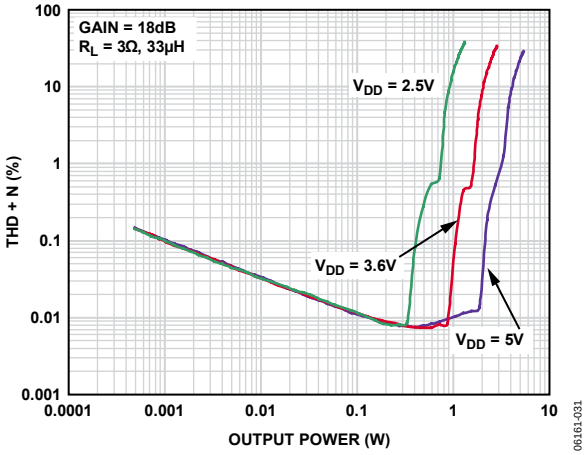


Figure 7. THD + N vs. Output Power into 3 Ω, A_V = 18 dB

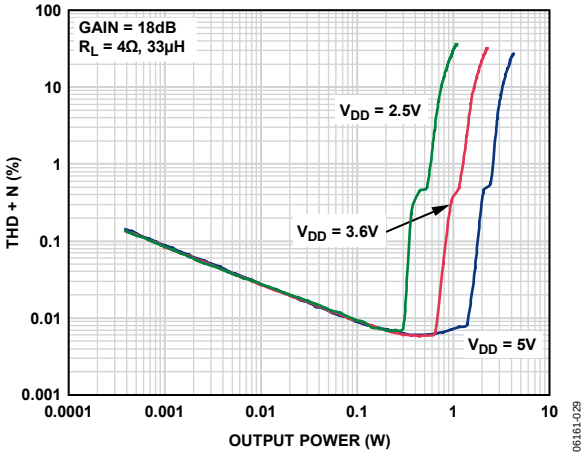


Figure 5. THD + N vs. Output Power into 4 Ω, A_V = 18 dB

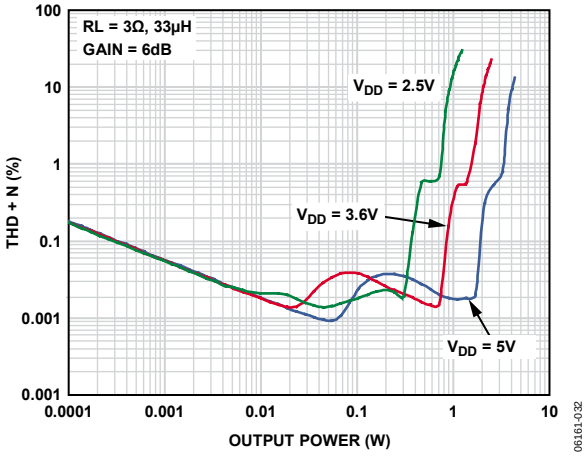


Figure 8. THD + N vs. Output Power into 3 Ω, A_V = 6 dB

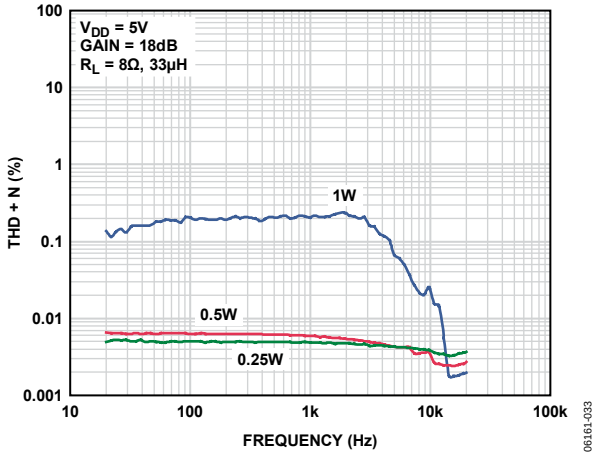


Figure 9. THD + N vs. Frequency, V_{DD} = 5.0 V, R_L = 8 Ω, A_V = 18 dB

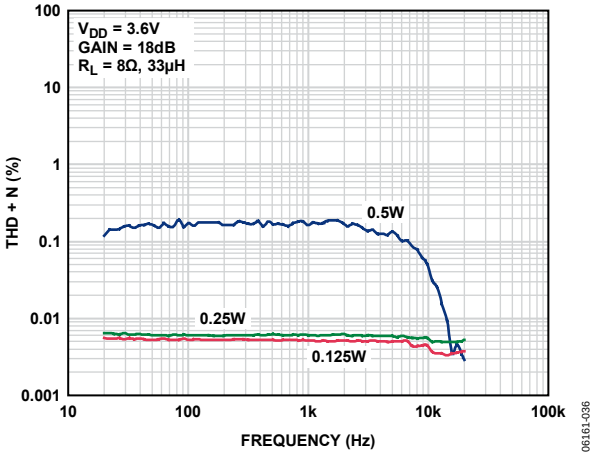


Figure 12. THD + N vs. Frequency, V_{DD} = 3.6 V, R_L = 8 Ω, A_V = 18 dB

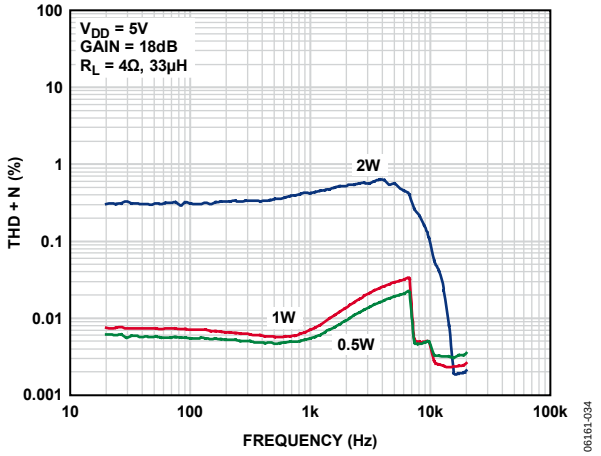


Figure 10. THD + N vs. Frequency, V_{DD} = 5.0 V, R_L = 4 Ω, A_V = 18 dB

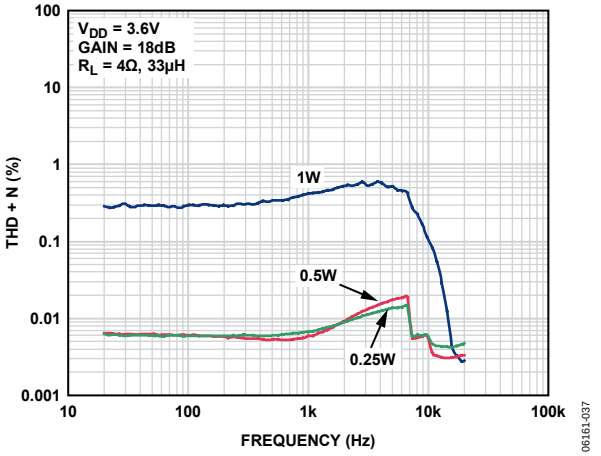


Figure 13. THD + N vs. Frequency, V_{DD} = 3.6 V, R_L = 4 Ω, A_V = 18 dB

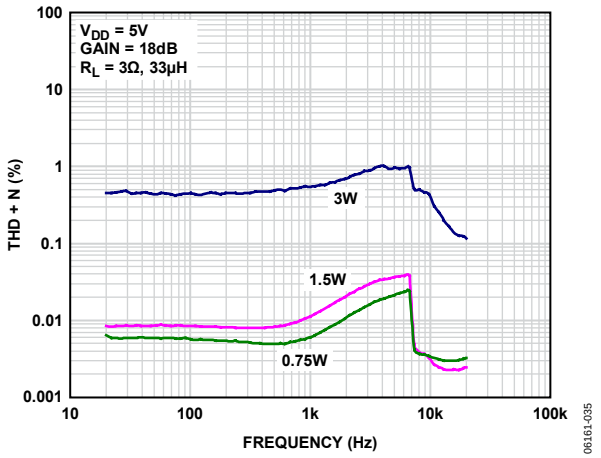


Figure 11. THD + N vs. Frequency, V_{DD} = 5.0 V, R_L = 3 Ω, A_V = 18 dB

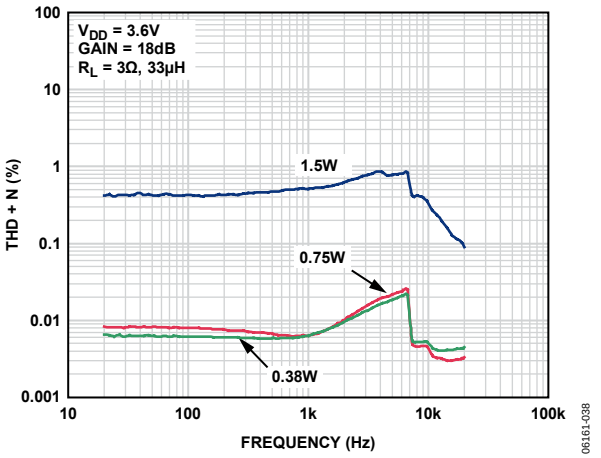


Figure 14. THD + N vs. Frequency, V_{DD} = 3.6 V, R_L = 3 Ω, A_V = 18 dB

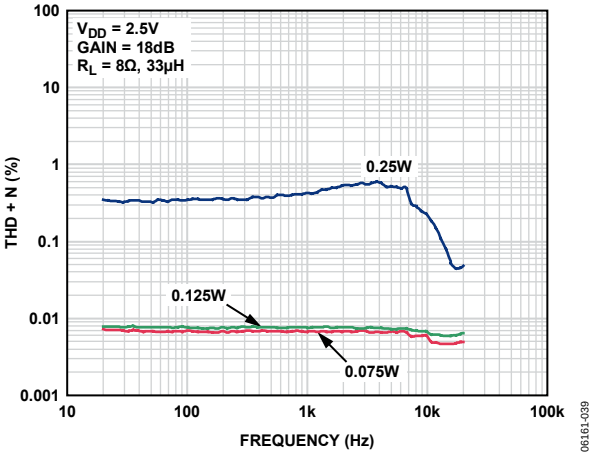


Figure 15. THD + N vs. Frequency, V_{DD} = 2.5 V, R_L = 8 Ω, A_V = 18 dB

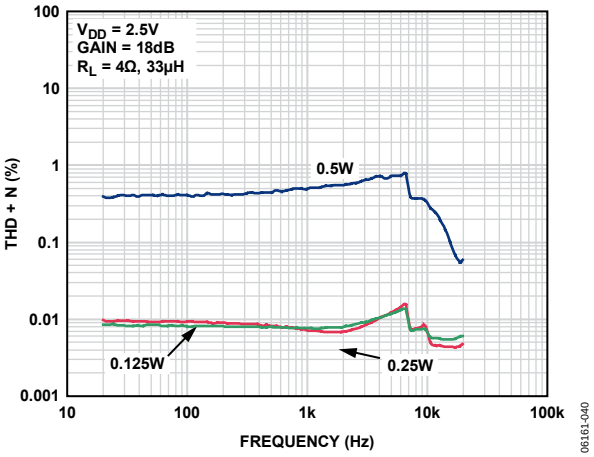


Figure 16. THD + N vs. Frequency, V_{DD} = 2.5 V, R_L = 4 Ω, A_V = 18 dB

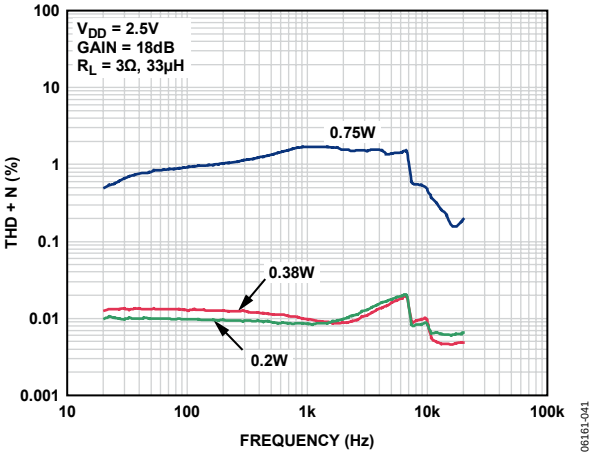


Figure 17. THD + N vs. Frequency, V_{DD} = 2.5 V, R_L = 3 Ω, A_V = 18 dB

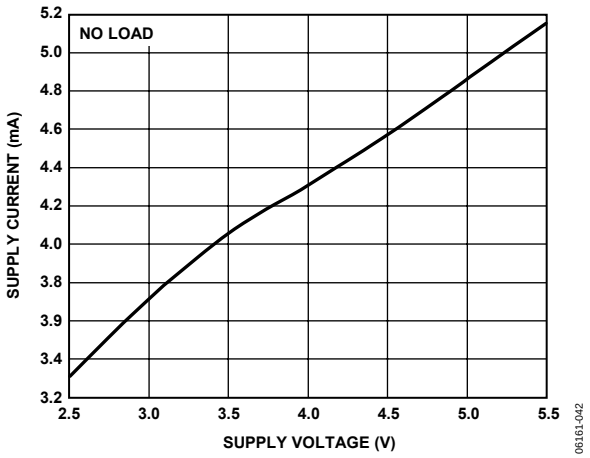


Figure 18. Supply Current vs. Supply Voltage, No Load

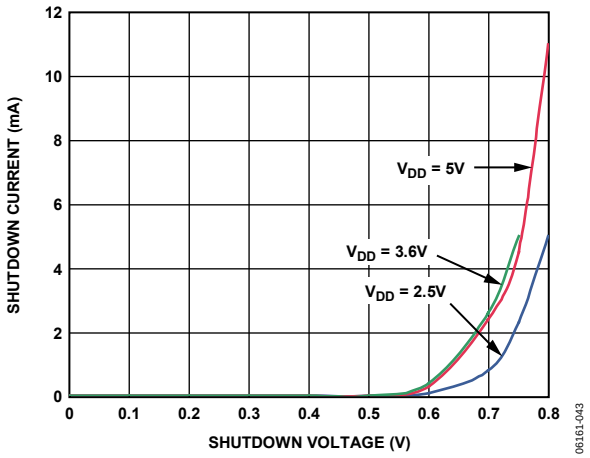


Figure 19. Shutdown Current vs. Shutdown Voltage

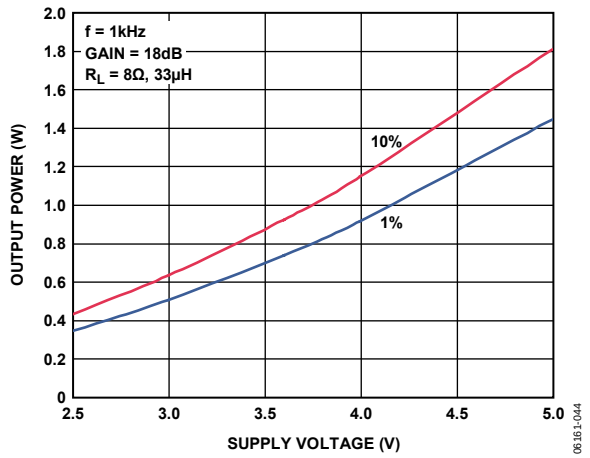


Figure 20. Maximum Output Power vs. Supply Voltage, R_L = 8 Ω, A_V = 18 dB

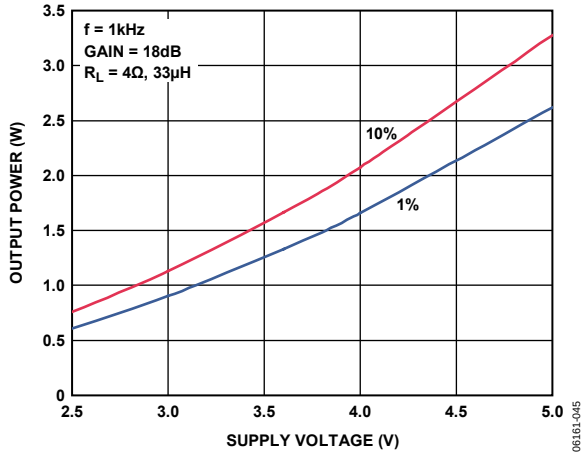


Figure 21. Maximum Output Power vs. Supply Voltage, R_L = 4 Ω, A_V = 18 dB

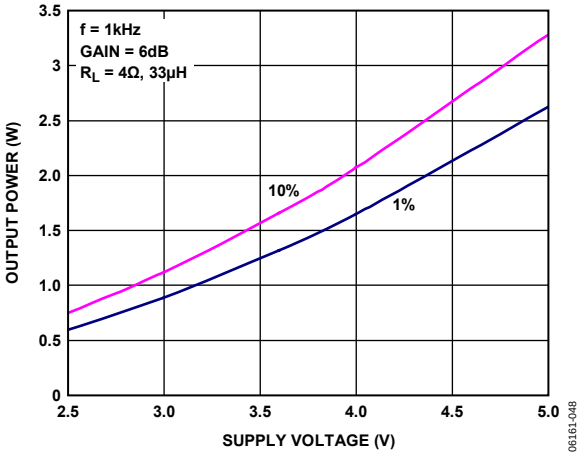


Figure 24. Maximum Output Power vs. Supply Voltage, R_L = 4 Ω, A_V = 6 dB

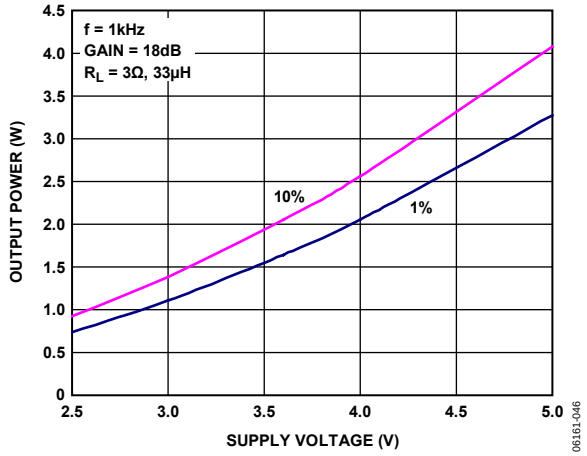


Figure 22. Maximum Output Power vs. Supply Voltage, R_L = 3 Ω, A_V = 18 dB

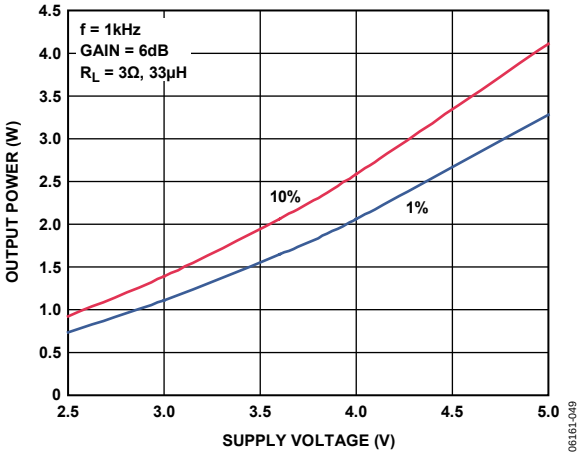


Figure 25. Maximum Output Power vs. Supply Voltage, R_L = 3 Ω, A_V = 6 dB

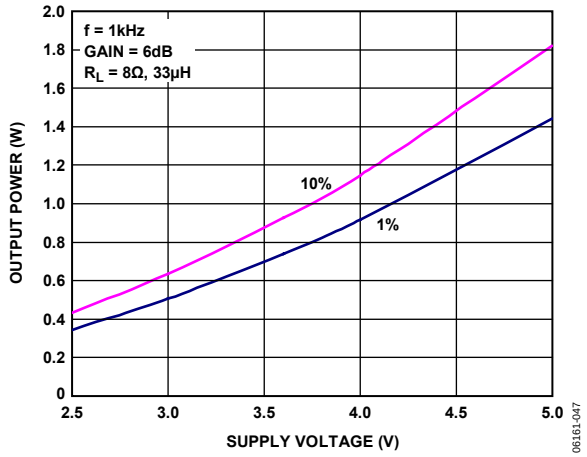


Figure 23. Maximum Output Power vs. Supply Voltage, R_L = 8 Ω, A_V = 6 dB

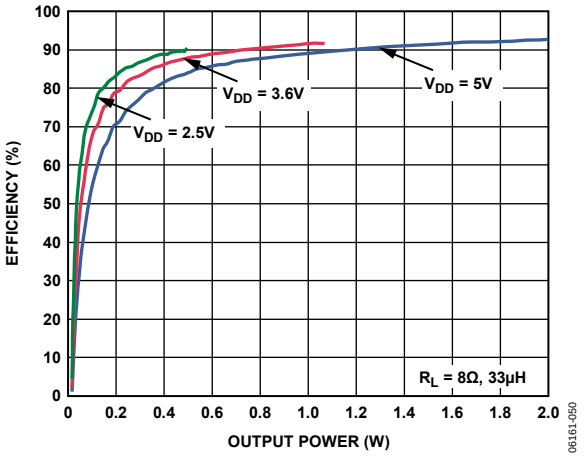


Figure 26. Efficiency vs. Output Power into 8 Ω

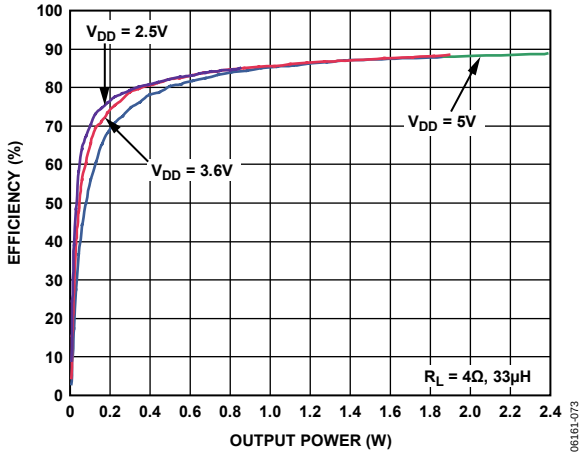


Figure 27. Efficiency vs. Output Power into 4 Ω

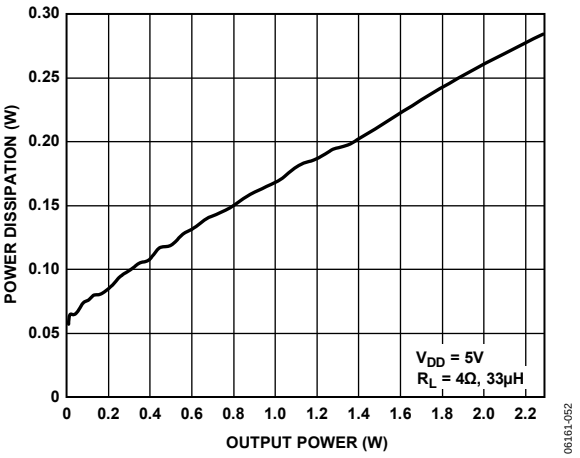


Figure 30. Power Dissipation vs. Output Power into 4 Ω at V_{DD} = 5.0 V

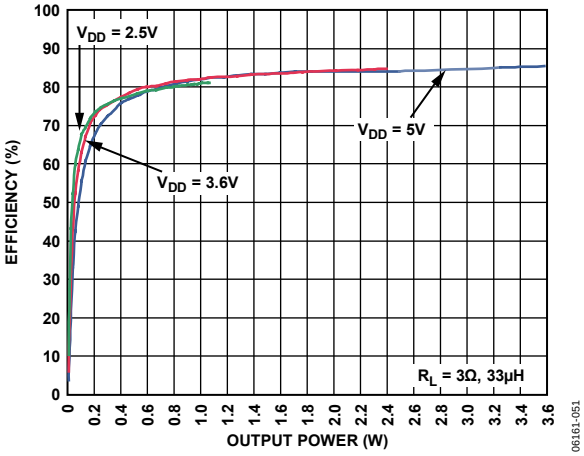


Figure 28. Efficiency vs. Output Power into 3 Ω

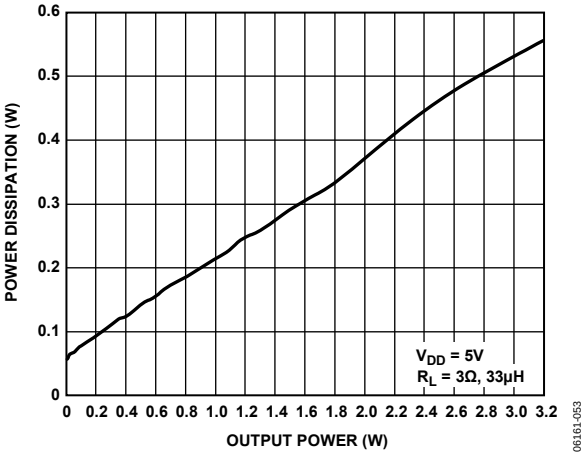


Figure 31. Power Dissipation vs. Output Power into 3 Ω at V_{DD} = 5.0 V

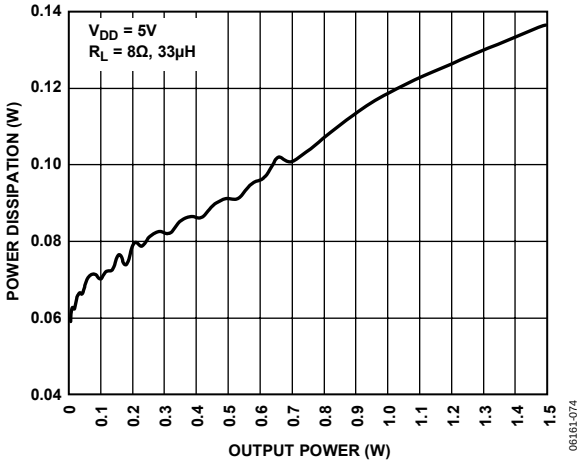


Figure 29. Power Dissipation vs. Output Power into 8 Ω at V_{DD} = 5.0 V

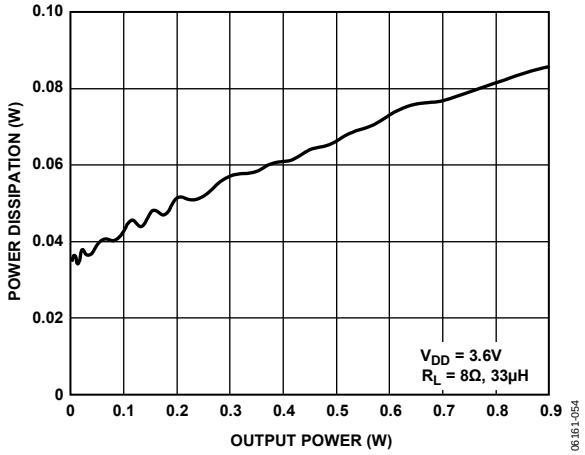


Figure 32. Power Dissipation vs. Output Power into 8 Ω at V_{DD} = 3.6 V

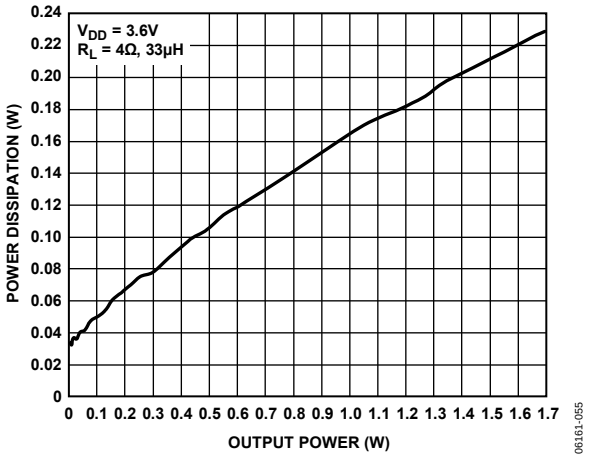


Figure 33. Power Dissipation vs. Output Power into 4 Ω at V_{DD} = 3.6 V

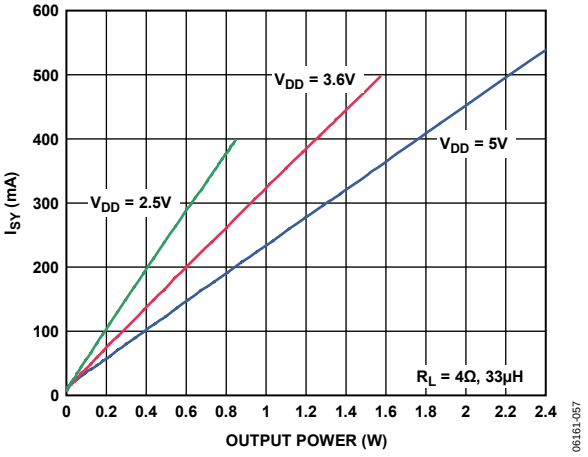


Figure 36. Supply Current vs. Output Power into 4 Ω

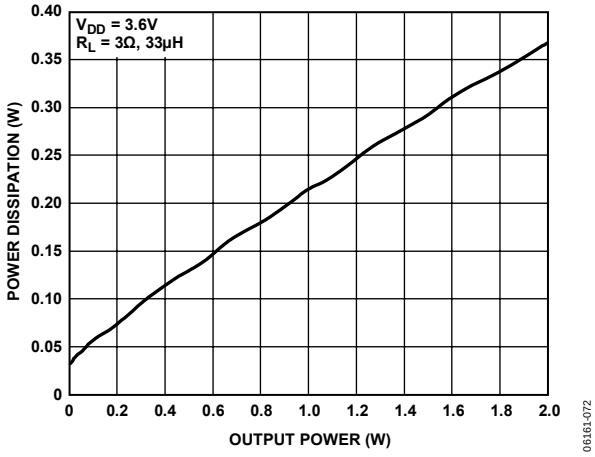


Figure 34. Power Dissipation vs. Output Power into 3 Ω at V_{DD} = 3.6 V

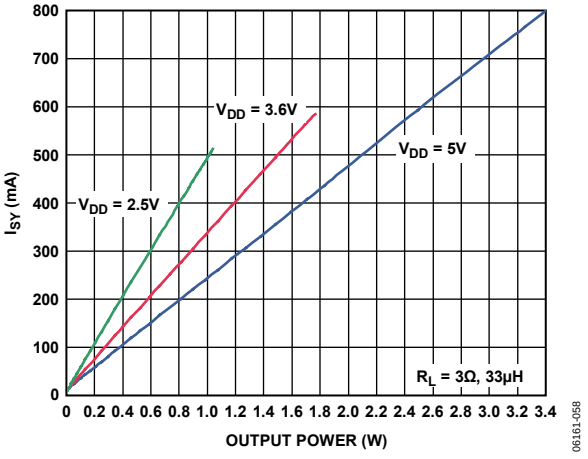


Figure 37. Supply Current vs. Output Power into 3 Ω

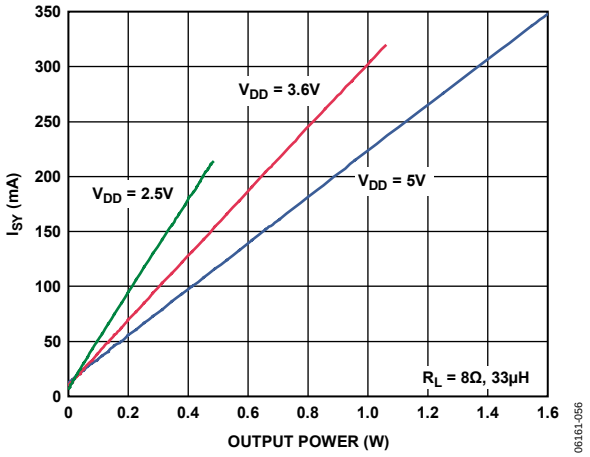


Figure 35. Supply Current vs. Output Power into 8 Ω

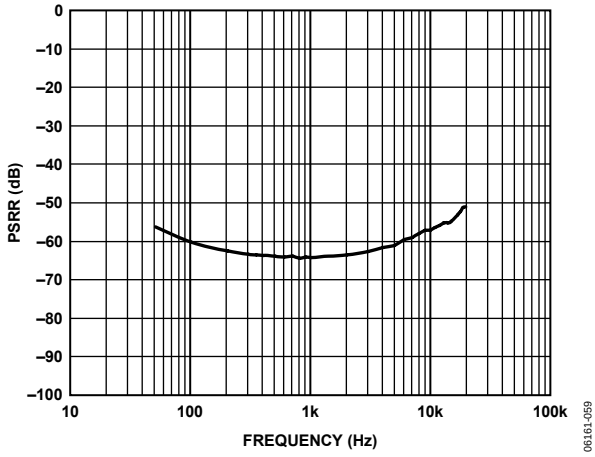


Figure 38. Power Supply Rejection Ratio vs. Frequency

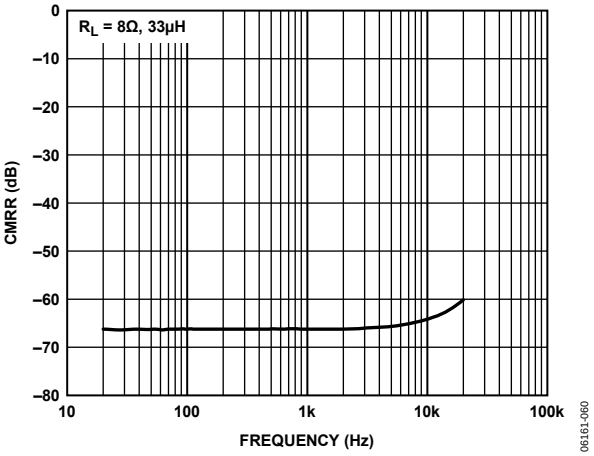


Figure 39. Common-Mode Rejection Ratio vs. Frequency

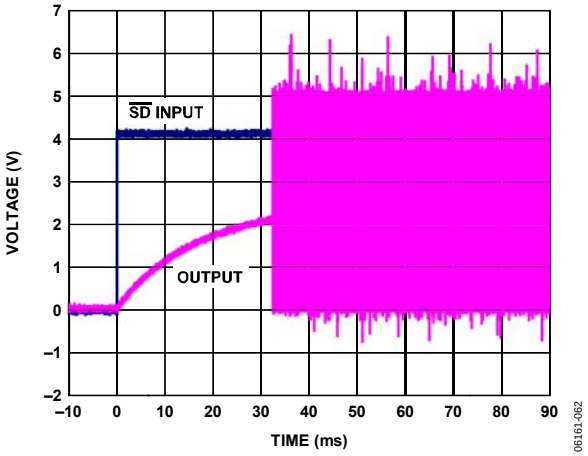


Figure 41. Turn-On Response

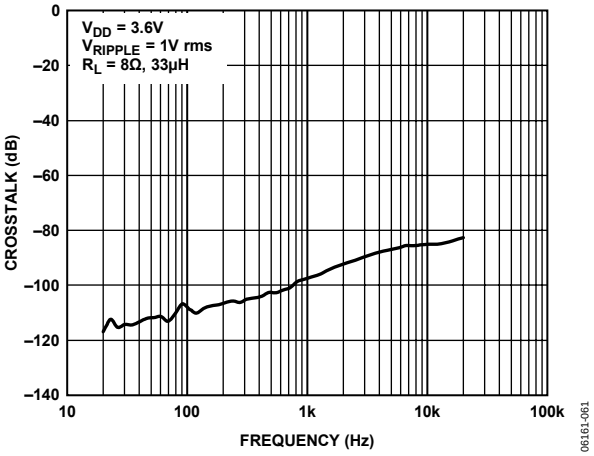


Figure 40. Crosstalk vs. Frequency

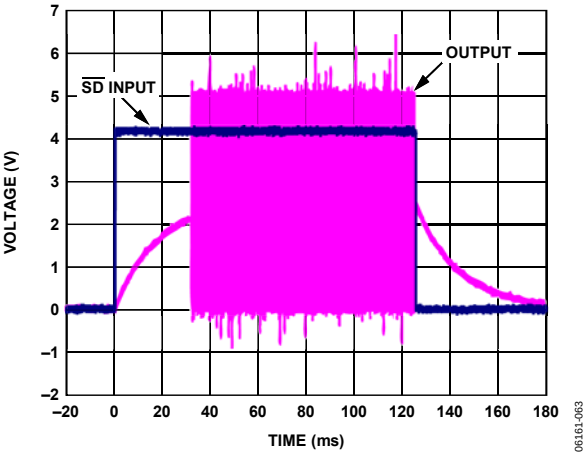


Figure 42. Turn-Off Response

TYPICAL APPLICATION CIRCUITS

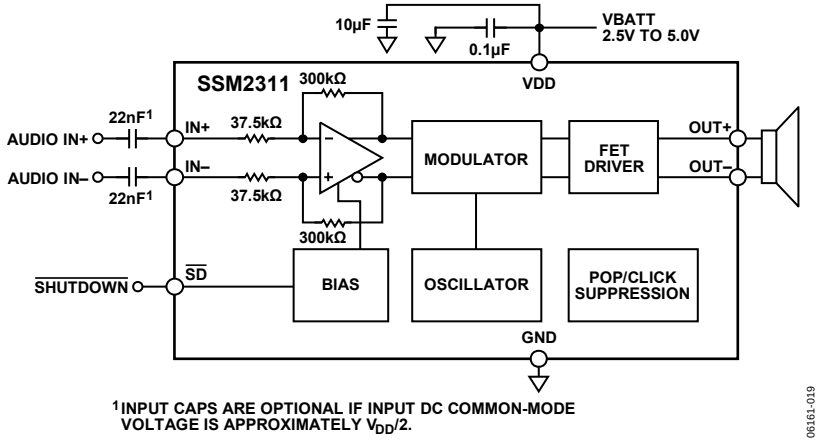


Figure 43. Differential Input Configuration

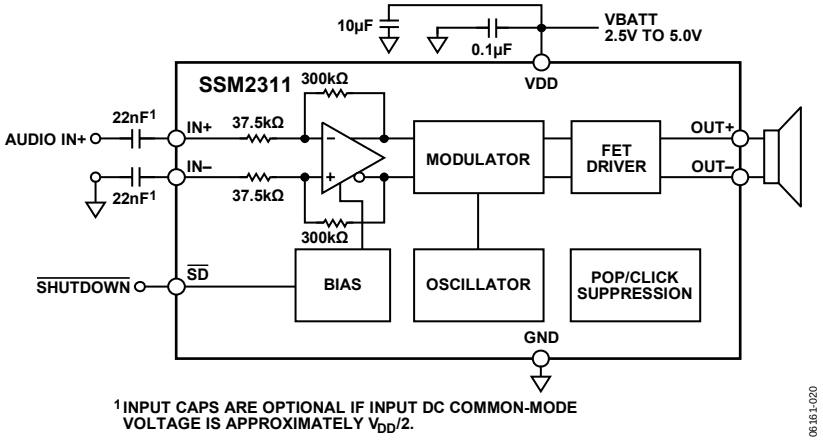


Figure 44. Single-Ended Input Configuration

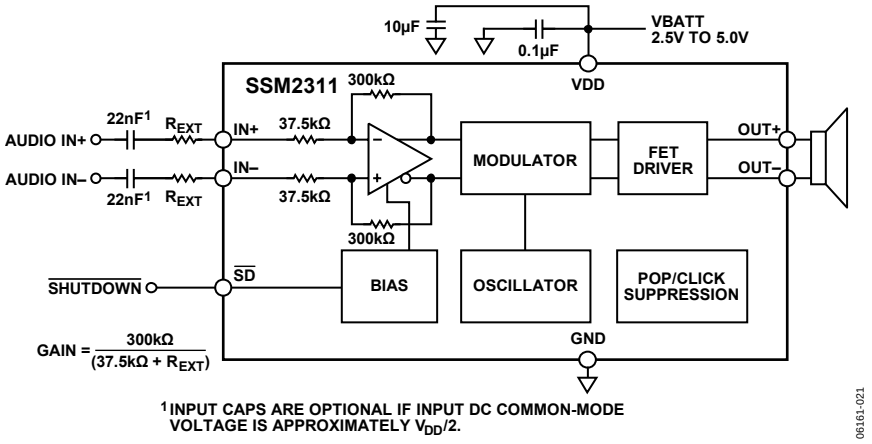


Figure 45. Differential Input Configuration, User-Adjustable Gain

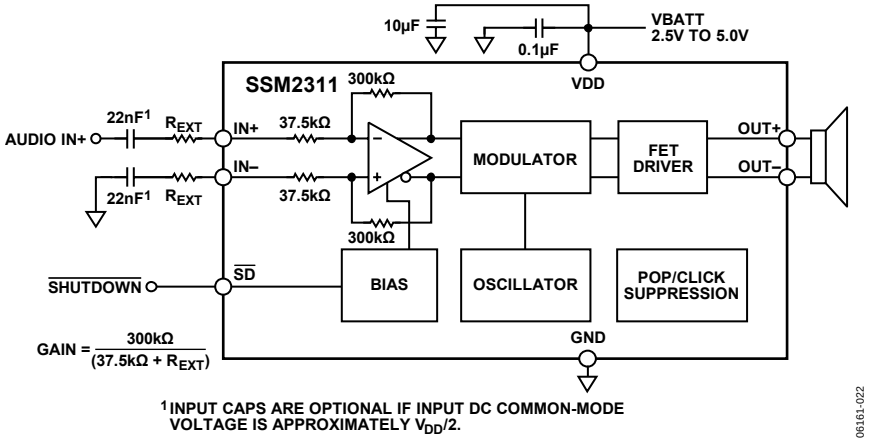


Figure 46. Single-Ended Input Configuration, User-Adjustable Gain

APPLICATION NOTES

OVERVIEW

The SSM2311 mono Class-D audio amplifier features a filterless modulation scheme that greatly reduces the external components count, conserving board space and thus reducing the system's cost. The SSM2311 does not require an output filter, but instead relies on the inherent inductance of the speaker coil and the natural filtering of the speaker and the human ear to fully recover the audio component of the square-wave output. While many Class-D amplifiers use some variation of pulse-width modulation (PWM), the SSM2311 uses Σ-Δ modulation to determine the switching pattern of the output devices. This provides a number of important benefits. Σ-Δ modulators do not produce a sharp peak with many harmonics in the AM frequency band, as pulse-width modulators often do. Σ-Δ modulation provides the benefits of reducing the amplitude of spectral components at high frequencies; that is, reducing EMI emission that might otherwise be radiated by speakers and long cable traces. Due to the inherent spread-spectrum nature of Σ-Δ modulation, the need for oscillator synchronization is eliminated for designs incorporating multiple SSM2311 amplifiers.

The SSM2311 also offers protection circuits for overcurrent and temperature protection.

GAIN

The SSM2311 has a default gain of 18 dB, but can be reduced by using a pair of external resistors with a value calculated as follows:

$$External\ Gain\ Settings = 300k/(37.5k + Rext)$$

POP-AND-CLICK SUPPRESSION

Voltage transients at the output of audio amplifiers can occur when shutdown is activated or deactivated. Voltage transients as low as 10 mV can be heard as an audio pop in the speaker. Clicks and pops can also be classified as undesirable audible transients generated by the amplifier system and therefore as not coming from the system input signal. Such transients can be generated when the amplifier system changes its operating mode. For example, the following can be sources of audible transients: system power-up/power-down, mute/unmute, input source change, and sample rate change. The SSM2311 has a pop-and-click suppression architecture that reduces these output transients, resulting in noiseless activation and deactivation.

LAYOUT

As output power continues to increase, care needs to be taken to lay out PCB traces and wires properly between the amplifier, load, and power supply. A good practice is to use short, wide PCB tracks to decrease voltage drops and minimize inductance. Ensure that track widths are at least 200 mil for every inch of track length for lowest DCR, and use 1 oz or 2 oz of copper PCB traces to further reduce IR drops and inductance. A poor layout increases voltage drops, consequently affecting efficiency. Use large traces for the power supply inputs and amplifier outputs to minimize losses due to parasitic trace resistance.

Proper grounding guidelines help to improve audio performance, minimize crosstalk between channels, and prevent switching noise from coupling into the audio signal. To maintain high output swing and high peak output power, the PCB traces that connect the output pins to the load and supply pins should be as wide as possible to maintain the minimum trace resistances. It is also recommended to use a large-area ground plane for minimum impedances.

In addition, good PCB layouts isolate critical analog paths from sources of high interference. High frequency circuits (analog and digital) should be separated from low frequency ones. Properly designed multilayer printed circuit boards can reduce EMI emission and increase immunity to the RF field by a factor of 10 or more compared with double-sided boards. A multilayer board allows a complete layer to be used for the ground plane, whereas the ground plane side of a double-sided board is often disrupted with signal crossover. If the system has separate analog and digital ground and power planes, the analog ground plane should be underneath the analog power plane, and, similarly, the digital ground plane should be underneath the digital power plane. There should be no overlap between analog and digital ground planes or analog and digital power planes.

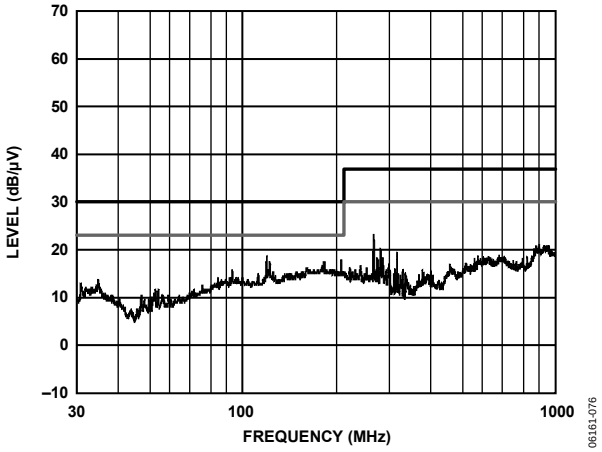


Figure 47. EMI Emissions from SSM2311

INPUT CAPACITOR SELECTION

The SSM2311 does not require input coupling capacitors if the input signal is biased from 1.0 V to V_{DD} − 1.0 V. Input capacitors are required if the input signal is not biased within this recommended input dc common-mode voltage range, if high-pass filtering is needed (Figure 43), or if using a single-ended source (Figure 44). If high-pass filtering is needed at the input, the input capacitor along with the input resistor of the SSM2311 forms a high-pass filter whose corner frequency is determined by the following equation:

$$f_C = 1/(2\pi \times R_{IN} \times C_{IN})$$

The input capacitor can significantly affect the performance of the circuit. Not using input capacitors degrades both the output offset of the amplifier and the PSRR performance.

PROPER POWER SUPPLY DECOUPLING

To ensure high efficiency, low THD, and high PSRR, proper power supply decoupling is necessary. Noise transients on the power supply lines are short-duration voltage spikes. Although the actual switching frequency can range from 10 kHz to 100 kHz, these spikes can contain frequency components that extend into the hundreds of megahertz. The power supply input needs to be decoupled with a good quality low ESL, low ESR capacitor—usually of around 4.7 µF. This capacitor bypasses low frequency noises to the ground plane. For high frequency transients noises, use a 0.1 µF capacitor as close as possible to the VDD pin of the device. Placing the decoupling capacitor as close as possible to the SSM2311 helps maintain efficiency performance.

OUTLINE DIMENSIONS

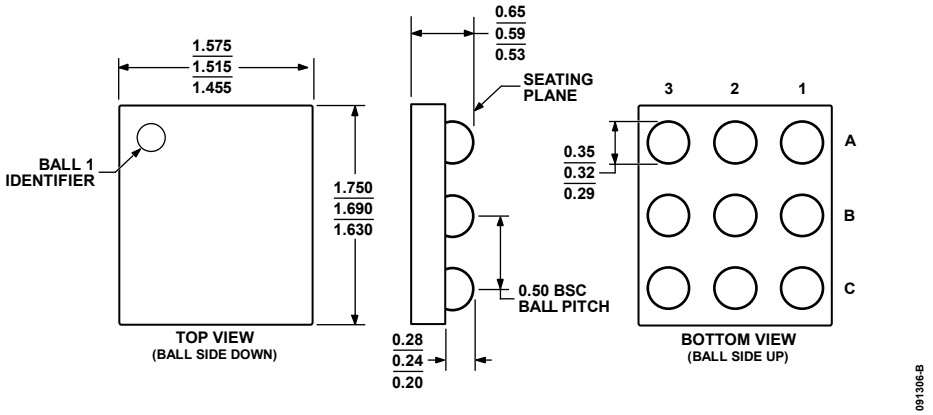


Figure 48. 9-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-9-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
SSM2311CBZ-R2[1]	−40°C to +85°C	9-Ball Wafer Level Chip Scale Package [WLCSP]	CB-9-1	A1G
SSM2311CBZ-REEL[1]	−40°C to +85°C	9-Ball Wafer Level Chip Scale Package [WLCSP]	CB-9-1	A1G
SSM2311CBZ-REEL7[1]	−40°C to +85°C	9-Ball Wafer Level Chip Scale Package [WLCSP]	CB-9-1	A1G
SSM2311-EVALZ[1]		Evaluation Board		
SSM2311-MINI-EVALZ[1]		Evaluation Board, 7 mm × 7 mm		

[1] Z = RoHS Compliant Part.

NOTES

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