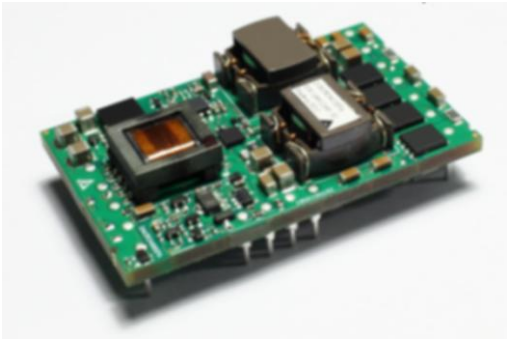
DIM3R3400

400W DC/DC Power Modules



FEATURES

- High efficiency 98.2% @ 48Vin, 400W
- High efficiency 98.5% @ 48Vin, 300W
- Size: 58.4x36.8x14.2mm(2.30”x1.45”x0.56”)
- Standard footprint
- Industry standard pin out
- Input UVLO, Main Output OCP, OTP
- Management power: OCP,OTP and OVP
- 3.3Vdc(3.6A) isolated management power for module self or other housekeeping functions.
- 5.0V/150mA BLUE_LED power
- Input OR'ing for the A/B dual input power feeds as well as A/B Enable signals
- Inrush protection and hot swap capability
- Integral EMI filter designed for the ATCA board to meet CISPR Class A
- Adjustable Hold Up Voltage from 50 to 95 V
- For charging the external holdup capacitors resulting in significant board real estate savings and bleed resistor power dissipation
- I2C interface for data monitoring and reporting
- Hardware alarms via opto-isolators for loss of A or B Feeds/Fuse
- ISO 9001, TL 9000, ISO 14001, QS9000, OHSAS18001 certified manufacturing facility
- UL/cUL 60950-1 (US & Canada)

Delphi Series DIM, 400W Dual Input Power Processing DC/DC Power Modules

The Delphi DIM series, 400W dual redundant input power processing isolated DC/DC converter is the latest offering from a world leader in power system technology and manufacturing — Delta Electronics, Inc. This product family provides up to 400 watts of power in an industry standard footprint and pinout. The DIM series is designed to simplify the task and reduce the board space of implementing dual redundant, hot swappable 48Vdc power distribution with EMI filtering and inrush current limiting for an ATCA (Advanced Telecommunications Computing Architecture) or other telecom boards. In addition to processing the dual redundant 48V bus, the DIM module also provides isolated auxiliary 3.3V (3.6A), and/or 5V (150mA) BLUE_LED power for other housekeeping functions. With creative design technology and optimization of component placement, these converters possess outstanding electrical and thermal performances, as well as extremely high reliability under highly stressful operating conditions. All models are fully protected from abnormal input/output voltage, current, and temperature conditions.

OPTIONS

- 5.0V LED Power disable or enable

APPLICATIONS

- Telecom / Datacom
- Wireless Networks
- Optical Network Equipment
- Server and Data Storage
- Industrial / Testing Equipment

TECHNICAL SPECIFICATIONS

PARAMETER	NOTES and CONDITIONS	DIM3R3400 (Standard)			
		Min.	Typ.	Max.	Units
ABSOLUTE MAXIMUM RATINGS					
Input Voltage					
Continuous				-75	Vdc
Transient	1ms			-100	Vdc
Reverse polarity	No damage,Low current			+75	Vdc
Operating Ambient Temperature		-40		85	°C
Storage Temperature		-55		125	°C
ISOLATION					
Input to SHELF_GND Voltage				1500	Vdc
Input to LOGIC_GND Voltage				2000	Vdc
MAIN INPUT (DUAL FEED) CHARACTERISTICS					
Operation Input Voltage Range		-36		-75	V
Input UVLO					
Turn-On Voltage Threshold	VRTN_OUT open load		27		Vdc
Turn-Off Voltage Threshold	VRTN_OUT open load		25		Vdc
Off Converter Input Current	Vin < UVLO voltage		35		mA
Maximum Input Current	Po=400W, 3.3V=0,Vin=-36 to -75V			12	A
Over Current Protection Setpiont		14	15.5	17	A
POWER & MAIN OUTPUT (-48V output)					
Input Power, Maximum Allowable				400	W
Efficiency	Po=400W, 3.3V/5.0V no load,Vin=-48V		98.5		%
Efficiency	Po=400W, 3.3V/5.0V no load,Vin=-48V		98.2		%
Management Power, Maximum Deliverable				12	W
Module Standby Current	Pout=0W, 3.3V=0W, 5.0V=0W				
Vin=-48V,			60		mA
Main Output External Output Filter Capacitance		80		680	µF
HOT SWAP					
Inrush Transient	Po=400W, Vin=-75V, 3.3V=0W, 5.0V=0W			2	A
INPUT A/B FEED LOSS / FUSE ALARM					
Alarm ON Input Voltage Threshold		-36.4	-38.4	-40.4	V
Transistor Collector to Emitter Voltage				40	Vdc
Transistor Collector to Emitter Current			50		mA
Transistor Collector Saturation Voltage			0.2	0.4	V
HOLD UP CAPACITANCE INTERFACE					
Hold-up Capacitor Voltage trim range		-50	-90	-95	V
Hold-up Capacitor Voltage Accuracy		-87.2	-90	-92.8	V
Hold-up Capacitor Charge Current			10		mA
Maxmum Hold-up Capacitance (C_HOLD)			1000		µF
To initiate hold up ,Input Voltage Threshold		-32.4	-34.5	-36.4	V
To arm hold up ,Input Voltage Threshold		-32.4	-34.5	-36.4	V

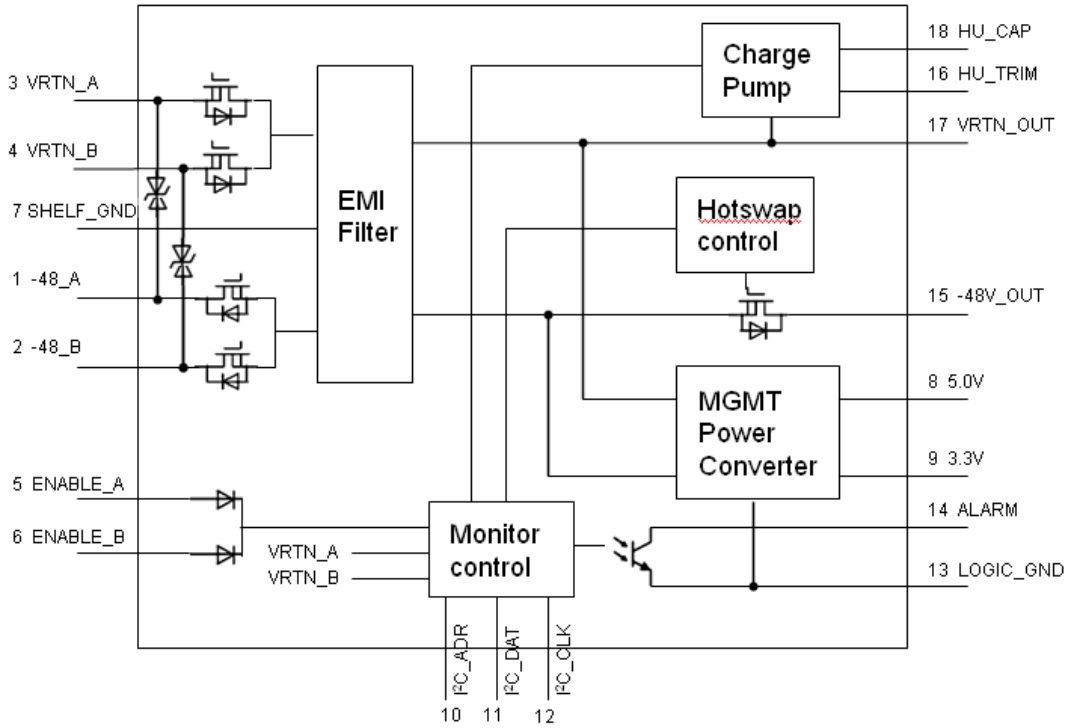
(T_A=25°C, airflow rate=300 LFM, V_{in}=-48Vdc, nominal Vout unless otherwise noted;)

TECHNICAL SPECIFICATIONS

PARAMETER	NOTES and CONDITIONS	DIM3R3400 (Standard)			
		Min.	Typ.	Max.	Units
MANAGEMENT POWER (3.3V)					
Operating Input Voltage	Continuous	-36	-48	-75	
Total Output Voltage Range (total)	Over Vin, load, temperature	3.17	3.30	3.43	V
Output Regulation					
Line Regulation	Vi= Vi,min to Vi,max		0.05	0.2	%Vo
Load Regulation	Io=Io,min to Io,max		0.05	0.2	%Vo
Temperature Regulation	Ta=Ta,min to Ta,max		1	2	%Vo
Output Voltage Overshoot				5	%Vo
Switching Frequency			450		KHz
Output Ripple and Noise	10μF Tan cap and 1μF ceramic cap				
RMS	5Hz to 20 MHz bandwidth		12	30	mV
Peak-to-peak	5Hz to 20MHz bandwidth		50	80	mV
Output Current		0		3.6	A
Over Current Protection	Hiccup mode	4	5.5	7	A
Output Over Voltage Protection	Voltage limitation mode	3.7		5.4	V
Dynamic Response (20 MHz bandwidth)	load step is 50%~100%~50%, slew rate is 0.1A/μS				
Peak Deviation			6		%Vo
Settling Time			100		μS
Turn-On Delay Times	I(3.3V)=3.6A		80		mS
Turn-On Rising Times	I(3.3V)=3.6A		2		mS
External Load Capacitance	Io=Io,min to Io,max		1000		μF
BLUE LED POWER (5V)					
Operating Input Voltage	Continuous	-36	-48	-75	Vdc
Total Output Voltage Range		4.9	5	5.1	Vdc
Output Ripple and Noise			30		mV
Operating Output Current Range		0		0.15	A
Dual Enable Input Characteristics					
Enable_A/B Threshold		32	34	36	V
Current drain per enable pin(Vin=-75V)				0.38	mA
Digital Signal Interface Characteristics					
Clock Rate			100	400	kHz
Measurement Tolerance					
Feed Voltage A/B				+/-3	%
Holdup Voltage				+/-3	%
-48V_OUT Current				+/-3	%
Temperature	NTC resistor temperature Above 25°C			+/-3	%
GENERAL SPECIFICATIONS					
Weight			30		Grams
Calculated MTBF	80% load,300LFM, 40°C Ta		2.49		Mhours
Over-Temperature Shutdown (Hot Spot)	Refer to Figure 13 for Hot spot location (48Vin,80%Po, 200LFM,Airflow from Vin- to Vin+)		130		°C
Over-Temperature Shutdown (NTC Resistor)	Refer to Figure 13 for NTC resistor location		125		°C
Note: Please attach thermocouple on NTC resistor to test OTP function, the hot spot's temperature is just for reference.					

(T_A=25°C, airflow rate=300 LFM, V_{in}=48Vdc, nominal Vout unless otherwise noted;)

DIM3R3 INTERNAL BLOCK DIAGRAM



PIN FUNCTIONS

PIN NO.	PIN NAME	DESCRIPTION
1	-48_A	-48V_A Feed (Externally Fused)
2	-48_B	-48V_B Feed (Externally Fused)
3	VRTN_A	VRTN_A Feed (Externally Fused)
4	VRTN_B	VRTN_B Feed (Externally Fused)
5	ENABLE_A	ENABLE_A Feed (Externally Fused) (Short Res, connected to VRTN_A on the back plane)
6	ENABLE_B	ENABLE_B Feed (Externally Fused) (Short Res, connected to VRTN_B on the back plane)
7	SHELF_GND	Shelf / Chassis / Safety Ground
8	5.0V	5.0V Isolated Power output (reference to LOGIC_GND)
9	3.3V	3.3V Isolated Output (reference to LOGIC_GND)
10	I2C_ADR	I2C Address Input (reference to LOGIC_GND)
11	I2C_DAT	I2C data (reference to LOGIC_GND)
12	I2C_CLK	I2C clock (reference to LOGIC_GND)
13	LOGIC_GND	Logic / Secondary / Isolated Ground
14	ALARM	Opto-isolated -48V A/B Feed Loss or Open Fuse Alarm (reference to LOGIC_GND)
15	-48V_OUT	OR'd and Inrush Protected –48V Output Bus ((Negative output to payload power converter))
16	HU_Trim	Hold Up cap voltage trim
17	VRTN_OUT	OR'd and Inrush Protected VRTN Output Bus (Positive output to payload power converter)
18	HU_CAP	Holdup/Bulk capacitor output voltage (Negative Connection to -48V_OUT)

ELECTRICAL CHARACTERISTICS CURVES

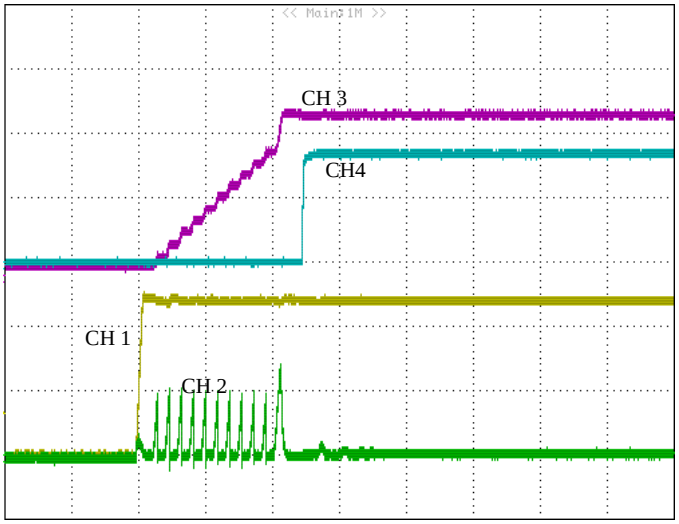


Figure 1: *Input voltage turn-on threshold (50mS/div):*
CH1: Vin (VRTN_A reference to -48V_A, 20V/div).
CH2: Iin (-48V_A, 1A/div).
CH3: VRTN_OUT reference to –48V_OUT (20V/div).
CH4: 3.3V(2V/div)
Test conditions:
(1) Feed A=48Vdc; Feed B=0Vdc
(2) I(VRTN_OUT)=0A, I(3.3V)=0A,I(5.0V)=0A.
(3) C2=470uF, C_hold=1000uF

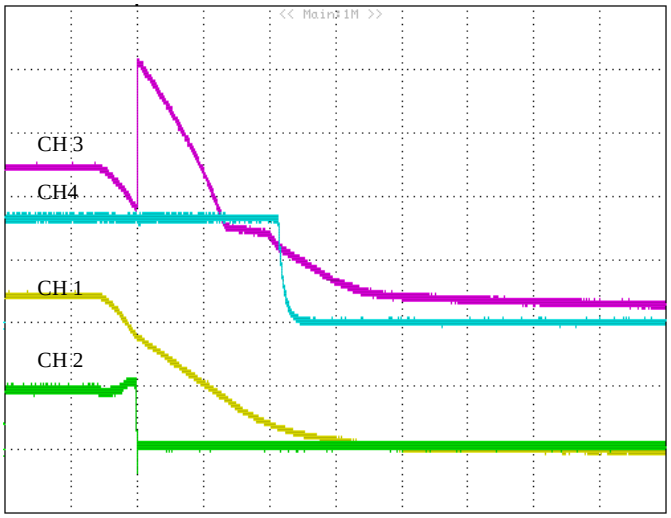


Figure 2: *Input voltage turn-off threshold (2mS/div):*
CH1: Vin (VRTN_AF reference to -48V_A, 20V/div).
CH2: Iin (-48V_A, 1A/div).
CH3: VRTN_OUT reference to. –48V_OUT (20V/div).
CH4: 3.3V(2V/div)
Test conditions:
(1) Feed A=37Vdc ; Feed B=0Vdc
(2) I(VRTN_OUT)=1A,I(3.3V)=0A,I(5.0V)=0A.
(3) C2=220uF, C_hold=1000uF

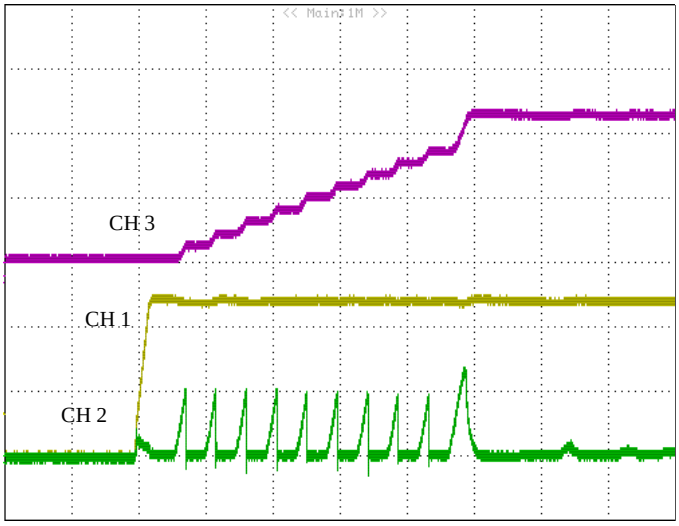


Figure 3: *Inrush current (20mS/div):*
CH1: Vin (VRTN_AF reference to -48V_AF, 20V/div).
CH2: Iin (-48V_AF, 1A/div).
CH3: VRTN_OUT reference to –48V_OUT (20V/div).

Test conditions:
(1) Feed A=48Vdc, Feed B=0Vdc.
(2) I(VRTN_OUT)=0A, I(3.3V)=0A, I(5.0V)=0A.
(3) C2=470uF, C_hold=1000uF

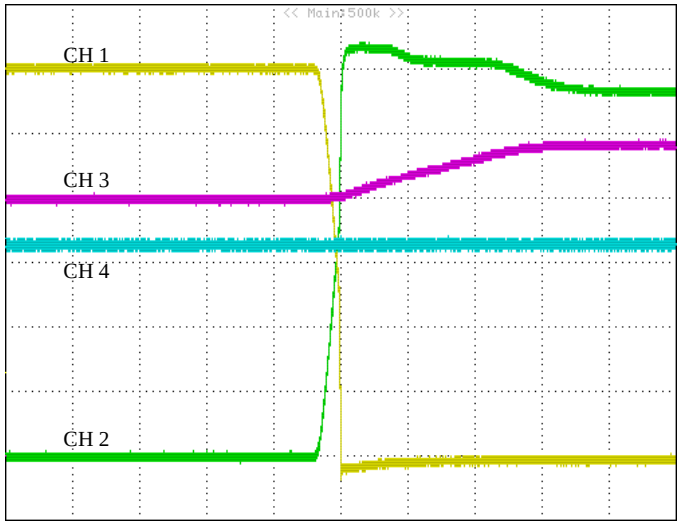


Figure 4: *Oring for one feed loss (500µS/div):*
CH1: IinA (1A/div)
CH2: IinB (1A/div).
CH3: VRTN_OUT reference to –48V_OUT (10V/div).
CH4: 3.3V (1V/div).

Test conditions:
(1) Feed A=40V, Feed B=48V;
(2) VRTN_OUT power=300W, I(3.3V)=3.6A, I(5.0V)=0A.
(3) C2=220uF, C_hold=1000uF

ELECTRICAL CHARACTERISTICS CURVES

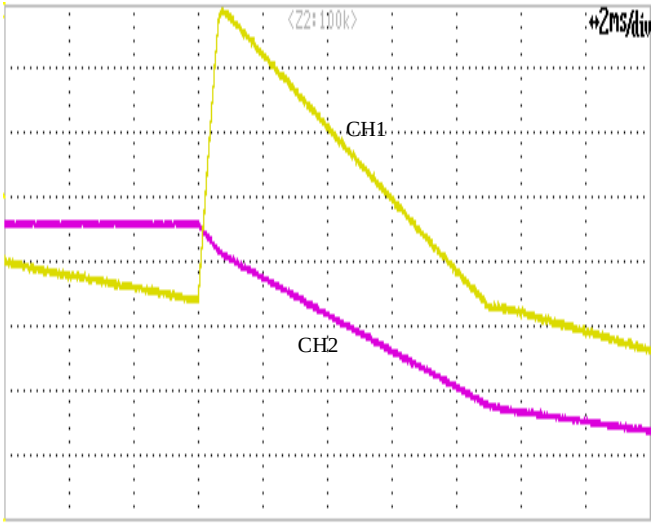


Figure 5: *Hold up performance (2mS/div):*
CH1: VRTN_OUT reference to –48V_OUT (10V/div)
CH2: HU_CAP (20V/div).

Test conditions:
(1) Feed A=48Vdc; Feed B=0Vdc
(2) Output power=300W
(3) C2=220uF, C_hold=1000uF

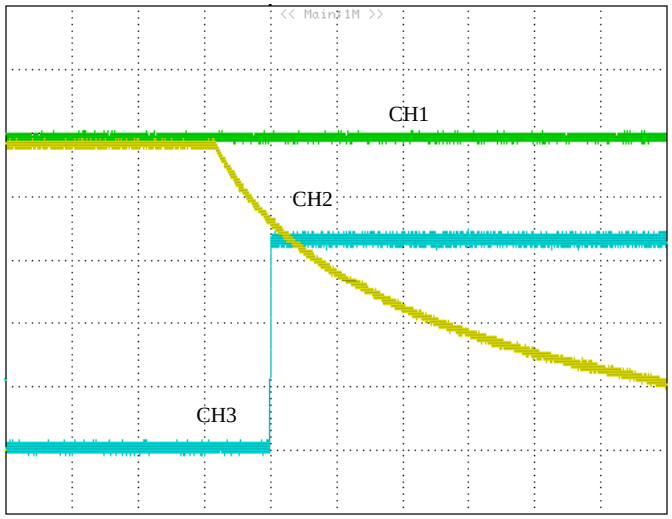


Figure 6: *-48V_ALARM with loss of Feed (10mS/div):*
CH1: VinA (VRTN_AF reference to -48V_AF, 10V/div).
CH2: VinB (VRTN_BF reference to -48V_BF, 10V/div).
CH3: ALARM (2V/div)

Test conditions:
(1) Feed B turn off from 48Vdc; Feed A=48Vdc.
(2) Output power=400W, I(3.3V)=3.6A,
I(5.0V)=0A.
(3) C2=220uF, C_hold=1000uF

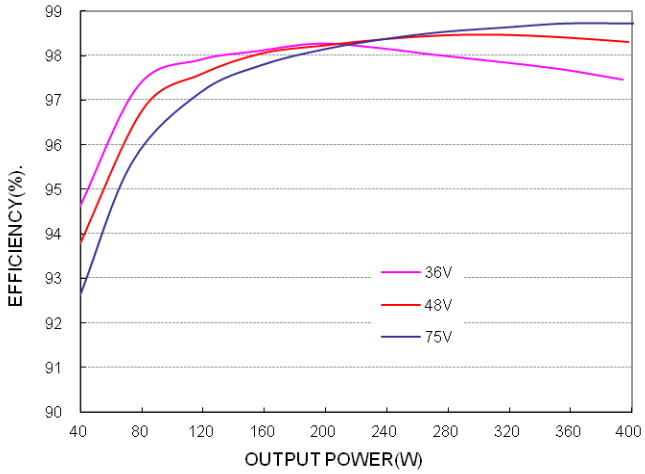


Figure 7: *Efficiency vs. load current for minimum, nominal, and maximum input voltage at 25°C:*

Test conditions:.
(1) I(3.3V)=0A; I(5.0V)=0A;
(2) C2=220uF, C_hold=1000uF
(3)Po(VRTN_OUT ref to -48V_OUT)from 40W to 400W

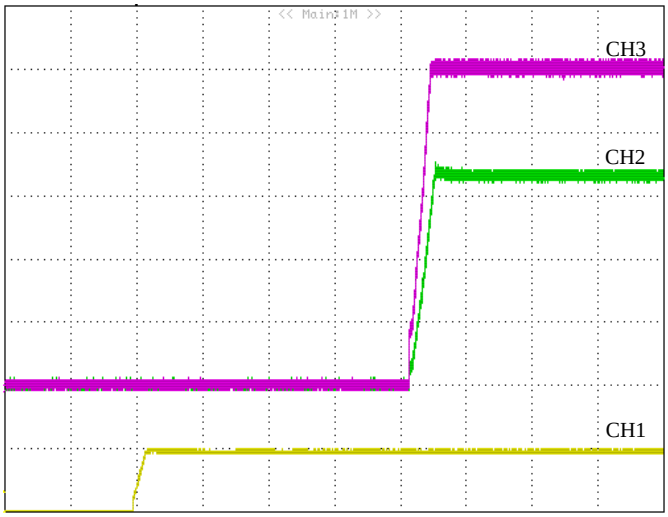


Figure 8: *3.3V and 5.0V start up waveform (20mS/div):*
CH1: VinA (VRTN_A referenced to -48V_AF, 50V/div).
CH2: V(3.3V) (1V/div);
CH3: V(5.0V) (1V/div)
Test conditions:
(1) Feed A=48Vdc; Feed B=0Vdc
(2) I(VRTN_OUT)=1A,I(3.3V)=3.6A,
I(5.0V)=0.15A
(3) C2=220uF, C_hold=1000uF

ELECTRICAL CHARACTERISTICS CURVES

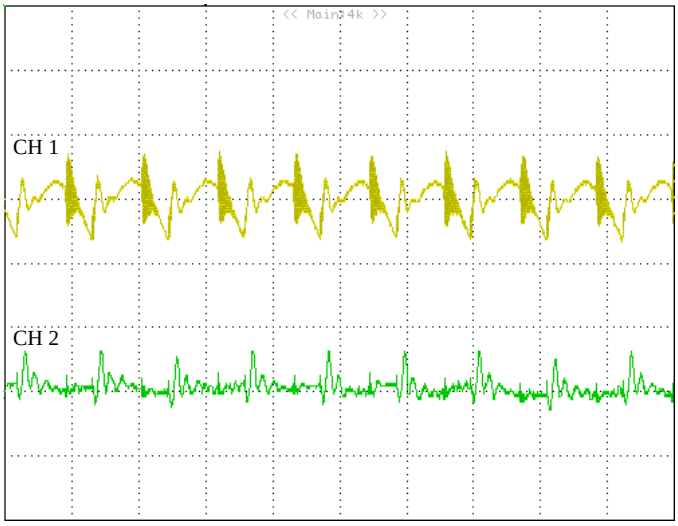


Figure 9: *3.3Vand 5.0V output ripple/noise (2uS/div):*
CH1: Vo, 3.3V (50mV/div).
CH2: Vo, 5.0V (50mV/div).

Test conditions:
(1) Feed A=48Vdc; Feed B=0Vdc
(2) I(3.3V)=3.6A,I(5.0V)=0.1A
(3) C2=220uF, C_hold=1000uF

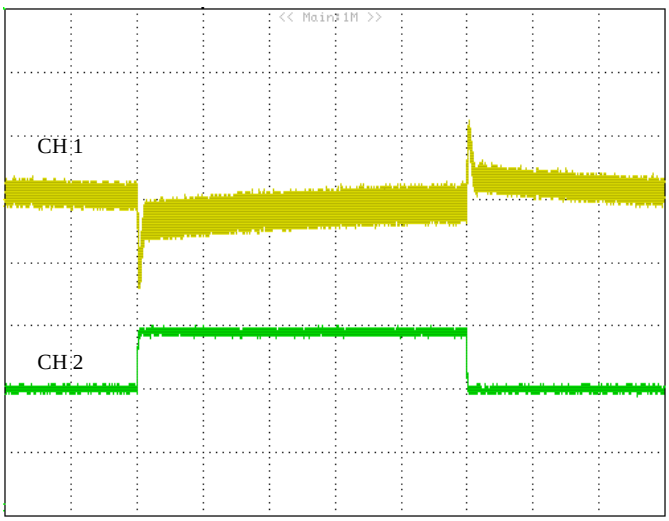
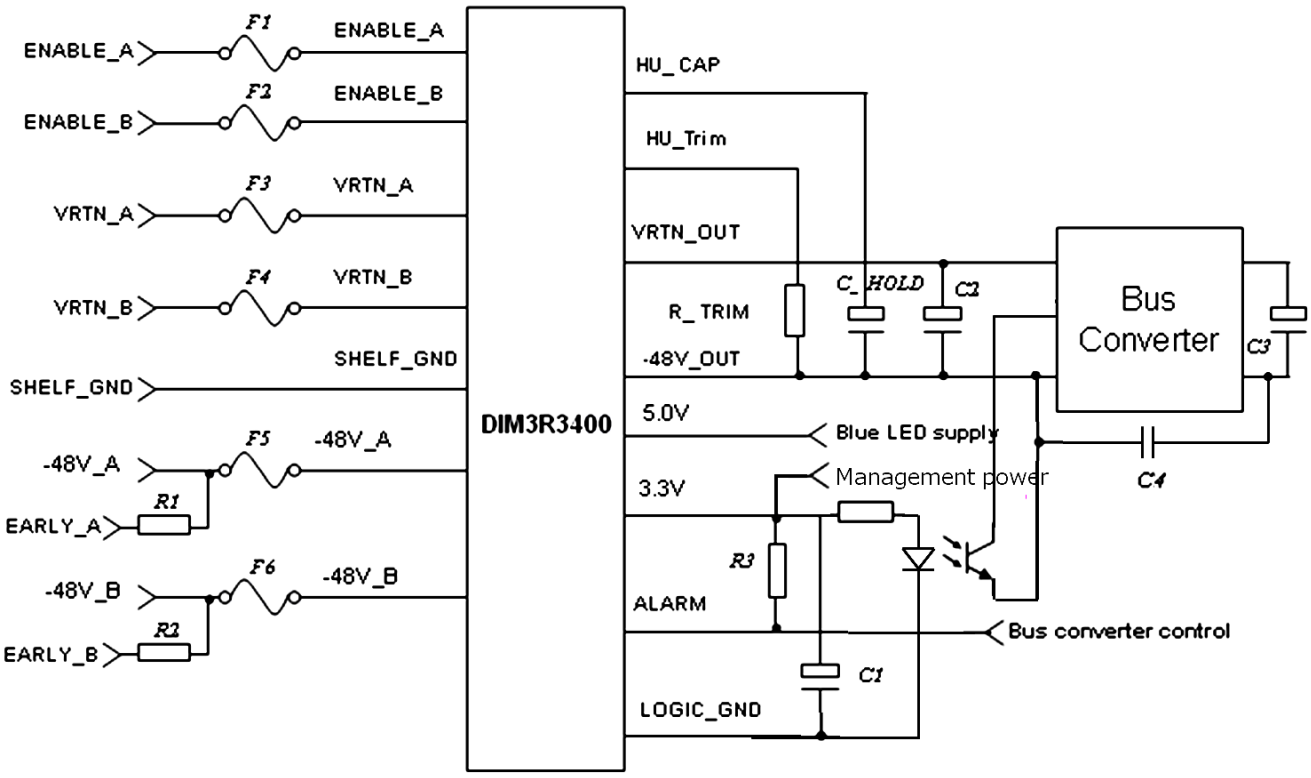


Figure 10: *3.3V dynamic response (1mS/div):*
CH1: Vo, 3.3V(100mV/div).
CH2: Io, 3.3V (1A/div)

Test conditions:
(1) Feed A=48Vdc; Feed B=0Vdc
(2) 3.3V load current (50%-75%-50% of Io,max,
di/dt = 0.1A/μs)
(3) C2=220uF, C_hold=1000uF

APPLICATION CIRCUITS



TYPICAL VALUES FOR ABOVE COMPONENTS:

POSITION	VALUE	NOTE
F1,F2	1A, FUSE	
F3,F4	15A, FUSE	
F5,F6	15A, FUSE	
R1,R2	15Ω, RESISTOR	
R3	3.3KΩ, RESISTOR	
C1	10μF, CAP	No additional output capacitors are required, this cap are highly recommended to reduce the switching ripple and noise.
C2	220~680μF	Recommended to use 2pcs EKZE101EC3221MK25S(220uF,ESR is 47mΩ) in parallel to improve output voltage stability.
C3		Defined by DC/DC converter application note
C4		Optional
C_HOLD	$\frac{2*Power*T_HLDP}{HU_CAP^2 - Vth^2}$	for the definition of parameters, please see page 10
R_ TRIM	500000/(V hu -50)-10000	Connect a resistor between Hold Up_ Trim and -48V_OUT can set the Hold up cap voltage, please see page 10

FEATURES AND DESIGN CONSIDERATIONS

Introduction

The DIM3R3400 module is designed to simplify the task and reduce the board space of an ATCA (Advanced Telecommunications Computing Architecture) power entry distribution requirements in the system board.

The main functionality of the module is to provide dual, redundant -48V A/B Feed OR'ing, inrush protection for hot swap capability, EMI filtering to attenuate the noise generated by the downstream DC/DC converters, and a Adjustable Hold Up Voltage from 50 to 95 V for charging the holdup capacitor. The module also has a management power supply which provides an 3.3V/3.6A management power and a 5V/150mA output (optional) to power the blue LED per PICMG 3.0 requirement.

The module provides A/B feed/fuse open alarm, over current protection, over voltage protection, and over temperature protection. It also provides input under voltage lock-out and input reverse polarity protection.

A/B Feed OR'ing

To improve the total power distribution efficiency, four internal MOSFETs are used to function as the OR'ing diodes. A control circuit is designed to keep about 60mV voltage drop across MOSFET. During full load operation, the MOSFETs are fully turned on. During light load, the MOSFETs work under a high Rdson condition. If the output current decreases to zero, the MOSFETs will be turned off. This design provides module a reverse voltage sustain function. The module shall not be damaged from reverse polarity connection in the event of mis-wiring of either input feeds at the shelf input terminals. Furthermore, a fast shut down circuit is designed for the negative current case. This design protects the common DC bus against hard short faults at the sourcing power supply output.

Hot Swap Functionality

The hot-swap function is designed to limit the inrush current charged to the bulk capacitor of the down stream bus converter. The current value and duration comply with the PICMG 3.0's Inrush Transient specs.

Although the inrush current for bulk capacitor is under control, special attentions need to be paid to the current for EMI filter because this circuit is in front of hot-swap circuit.

EMI Filtering

An internal EMI filter is designed for the ATCA board to meet the system conducted emission requirements of CISPR 22 Class B when used with Delta DC/DC converters.

Figure 11 shows the EMI performance of DIM3R3400 when it worked with Delta power module Q48SQ12033NRFH. It meets CISPR 22 Class B requirement.

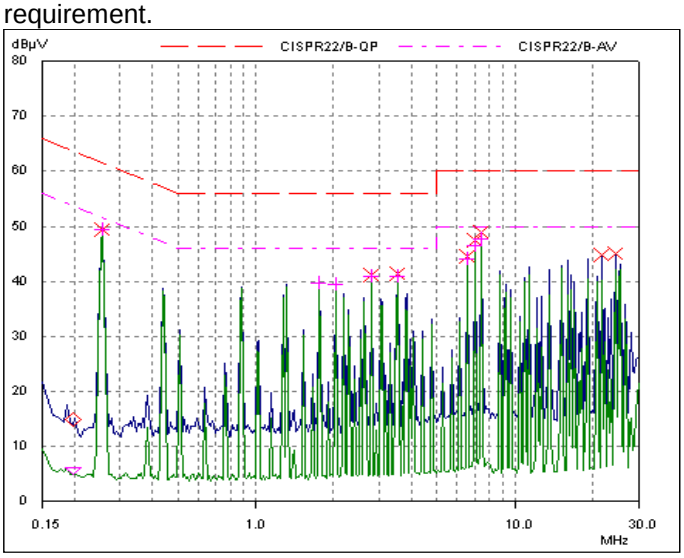


Figure 11,DIM3R3400 EMI(work with Delta power module Q48SQ12033NRFH).

Holdup Capacitor Charging

An off line holdup capacitor (C_HLDP) is needed to store energy for the holdup time requirement. C_HLDP is charged to a set voltage Vcap(A resistor connect from Hold up _trim to -48V_out will set the cap voltage). For a fixed energy storage requirement, high capacitor voltage reduces capacitor capacitance and size. A constant current circuit charges C_HLDP before its voltage reaches the high limitation and isolates it from power train circuit. The discharge switch will turn on if both A&B feeds have dropped below –35V (typical). C_HLDP will be connected to power train and provided the energy for system operation.

C_HLDP is calculated by the following equation:

$$C_HLDP = \frac{2 * Power * T_HLDP}{Vcap * Vcap - Vth * Vth}$$

Where Power is the input power to the downstream DC/DC converter and 3.3V input management converter power; T_HLDP is the holdup time requirement; Vth is the minimum input voltage threshold of the downstream DC/DC converter.

FEATURES AND DESIGN CONSIDERATIONS (CONTINUED)

The PICMG 3.0's requirements for the 0 Vdc transient is going to remain 5mS the fall slew rate is 50V/ms and rise slew rate 12.5 V/ms. This requirement will lead to a 8.7ms T_HLDP requirement assuming power is interrupted at -35Vdc (Vth).

Considering Power is 435.85W(The downstream DC/DC converter input power is 400W/95%=421W;the 3.3V power is 3.3V*3.6A/80%=14.85W,So total power is 435.85W), Vth is 35V, Vcap=90V,

$$C_HLDP = \frac{2*435.85*8.7}{90^2 - 35^2} = 1103(uF)$$

When the input voltage is at the threshold of discharge, C_HLDP will go off line and the charge pump will recharge it .

External Hold Up Trim Resistor

Rtrim is the external hold-up trim resistance for a given desired nominal hold-up capacitor charge voltage (Vcap), the detailed equation is

$$R_{trim} = \frac{500000}{Vhu - 50} - 10000(\Omega)$$

Over-Current Protection

DIM3R3400 provides over current protection levels to protect downstream DC/DC converter over power rating. When the downstream DC/DC converter over power rating and caused our output current exceeds the current limit level, the module will shut down immediately. After a fixed delay time, the module will try to restart. Then it will go through the restarting procedure.

A/B Feed / Fuse Alarm (-48V_ALARM)

The input feeds A and B are monitored. The module will send an opto-isolated signal if any of the feed is below the voltage threshold (typical 38.4V). Therefore, the loss of any A or B feed can be detected. The opto coupler transistor on state indicates a normal status and off state indicates a fault condition.

Input Under Voltage Lockout

The input under-voltage lockout prevents the module from being damaged by low input voltage. When the input voltage is lower than its threshold voltage, the module will be turned off. The lockout occurs between -26V to -28V.

Transient Over Voltage Protection

The PICMG 3.0 requires the module work normally under 100V/10μS input voltage transient. DIM3R3400 can meet the requirement. An internal TVS with 80V/1500W peak pulse power rating will suppress the 100V transient voltage. For the 100V pulse voltage, the power train impedance will damp it below internal components rating without shut down the module.

Management Power(3.3V) and Blue_LED Power(5.0V)

The module contains two isolated DC output. The first output provides up to 3.3V/3.6A management power (reference to LOGIC_GND). This power is used to power the IPM controller for the ATCA board or to power up system controller for other applications. The second isolated output, 5V/150mA, is used to power the Blue LED per PICMG 3.0 requirement.

The management power is available as soon as the input voltage levels are within –36Vdc to –75Vdc. short circuit and over voltage protected are built in it. The module will going into hiccup mode when OCP or short happened. The output voltage will keep a constant when over voltage happened, and the value is the ovp point. No additional output capacitors are required, but a 22μF tantalum/ceramic and a 0.01μF to 0.1μF ceramic capacitors are highly recommended to reduce the switching ripple and noise. Higher output capacitance may be required in case of large input line or output load transient conditions.

I2C DATA REPORTING INTERFACE:

The module has a digital I2C Serial interface to allow the module to be monitored by the system. The module supports 3 I2C signal lines, Data, Clock and 1 Address line I2C_ADR. the Delta I2C Serial Interface monitors 5 analog parameters and 6 status bits. The actual analog parameter values are calculated by multiplying by the specified scaling factors (see table1). The status bits are interpreted in Table 2. The initial value of all registers is zero. Data in the registers begins updating 300ms after management power startup, and continues updating at approximately 100ms intervals during steady-state operation. All registers are updated simultaneously. The I2C_DAT and the I2C_CLK have been pull high to internal 3.3V.

Data_Pointer Value	Parameter	Description	Scaling Factor
1Eh	Status Bits	Digital Signals (see Table2)	N/A
1Fh	HU_CAP	Voltage between HU_CAP and -48V_OUT	0.398V/bit
21h	-48V_Current	-48V Output Current	0.094A/bit
22h	-48V_A	Voltage between VRTN_A and -48V_A	0.325V/bit
23h	-48V_B	Voltage between VRTN_B and -48V_B	0.325V/bit
28h	Temperature	Average Unit Temperature	(1°C/bit)

Table 1: Internal register memory map.

Bit	Name	Description	Value	Translation
0	ENABLE_A	Enable A Signal State	0	En_A is Disabled
			1	En_A is Enabled
1	ENABLE_B	Enable B Signal State	0	En_B is Disabled
			1	En_B is Enabled
2	ALARM	Alarm Signal State	0	Primary side Alarm is not SET
			1	Primary side Alarm is SET
3	N/A	Reserved		
4	HOLDUP	Holdup Switch State	0	Holdup Cap is not connected to -48V Out
			1	Holdup Cap is connected to -48V Out
5	HOTSWAP	Hotswap Switch State	0	Hotswap switch is OFF
			1	Hotswap switch is ON
6	VOUT_LOW	-48V Output Under-Voltage Alarm	0	Output voltage is below threshold
			1	Output voltage is above threshold
7	N/A	Reserved		

Table 2: The status byte represents 6 different digital signals and their digital state.
Note: 1)Bit0=>LSB, Bit7=>MSB

I2C PROTOCOL:

To begin communication, a master device starts out in Master Transmit mode. The master device sends out a Start bit followed by the address byte of the slave it intends to communicate with. This is followed by a single Read/Write bit, which determines whether the master intends to transmit to or receive data from the slave device.

If the requested slave exists on the bus, it will respond with an Acknowledge bit, otherwise known as an ACK. The master then continues in either Transmit mode or Receive mode and the slave continues in the complement, either in Receive mode or Transmit mode, respectively.

A Start bit is indicated by a high-to-low transition of the SDAx line while the SCLx line is held high. Address and data bytes are sent out, Most Significant bit (MSb) first. The Read/Write bit is sent out as a logical one when the master intends to read data from the slave, and is sent out as a logical zero when it intends to write data to the slave.

If the master intends to read from the slave, then it repeatedly receives a byte of data from the slave, and responds after each byte with an ACK bit. In this example, the master device is in Master Receive mode and the slave is Slave Transmit mode.

On the last byte of data communicated, the master device may end the transmission by sending a Stop bit. If the master device is in Receive mode, it sends the Stop bit in place of the last ACK bit. A Stop bit is indicated by a low-to-high transition of the SDAx line while the SCLx line is held high.

Reading from any internal register of the Delta monitor requires that an internal register, Data_Pointer, be initialized prior to reading (see Figure 16).

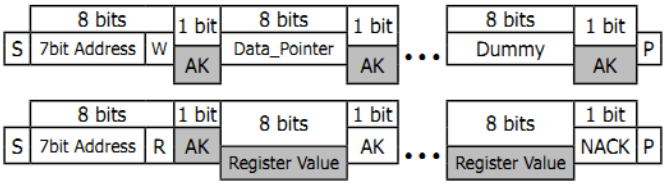


Figure 16: *Typical I2C read transmission. Note: S = START, W = WRITE, R = READ, AK = acknowledged, NACK = NOT acknowledged, P = STOP. Clear boxed originate in the I2C Master and shaded boxed originate in the I2C Slave.*

I2C PROTOCOL:

Data_Pointer is write-only. It is written from the second byte of any I2C WRITE message (the first byte is the 7 bit I2C Address and the R/W bit). Subsequent data bytes in a WRITE message (3rd Byte and beyond) only increment Data_Pointer.

Any READ message will return the value of the internal register referenced by Data_Pointer and increments Data_Pointer by one. For instance, if the master acknowledges (AK), the next internal register referenced by Data_Pointer will be returned and Data_Pointer will be incremented by one. This process is repeated until the master does not acknowledge (NACK) and issues a STOP bit.

Data_Pointer is an 8bit value. It is initialized to 00h at reset, and after reaching FFh, it will not overflow.

Writing to registers not defined in Table1 has no effect. Reading from these undefined registers will return 00h. In both cases Data_Pointer is incremented.

Example from the point of view of the I2C Master:

1) START transmission.
2) Send 52h (addresses unit for writing, given address 52h was selected as shown in Table 4).
3) Send 1Eh (loads 1Eh into Data_Pointer).
4) STOP transmission.
5) START next transmission.
6) Send 53h (addresses unit for reading).
7) Unit will respond with the value of Status Bits (register 1Eh as shown in Table 1).
8) ACK (Data_Pointer is automatically incremented to 1Fh).
9) Unit will respond with the value of HU_CAP (register 1Fh).
10) NACK.
11) Stop Transmission.

I2C ADDRESS STRUCTURE:

7 bit I2C Address + R/W bit

Four bits are fixed (0101), three bits (xyz) are variable, and the least-significant bit is the read/write bit.

8 bit I²C Address		
0 1 0 1	x y z *	R/W

Table 3: I2C address structure.

I2CADRESS SELECTION:

The three bits (xyz) of the I2C Address are set with a single external resistor from the I2C_ADR (pin10) to LOGIC_GND (pin13). The 8 possible addresses are shown in Table4 with the respective resistance values.

External programming resistances for I2C address selection		
I2C address for write (R/W = 0)	xyz from Table 3	R(Ω)
5Eh	111	Open
5Ch	110	100000
5Ah	101	40200
58h	100	20000
56h	11	10000
54h	10	4020
52h	1	2000
50h	0	Short

Table 4: I2C address selection

THERMAL CONSIDERATIONS

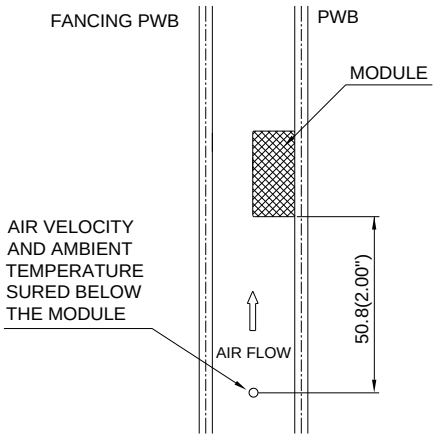
Thermal management is an important part of the system design. To ensure proper, reliable operation, sufficient cooling of the power module is needed over the entire temperature range of the module. Convection cooling is usually the dominant mode of heat transfer.

Hence, the choice of equipment to characterize the thermal performance of the power module is a wind tunnel.

Thermal Testing Setup

Delta's DC/DC power modules are characterized in heated vertical wind tunnels that simulate the thermal environments encountered in most electronics equipment. This type of equipment commonly uses vertically mounted circuit cards in cabinet racks in which the power modules are mounted.

The following figure shows the wind tunnel characterization setup. The power module is mounted on a test PWB and is vertically positioned within the wind tunnel. The space between the neighboring PWB and the top of the power module is constantly kept at 6.35mm (0.25").



Note: Wind Tunnel Test Setup Figure Dimensions are in millimeters and (Inches)

Figure 12: *Wind tunnel test setup*

Thermal Derating

Heat can be removed by increasing airflow over the module. To enhance system reliability, the power module should always be operated below the maximum operating temperature. If the temperature exceeds the maximum module temperature, reliability of the unit may be affected.

THERMAL CURVES

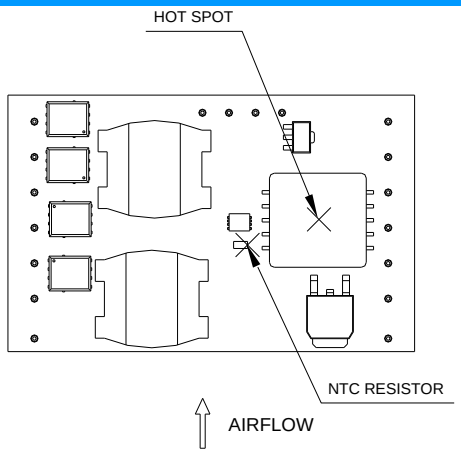


Figure 13: ** Hot spot& NTC resistor temperature measured points. The allowed maximum hot spot temperature is defined at 115℃*

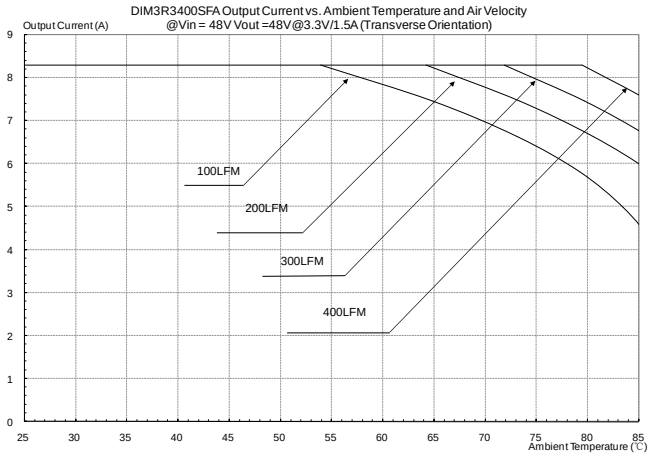


Figure 14: *Output current vs. ambient temperature and air velocity @Vin=48V,Vout=48V@3.3V/1.5A (Transverse Orientation, Airflow from Vin- to Vin+)*

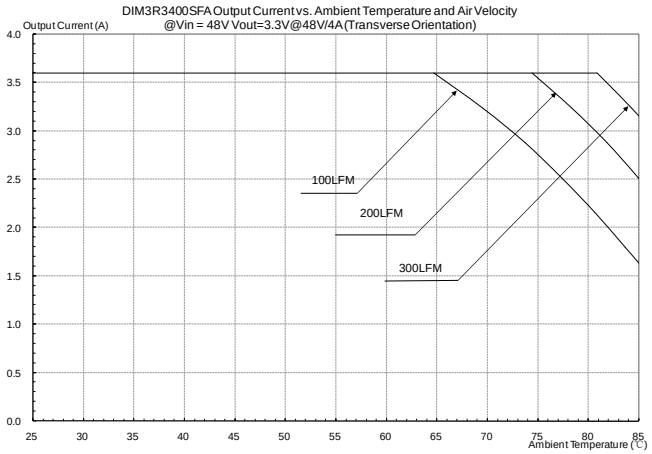
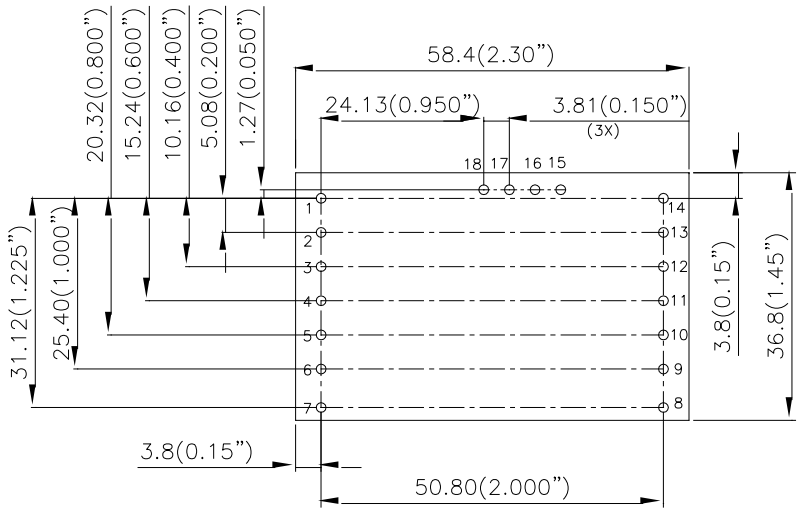
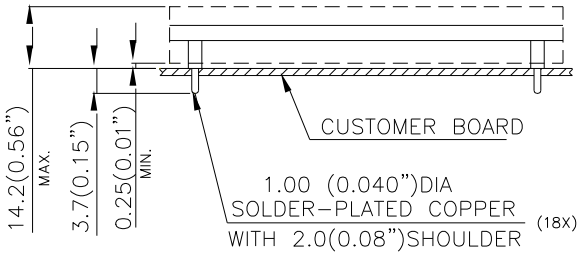


Figure 15: *Output current vs. ambient temperature and air velocity @Vin=48V,Vout=3.3V@48V/4A (Transverse Orientation, Airflow from Vin- to Vin+)*

MECHANICAL DRAWING



TOP VIEW



SIDE VIEW

Pin#	Function
1	-48V_A
2	-48V_B
3	VRTN_A
4	VRTN_B
5	ENABLE_A
6	ENABLE_B
7	SHELF_GND
8	5.0V
9	3.3V
10	I2C_ADR
11	I2C_DAT
12	I2C_CLK
13	LOGIC_GND
14	ALARM
15	-48V_OUT
16	HU_TRIM
17	VRTN_OUT
18	HU_CAP

NOTES:
DIMENSIONS ARE IN MILLIMETERS AND (INCHES)
TOLERANCES: X.Xmm±0.5mm(X.XX in.±0.02 in.)
X.XXmm±0.25mm(X.XXX in.±0.010 in.)

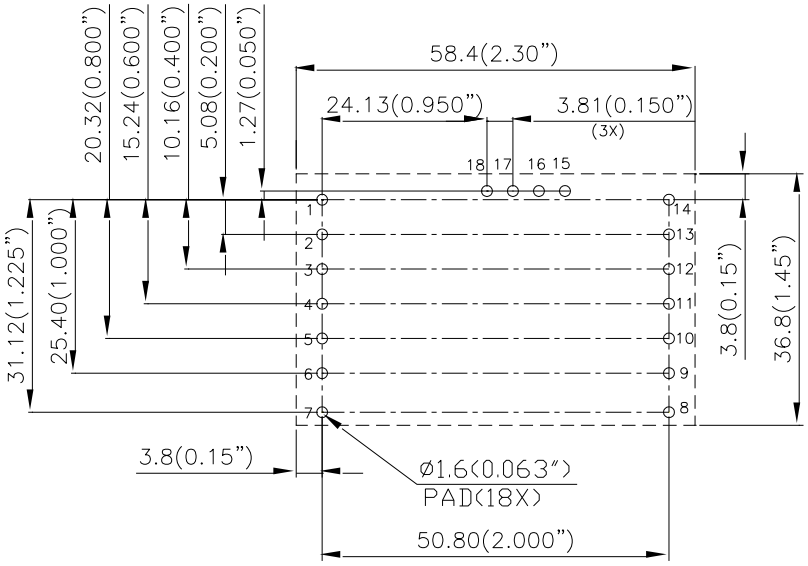
Pin No	Name	Function
1	-48V_A	-48V_A Feed (Externally Fused)
2	-48V_B	-48V_B Feed (Externally Fused)
3	VRTN_A	VRTN_AF Feed (Externally Fused)
4	VRTN_B	VRTN_BF Feed (Externally Fused)
5	ENABLE_A	ENABLE_AF Feed (Externally Fused) (Short Res, connected to VRTN_A on the back plane)
6	ENABLE_B	ENABLE_BF Feed (Externally Fused) (Short Res, connected to VRTN_B on the back plane)
7	SHELF_GND	Shelf / Chassis / Safety Ground
8	5.0V	5V Isolated Power output (reference to LOGIC_GND)
9	3.3V	3.3V Isolated Output (reference to LOGIC_GND)
10	I2C_ADDRESS	I2C Address Input (reference to LOGIC_GND)
11	I2C_DATA	I2C data (reference to LOGIC_GND)
12	I2C_CLOCK	I2C clock (reference to LOGIC_GN)
13	LOGIC_GND	Logic / Secondary / Isolated Ground
14	ALARM	Opto-isolated -48V A/B Feed Loss or Open Fuse Alarm (reference to LOGIC_GND)
15	-48V_OUT	OR'd and Inrush Protected –48V Output Bus ((Negative output to payload power converter))
16	HU_Trim	Hold Up cap voltage trim
17	VRTN_OUT	OR'd and Inrush Protected VRTN Output Bus (Positive output to payload power converter)
18	HU_CAP	Holdup/Bulk capacitor output voltage (Negative Connection to -48V_OUT)

Pin Specification:

Pins 1-18 1.00mm (0.040") diameter

All pins are copper alloy with Matte Sn over Ni plating.

RECOMMENDED PAD LAYOUT



RECOMENDED P.W.B. PAD LAYOUT

NOTES:
DIMENSIONS ARE IN MILLIMETERS AND (INCHES)
TOLERANCES: X.Xmm±0.5mm(X.XX in.±0.02 in.)
X.XXmm±0.25mm(X.XXX in.±0.010 in.)

Pin#	Function
1	−48V_A
2	−48V_B
3	VRTN_A
4	VRTN_B
5	ENABLE_A
6	ENABLE_B
7	SHELF_GND
8	5.0V
9	3.3V
10	I2C_ADR
11	I2C_DAT
12	I2C_CLK
13	LOGIC_GND
14	ALARM
15	−48V_OUT
16	HU_TRIM
17	VRTN_OUT
18	HU_CAP

PART NUMBERING SYSTEM

DIM	3R3	400	S	F	A
Product Series	Management Power	Output Power	Pin Length		Option code
DIM - ATCA Input Module	3R3 - with 3.3V	400 -400W	S - 0.145”	F- RoHS 6/6 (Lead Free)	A - Standard Functions

MODEL LIST

MODEL NAME	INPUT		Main OUTPUT 1	OUTPUT 2 Management Power	OUTPUT 3 Blue LED Power	Eff @ 400W Main Po
DIM3R3400SFA	36V~75V	400W	36V~75V	3.3V/3.6A	5V/0.15A	98.2%

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