DATA SHEET

PCA8514
Stand-alone OSD

Product specification
File under Integrated Circuits, IC14

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PHILIPS

CONTENTS

1 FEATURES
2 GENERAL DESCRIPTION
3 ORDERING INFORMATION
4 BLOCK DIAGRAM
5 PINNING INFORMATION
5.1 Pinning
5.2 Pin description
6 SERIAL I/O
6.1 I²C-bus serial interface
6.2 High-speed serial interface (HIO)
7 CHARACTER FONTS
7.1 Character font address map
7.2 Character font ROM
8 DISPLAY RAM ORGANIZATION
8.1 Description of display RAM codes
8.2 Loading character data into display RAM
8.3 Writing character data to display RAM
9 COMMANDS
9.1 Command 0
9.2 Command 1
9.3 Command 2
9.4 Command 3
9.5 Command 4
9.6 Command 5
9.7 Command 6
9.8 Command 7
9.9 Command 8
9.10 Command 9
9.11 Command A
9.12 Commands B, C and D
9.13 Command E
9.14 Command F
9.15 Command G
10 MISCELLANEOUS
10.1 Space and Carriage Return Codes in different Background/Shadowing modes
10.2 Combination of character font cells
11 OSD CLOCK
12 OSD CLOCK SELECTION FOR DIFFERENT TV STANDARDS
12.1 OSD frequency
12.2 Maximum number of characters per row
12.3 Maximum number of rows per frame
13 OUTPUT PORTS
13.1 Mask options
14 DEFAULT VALUES AFTER POWER-ON-RESET
15 LIMITING VALUES
16 DC CHARACTERISTICS
17 AC CHARACTERISTICS
18 PACKAGE OUTLINES
19 SOLDERING
19.1 Introduction
19.2 DIP
19.3 SO
20 DEFINITIONS
21 LIFE SUPPORT APPLICATIONS
22 PURCHASE OF PHILIPS I²C COMPONENTS

1 FEATURES

- Display RAM: 256 × 12 bits
- Display character fonts: 128 (fixed in ROM, mask programmable)
- Starting position of the first character displayed: 64 vertical and 64 horizontal starting positions can be selected by software
- Character size: 4 different character sizes on a line-by-line basis (1 dot = 1H/1V; 2H/2V; 3H/3V and 4H/4V)
- Character matrix: 12 × 18 with no spacing between characters and no rounding function
- Foreground colours: 16 combinations of Red, Green, Blue and Intensity on character-by-character basis
- Background/shadowing modes: 4 modes available, No background, Box shadowing, North-West shadowing and Frame shadowing (raster blanking) on frame basis
- Background colours: 16 combinations of Red, Green, Blue and Intensity on word-by-word basis. Available when background mode is in either the Box shadowing, North-West shadowing or Frame shadowing mode
- OSD oscillator: on-chip Phase-Locked Loop (PLL)
- Character blinking ratio: 1 : 1, 1 : 3 and 3 : 1 (programmable frequency of $\frac{1}{16}$, $\frac{1}{32}$, $\frac{1}{64}$ or $\frac{1}{128}$ of f_{VSYNC}) on character basis
- Display format: flexible display format by using the Carriage Return Code, maximum number of characters per line is also flexible and depends upon the OSD clock frequency
- Spacing between lines: 4 choices comprising 0, 4, 8 and 12 horizontal scan lines
- Display character RAM address auto-post-increment when writing data
- Fast I^2C-bus serial interface (400 kbaud) or High-speed 3-wire serial interface (1 Mbaud) for data/command transfer
- ACM (Active Character Monitor) specifically for use in camcorder applications on word basis; can also be used as a 5th colour control with R, G, B and I signals
- Programmable active input polarity of HSYNC and VSYNC
- Programmable output polarity of R, G, B, I and FB
- Supply voltage: 5 V ±10%
- Operating temperature: –20 to +70 °C
- Package: SDIP24 or SO24.

2 GENERAL DESCRIPTION

The PCA8514 is a member of the PCA85XX CMOS family and is an on-screen character display generator controlled by a microcontroller via the on-chip fast I^2C-bus interface or the on-chip High-speed 3-wire serial interface. It is suitable for use in high-end TV or camcorder applications and has also been designed for use in conventional mid-end TV with advanced graphic features.

3 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCA8514P	SDIP24	plastic shrink dual in-line package; 24 leads (400 mil)	SOT234-1
PCA8514T	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1

4 BLOCK DIAGRAM

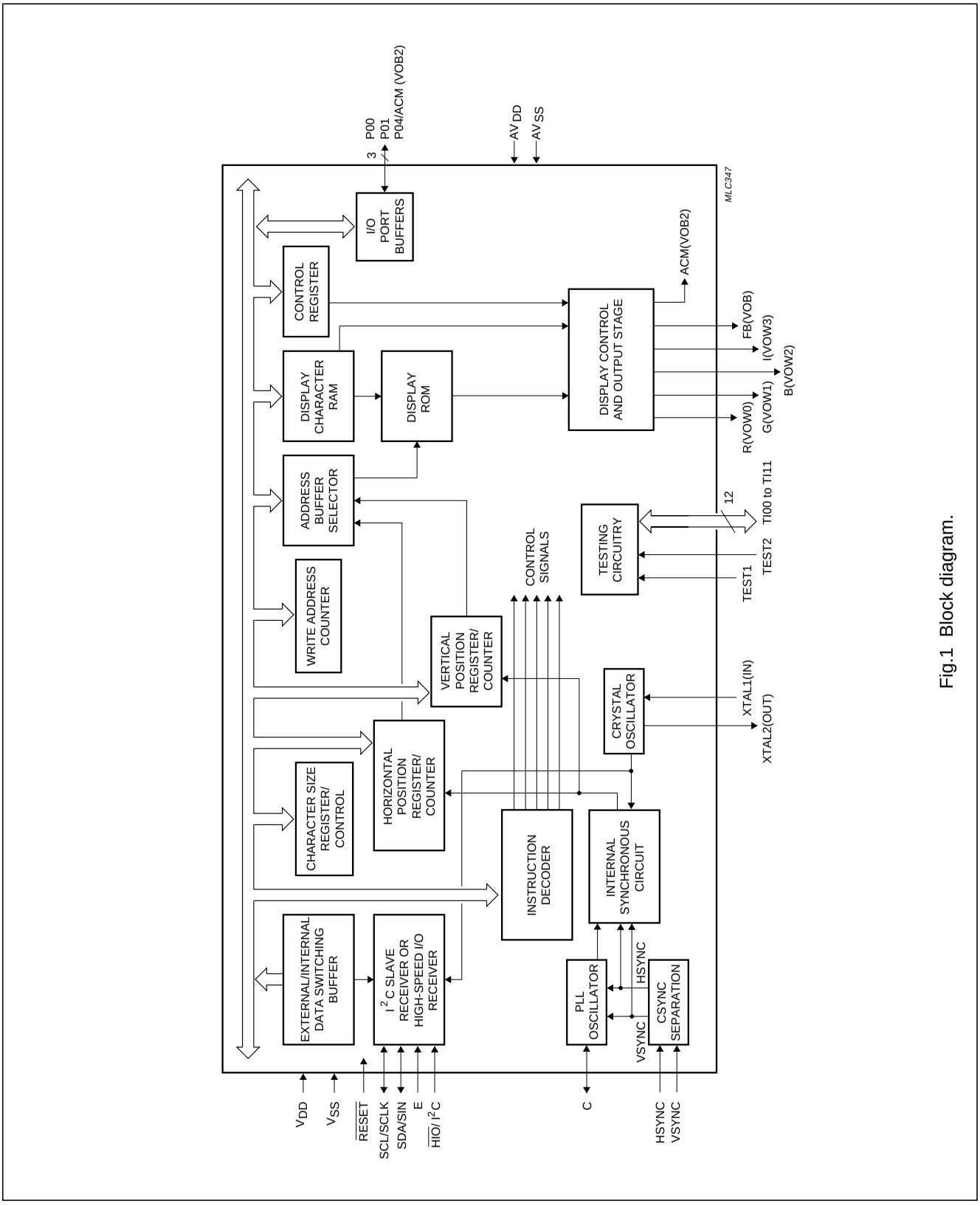


Fig.1 Block diagram.

5 PINNING INFORMATION

5.1 Pinning

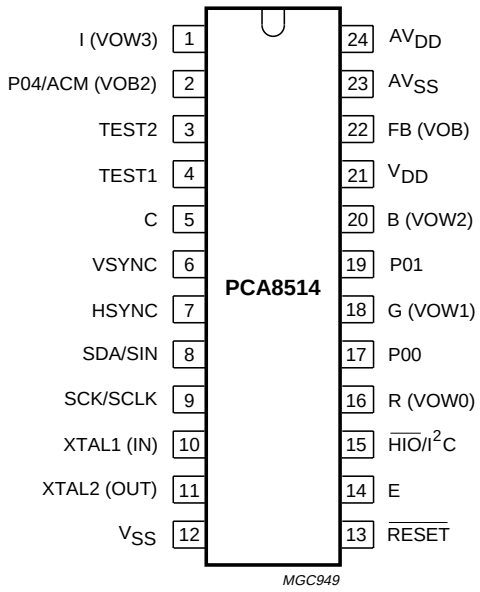


Fig.2 Pin configuration for SDIP24 and SO24.

5.2 Pin description

Table 1 SDIP24 and SO24 packages

SYMBOL	PIN	I/O	DESCRIPTION
I (VOW3)	1	O	Character output signal for intensity control.
P04/ACM (VOB2)	2	O	Port 04 output or Active Character Monitor output (VOB2).
TEST2	3	I	Test mode selection; for normal operation TEST2 is connected to $V_{SS.}$
TEST1	4	I	Test mode selection; for normal operation TEST1 is connected to V_{SS}.
C	5	I/O	Capacitor connection for on-chip OSD PLL oscillator.
VSYNC	6	I	Vertical synchronization input, active polarity programmable.
HSYNC	7	I	Horizontal synchronization input, active polarity programmable.
SDA/SIN	8	I/O	Data line of the I^2C-bus interface or the data line for the High-speed serial interface.
SCL/SCLK	9	I/O	Clock line of the I^2C-bus interface or the clock line for the High-speed serial interface.
XTAL1 (IN)	10	I	System clock input.
XTAL2 (OUT)	11	O	System clock output.
V_{SS}	12	I	Ground, digital.
$\overline{\text{RESET}}$	13	I	Master reset input (active LOW).
E	14	I	Chip enable (active HIGH) for the High-speed serial interface. When the I^2C-bus interface is selected this pin should be connected to V_{SS}.
$\overline{\text{HIO}}/I^2C$	15	I	Serial interface selection. When this pin is LOW the High-speed serial interface is selected; when this pin is HIGH the I^2C-bus interface is selected.
R (VOW0)	16	O	Character output signal: VOW0 for Red.
P00	17	I/O	General purpose I/O Port 00.
G (VOW1)	18	O	Character output signal: VOW1 for Green.
P01	19	I/O	General purpose I/O Port 01.
B (VOW2)	20	O	Character output signal: VOW2 for Blue.
V_{DD}	21	I	Power supply, digital.
FB (VOB)	22	O	Fast Blanking output (VOB).
AV_{SS}	23	I	Ground, analog.
AV_{DD}	24	I	Power supply, analog.

6 SERIAL I/O

The PCA8514 has two means by which it can communicate with a microcontroller: a fast I²C-bus serial interface and a High-speed serial interface. Selection of either interface is achieved via pin 15, $\overline{HIO}$/I²C. When $\overline{HIO}$/I²C is LOW, the HIO serial interface is selected. When $\overline{HIO}$/I²C is HIGH, the I²C-bus serial interface is selected.

The PCA8514 is programmed by a series of commands sent via one of these interfaces. There are 16 commands; each command selecting different functions of the PCA8514. The 16 commands are described in detail in Chapter 9.

6.1 I²C-bus serial interface

The I²C-bus serial interface is selected by driving pin 15 ($\overline{HIO}$/I²C) HIGH. Data transmission conforms to the fast I²C-bus protocol; the maximum transmission rate being 400 kHz. The PCA8514 operates in the slave receiver mode and therefore in normal operation is 'write only' from the master device.

The format of the data streams sent via the I²C-bus interface is shown in Fig.3. The first data byte is the slave address 1011 101X_b. The last bit of the slave address is always a logic 0, except in the Test mode when it could be a logic 1. Subsequent data bytes contain the commands for control of the device. Upon the successful reception of a complete data byte by the shift register, an Acknowledge bit is sent. A STOP condition terminates the data transfer operation.

The I²C-bus interface is reset to its initial state (waiting for a slave address call) by the following conditions:

- After a master reset
- After a bus error has been detected on the I²C-bus interface.

Under both these conditions the data held in the shift register is abandoned.

6.1.1 MAXIMUM SPEED OF THE I²C-BUS

The maximum I²C-bus transmission rate that the PCA8514 can receive is 400 kHz. However, if the data byte being transmitted is for display RAM then internal synchronization of the write operation from the shift register to the display RAM location is necessary. This will reduce the maximum transmission speed.

The synchronization process is carried out by on-chip hardware and takes place during the HSYNC retrace period when VSYNC is inactive. The I²C-bus clock is pulled LOW if a complete display RAM data byte is received before HSYNC becomes active. The I²C-bus clock will be released when HSYNC becomes active and then the contents of the shift register will be written into the display RAM location.

6.2 High-speed serial interface (HIO)

The High-speed serial interface is selected when pin 15 ($\overline{HIO}$/I²C) is pulled LOW. The High-speed serial interface has a 3-wire communication protocol; the maximum transmission rate being 1 MHz. The interface protocol is illustrated in Fig.4 and described below.

1. Pin 14 (E) the chip enable pin is driven HIGH. This LOW-to-HIGH transition clears the shift register and resets the serial input circuit.
2. On the first HIGH-to-LOW transition of SCLK after the interface has been enabled, the first data bit (D0) must be present at the SIN pin.
3. On the following LOW-to-HIGH transition of SCLK, the first data bit (D0) will be latched into the shift register.
4. On the next HIGH-to-LOW transition of SCLK the second data bit (D1) must be present at the SIN pin. Data bit (D1) will be latched into the shift register on the following LOW-to-HIGH transition of SCLK.
5. The operation specified in step 4 above is repeated another 6 times, thus loading the shift register with a complete data byte. This data byte is then transferred to the command interpreter which takes the appropriate action.
6. Providing the chip enable signal remains HIGH, a 2nd data byte can be transferred. The 1st data bit of the next data transfer takes place on the falling edge of the SCLK signal.

The following points should be noted:

- If the chip enable signal is pulled LOW at any time the shift operation in progress is stopped and the HIO slave receiver is disabled
- The rising edge of the chip enable signal resets the HIO slave receiver.

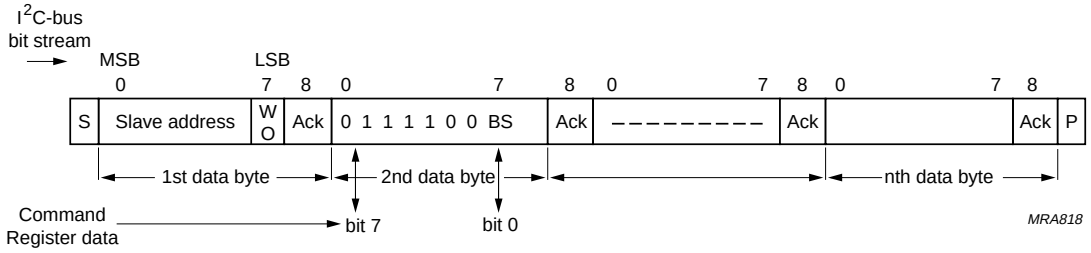
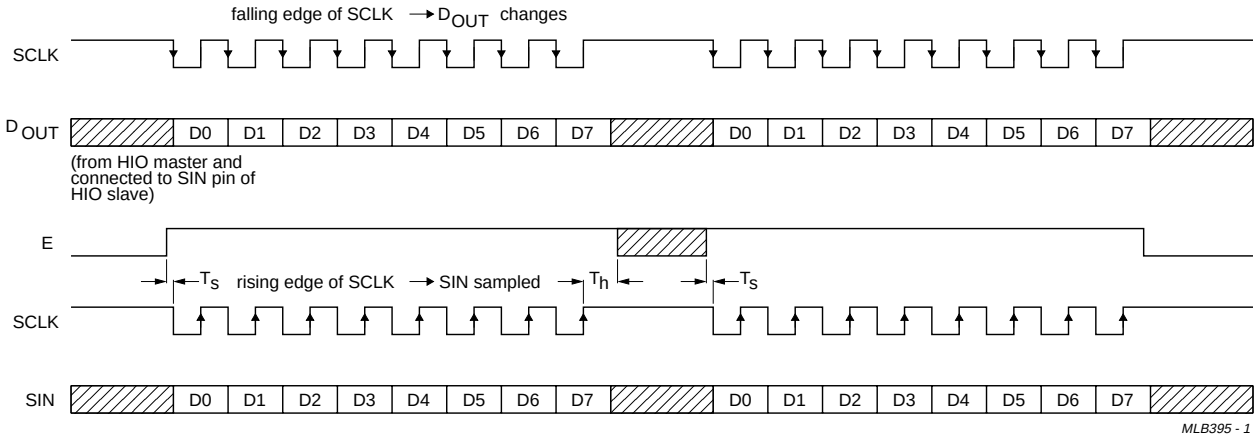


Fig.3 I^2C-bus write timing diagram - data stream.



(1) $T_s \geq 1\ \mu s$; $T_h \geq 1\ \mu s$.

Fig.4 High-speed I/O format.

7 CHARACTER FONTS

128 character fonts may be held in ROM; 125 customer selected fonts and three reserved character font codes. Customer selected fonts are mask programmable. Each character font is stored in a 12 × 19 dot matrix, as shown in Fig.5. Elements in Rows 1 to 18 can be selected as visible dots on the screen; Row 0 is used only for the combination of two characters in a vertical direction, when the North-West shadowing mode is selected (see Sections 9.9 and 10.2). Extremely high resolution can be achieved by having no spacing between characters on the same line and by programming the inter-line spacing to zero. The 12 × 18 dot matrix is suitable for the display of semigraphic patterns, Kanji, Hiragana, Katagana or even Chinese characters.

7.1 Character font address map

Figure 6 shows the character font address map in ROM and RAM. Addresses 7FH and 7EH hold the reserved codes for space and carriage return functions respectively; address 7DH is reserved for testing purposes and addresses (00H to 7CH) contain the character font codes.

7.2 Character font ROM

ROM is divided into two parts: ROM1 and ROM2. The organization of the bit patterns stored in ROM1 and ROM2 is shown in Fig.7.

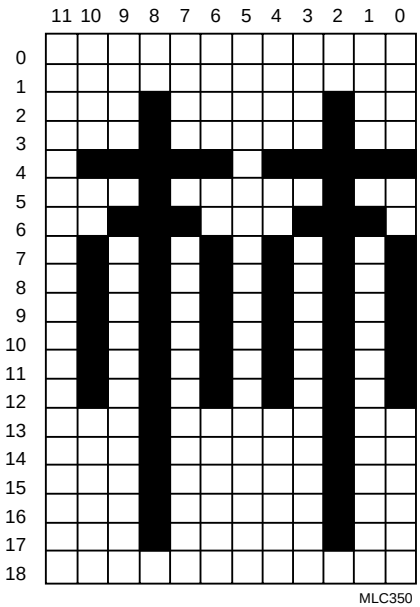


Fig.5 Character dot matrix organization.

The file format to submit to Philips for customized character sets is also shown in Fig.7. The following points should be noted:

1. Row 0 of each font is reserved for vertical combination of two fonts.
2. When two font cells are combined in a vertical direction Row 0 of the lower font must contain the same bit pattern as held in Row 18 of the character above it.
3. Binary 1 denotes visual dots; binary 0 denotes a blank space.
4. ROM1 and ROM2 data files are in INTEL hex format on a byte basis. Each byte is structured High nibble followed by Low nibble.
5. The remaining unused 16 bytes (one character font) in ROM1/ROM2 must be filled with FFH.
6. CS denotes Checksum.

A software package (OSDGEM) that assists in the design of character fonts on-screen and that also automatically generates the bit pattern HEX files, is available on request. The package is run under the MS-DOS environment for IBM compatible PCs.

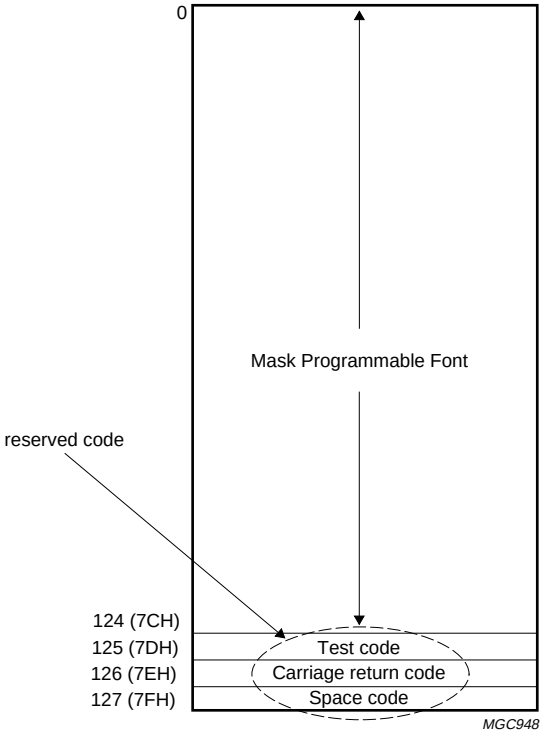


Fig.6 ROM address map.

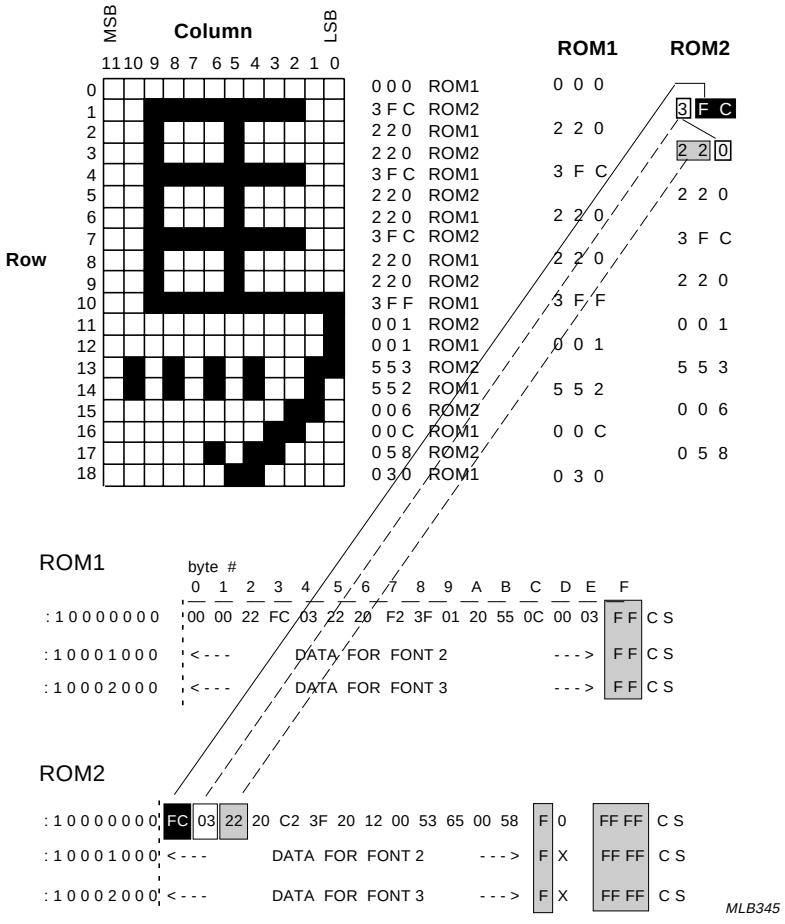


Fig.7 Character font pattern stored in ROM1 and ROM2.

8 DISPLAY RAM ORGANIZATION

The display RAM is organized as 256 × 12 bits. The general format of each RAM location is as follows. Bits <11-5> hold character data and allow a choice from 125 customer designed character fonts to be selected or one of three reserved codes. Bits <4-0> contain the attributes of the character font, for example colour, character size etc.

8.1 Description of display RAM codes

There are four data formats for display RAM code:

1. Character Font Code
2. Test Code
3. Carriage Return Code
4. Space Code.

The above data formats allow great flexibility in the creation of On Screen Displays; see Fig.8.

8.1.1 CHARACTER FONT CODE

If bits <11-5> are in the range (00H to 7CH), then this is a Character Font Code. 1 of 125 customer designed character fonts can be selected. Bits <4-1> determine the colour of the character, a choice of 16 colours being available. Bit <0> determines whether the character blinks or not. The format of the Character Font Code is shown in Table 2.

8.1.2 TEST CODE

If bits <11-5> hold 7DH, then this is a special code reserved for testing purposes only.

8.1.3 CARRIAGE RETURN CODE

If bits <11-5> hold 7EH, then this is the Carriage Return Code. A transparent pattern will be displayed on the screen and the next character will be displayed at the beginning of the next line. Bits <4-3> select the size of the characters to be displayed on the next line. Bits <2-1> determine the spacing between lines of displayed characters. Bit <0> is the End of Display bit and indicates the end of display of the current screen before exhaustion of display RAM (i.e. before the 256th RAM location). The format of the Carriage Return Code is shown in Table 3.

8.1.4 SPACE CODE

If bits <11-5> hold 7FH, then this is the Space Code. A transparent pattern, equal to one character width, will be displayed on the screen. A mask programmable option is available that allows the space character to be transparent or to have a programmable background colour; see Section 13.1. Bits <4-1> determine the background colour of the characters that follow the Space Code in both the Box shadowing and North-West shadowing modes. Bit <0> is the Active Character Monitor (ACM) enable/disable bit. The ACM signal is specifically for use in camrecorder applications where part of the display is to be recorded on tape and displayed on the screen, whilst the remaining part is for display only. Figure 9 shows a typical ACM application. During the back-tracing period R, G, B, I, FB and ACM are inactive. The format of the Space Code is shown in Table 4.

Table 2 Format of Character Font Code

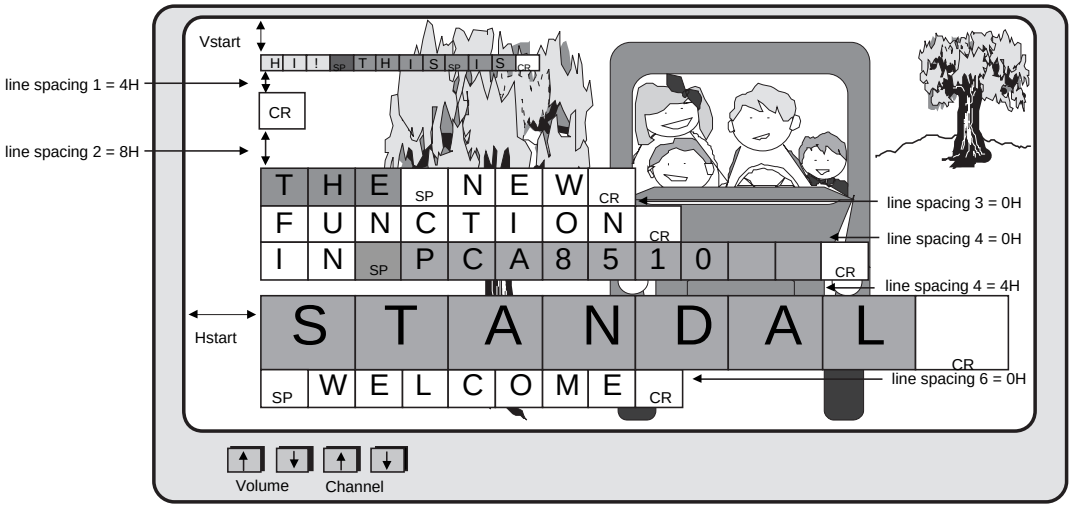
11	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
C6	C5	C4	C3	C2	C1	C0	T4	T3	T2	T1	T0
Character Font Code (00H - 7CH)							Foreground colour				Blink

Table 3 Format of Carriage Return Code

11	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
C6	C5	C4	C3	C2	C1	C0	T4	T3	T2	T1	T1
Carriage Return Code (7EH)							Character size		Line Spacing		End

Table 4 Format of Space Code

11	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
C6	C5	C4	C3	C2	C1	C0	T4	T3	T2	T1	T0
Space Code (7FH)							Background colour				ACM

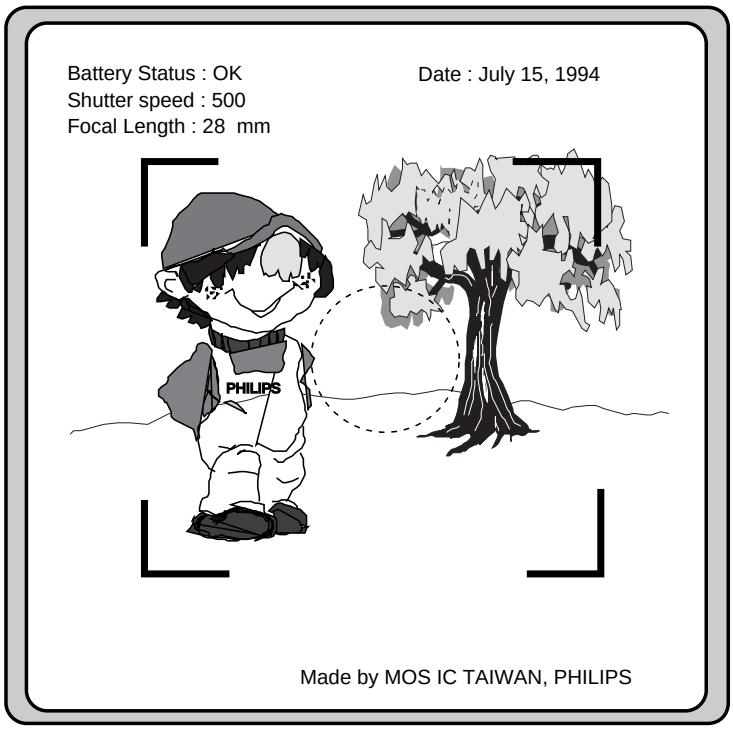


MRA832

Four different background colours (in box shadowing mode):

- BLACK
- RED
- GREEN
- BLUE

Fig.8 Example of On Screen Display.



In this example, all the characters are displayed on the viewfinder. As only the data 'Date : July 15, 1994' is to be recorded onto the tape, only these characters' ACM attribute bit is set to a logic 1.

Fig.9 Example of ACM signal for use in camrecorder applications.

8.2 Loading character data into display RAM

Three registers are used to address and load data into the display RAM. These registers are described below.

8.2.1 DCR ADDRESS REGISTER (DCRAR)

Table 5 DCR Address Register

7	6	5	4	3	2	1	0
A7	A6	A5	A4	A3	A2	A1	A0

This register holds the address of the location in display RAM into which data is to be written. Command 3 loads the High nibble of the address into this register; Command 4 loads the Low nibble of the address.

8.2.2 DCR ATTRIBUTE REGISTER (DCRTR)

Table 6 DCR Attribute Register

7	6	5	4	3	2	1	0
–	–	–	T4	T3	T2	T1	T0

The Attribute Register is loaded with character font attribute data using Command 2. The data will be loaded into bits <4-0> of the location in RAM addressed by the contents of DCRAR. Bits 7 to 5 are not used and are reserved.

8.2.3 DCR CHARACTER REGISTER (DCRCR)

Table 7 DCR Character Register

7	6	5	4	3	2	1	0
–	C6	C5	C4	C3	C2	C1	C0

This register holds the character font data loaded by Command 5. The data will be loaded into bits <12-5> of the location in RAM addressed by the contents of DCRAR.

8.3 Writing character data to display RAM

The procedure for writing character data to the display RAM is as follows:

1. Select the start address in display RAM. The start address can take any value between 0 and 255. Command 3 is used to load the High nibble of the start address. Command 4 is used to load the Low nibble of the start address. The start address is stored in DCRAR.
2. Load the character attributes into DCRTR using Command 2. The actual attribute selected is dependent upon whether the Character Font Code, Carriage Return Code or Space Code has been selected by Command 5 (see Section 8.1).

   If the attributes of a series of displayed characters are the same, the contents of this register need not be updated.
3. Load the Character Font data into DCTCR using Command 5. This command signals that a complete command byte is available and the data held in registers DCRTR and DCRCR is loaded into the RAM location pointed to by the address stored in DCRAR. The address held in DCRAR is then incremented by ‘1’ pointing to the next RAM location in anticipation of the next operation.

A description of all the Commands is given in Chapter 9.

9 COMMANDS

The PCA8514 is programmed by a series of commands sent by a microcontroller via the I^2C-bus interface or the High-speed serial interface. 16 commands (Commands 0 to G) are available for selecting the various functions of the PCA8514. A command overview is shown in Table 8; full descriptions of each command are given in Sections 9.1 to 9.15.

Table 8 Command overview (note 1)

COMMAND		BS1	BS0	7	6	5	4	3	2	1	0
0	Command Bank selection	X	X	0	1	1	1	1	0	BS1	BS0
1	Not used in the PCA8514	0	0	1	–	–	–	–	–	–	–
2	Character attributes	X	0	0	0	0	T4	T3	T2	T1	T0
3	Display Character Address High	0	0	0	0	1	0	A7	A6	A5	A4
4	Display Character Address Low	0	0	0	0	1	1	A3	A2	A1	A0
5	Character font selection - Bank 2	1	0	1	C6	C5	C4	C3	C2	C1	C0
6	OSD PLL oscillator divisor	0	1	0	0	D5	D4	D3	D2	D1	D0
7	Scan mode, polarity of FB, ACM, R, G, B and I; OSD enable/disable	0	1	0	1	0	0	M1	M0	Bp	EN
8	Polarity of HSYNC and VSYNC, Display mode	0	1	0	1	0	1	Hp	Vp	S1	S0
9	Blinking frequency, blinking frequency active ratio	0	1	0	1	1	0	BF1	BF0	BR1	BR0
A	I/O port selection	0	1	0	1	1	1	0	A/P	0	0
B	Vertical start position High	0	1	1	0	0	1	V5	V4	V3	V2
C	Vertical start position Low/ Horizontal start position High	0	1	1	0	1	0	V1	V0	H5	H4
D	Horizontal start position Low	0	1	1	0	1	1	H3	H2	H1	H0
E	Write to ports P00, P01 and P04	0	1	1	1	X	P04	X	X	P01	P00
F	Background colour in Frame shadowing mode	0	0	0	1	0	0	R	G	B	I
G	Enable/disable OSD horizontal stabilization circuit (Regen H), selection of Half-tone background mode and character size of first line	0	0	0	1	0	1	HM3	HT2	FS1	FS0

Note

1. ‘X’ denotes don’t care state.

9.1 Command 0

Table 9 Command 0 format

7	6	5	4	3	2	1	0
0	1	1	1	1	0	BS1	BS0

Command 0 is used to select the Command Bank. Bits BS1 and BS0 are the two flags that indicate the current Command Bank being executed. During a master reset these two bits are cleared (BS1 = 0, BS0 = 0). Each command has its own associated Command Bank, this is shown in Table 8.

9.2 Command 1

Command 1 is not used in the PCA8514.

9.3 Command 2

Table 10 Command 2 format

BS1	BS0	7	6	5	4	3	2	1	0
X	0	0	0	0	T4	T3	T2	T1	T0

This command writes character attribute data into the DCR Attribute Register. The actual character attribute is dependent upon the code selected by Command 5.

Sections 9.3.1 to 9.3.2 define the character attribute data loaded by Command 2 when Command 5 selects either a Character Font Code, a Carriage Return Code or a Space code. See Tables 2, 3 and 4 for the three code formats.

9.3.1 Character Font Code attributes

Command 2 when used in conjunction with a Character Font Code (00H to 7CH) will select 1 of 16 foreground colours and enables/disables the Blinking function.

Table 11 Selection of Foreground colour

T4	T3	T2	T1
R	G	B	I
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

Table 12 Selection of Blinking function

T0	BLINKING
0	OFF
1	ON

9.3.2 Carriage Return Code attributes

Command 2 when used in conjunction with the Carriage Return Code (7EH) determines the size of characters to be displayed on the next line, sets the spacing between lines of characters and enables/disables the display.

The character size is also a function of the TV scanning standard being used and f_{OSD}; this is explained in Chapter 12.

Table 13 Selection of character size

T4	T3	CHARACTER DOT SIZE
0	0	1H/1V (the default size)
0	1	2H/2V
1	0	3H/3V
1	1	4H/4V

Table 14 Selection of line spacing

T2	T1	LINE SPACING (BETWEEN TWO ROWS)
0	0	0H line
0	1	4H line
1	0	8H line
1	1	12H line

Table 15 End of display control

T0	DISPLAY CONTROL
0	Continue to display next character. This is also the default setting.
1	End of display.

9.3.3 Space Code attributes

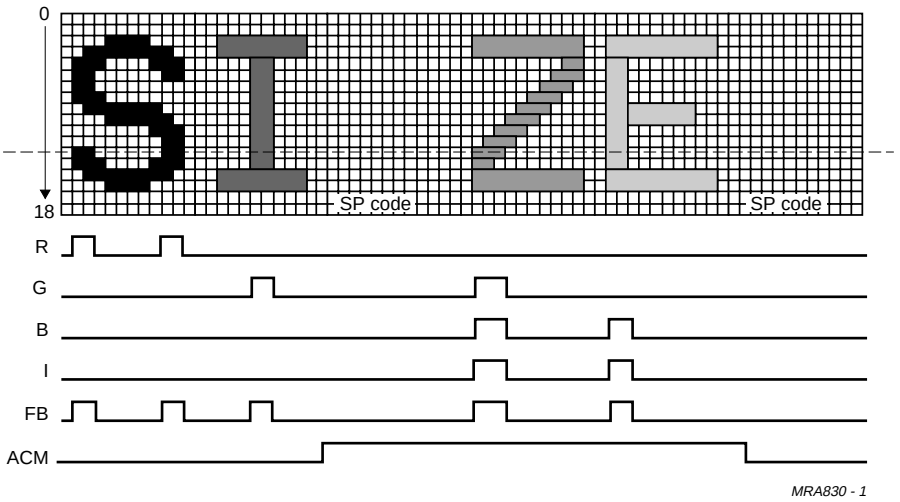
Command 2 when used in conjunction with the Space Code (7FH) selects the background colour of characters in Box shadowing or North-West shadowing modes and also controls the Active Character Monitor pin. The ACM pin will remain active until a Space Code is received that resets the ACM bit to logic 0. The ACM timing diagram is shown in Fig.10.

Table 16 Selection of Background colour

T4	T3	T2	T1
R	G	B	I
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

Table 17 ACM control

T0	ACM PIN
0	The ACM pin is inactive; this is also the default setting.
1	The ACM function is active for all characters displayed following this Space Code.



'S' : Red
'I' : Green
'Z' : Green + Blue + Intensity
'E' : Blue + Intensity

1st SP code : ACM = on
2nd SP code: ACM = off

Fig.10 R, G, B, I - ACM timing.

9.4 Command 3

Table 18 Command 3 format

BS1	BS0	7	6	5	4	3	2	1	0
0	0	0	0	1	1	A7	A6	A5	A4

Command 3 loads the DCR Address Register with the 4 MSBs of the RAM address to which data will be written.

9.5 Command 4

Table 19 Command 4 format

BS1	BS0	7	6	5	4	3	2	1	0
0	0	0	0	1	1	A3	A2	A1	A0

Command 4 loads the DCR Address Register with the 4 LSBs of the RAM address to which data will be written.

9.6 Command 5

Table 20 Command 5 format

BS1	BS0	7	6	5	4	3	2	1	0
1	0	1	C6	C5	C4	C3	C2	C1	C0

Command 5 is used to load character data into the DCR Character Register. The data will specify either a Character Font Code, the Test Code, the Carriage Return Code or the Space Code. These codes are explained in detail in Section 8.1.

9.7 Command 6

Table 21 Command 6 format

BS1	BS0	7	6	5	4	3	2	1	0
0	1	0	0	D5	D4	D3	D2	D1	D0

Command 6 loads the programmable 6-bit counter of the OSD clock oscillator. The output frequency (f_{OSD}) is a function of the decimal value of the 6-bits loaded in by Command 6; see Chapter 11.

9.8 Command 7

Table 22 Command 7 format

BS1	BS0	7	6	5	4	3	2	1	0
0	1	0	1	0	0	M1	M0	Bp	EN

This command loads Control Register 1 with data that selects the scanning mode, the output polarity of signals FB, ACM, R, G, B and I, and also enables/disables the OSD clock.

With reference to the scanning modes: 1V/2V is the conventional NTSC or PAL scanning mode; 1V/2H is the Line Progress Scan used for the IDTV in NTSC and 2V/2H is for the PAL system and is known as 50 to 100 Hz scan conversion.

Table 23 Selection of Scanning Mode

M1	M0	SCAN MODE
0	0	1V/1H; NTSC 525LPF/60 Hz or PAL 625LPF/50 Hz; see Fig.11. This is the default setting.
0	1	reserved
1	0	1V/2H; NTSC 1050LPF/60 Hz; see Fig.11.
1	1	2V/2H; PAL 1250LPF/100 Hz; see Fig.12.

Table 24 Selection of output polarity (see Fig.13)

Bp	OUTPUT POLARITY (FB, ACM, R, G, B, I)
0	active LOW
1	active HIGH (the default setting)

Table 25 OSD clock control

EN	OSD CLOCK
0	disabled (the default setting)
1	enabled

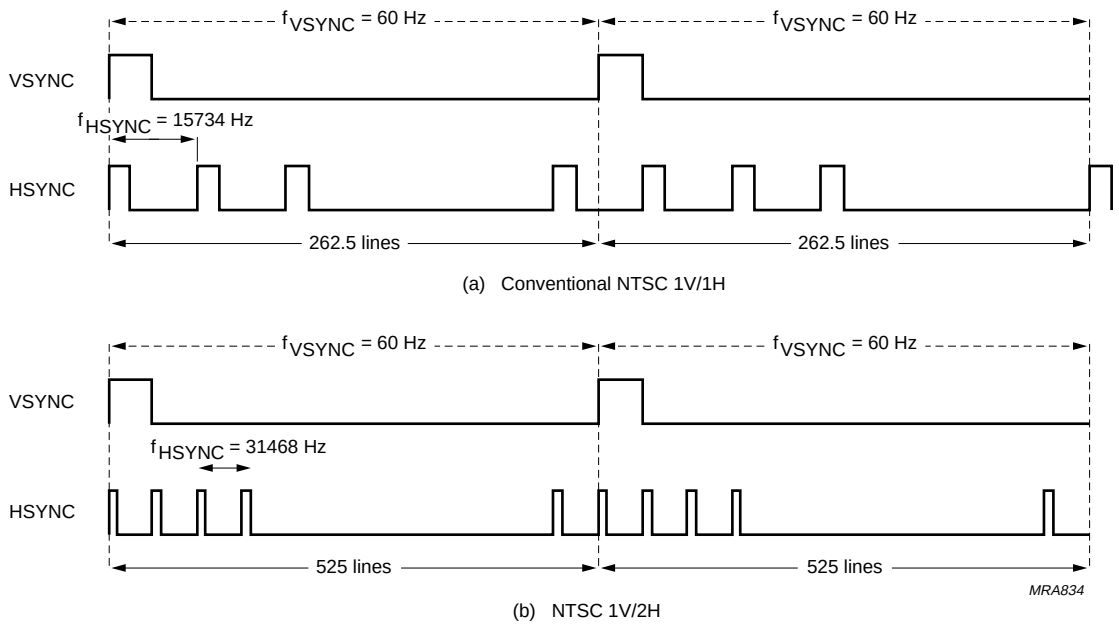


Fig.11 NTSC scan formats.

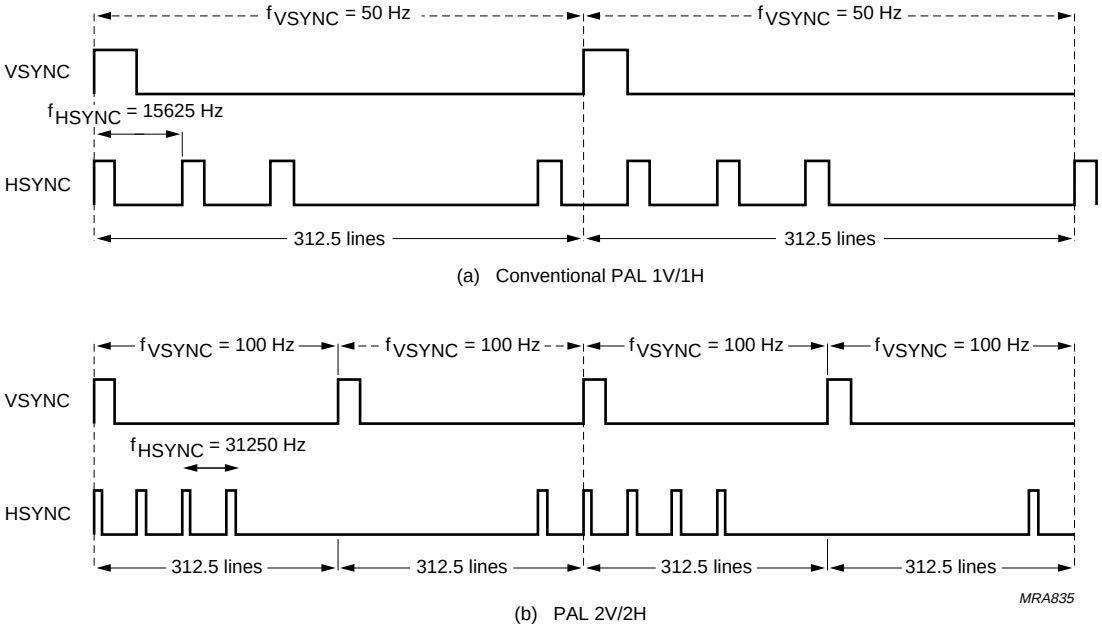


Fig.12 PAL scan formats.

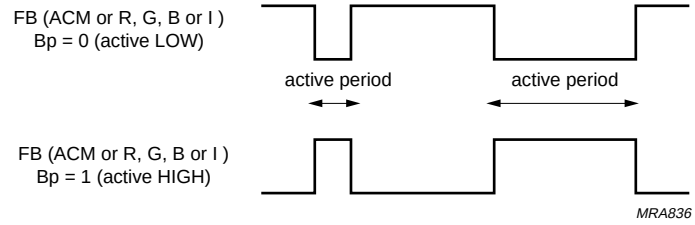


Fig.13 Active levels of FB, R, G, B, and I signals.

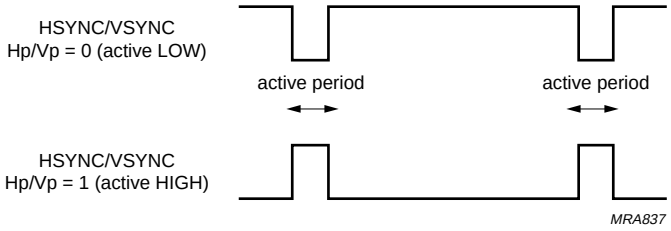


Fig.14 Active levels of HSYNC and VSYNC signals.

9.9 Command 8

Table 26 Command 8 format

BS1	BS0	7	6	5	4	3	2	1	0
0	1	0	1	0	1	Hp	Vp	S1	S0

Command 8 loads Control Register 2 with data that selects the input polarity of HSYNC and VSYNC (see Fig.14) and also selects the Display modes.

Table 27 Selection of input polarity of HSYNC/VSYNC

Hp/Vp	INPUT POLARITY
0	active LOW (the default setting)
1	active HIGH

Table 28 Selection of Display Mode

S1	S0	DISPLAY MODE
0	0	Mode 0: this is the No background mode. The OSD characters are superimposed on the TV video signals (see Fig.15).
0	1	Mode 1: this is the North-West shadowing mode; available only with character sizes 2V/2H or 4V/4H. The shadows are generated as if a light source was placed North-West of the character (see Figs 16 to 18). The shadows generated lie within 18 rows in a vertical direction but can be extended by one bit to the next characters first column, in a horizontal direction (see Figs 19 and 20).
1	0	Mode 2: this is the Box shadowing mode. A background dot matrix of 12×18 bits surrounds the character font; see Figs 21 and 22.
1	1	Mode 3: this is the Frame shadowing (raster blanking) mode. A background colour fills the whole screen when no bit patterns are being displayed (see Fig.23). 1 of 16 background colours can be selected using Command F; the default background colour is Blue.

9.10 Command 9

Table 29 Command 9 format

BS1	BS0	7	6	5	4	3	2	1	0
0	1	0	1	1	0	BF1	BF0	BR1	BR0

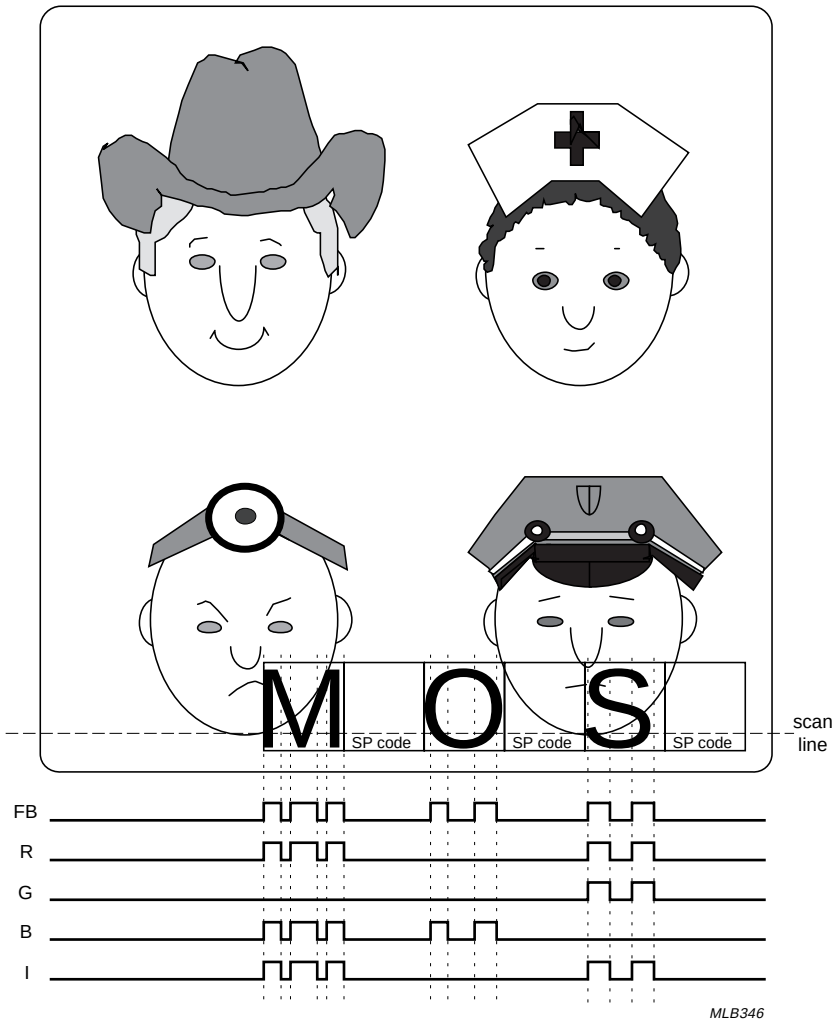
This command loads Control Register 3 with data that controls both the character blinking frequency and the active ratio of the character blinking frequency.
Figures 25 to 29 show how blinking influences the display in different display modes.

Table 30 Selection of Blinking frequency

BF1	BF0	BLINKING FREQUENCY (Hz)
0	0	$\frac{f_{VSYNC}}{16}$; this is the default setting
0	1	$\frac{f_{VSYNC}}{32}$
1	0	$\frac{f_{VSYNC}}{64}$
1	1	$\frac{f_{VSYNC}}{128}$

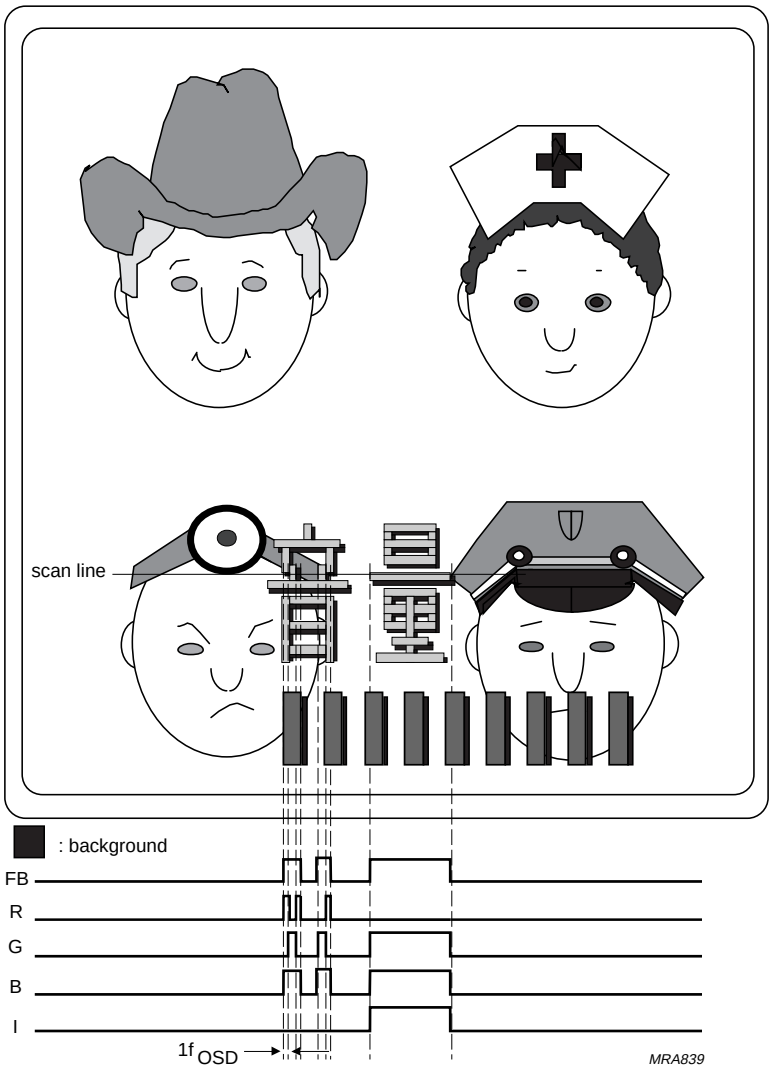
Table 31 Selection of active ratio of character blinking

BR1	BR0	ACTIVE RATIO
0	0	3 : 1 (the default setting)
0	1	1 : 1
1	0	1 : 3
1	1	reserved



'M' : Red + Blue + Intensity
'O' : Blue
'S' : Red + Green + Intensity
Bp = 1

Fig.15 Mode 0: No background mode.



1st character: GREEN
2nd character: GREEN + BLUE + INTENSITY
background: RED + BLUE
Bp = 1 (active HIGH)
Available only in character sizes 2V/2H or 4V/4H.

Fig.16 Mode 1: North-West shadowing mode.

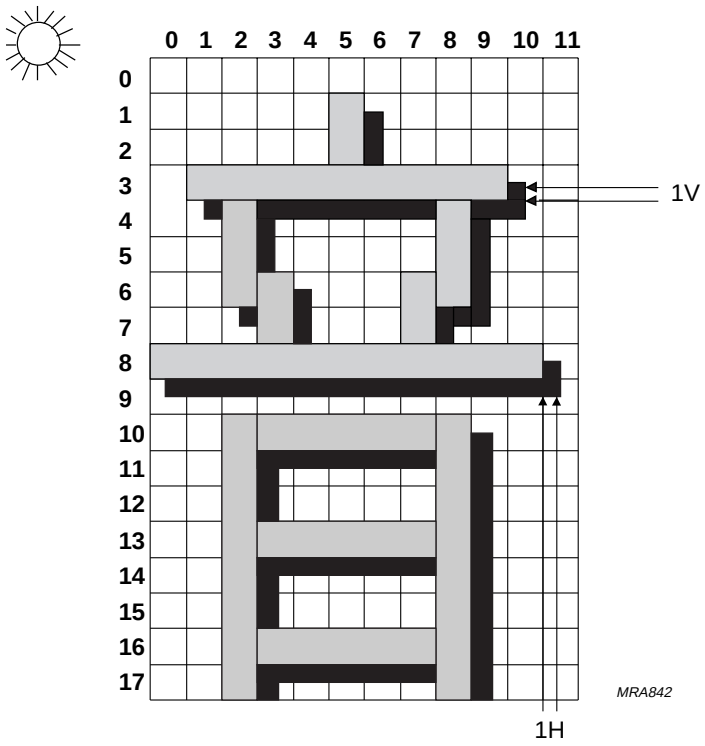


Fig.17 Example of North-West shadowing mode - size 2V/2H.

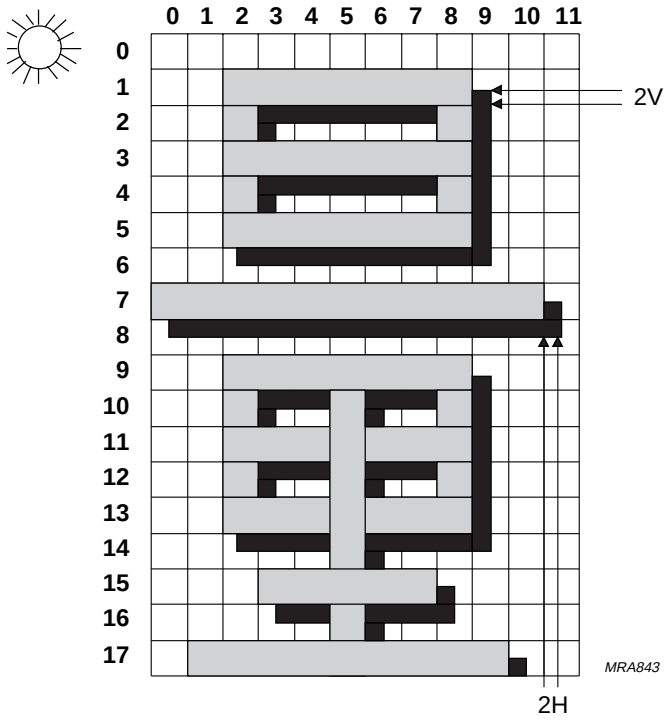


Fig.18 Example of North-West shadowing mode - size 4V/4H.

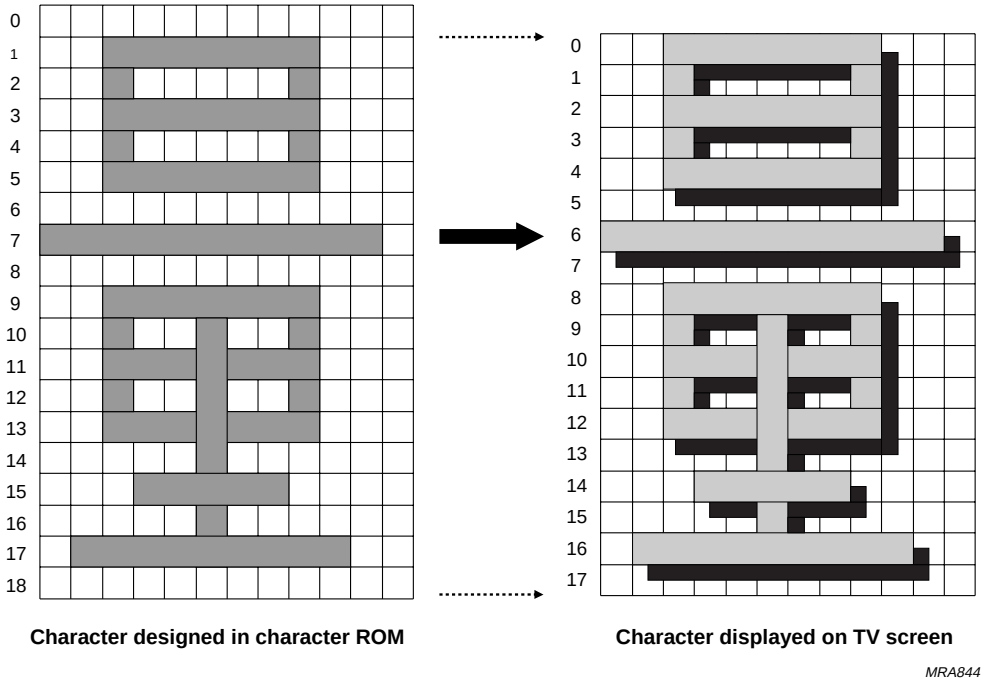


Fig.19 Example of North-West shadowing mode.

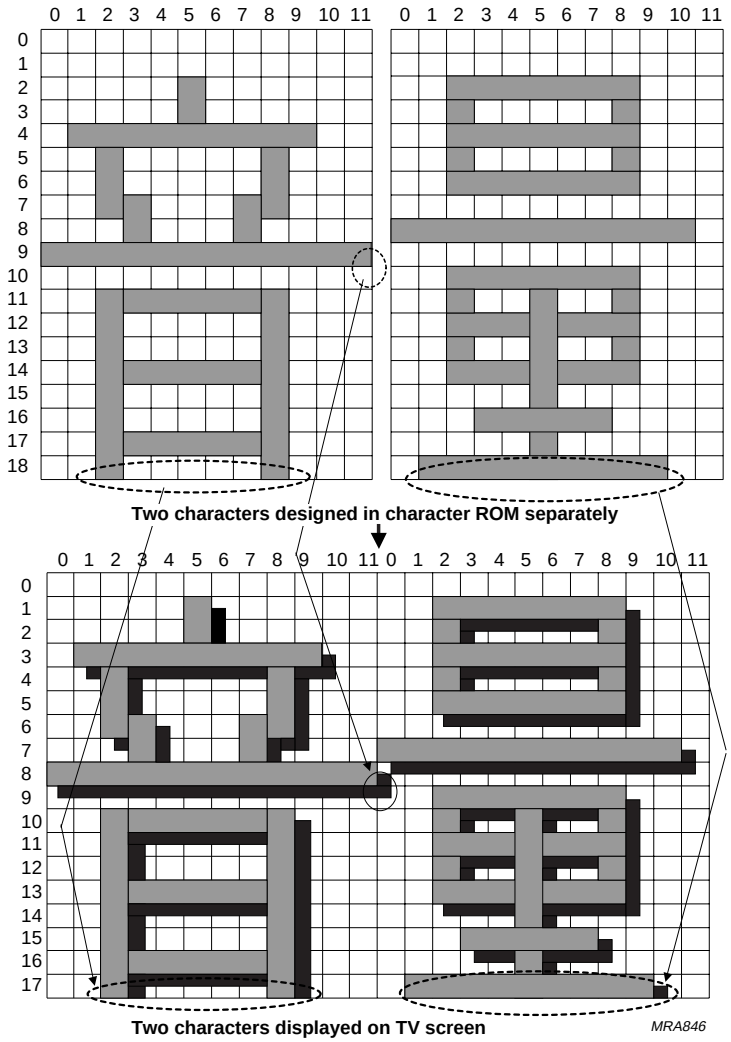


Fig.20 North-West shadowing.

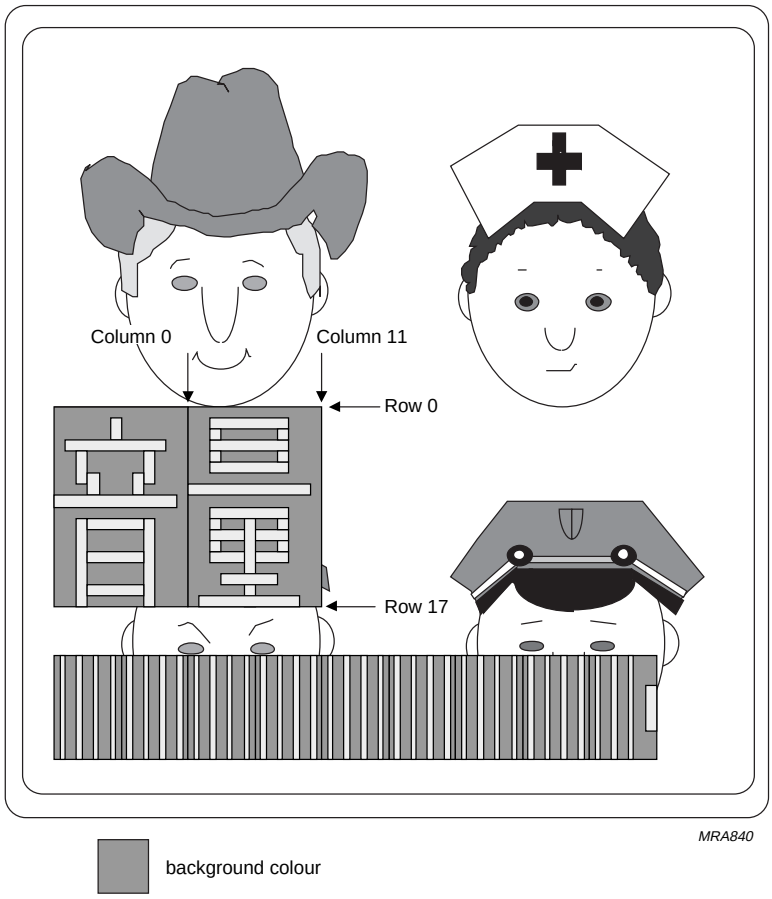


Fig.21 Mode 2: Box shadowing mode.

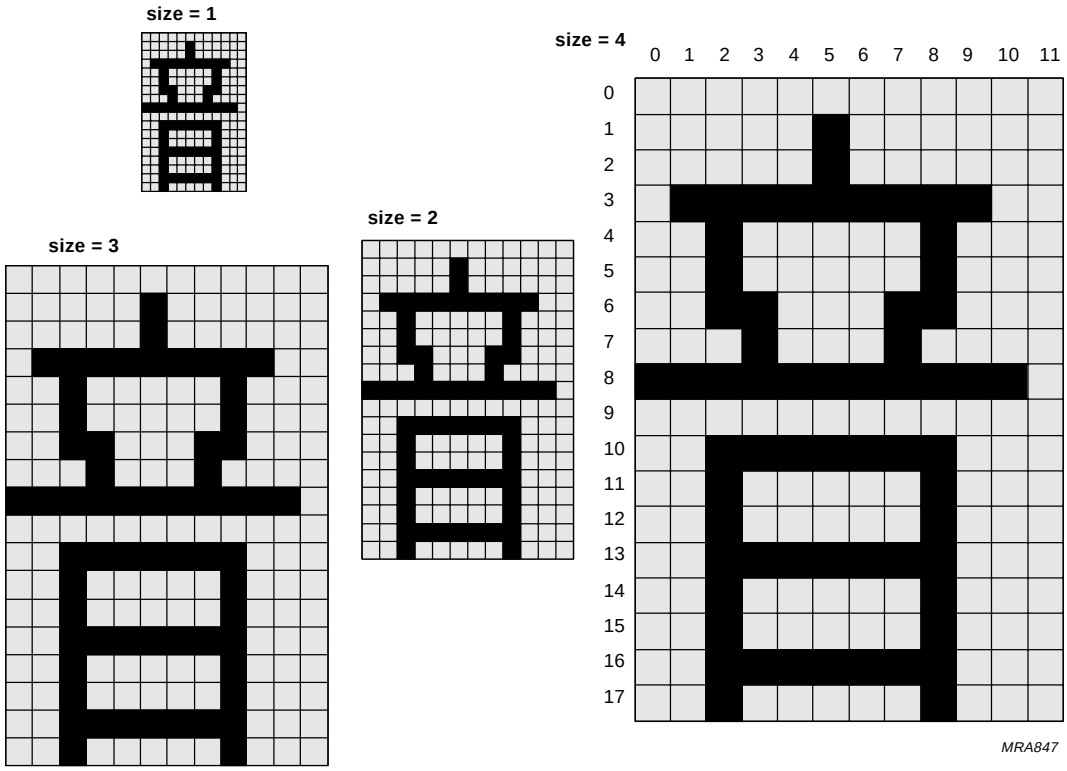


Fig.22 Example of Box shadowing mode.

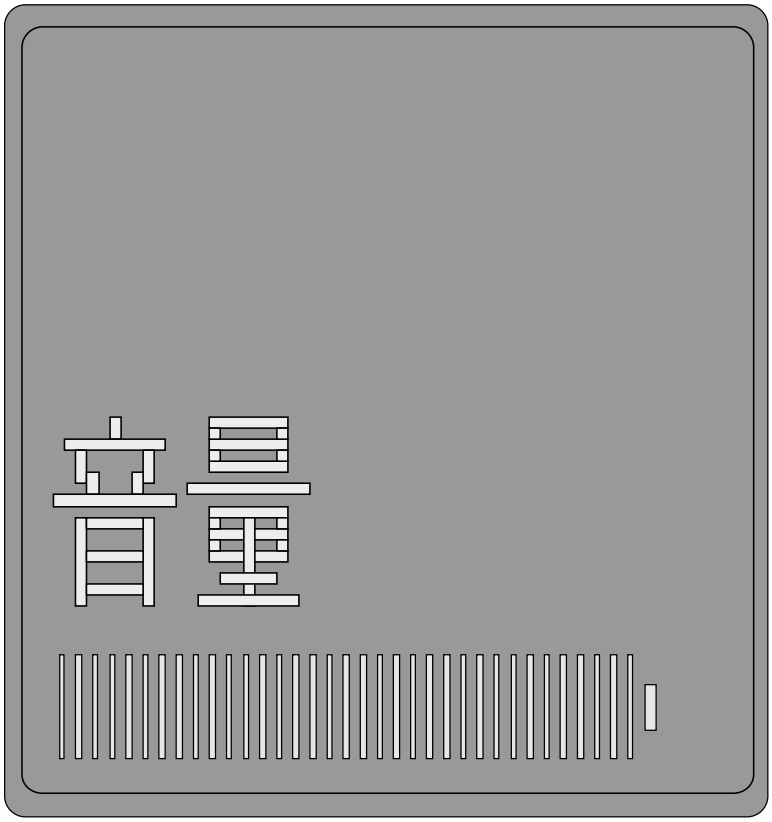


Fig.23 Mode 3: Frame shadowing mode.

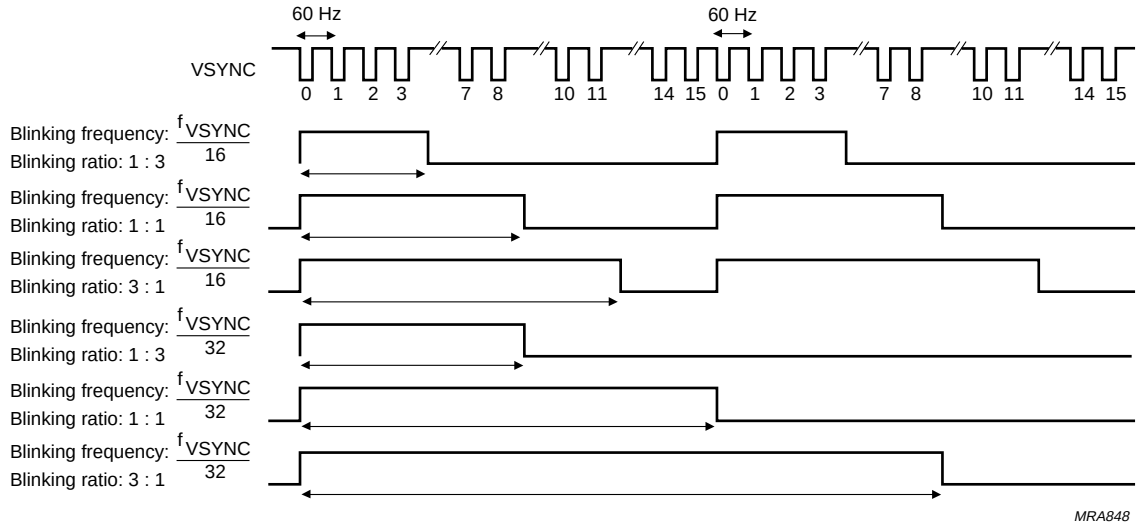


Fig.24 Timing diagram of character blinking frequency and blinking ratio.

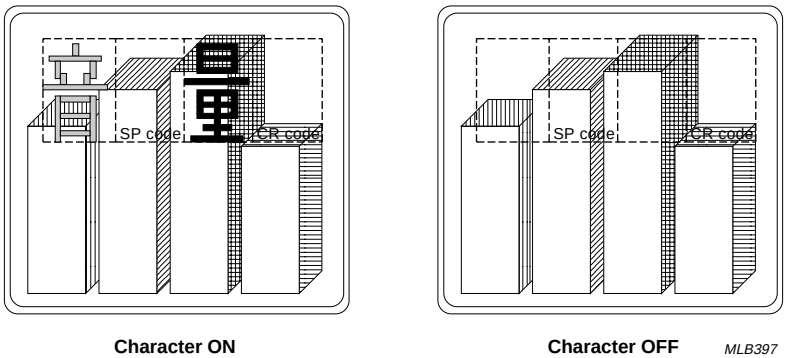


Fig.25 Blinking in No background mode.

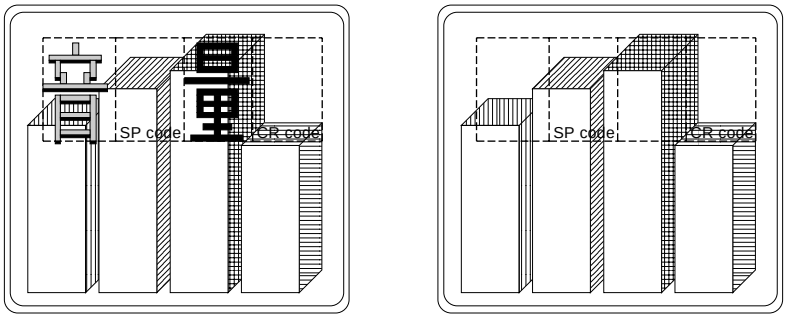


Fig.26 Blinking in North-West shadowing mode.

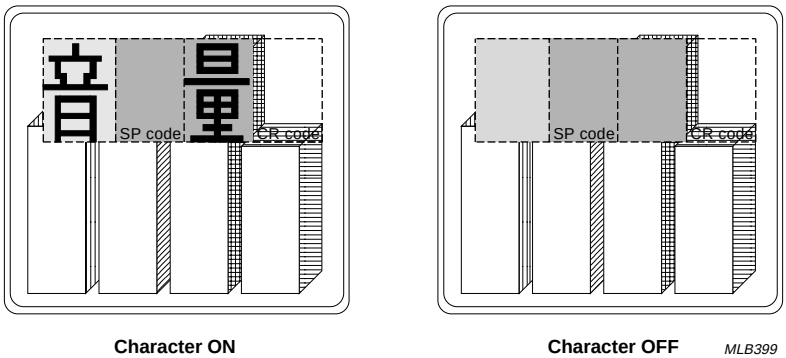


Fig.27 Blinking in Box shadowing mode (Space Code with background).

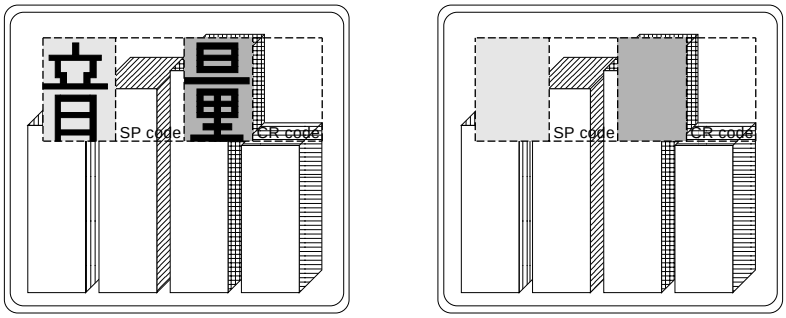


Fig.28 Blinking in Box shadowing mode (Space Code without background).

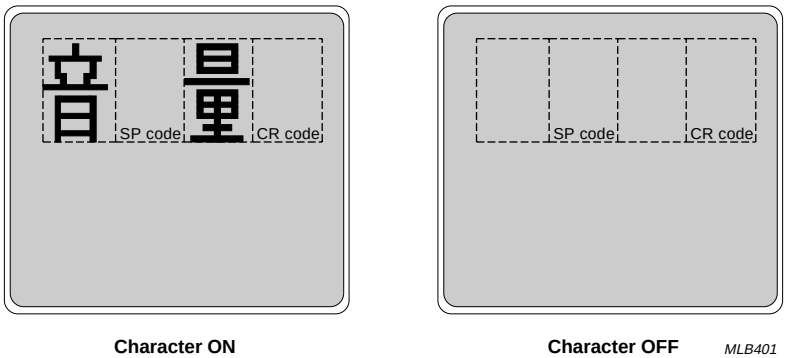


Fig.29 Blinking in Frame shadowing mode.

9.11 Command A

Table 32 Command A format

BS1	BS0	7	6	5	4	3	2	1	0
0	1	0	1	1	1	0	A/P	0	0

Command A loads Control Register 4 with data that determines the function of pin 2 (P04/ACM(VOB2)).

Table 33 Selection of P04 or ACM

A/P	PIN FUNCTION
0	P04 is selected as an output port. Data is written to this port using Command E. This is also the default setting.
1	ACM function selected; can also be used as the 5th colour signal.

9.12 Commands B, C and D

Table 34 Command B format

BS1	BS0	7	6	5	4	3	2	1	0
0	1	1	0	0	1	V5	V4	V3	V2

Table 35 Command C format

BS1	BS0	7	6	5	4	3	2	1	0
0	1	1	0	1	0	V1	V0	H5	H4

Table 36 Command D format

BS1	BS0	7	6	5	4	3	2	1	0
0	1	1	0	1	1	H3	H2	H1	H0

These three commands determine the vertical and horizontal start positions of the display. 64 vertical and 64 horizontal start positions can be selected. After a master reset, starting positions are not guaranteed and therefore must be programmed by the user. The horizontal start position (HP) and the vertical start position (VP) may be calculated as follows:

$$HP = [4 \times (H5 \rightarrow H0) + 5] \times f_{OSD}$$

Where (H5 → H0) is the decimal value of these 6 bits and (H5 → H0) ≥ 4.

$$VP = [4 \times (V5 \rightarrow V0)] \times \text{number of scan lines}$$

Where (V5 → V0) is the decimal value of these 6 bits and (V5 → V0) ≥ 0.

9.13 Command E

When output ports P00, P01 and P04 are enabled, Command E is used to write data to them.

Table 37 Command E format

BS1	BS0	7	6	5	4	3	2	1	0
0	1	1	1	X	P04	X	X	P01	P00

9.14 Command F

Table 38 Command F format

BS1	BS0	7	6	5	4	3	2	1	0
0	0	0	1	0	0	R	G	B	I

This command loads Control Register 5 with data that determines the background colour in Frame shadowing mode.

9.15 Command G

Table 39 Command G format

BS1	BS0	7	6	5	4	3	2	1	0
0	0	0	1	0	1	HM3	HT2	FS1	FS0

Command G is used to enable/disable the OSD horizontal stabilization circuit, to select the Half-tone mode and to select the character size of the first line.

In the Half-tone mode, excellent semi-transparent half-tone effects can be obtained with OSD frequencies in the range 4 to 7 MHz. This mode also enhances the background colour with intensity output. For further details on the half-tone effect refer to *"The programming guide for the PCA8514"*, report number MICT/AN9402.

Table 40 Horizontal stabilization circuit control

HM3	STATE OF STABILIZATION CIRCUIT
0	Stabilization circuit disabled (the default state).
1	Horizontal stabilization circuit enabled.

Table 41 Selection of Half-tone mode

HT2	HALF-TONE MODE
0	Half-tone mode not selected (the default state).
1	Half-tone mode available when ACM bit = 1.

Table 42 Selection of the character size for the first line

FS1	FS0	CHARACTER DOT SIZE
0	0	1H/1V (the default size)
0	1	2H/2V
1	0	3H/3V
1	1	4H/4V

10 MISCELLANEOUS

10.1 Space and Carriage Return Codes in different Background/Shadowing modes

Figures 30 to 34 show the Space Code and Carriage Return Code in the 4 different Background/Shadowing modes:

- Mode 0: the No background mode. Both the Space Code and the Carriage Return Code are displayed as transparent (no bit) patterns with the video signal as the background. This is shown in Fig.30.
- Mode 1: the North-West shadowing mode. Both codes are displayed in the same manner as for Mode 0. This is shown in Fig.31.
- Mode 2: the Box shadowing mode. The Space Code is displayed as an opaque pattern with a selected background colour. This will also be the background colour of the character following the Space Code. The Carriage Return Code however, is displayed as a transparent (no bit) pattern superimposed on the video signal. This is shown in Fig.32.

  The Space Code can also be displayed as a transparent pattern on the video signal, and this is shown in Fig.33. The choice of whether the Space Code displays an opaque pattern or a transparent pattern is mask programmable.
- Mode 3: the Frame shadowing mode. The Space Code and Carriage Return Code are displayed as transparent patterns with background colour. This is shown in Fig.34.

10.2 Combination of character font cells

Two (or more) character font cells may be combined in a horizontal or vertical direction to create a new higher resolution pattern.

The combination of two cells in a horizontal direction is straight forward and requires no special precautions to be taken. When combining character cells in this manner all 4 Background/Shadowing modes are available. An example of combining two character font cells in a horizontal direction is shown in Fig.35.

However, the combination of two character font cells in a vertical direction is more difficult and care must be taken; otherwise, the new pattern may be created with gaps in its shadowing. An example of a character pattern with gaps is shown in Fig.37. Providing the steps listed below are followed no problems with shadowing will occur.

- The line spacing between two rows of characters must be programmed to 0H. This procedure is explained in Section 9.3.2.
- If the North-West shadowing mode is selected then when combining two character cells in a vertical direction Row 0 must contain the same bit pattern as held in Row 18 of the character directly above it. This is shown in Fig.38.
- If North-West shadowing is not required then Row 0 should contain all zeros.

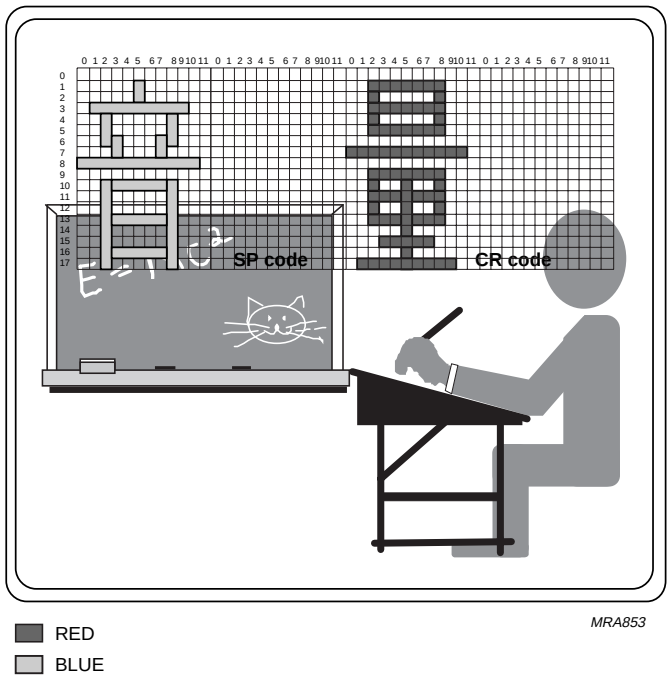


Fig.30 Space Code and Carriage Return Code in No Background mode - transparent pattern.

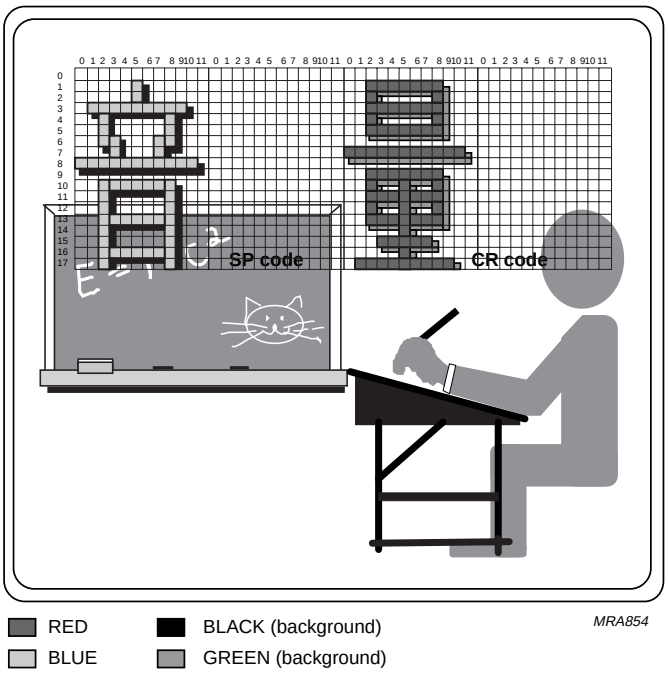
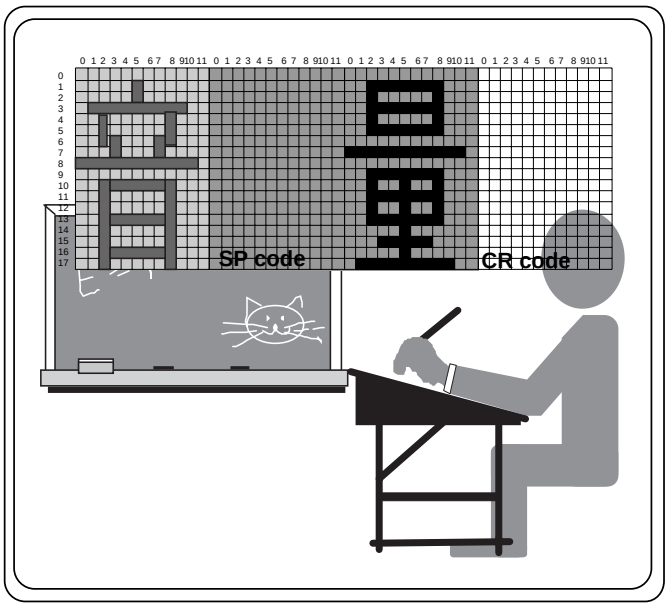
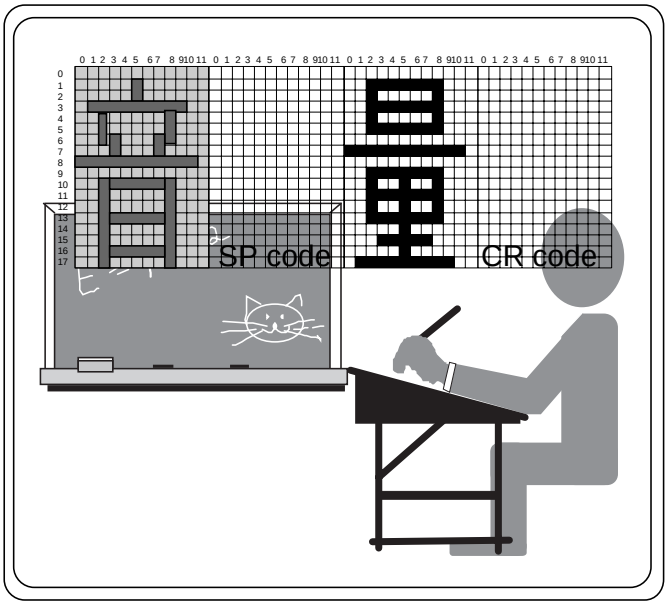


Fig.31 Space Code and Carriage Return Code in North-West shadowing mode - transparent pattern.



SP code is an opaque pattern with the background colour of the character it intends to change or keep.
CR code is always a transparent pattern with the video signal as its background.
SP code can change the background colour of itself and the character/word next to it (in this example: from cyan to yellow).

Fig.32 Space Code and Carriage Return Code in Box shadowing mode.

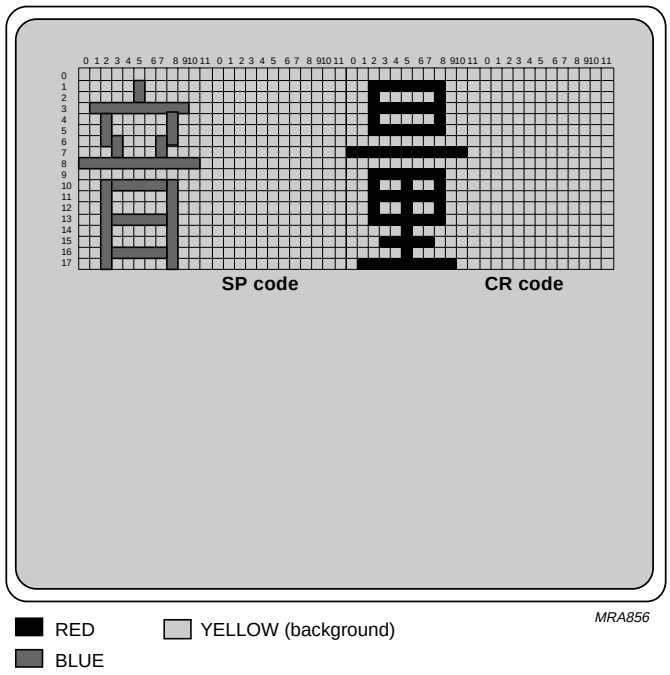


SP code is an transparent pattern with no background colour.

CR code is always a transparent pattern with the video signal as its background.

SP code can change the background colour the character/word next to it (in this example : from cyan to yellow).

Fig.33 Space Code and Carriage Return Code in Box shadowing mode.



SP and CR codes are both transparent patterns coloured the same as the background colour.

Fig.34 Space Code and Carriage Return Code in Frame shadowing mode.

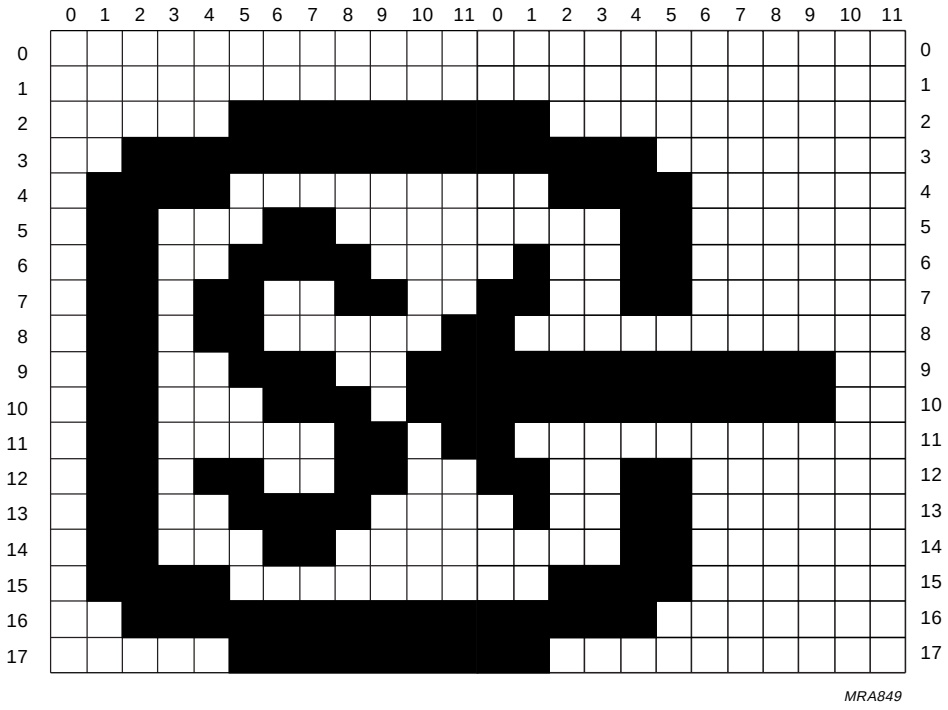


Fig.35 Combination of two character cells in a horizontal direction to create a new font.

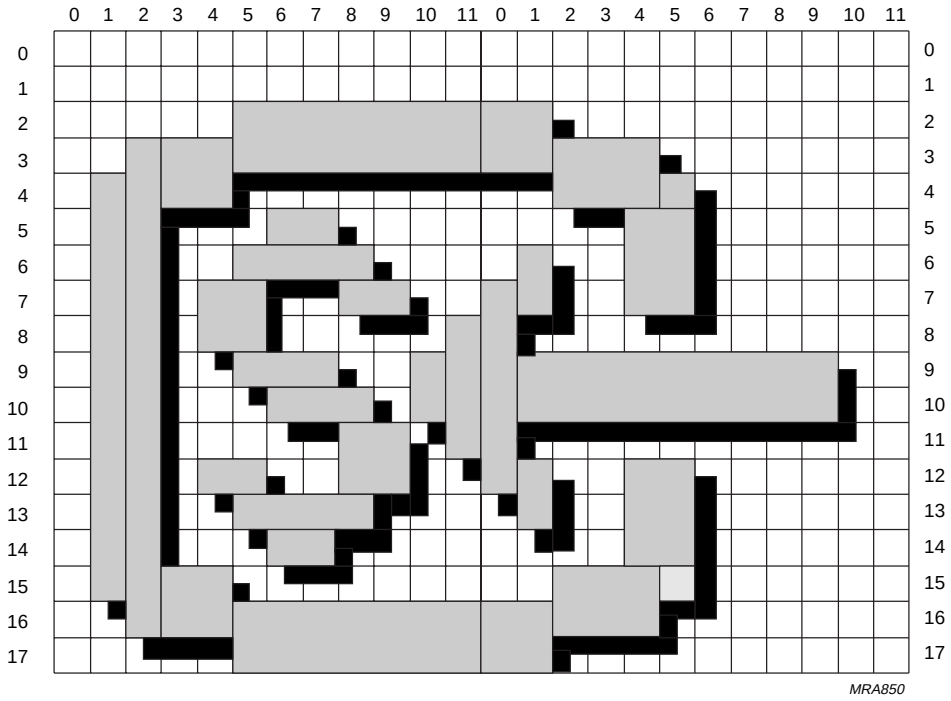


Fig.36 Combination of two character cells in a horizontal direction to create a new font North-West shadowing mode.

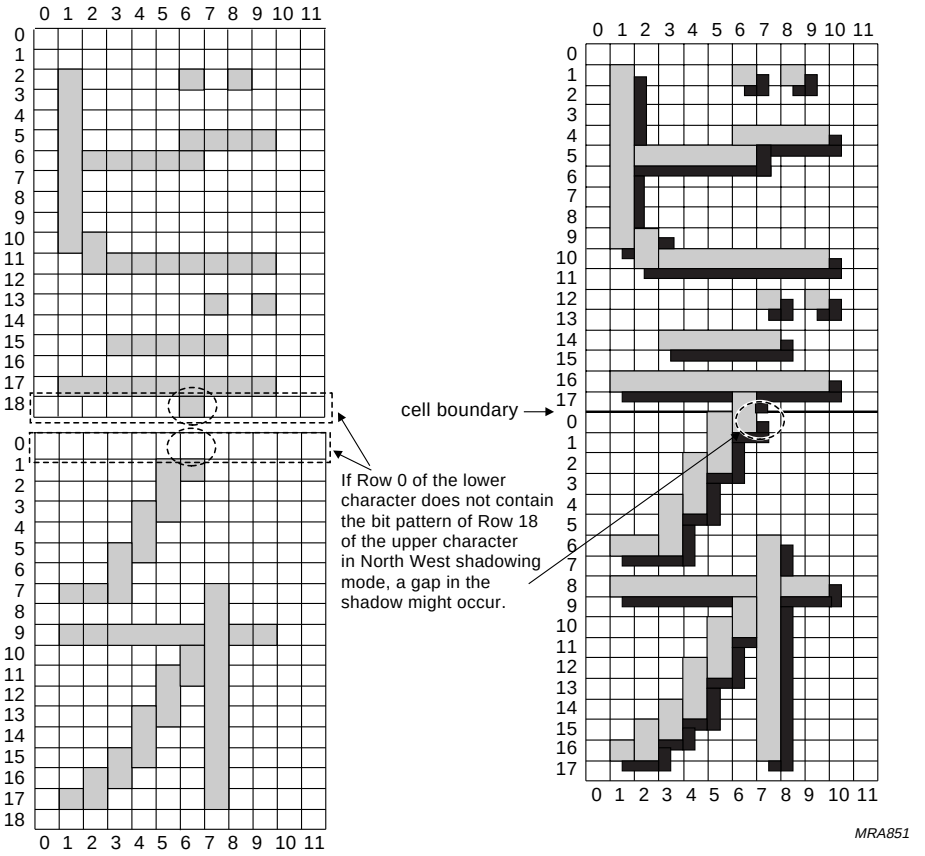


Fig.37 Combination of two characters in a vertical direction - with gap.

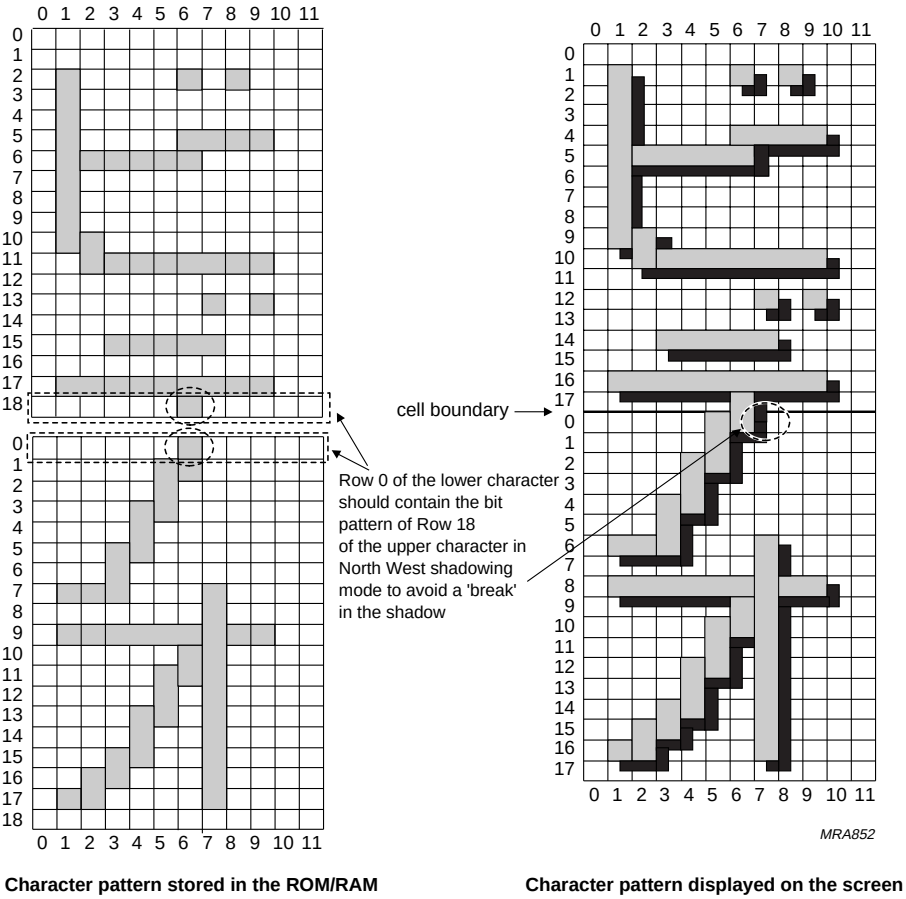


Fig.38 Combination of two characters in a vertical direction - with no gap.

11 OSD CLOCK

The on-chip clock generator comprises Phase-Locked Loop circuitry and is shown in Fig.39. The frequency of the OSD clock is programmable and is determined by the contents of the 6-bit counter, which is loaded using Command 6. The OSD clock frequency is calculated as shown below; frequencies within the range 4 to 14 MHz can be selected.

$$f_{OSD} = f_{HSYNC} \times 16 \times (PLLCN)$$

Where: 16 < (PLLCN) < 40; (PLLCN) is the decimal value held in the 6-bit counter.

The Voltage Controlled Oscillator (VCO) is synchronized to the HIGH-to-LOW edge of f_1 (see Fig.39) which is always on the trailing edge of f_{HSYNC}. The programmable active level detector will pass the HSYNC signal if it is programmed as active HIGH or invert the HSYNC signal if it is programmed as active LOW. The 4-bit prescaler increments or decrements the output of the VCO in steps of $(16 \times f_{HSYNC})$.

The OSD clock is enabled/disabled using Command 7; see Section 9.8. When the OSD clock is disabled, the oscillator remains active, therefore the transient time from the OSD clock start-up to locking into the external H_{SYNC} signal is reduced. As the on-chip oscillator is always active after power-on, when the OSD clock is enabled no large currents flow (as for RC or LC oscillators); therefore radiated noise is dramatically reduced.

Character width is a function of the OSD clock frequency; decreasing f_{OSD} increases the width of the characters. Therefore, for optimum character display quality the choice of the OSD clock frequency is important; this is explained in Chapter 12.

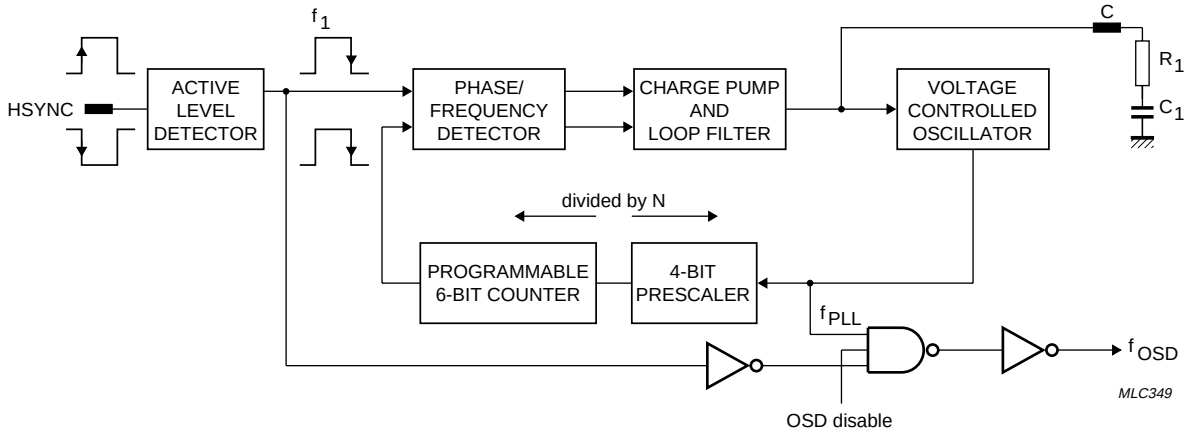


Fig.39 Block diagram of OSD oscillator.

12 OSD CLOCK SELECTION FOR DIFFERENT TV STANDARDS

12.1 OSD frequency

The PCA8514 supports four different TV scanning standards. To obtain the best quality character display, each TV standard requires a different OSD frequency. To cater for this requirement the PCA8514 provides a programmable OSD clock that generates frequencies in the range 4 to 14 MHz. The three examples given below illustrate the OSD clock requirements for different TV scanning standards.

12.1.1 NTSC 525LPF/60 Hz and PAL 625LPF/50 Hz

The OSD clock is applied directly to the OSD circuitry and can take any value within the 4 to 14 MHz frequency range. The NTSC 525LPF/60 Hz standard when used with a 19 inch screen and an OSD clock of 8 MHz, produces a character dot width of 13.2 mm.

12.1.2 NTSC 1050LPF/60 Hz

With this standard, in order to obtain the same character dot width as in the NTSC 525LPF/60 Hz standard that uses an OSD clock of 7 MHz; the OSD clock must be doubled to 14 MHz because the horizontal frequency is doubled.

To keep the same character height as that in the NTSC 525LPF/60 Hz standard, HSYNC is also divided by two, internally.

12.1.3 PAL 1250LPF/100 Hz

With this standard, in order to obtain the same character dot width as in the PAL 625LPF/50 Hz standard; the OSD clock must be doubled.

HSYNC is applied directly to the OSD circuitry without being divided by two as both the horizontal frequency (1250 Hz) and the vertical frequency (100 Hz) are doubled.

12.2 Maximum number of characters per row

The number of characters per row is a function of the OSD clock frequency and the TV standard used.

With reference to Fig.40 the active video signal period of a horizontal line is 53.5 μs. However, in order to reduce jittering at the screen edge, overscan is normally applied by the TV manufacturer and this reduces the visible video signal period to 48.15 μs. The examples given below show how the number of characters per row and the character width may be obtained for the NTSC 525LPF/60 Hz TV standard using different OSD clock frequencies.

12.2.1 NTSC 525LPF/60 Hz; f_{OSD} = 6 MHz

- As f_{OSD} = 6 MHz: t_{OSD} = 0.1666 μs.
- The number of visible dots on one horizontal line is 290 (48.15 μs/0.1666 μs). However, as the starting position of the first character dot is approximately 45 dots after HSYNC, the actual visible number of dots per line is 245.
- Each character is composed of a 12 × 18 dot matrix; therefore the maximum number of characters on one line is 20 (245/12).
- If a 19 inch TV screen is used, the width of a horizontal line is approximately 370 mm and this gives a character width of 18.5 mm.

12.2.2 NTSC 525LPF/60 Hz; f_{OSD} = 10 MHz

- As f_{OSD} = 10 MHz: t_{OSD} = 0.1 μs.
- The number of visible dots on one horizontal line is 481 (48.15 μs/0.1 μs). Allowing for the initial starting position of 45 dots, the actual number of visible dots per line is 436.
- Each character is composed of a 12 × 18 dot matrix; therefore the maximum number of characters on one line is 36.
- With a 19 inch TV screen, the width of a horizontal line is approximately 370 mm and the character width is 10.3 mm.

12.3 Maximum number of rows per frame

The number of rows per frame is a function of the number of active lines per display field and the number of vertical dots in the character matrix (which is 18). The number of rows per frame (N) is calculated as shown below.

$$N = \frac{\text{number of active lines per field}}{18}$$

The four examples shown below illustrate how the maximum number of rows per frame is obtained for each TV scanning standard.

12.3.1 NTSC 525LPF/60 Hz

The number of active lines per field for this standard is between 241.5 and 249H (see Fig.41). If the value of 241 is used then the maximum number of rows per frame is 13.

12.3.2 PAL 625LPF/50 Hz

The number of active lines per field for this standard is 280. Therefore, the maximum number of rows per frame is 15.

12.3.3 NTSC 1050LPF/60 Hz

For this standard the number of active lines per frame is double that of the NTSC 525LPF/60 Hz standard. However, as HSYNC is divided by two internally, the maximum number of rows per frame is also 13.

12.3.4 PAL 1250LPF/100 Hz

With this standard it is not necessary to divide HSYNC by two as both the horizontal and vertical frequency are doubled. The maximum number of rows per frame is 15.

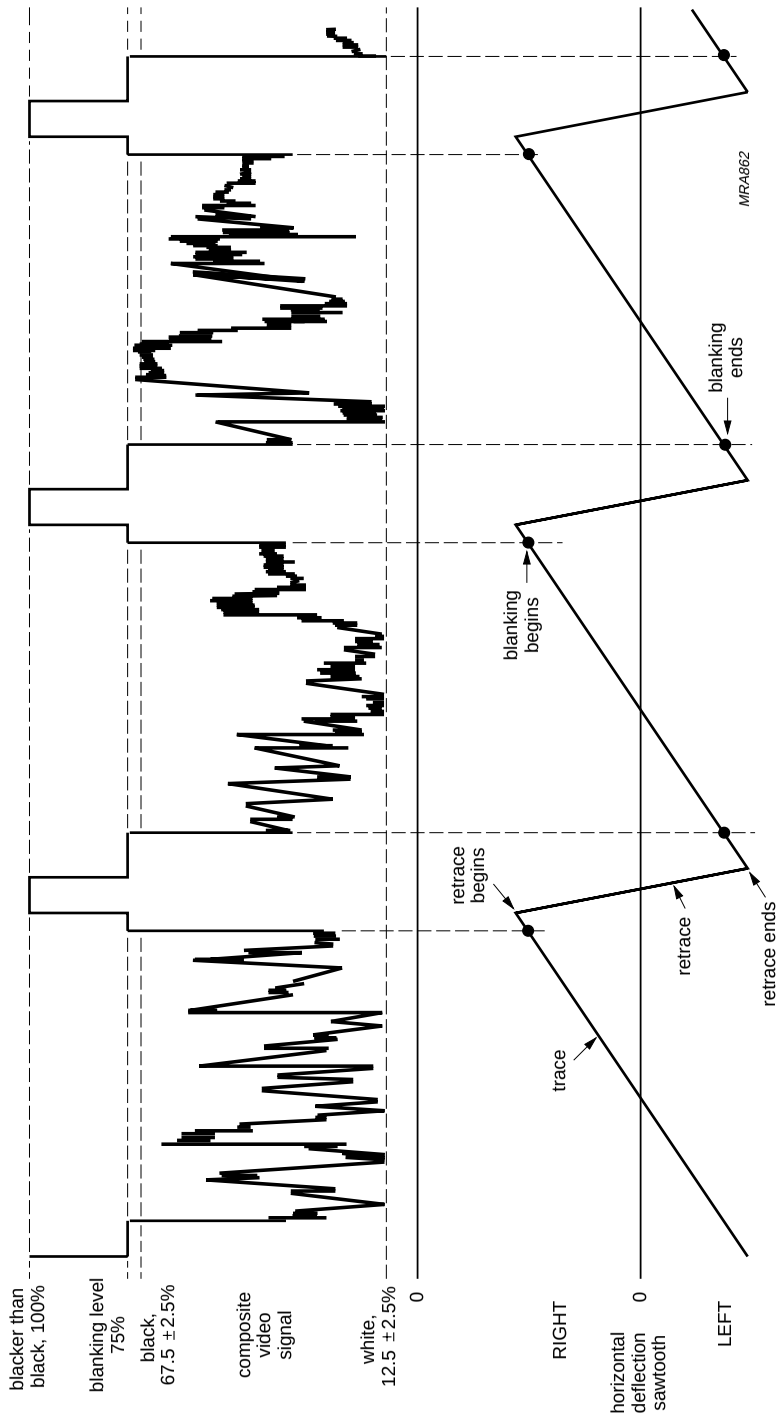


Fig.40 Composite video signal for three horizontal lines compared to three horizontal deflection sawteeth (NTSC 525LPF/60 Hz).

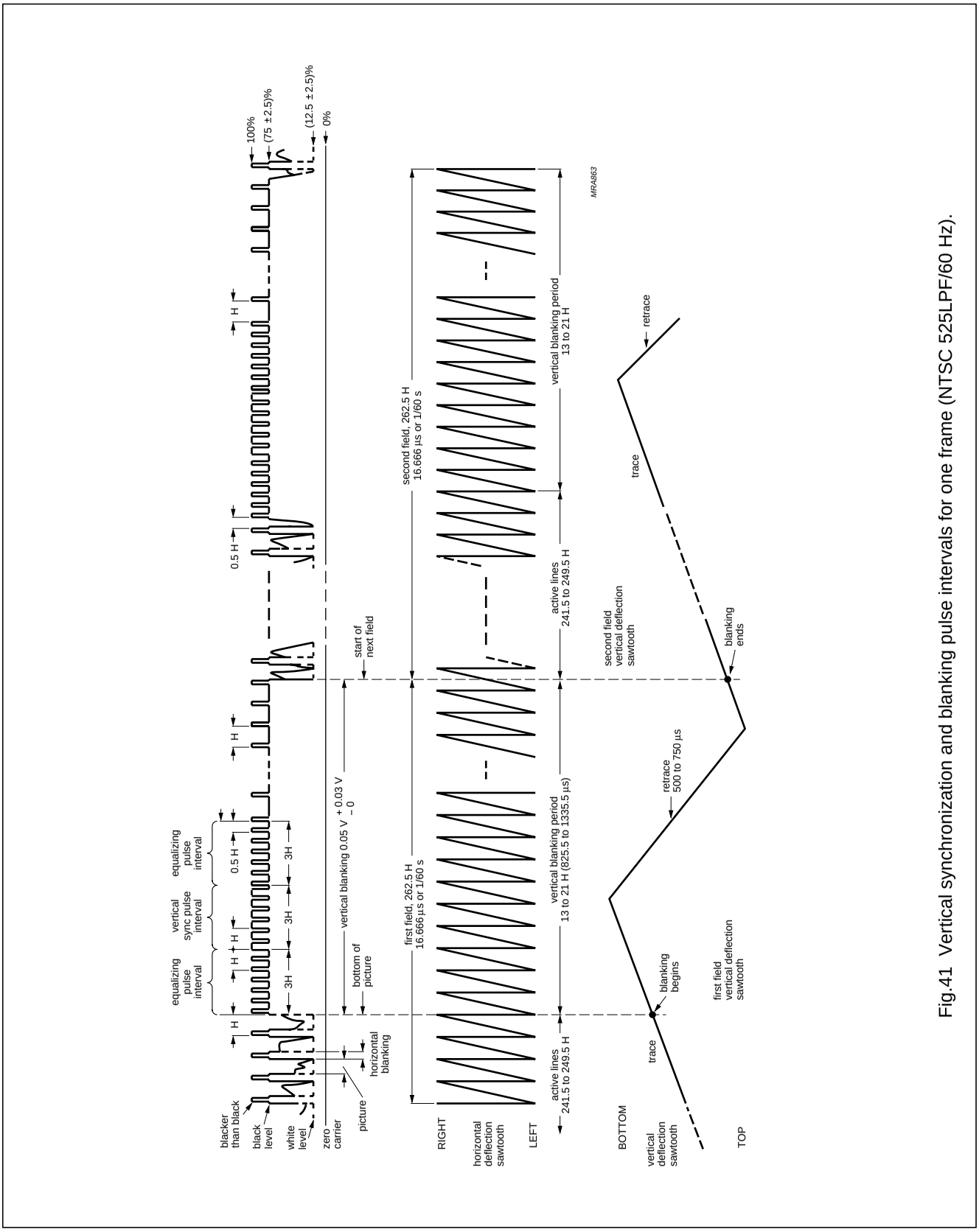


Fig.41 Vertical synchronization and blanking pulse intervals for one frame (NTSC 525LPF/60 Hz).

13 OUTPUT PORTS

The three output ports P00, P01 and P04 can be configured using one of three mask options. The three output mask options are specified below:

Option 1 Standard output with switched pull-up current source. See Figs 42 and 45.

Option 2 Open-drain output. See Figs 43 and 46.

Option 3 Push-pull output. See Figs 44 and 47.

The state of each output port after a Power-on-reset can also be selected using the mask options. All the available mask options for the PCA8514 are given in Section 13.1.

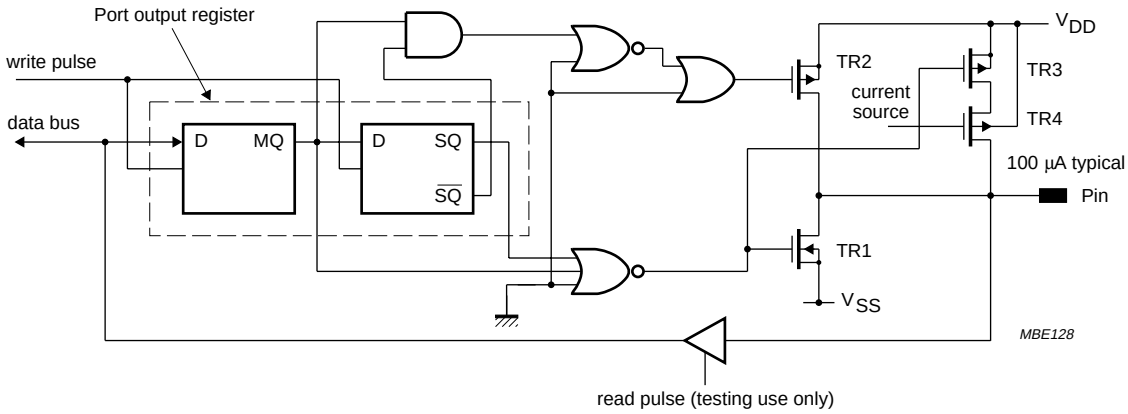


Fig.42 Standard output with switched pull-up current source (Option 1 - P00 and P01).

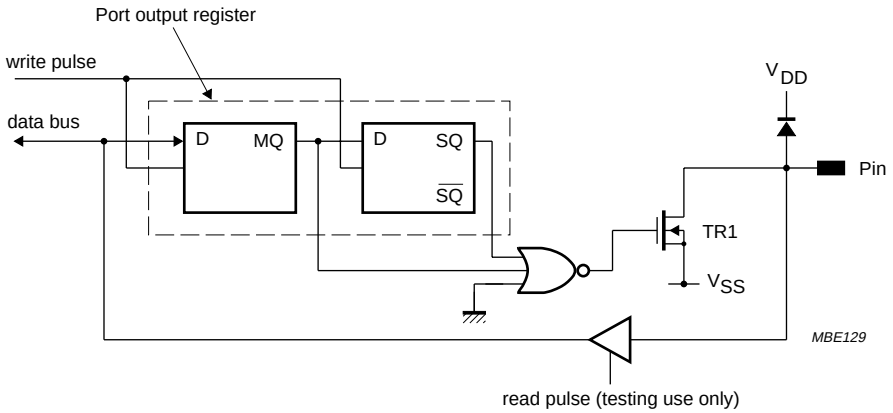


Fig.43 Open-drain output (Option 2 - P00 and P01).

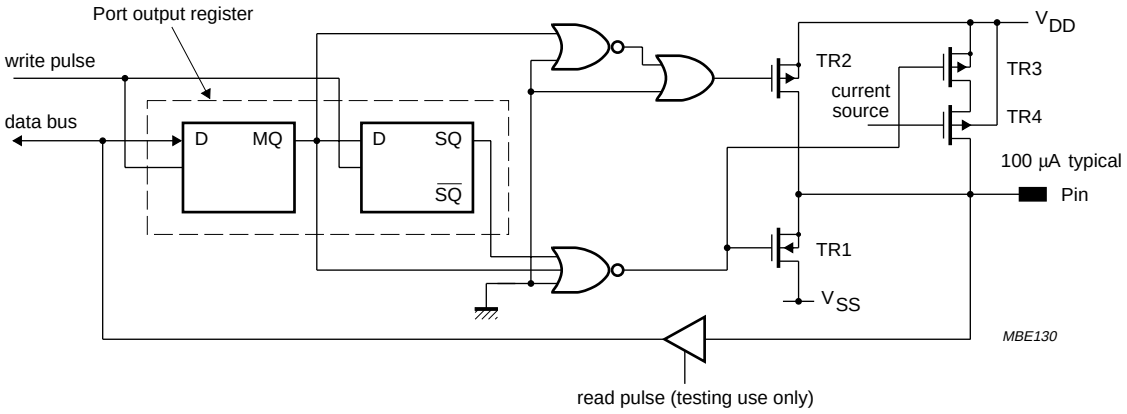


Fig.44 Push-pull output (Option 3 - P00 and P01).

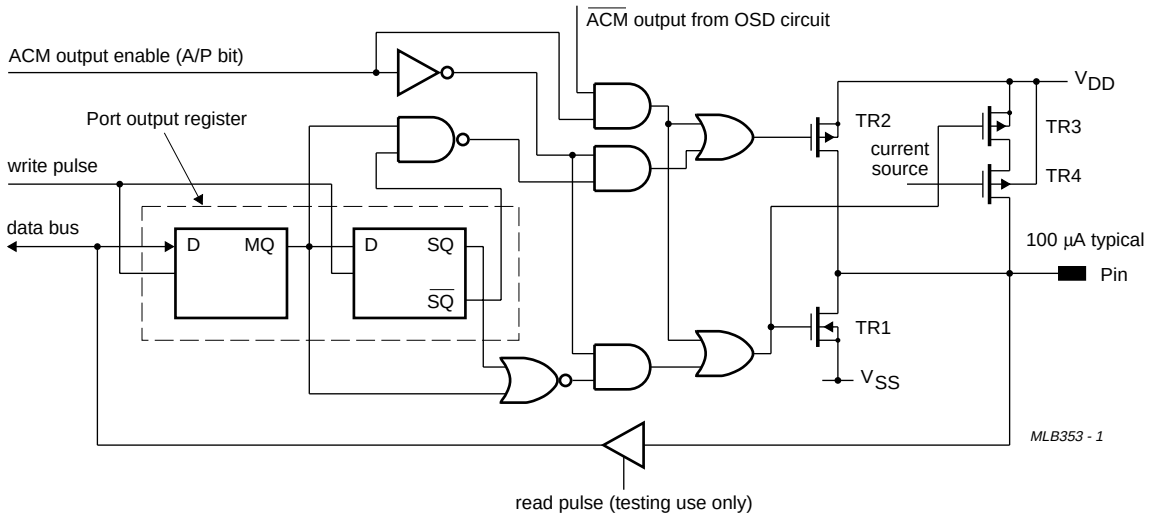


Fig.45 Standard output with switched pull-up current source (Option 1 - P04).

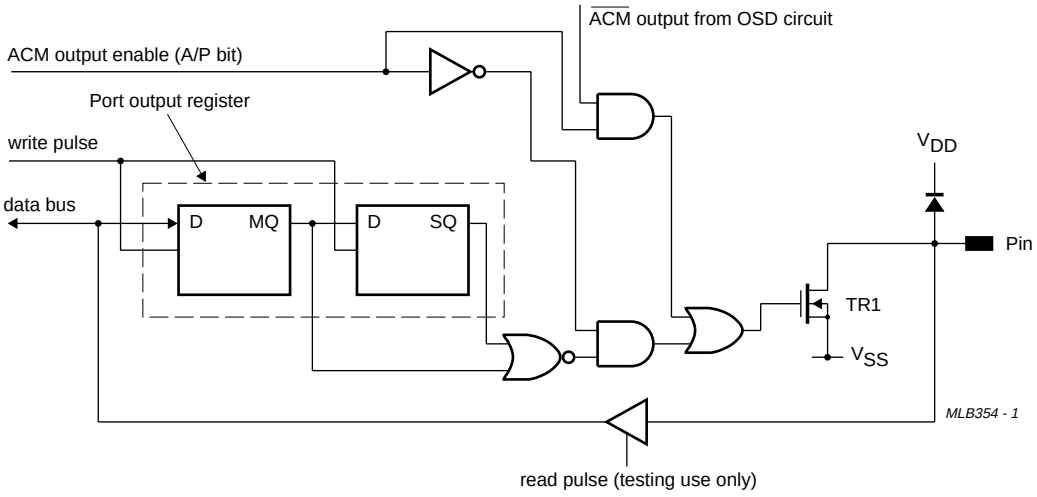


Fig.46 Open-drain output (Option 2 - P04).

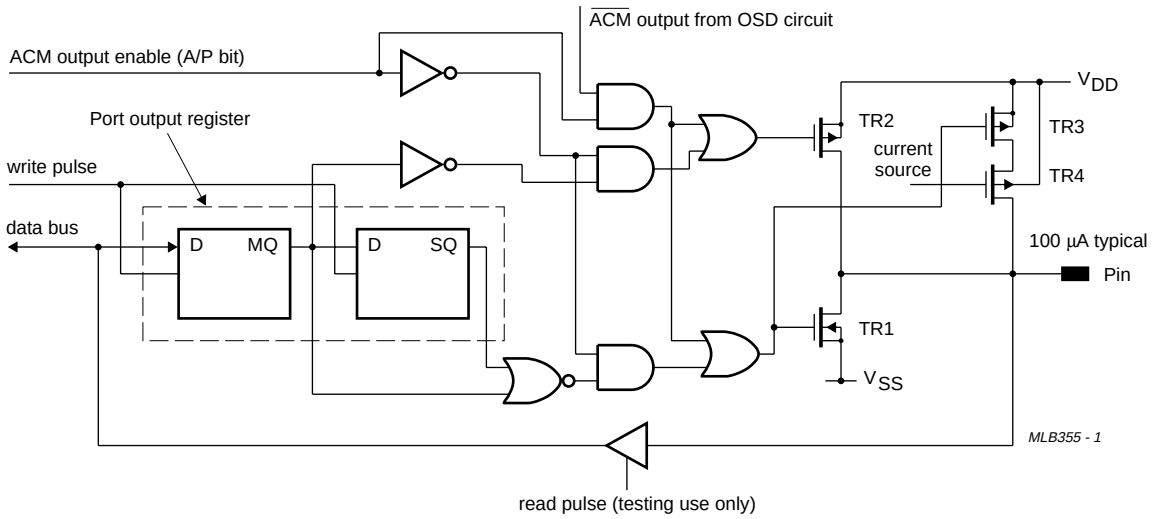


Fig.47 Push-pull output (Option 3 - P04).

13.1 Mask options

Tables 43 to 47 list the available mask options for the PCA8514. Table 46 is intended for customer use when ordering the device.

Table 43 Port configuration options

OPTION	PORT
1, 2 or 3	P00
1, 2 or 3	P01
1, 2 or 3	P04

Table 44 Port state after Power-on-reset

OPTION	PORT
HIGH	P00
HIGH	P01
HIGH or LOW	P04

Table 45 Space Code options

OPTION	SHADOWING MODE
Transparent pattern	Available in Box shadowing mode only; see Fig.33.
Opaque pattern	Available in Box shadowing mode only; see Fig.32.

Table 46 Customer selected mask options

FEATURE	OPTION
Output port configurations	
P00	
P01	
P04	
Port state after Power-on-reset	
P00	
P01	
P04	
Oscillator tranconductance	
LOW	
MEDIUM	
HIGH	
Space Code pattern	
Transparent	
Opaque	

Table 47 System oscillator transconductance options

OPTION	TRANSCONDUCTANCE (mS)	f_{osc} - QUARTZ CRYSTAL (MHz)	f_{osc} - CERAMIC RESONATOR (MHz)
LOW (g_{mL})	0.7	1 to 6	–
MEDIUM (g_{mM})	1.6	4 to 12	1 to 6
HIGH (g_{mH})	4.5	–	3 to 16

14 DEFAULT VALUES AFTER POWER-ON-RESET

The default values of registers after a Power-on-reset are specified in Table 48. All other settings must be initialized by the user after a Power-on-reset.

Table 48 Default values

REGISTER	BIT	STATE AFTER RESET	DESCRIPTION
User directly controllable registers			
Control Register 1	M1	0	Scanning mode selection bits. Conventional NTSC 525LPF/60 Hz and/or PAL 625LPF/50 Hz selected.
	M0	0	
	Bp	1	Polarity control bit; the output polarities of FB, ACM, R, G, B and I are active HIGH.
	EN	0	OSD enable/disable control bit; the OSD is disabled.
Control Register 2	Hp	0	HSYNC input polarity control bit; the input polarity is active LOW.
	Vp	0	VSYNC input polarity control bit; the input polarity is active LOW.
	S1	0	Display mode selection bits; the North-West shadowing mode is selected.
	S0	1	
Control Register 3	BF1	0	Blinking frequency control bits. The blinking frequency is set to f_{VSYNC}/16 Hz.
	BF0	0	
	BR1	0	Active ratio of blinking frequency control bits. The active ratio is set to 3 : 1.
	BR0	0	
Control Register 4	A/P	0	Port control bit. Pin 2 (P04/ACM/VOB2) is selected as an output port pin.
Control Register 5	R	0	Background colour selection bits in Frame shadowing mode; the default colour is Blue.
	G	0	
	B	1	
	I	0	
–	BS1	0	Command Bank selection bits. Command Bank 00 is selected.
	BS0	0	
User indirectly controllable registers			
ACM	ACM	0	The ACM output is LOW unless changed by the Space Code.
Background colour	B	1	The Background colour selected is Blue unless changed by the Space Code.
	R	0	
	G	0	
	I	0	
Character size	T4	0	The default character size is 1V/1H. A different value can be selected by using the Carriage Return Code.
	T3	0	
End of display	T0	0	Will continue to display next character (if the OSD clock is enabled).

15 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	–0.5	+7.0	V
V_I	all input voltages	–0.5	V_{DD} + 0.5	V
I_{OH}	maximum source current for all port lines	–	–5.0	mA
I_{OL}	maximum sink current for all port lines	–	5.0	mA
P_{tot}	total power dissipation	–	500	mW
T_{stg}	storage temperature	–55	+125	°C
T_{amb}	operating ambient temperature	–20	+70	°C

16 DC CHARACTERISTICS

V_{DD} = 5 V ±10%; V_{SS} = 0 V; T_{amb} = –20 to +70 °C. All voltages with respect to V_{SS} unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	operating supply voltage		4.5	5.0	5.5	V
I_{DD}	operating supply current	V_{DD} = 5 V; f_{xtal} = 3 MHz; f_{OSD} = 10 MHz	–	5	10	mA
		V_{DD} = 5 V; f_{xtal} = 3 MHz; f_{OSD} = Stop	–	7	14	mA
		V_{DD} = 5 V; f_{xtal} = 3 MHz; f_{OSD} = Stop	–	1	2	mA
$\overline{\text{RESET}}$, TEST1, TEST2, HSYNC, VSYNC, E and $\overline{\text{HIO}}$/ I²C inputs						
V_{IL}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
I_{LI}	input leakage current	$V_{SS} < V_I < V_{DD}$	±0.01	±0.20	±10	µA
Ports P00 to P03 (with combined functions) inputs						
V_{IL}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
I_{LI}	input leakage current	$V_{SS} < V_I < V_{DD}$	–	–	±10	µA
Ports P00 to P03 (with combined functions) outputs						
I_{OL}	LOW level output sink current	V_{DD} = 5 V; V_O = 0.4 V	5.0	12.0	–	mA
I_{OH1}	HIGH level pull-up output source current	V_{DD} = 5 V; $V_O = 0.7V_{DD}$	–40	–100	–	µA
		V_{DD} = 5 V; $V_O = V_{SS}$	–	–140	–400	µA
I_{OH2}	HIGH level push-pull output source current	V_{DD} = 5 V; $V_O = V_{DD}$ – 0.4 V	–3.0	–7.0	–	mA
SDA/SIN and SCK/SCLK inputs						
V_{IL}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
SDA/SIN and SCK/SCLK outputs						
I_{OL}	LOW level open-drain sink current	V_{DD} = 5 V; V_O = 0.4 V	3.0	–	–	mA
R, G, B, I, FB and P04/ACM outputs						
I_{OL}	LOW level push-pull output sink current	V_{DD} = 5 V; V_O = 0.4 V	3.2	5.5	–	mA
I_{OH1}	HIGH level pull-up output source current	V_{DD} = 5 V; $V_O = 0.7V_{DD}$	–40	–100	–	µA
		V_{DD} = 5 V; $V_O = V_{SS}$	–	–140	–400	µA
I_{OH2}	HIGH level push-pull output source current	V_{DD} = 5 V; $V_O = V_{DD}$ – 0.4 V	–1.6	–2.4	–	mA

17 AC CHARACTERISTICS

V_{DD} = 5 V ±10%, V_{SS}= 0 V.

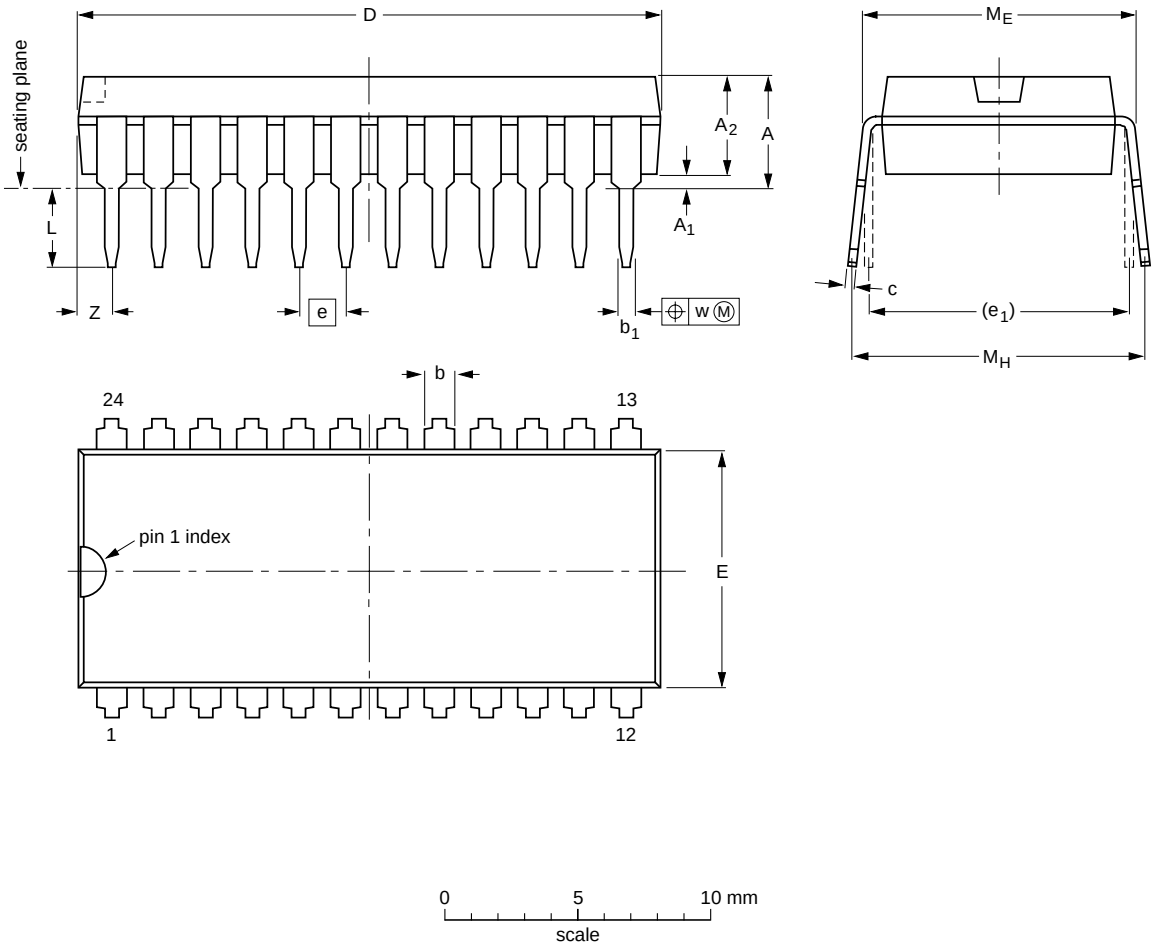
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f_{xtal}	crystal oscillator frequency	note 1	0.5	3.0	6.0	MHz
f_{OSD}	OSD oscillator frequency	1V/1H scanning mode	4.0	7.0	10.0	MHz
		1V/2H and 2V/2H scanning modes	4.0	12.0	14.0	MHz
C_{OSD}	external capacitance at pin C		0.4	–	4.0	µF
R_{OSD}	external resistance at pin C		5.0	–	15.0	kΩ

Note

1. The minimum frequency should be 3 times greater than the maximum I^2C-bus frequency or the HIO frequency used in the system.

18 PACKAGE OUTLINES

SDIP24: plastic shrink dual in-line package; 24 leads (400 mil) **SOT234-1**



DIMENSIONS (mm are the original dimensions)

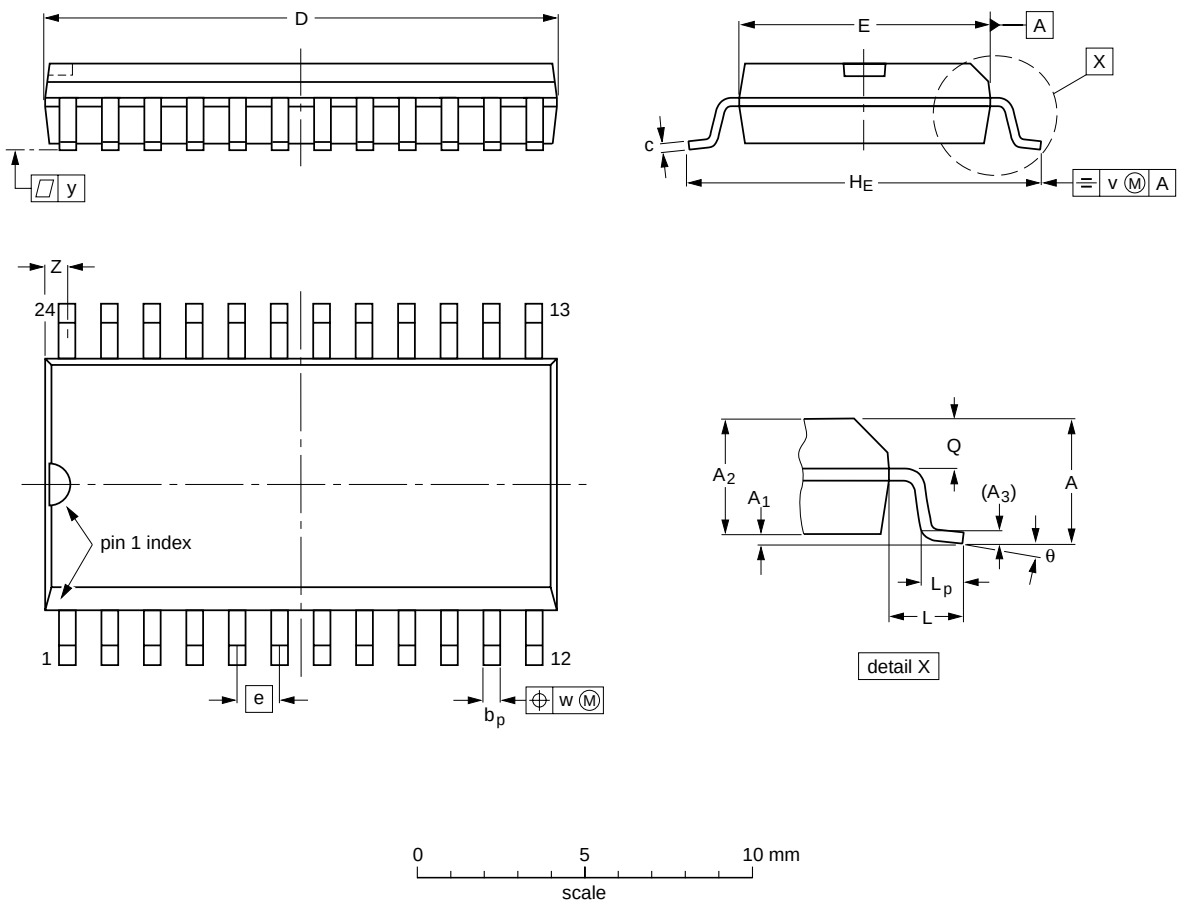
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.8	1.3 0.8	0.53 0.40	0.32 0.23	22.3 21.4	9.1 8.7	1.778	10.16	3.2 2.8	10.7 10.2	12.2 10.5	0.18	1.6

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT234-1						~~92-11-17~~ 95-02-04

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				~~95-01-24~~ 97-05-22

19 SOLDERING

19.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

19.2 DIP

19.2.1 Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

19.2.2 Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

19.3 SO

19.3.1 Reflow soldering

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

19.3.2 Wave soldering

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

19.3.3 Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

20 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

21 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

22 PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

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