PRELIMINARY
CUSTOMER PROCUREMENT SPECIFICATION

Z86C60/65

CMOS Z8® 32K ROM MICROCONTROLLER

FEATURES

Part	ROM (KB)	RAM* (Bytes)	I/O	Speed (MHz)	28-pin DIP
Z86C60	16	256	22	16	X
Z86C65	32	256	22	16	X

*General-Purpose

- 28-Pin DIP Package
- 3.0V to 5.5V Operating Range
- Low-Power Consumption: 200 mW
- Fast Instruction Pointer: 0.75 µs @ 16 MHz
- Two Standby Modes: STOP and HALT
- Low EMI Mode Option
- Auto Latches
- Two Programmable 8-Bit Counter/Timers Each with 6-Bit Programmable Prescaler
- Three Vectored, Priority Interrupts from Three Different Sources
- On-Chip Oscillator that Accepts a Crystal Ceramic Resonator, LC, or External Clock Source
- ROM Mask Options:
  – ROM Protect
  – RAM Protect

GENERAL DESCRIPTION

The Z86C60/65 microcontrollers introduce a new level of sophistication to single-chip architecture. The Z86C65 is a member of the Z8 single-chip microcontroller family with 32 Kbytes of ROM and 256 bytes of RAM. The Z86C60 is identical, except that it only has 16 Kbytes of ROM.

The Z86C60/65 are housed in a 28-pin DIP package, and manufactured in CMOS technology. The Z86C96 ROMless Z8 will support the Z86C60/65.

Zilog's CMOS microcontroller offers fast execution, more efficient use of memory, more sophisticated interrupts, input/output bit manipulation capabilities, and easy hardware/software system expansion along with low cost and low power consumption.

The Z86C60/65 architecture is characterized by Zilog's 8-bit microcontroller core. The device offers a flexible I/O scheme, an efficient register and address space structure, multiplexed capabilities between address/data, I/O, and a number of ancillary features that are useful in many industrial and advanced scientific applications.

For applications which demand powerful I/O capabilities, the Z86C60/65 fulfills this with 22 pins dedicated to input and output. These lines are grouped into four ports. Each port is configurable under software control to provide timing, status signals, serial or parallel I/O with or without handshake, and an address/data bus for interfacing external memory.

There are three basic address spaces available to support this wide range of configurations: Program Memory, Data Memory, and 236 General-Purpose Registers.

To unburden the program from coping with the real-time problems such as counting/timing and serial data communication, the Z86C60/65 offers two on-chip counter/timers with a large number of user selectable modes.

Notes:
All Signals with a preceding front slash, "/", are active Low, e.g., B//W (WORD is active Low); /B/W (BYTE is active Low, only).

Power connections follow conventional descriptions below:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

GENERAL DESCRIPTION

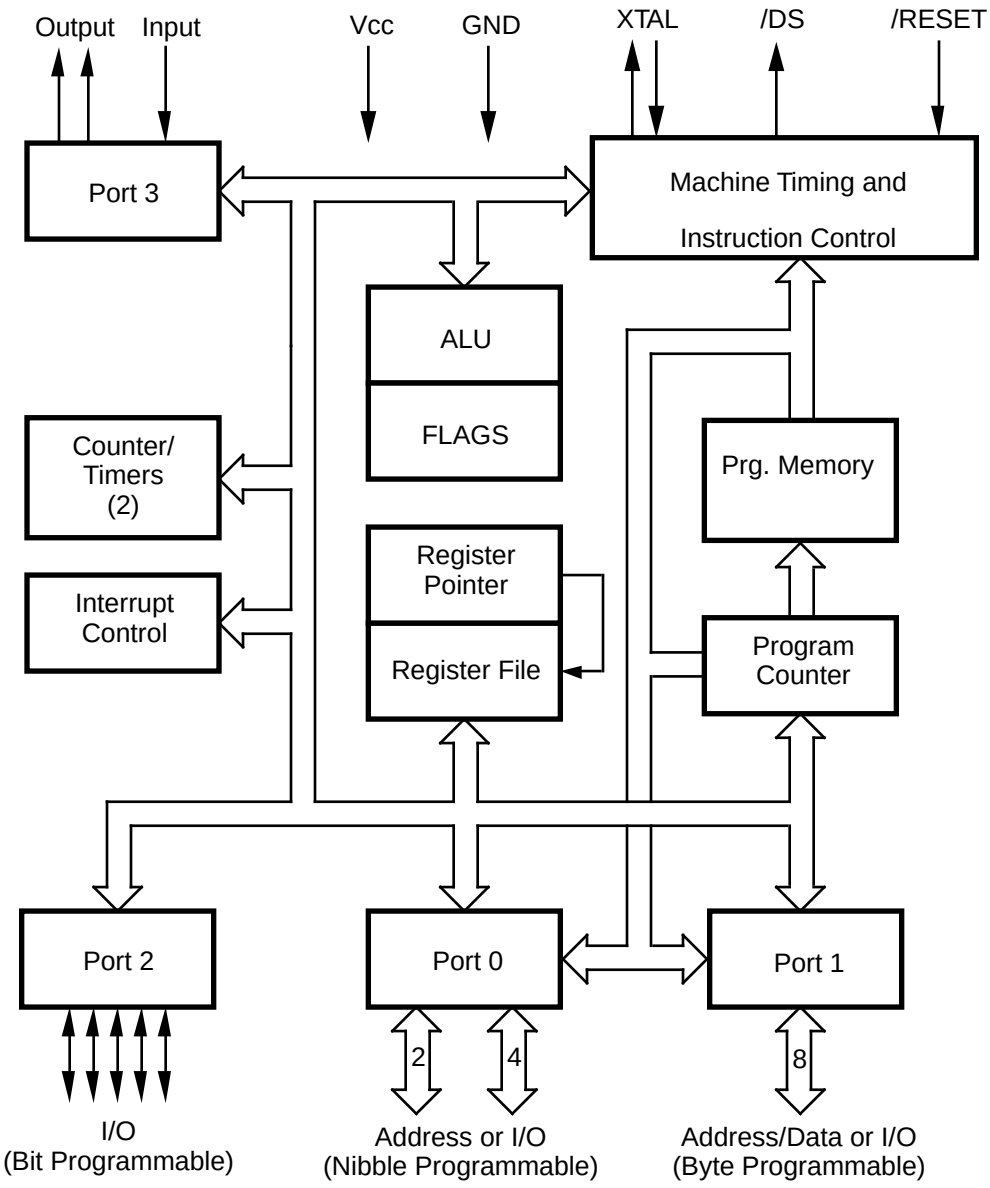


Figure 1. Z86C60/65 Functional Block Diagram

PIN DESCRIPTION

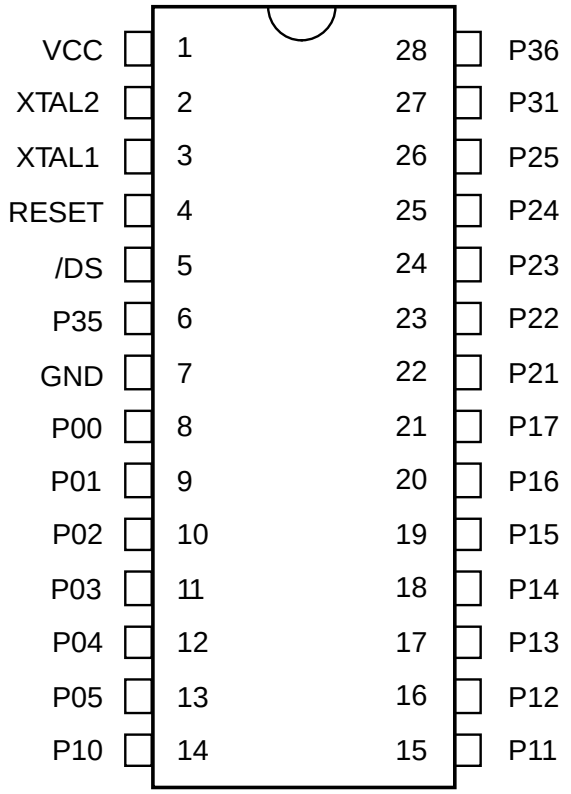


Figure 2. Z86C60/65 28-Pin DIP Pin Assignments

Z86C60/65 28-Pin DIP Pin Identification

Pin #	Symbol	Function	Direction
1	V_{CC}	Power Supply	Input
2	XTAL2	Crystal, Oscillator Clock	Output
3	XTAL1	Crystal, Oscillator Clock	Input
4	/RESET	Reset	Input
5	/DS	Data Strobe	Output
6	P35	Port 3, Pin 5	Output
7	GND	Ground	Input
8-13	P05-P00	Port 0, Pins 0,1,2,3,4,5	In/Output
14-21	P17-P10	Port 1, Pins 0,1,2,3,4,5,6,7	In/Output
22-26	P25-P21	Port 2, Pins 1,2,3,4,5	In/Output
27	P31	Port 3, Pin 1	Input
28	P36	Port 3, Pin 6	Output

ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Min	Max	Units
V_{CC}	Supply Voltage*	–0.3	+7.0	V
T_{STG}	Storage Temp	–65	+150	C
T_A	Oper Ambient Temp	†	†	

Notes:
* Voltages on all pins with respect to GND.
† See ordering information

Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period may affect device reliability.

STANDARD TEST CONDITIONS

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (Test Load).

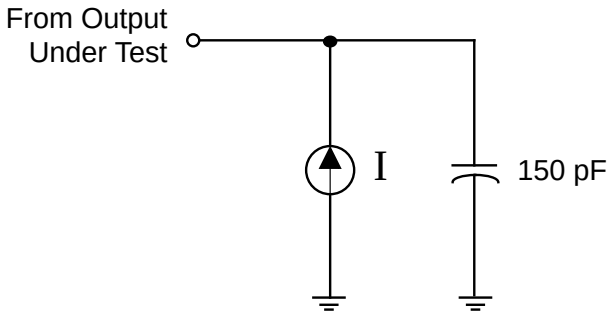


Figure 3. Test Load Diagram

DC ELECTRICAL CHARACTERISTICS

Z86C60/65

Sym	Parameter	T_A = 0°C to +70°C Min	Max	Typical at 25°C	Units	Conditions
V_{CC}	Operating Voltage	4.5	5.5		V	[3]
	Max Input Voltage		7		V	[3] I_{IN} < 250 µA
V_{CH}	Clock Input High Voltage	0.85V_{CC}	V_{CC}+0.3		V	Driven by External Clock Generator
V_{CL}	Clock Input Low Voltage	V_{SS}–0.3	0.8		V	Driven by External Clock Generator
V_{IH}	Input High Voltage	2	V_{CC}+0.3		V	
V_{IL}	Input Low Voltage	V_{SS}–0.3	0.2V_{CC}		V	
V_{OH}	Output High Voltage	2.4	V_{CC}		V	I_{OH} = –2.0 mA
V_{OH}	Output High Voltage		V_{CC}–100 mV		V	I_{OH} = –100 µA
V_{OH}	Output High Voltage (Low EMI)	2.4			V	I_{OH} = –0.5 mA
V_{OL}	Output Low Voltage		0.4		V	I_{OL} = +5.0 mA [2]
V_{OL}	Output Low Voltage (Low EMI)		0.4		V	I_{OL} = +2.0 mA [2]
V_{RH}	Reset Input High Voltage	0.85V_{CC}	V_{CC}+0.3		V	
V_{RI}	Reset Input Low Voltage	–0.3	0.2V_{CC}		V	
I_{IL}	Input Leakage	–2	2		µA	V_{IN} = 0V, V_{CC}
I_{OL}	Output Leakage	–2	2		µA	V_{IN} = 0V, V_{CC}
I_{IR}	Reset Input Current		–180		µA	V_{RL} = 0V
I_{CC}	Supply Current (Standard Mode)		35	24	mA	[1] @16 MHz
I_{CC}	Supply Current (Low EMI)		6.0	4.0	mA	@4 MHz
I_{CC1}	Standby Current (Standard Mode)		15	4.5	mA	[1] HALT Mode V_{IN} = 0V, V_{CC} @16 MHz
I_{CC1}	Standby Current (Low EMI)		1.6	0.8	mA	@4 MHz
I_{CC2}	Standby Current		10	5	µA	[1] STOP Mode V_{IN} = 0V, V_{CC}
I_{ALL}	Auto Latch Low Current	–14	+14	5	µA	V_{CC} = 5.0V

Notes:

[1] All inputs driven to either 0V or V_{CC}, outputs floating.

[2] V_{CC} = 4.5V to 5.5V

[3] /Reset pin must be a maximum of V_{CC} + 0.3V.

AC CHARACTERISTICS

Additional Timing Diagram

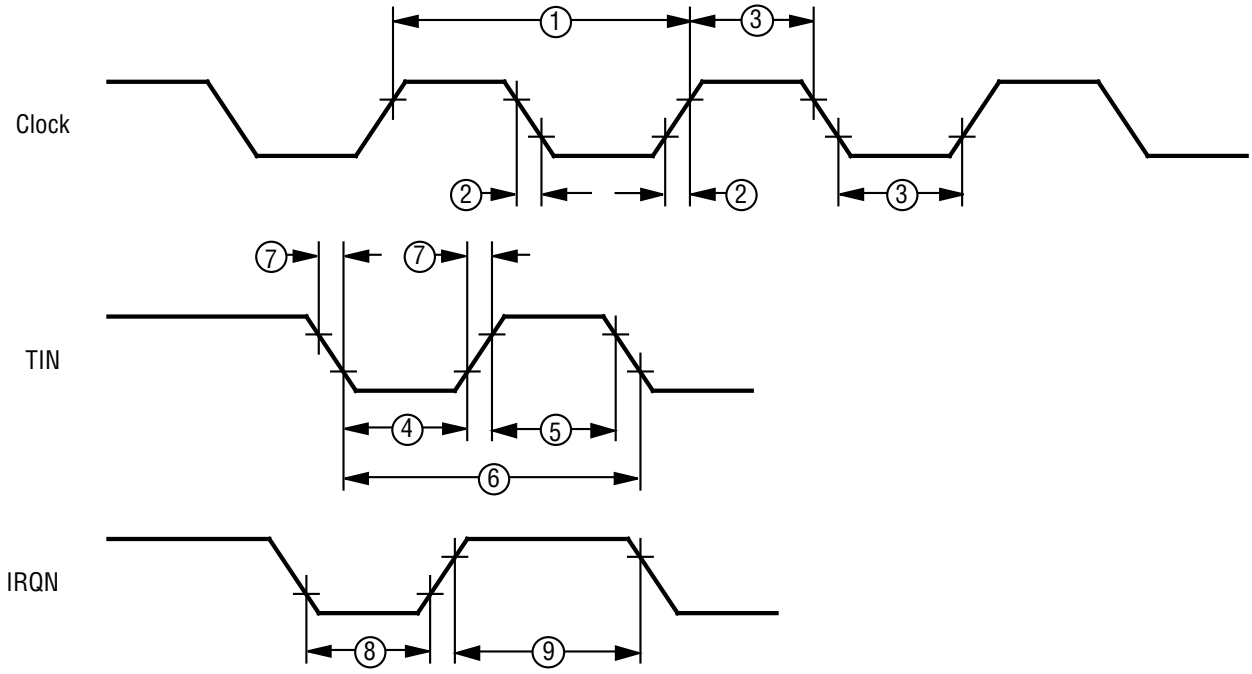


Figure 4. Additional Timing

AC CHARACTERISTICS

Additional Timing Table
Z86C60/65 (Standard Mode Only)

No	Symbol	Parameter	T_A = 0°C to +70°C 16 MHz Min	Max	Units	Notes
1	TpC	Input Clock Period	62.5	DC	ns	[1]
2	TrC,TfC	Clock Input Rise & Fall Times		10	ns	[1]
3	TwC	Input Clock Width	31		ns	[1]
4	TwTinL	Timer Input Low Width	75		ns	[2]
5	TwTinH	Timer Input High Width	5 TpC		ns	[2]
6	TpTin	Timer Input Period	8 TpC		ns	[2]
7	TrTin,TfTin	Timer Input Rise and Fall Times	100		ns	[2]
8 a	TwIL	Interrupt Request Input Low Times	70		ns	[2,4]
8 b	TwIL	Interrupt Request Input Low Times	5 TpC		ns	[2,5]
9	TwIH	Interrupt Request Input High Times	5 TpC		ns	[2,3]

Notes:

[1] Clock timing references use $0.85V_{CC}$ for a logic 1 and 0.8V for a logic 0.
[2] Timing references use 2.0V for a logic 1 and 0.8V for a logic 0.
[3] Interrupt references request through Port 3.
[4] Interrupt request through Port 3 (P33-P31).
[5] Interrupt request through Port 30.

Pre-Characterization Product:

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Zilog, Inc. 210 East Hacienda Ave.
Campbell, CA 95008-6600
Telephone (408) 370-8000
FAX 408 370-8056
Internet: http://www.zilog.com