TC7129

4-1/2 Digit Analog-to-Digital Converters with On-Chip LCD Drivers

Features:

- Count Resolution: ±19,999
- Resolution on 200 mV Scale: 10 µV
- True Differential Input and Reference
- Low Power Consumption: 500 µA at 9V
- Direct LCD Driver for 4-1/2 Digits, Decimal Points, Low Battery Indicator, and Continuity Indicator
- Overrange and Underrange Outputs
- Range Select Input: 10:1
- High Common Mode Rejection Ratio: 110 dB
- External Phase Compensation Not Required

Applications:

- Full-Featured Multimeters
- Digital Measurement Devices

Device Selection Table

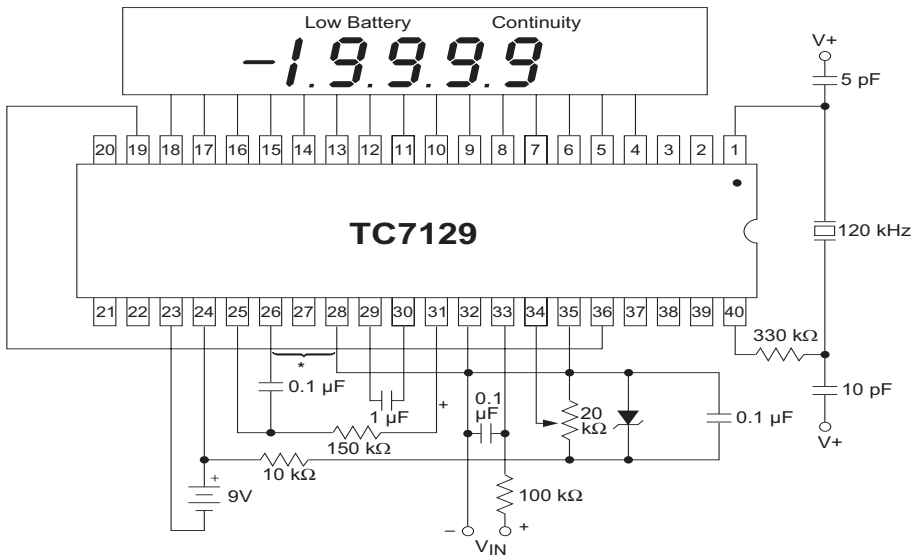
Package Code	Pin Layout	Package	Temperature Range
TC7129CPL	Normal	40-Pin PDIP	0°C to +70°C
TC7129CKW	Formed	44-Pin PQFP	0°C to +70°C
TC7129CLW	–	44-Pin PLCC	0°C to +70°C

General Description:

The TC7129 is a 4-1/2 digit Analog-to-Digital Converter (ADC) that directly drives a multiplexed Liquid Crystal Display (LCD). Fabricated in high-performance, low-power CMOS, the TC7129 ADC is designed specifically for high-resolution, battery-powered digital multimeter applications. The traditional dual-slope method of A/D conversion has been enhanced with a successive integration technique to produce readings accurate to better than 0.005% of full-scale and resolution down to 10 µV per count.

The TC7129 includes features important to multimeter applications. It detects and indicates low battery condition. A continuity output drives an annunciator on the display and can be used with an external driver to sound an audible alarm. Overrange and underrange outputs, along with a range-change input, provide the ability to create auto-ranging instruments. For snapshot readings, the TC7129 includes a latch-and-hold input to freeze the present reading. This combination of features makes the TC7129 the ideal choice for full-featured multimeter and digital measurement applications.

Typical Application

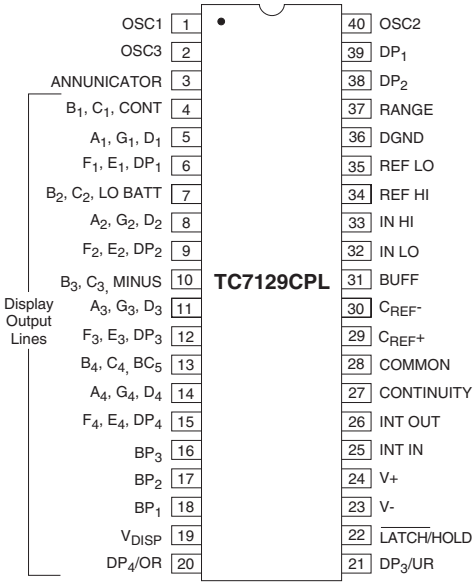


***Note:** RC network between pins 26 and 28 is not required.

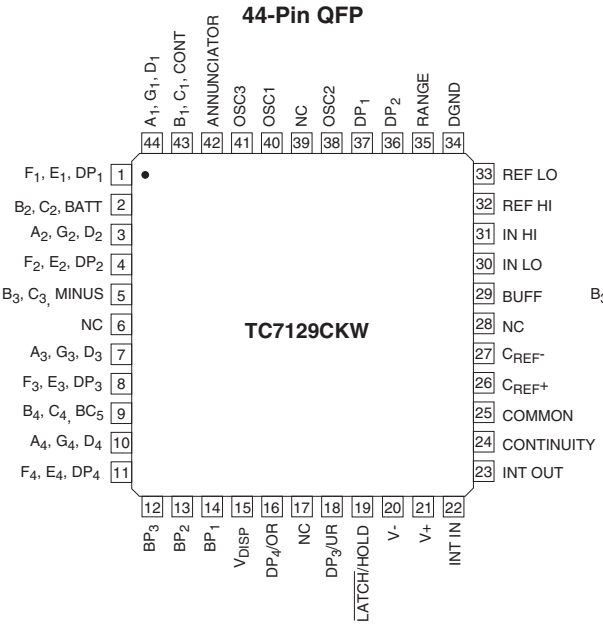
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Package Types

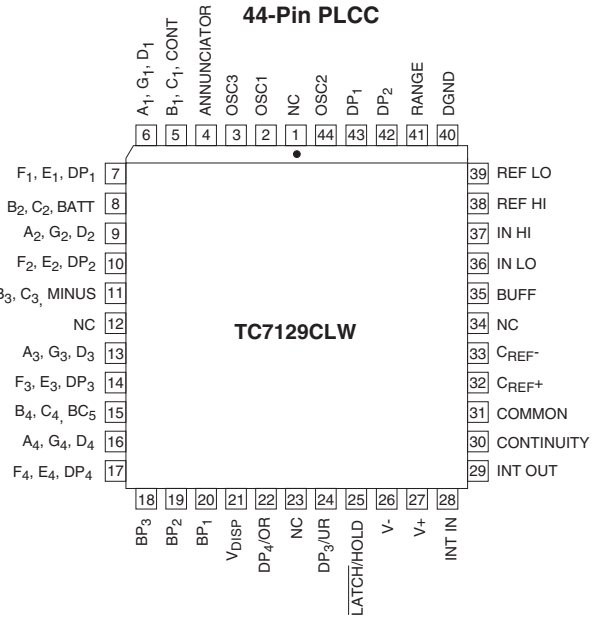
40-Pin PDIP



44-Pin QFP



44-Pin PLCC



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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings*

Supply Voltage (V+ to V-) 15V
Reference Voltage (REF HI or REF LO) ..... V+ to V–
Input Voltage (IN HI or IN LO) **(Note 1)**..... V+ to V–
V_{DISP} ..... V+ to (DGND – 0.3V)
Digital Input (Pins 1, 2, 19, 20,
21, 22, 27, 37, 39, 40)..... DGND to V+
Analog Input (Pins 25, 29, 30) ..... V+ to V–
Package Power Dissipation ($T_A \leq 70°C$)
Plastic DIP 1.23W
PLCC 1.23W
Plastic QFP 1.00W
Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range..... -65°C to +150°C

*Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

TC7129 ELECTRICAL SPECIFICATIONS

Electrical Characteristics: V+ to V– = 9V, V_{REF} = 1V, T_A = +25°C, f_{CLK} = 120 kHz, unless otherwise indicated. Pin numbers refer to 40-pin DIP.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Input						
	Zero Input Reading	–0000	0000	+0000	Counts	V_{IN} = 0V, 200 mV scale
	Zero Reading Drift	—	±0.5	—	µV/°C	V_{IN} = 0V, 0°C < T_A < +70°C
	Ratiometric Reading	9996	—	10000	Counts	V_{IN} = V_{REF} = 1000 mV, Range = 2V
	Range Change Accuracy	0.9999	1.0000	1.0001	Ratio	V_{IN} = 1V on High Range, V_{IN} = 0.1V on Low Range
RE	Rollover Error	—	1	2	Counts	V_{IN}– = V_{IN}+ = 199 mV
NL	Linearity Error	—	1	—	Counts	200mV Scale
CMRR	Common Mode Rejection Ratio	—	110	—	dB	V_{CM} = 1V, V_{IN} = 0V, 200 mV scale
CMVR	Common Mode Voltage Range	—	(V-) + 1.5	—	V	V_{IN} = 0V
		—	(V+) – 1	—	V	200 mV scale
e_N	Noise (Peak-to-Peak Value not Exceeded 95% of Time)	—	14	—	μV_{P-P}	V_{IN} = 0V 200 mV scale
I_{IN}	Input Leakage Current	—	1	10	pA	V_{IN} = 0V, pins 32, 33
	Scale Factor Temperature Coefficient	—	2	7	ppm/°C	V_{IN} = 199 mV, 0°C < T_A < +70°C External V_{REF} = 0 ppm/°C

Note 1: Input voltages may exceed supply voltages, provided input current is limited to ±400 µA. Currents above this value may result in invalid display readings, but will not destroy the device if limited to ±1 mA. Dissipation ratings assume device is mounted with all leads soldered to printed circuit board.

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TC7129 ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: V+ to V– = 9V, V_{REF} = 1V, T_A = +25°C, f_{CLK} = 120 kHz, unless otherwise indicated. Pin numbers refer to 40-pin DIP.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Power						
V_{COM}	Common Voltage	2.8	3.2	3.5	V	V+ to pin 28
	Common Sink Current	—	0.6	—	mA	ΔCommon = +0.1V
	Common Source Current	—	10	—	µA	ΔCommon = -0.1V
DGND	Digital Ground Voltage	4.5	5.3	5.8	V	V+ to pin 36, V+ to V– = 9V
	Sink Current	—	1.2	—	mA	ΔDGND = +0.5V
	Supply Voltage Range	6	9	12	V	V+ to V–
I_S	Supply Current Excluding Common Current	—	0.8	1.3	mA	V+ to V– = 9V
f_{CLK}	Clock Frequency	—	120	360	kHz	
	V_{DISP} Resistance	—	50	—	kΩ	V_{DISP} to V+
	Low Battery Flag Activation Voltage	6.3	7.2	7.7	V	V+ to V–
Digital						
	Continuity Comparator Threshold Voltages	100	200	—	mV	V_{OUT} pin 27 = High
		—	200	400	mV	V_{OUT} pin 27 = Low
	Pull-down Current	—	2	10	µA	Pins 37, 38, 39
	"Weak Output" Current Sink/Source	—	3/3	—	µA	Pins 20, 21 sink/source
		—	3/9	—	µA	Pin 27 sink/source
	Pin 22 Source Current	—	40	—	µA	
	Pin 22 Sink Current	—	3	—	µA	

Note 1: Input voltages may exceed supply voltages, provided input current is limited to ±400 µA. Currents above this value may result in invalid display readings, but will not destroy the device if limited to ±1 mA. Dissipation ratings assume device is mounted with all leads soldered to printed circuit board.

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2.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin No. 40-Pin PDIP	Pin No. 44-Pin PQFP	Pin No. 44-Pin PLCC	Symbol	Function
1	40	2	OSC1	Input to first clock inverter.
2	41	3	OSC3	Output of second clock inverter.
3	42	4	ANNUNCIATOR	Backplane square wave output for driving annunciators.
4	43	5	B_1, C_1, CONT	Output to display segments.
5	44	6	A_1, G_1, D_1	Output to display segments.
6	1	7	F_1, E_1, DP_1	Output to display segments.
7	2	8	B_2, C_2, LO BATT	Output to display segments.
8	3	9	A_2, G_2, D_2	Output to display segments.
9	4	10	F_2, E_2, DP_2	Output to display segments.
10	5	11	B_3, C_3, MINUS	Output to display segments.
11	7	13	A_3, G_3, D_3	Output to display segments.
12	8	14	F_3, E_3, DP_3	Output to display segments.
13	9	15	B_4, C_4, BC_5	Output to display segments.
14	10	16	A_4, D_4, G_4	Output to display segments.
15	11	17	F_4, E_4, DP_4	Output to display segments.
16	12	18	BP_3	Backplane #3 output to display.
17	13	19	BP_2	Backplane #2 output to display.
18	14	20	BP_1	Backplane #1 output to display.
19	15	21	V_{DISP}	Negative rail for display drivers.
20	16	22	DP_4/OR	**Input:** When high, turns on most significant decimal point. **Output:** Pulled high when result count exceeds ±19,999.
21	18	24	DP_3/UR	**Input:** Second-most significant decimal point on when high. **Output:** Pulled high when result count is less than ±1000.
22	19	25	$\overline{\text{LATCH}}$/HOLD	**Input:** When floating, ADC operates in Free Run mode. When pulled high, the last displayed reading is held. When pulled low, the result counter contents are shown incrementing during the de-integrate phase of cycle. **Output:** Negative going edge occurs when the data latches are updated. Can be used for converter status signal.
23	20	26	V–	Negative power supply terminal.
24	21	27	V+	Positive power supply terminal and positive rail for display drivers.
25	22	28	INT IN	Input to integrator amplifier.
26	23	29	INT OUT	Output of integrator amplifier.
27	24	30	CONTINUITY	**Input:** When low, continuity flag on the display is off. When high, continuity flag is on. **Output:** High when voltage between inputs is less than +200 mV. Low when voltage between inputs is more than +200 mV.
28	25	31	COMMON	Sets common mode voltage of 3.2V below V+ for DE, 10X, etc. Can be used as pre-regulator for external reference.
29	26	32	C_{REF}+	Positive side of external reference capacitor.
30	27	33	C_{REF}–	Negative side of external reference capacitor.
31	29	35	BUFFER	Output of buffer amplifier.
32	30	36	IN LO	Negative input voltage terminal.
33	31	37	IN HI	Positive input voltage terminal.
34	32	38	REF HI	Positive reference voltage.
35	33	39	REF LO	Negative reference voltage

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TABLE 2-1: PIN FUNCTION TABLE (CONTINUED)

Pin No. 40-Pin PDIP	Pin No. 44-Pin PQFP	Pin No. 44-Pin PLCC	Symbol	Function
36	34	40	DGND	Internal ground reference for digital section. See **Section 4.2.1 "±5V Power Supply"**.
37	35	41	RANGE	3 µA pull-down for 200 mV scale. Pulled high externally for 2V scale.
38	36	42	DP_2	Internal 3 µA pull-down. When high, decimal point 2 will be on.
39	37	43	DP_1	Internal 3 µA pull-down. When high, decimal point 1 will be on.
40	38	44	OSC2	Output of first clock inverter. Input of second clock inverter.
—	6,17, 28, 39	12, 23, 34, 1	NC	No connection.

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3.0 DETAILED DESCRIPTION

(All pin designations refer to 40-pin PDIP.)

The TC7129 is designed to be the heart of a high-resolution analog measurement instrument. The only additional components required are a few passive elements: a voltage reference, a LCD and a power source. Most component values are not critical; substitutes can be chosen based on the information given below.

The basic circuit for a digital multimeter application is shown in Figure 3-1. See **Section 4.0 "Typical Applications"**, for variations. Typical values for each component are shown. The sections below give component selection criteria.

3.1 Oscillator (X_{OSC}, C_{O1}, C_{O2}, R_O)

The primary criterion for selecting the crystal oscillator is to choose a frequency that achieves maximum rejection of line frequency noise. To do this, the integration phase should last an integral number of line cycles. The integration phase of the TC7129 is 10,000 clock cycles on the 200 mV range and 1000 clock cycles on the 2V range. One clock cycle is equal to two oscillator cycles. For 60 Hz rejection, the oscillator frequency should be chosen so that the period of one line cycle equals the integration time for the 2V range.

EQUATION 3-1:

$$1/60 \text{ second} = 16.7 \text{ msec} = \frac{1000 \text{ clock cycles} * 2 \text{ OSC cycles/clock cycle}}{\text{OSC Frequency}}$$

This equation gives an oscillator frequency of 120 kHz. A similar calculation gives an optimum frequency of 100 kHz for 50 Hz rejection.

The resistor and capacitor values are not critical; those shown work for most applications. In some situations, the capacitor values may have to be adjusted to compensate for parasitic capacitance in the circuit. The capacitors can be low-cost ceramic devices.

Some applications can use a simple RC network instead of a crystal oscillator. The RC oscillator has more potential for jitter, especially in the least significant digit. See **Section 4.5 "RC Oscillator"**.

3.2 Integrating Resistor (R_{INT})

The integrating resistor sets the charging current for the integrating capacitor. Choose a value that provides a current between 5 µA and 20 µA at 2V, the maximum full-scale input. The typical value chosen gives a charging current of 13.3 µA:

EQUATION 3-1:

$$I_{CHARGE} = \frac{2V}{150\ k\Omega} \quad 13.3\ \mu A$$

Too high a value for R_{INT} increases the sensitivity to noise pickup and increases errors due to leakage current. Too low a value degrades the linearity of the integration, leading to inaccurate readings.

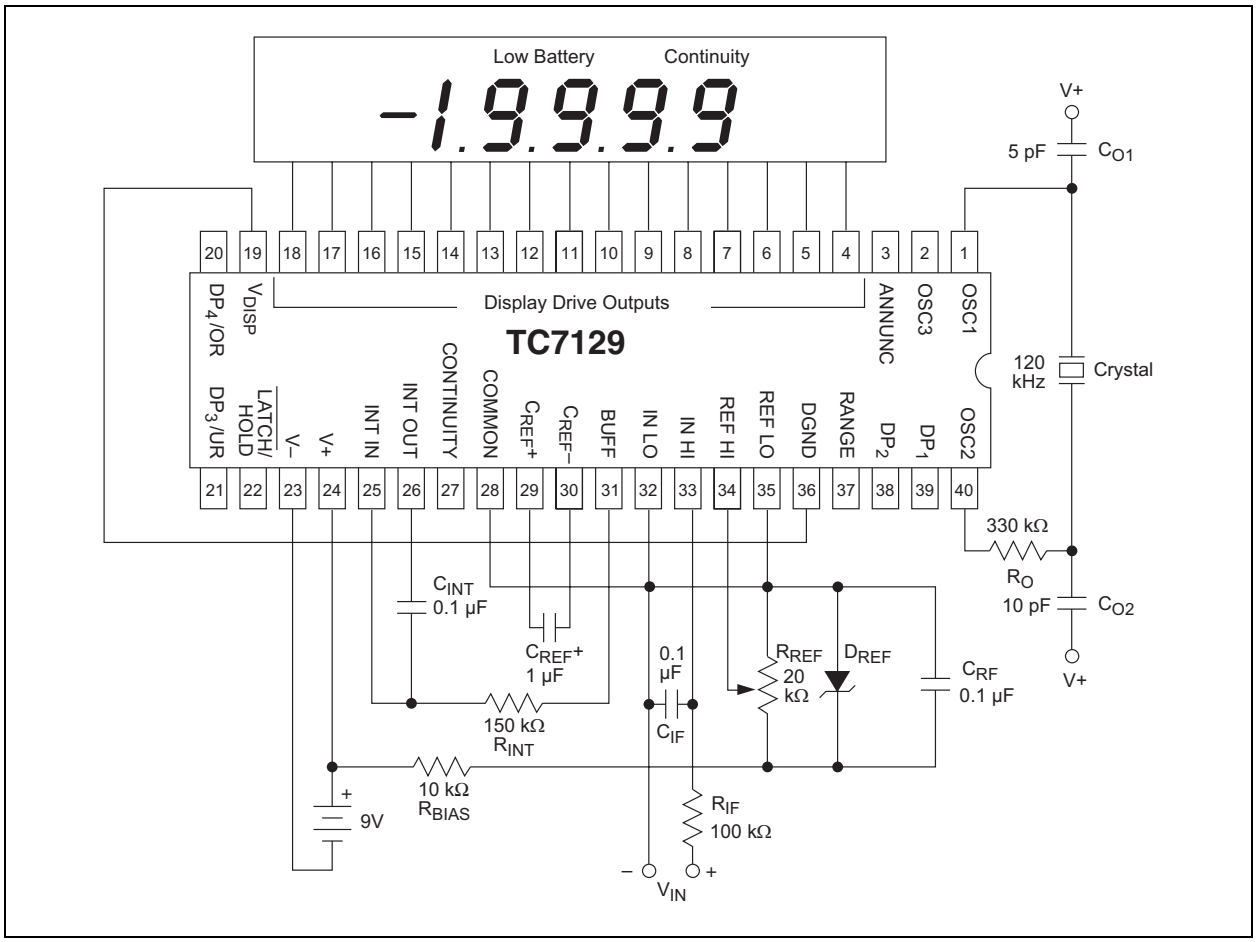


Figure 3-1: *Standard Circuit.*

3.3 Integrating Capacitor (C_{INT})

The charge stored in the integrating capacitor during the integrate phase is directly proportional to the input voltage. The primary selection criterion for C_{INT} is to choose a value that gives the highest voltage swing while remaining within the high-linearity portion of the integrator output range. An integrator swing of 2V is the recommended value. The capacitor value can be calculated using the following equation:

EQUATION 3-1:

$$C_{INT} = \frac{t_{INT} \times I_{INT}}{V_{SWING}}$$

Where t_{INT} is the integration time.

Using the values derived above (assuming 60 Hz operation), the equation becomes:

EQUATION 3-2:

$$C_{INT} = \frac{16.7\ \text{msec} \times 13.3\ \mu\text{A}}{2\text{V}} = 0.1\ \mu\text{A}$$

The capacitor should have low dielectric absorption to ensure good integration linearity. Polypropylene and Teflon® capacitors are usually suitable. A good measurement of the dielectric absorption is to connect the reference capacitor across the inputs by connecting:

Pin-to-Pin:

20 → 33 (C_{REF}+ to IN HI)

30 → 32 (C_{REF}– to IN LO)

A reading between 10,000 and 9998 is acceptable; anything lower indicates unacceptably high dielectric absorption.

3.4 Reference Capacitor (C_{REF})

The reference capacitor stores the reference voltage during several phases of the measurement cycle. Low leakage is the primary selection criterion for this component. The value must be high enough to offset the effect of stray capacitance at the capacitor terminals. A value of at least 1 µF is recommended.

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3.5 Voltage Reference (D_{REF}, R_{REF}, R_{BIAS}, C_{RF})

The reference potentiometer (R_{REF}) provides an adjustment for adjusting the reference voltage; any value above 20 kΩ is adequate. The bias resistor (R_{BIAS}) limits the current through D_{REF} to less than 150 µA. The reference filter capacitor (C_{RF}) forms an RC filter with R_{BIAS} to help eliminate noise.

3.6 Input Filter (R_{IF}, C_{IF})

For added stability, an RC input noise filter is usually included in the circuit. The input filter resistor value should not exceed 100 kΩ. A typical RC time constant value is 16.7 msec to help reject line frequency noise. The input filter capacitor should have low leakage for a high-impedance input.

3.7 Battery

The typical circuit uses a 9V battery as a power source. However, any value between 6V and 12V can be used. For operation from batteries with voltages lower than 6V and for operation from power supplies, see **Section 4.2 "Powering the TC7129"**.

4.0 TYPICAL APPLICATIONS

4.1 TC7129 as a Replacement Part

The TC7129 is a direct pin-for-pin replacement part for the ICL7129. Note, however, that the ICL7129 requires a capacitor and resistor between pins 26 and 28 for phase compensation. Since the TC7129 uses internal phase compensation, these parts are not required and, in fact, must be removed from the circuit for stable operation.

4.2 Powering the TC7129

While the most common power source for the TC7129 is a 9V battery, there are other possibilities. Some of the more common ones are explained below.

4.2.1 ±5V Power Supply

Measurements are made with respect to power supply ground. DGND (pin 36) is set internally to about 5V less than V+ (pin 24); it is not intended to be a power supply input and must not be tied directly to power supply ground. It can be used as a reference for external logic, as explained in **Section 4.3 "Connecting to External Logic"**, (see Figure 4-1).

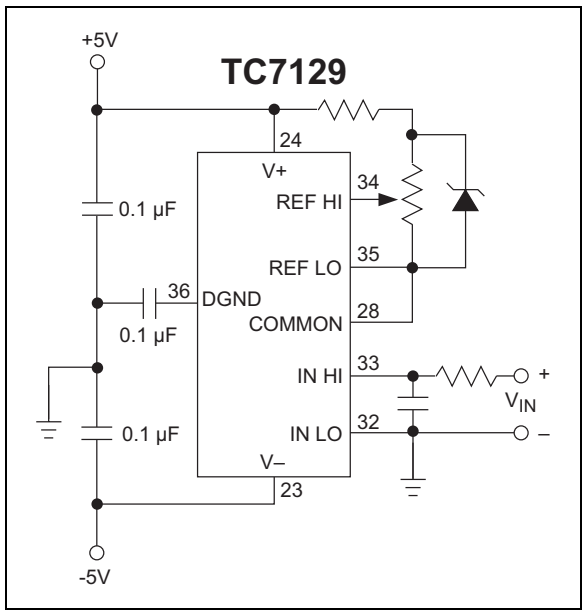


Figure 4-1: *Powering the TC7129 From a ±5V Power Supply.*

4.2.2 Low Voltage Battery Source

A battery with voltage between 3.8V and 6V can be used to power the TC7129 when used with a voltage doubler circuit, as shown in Figure 4-2. The voltage doubler uses the TC7660 DC-to-DC voltage converter and two external capacitors.

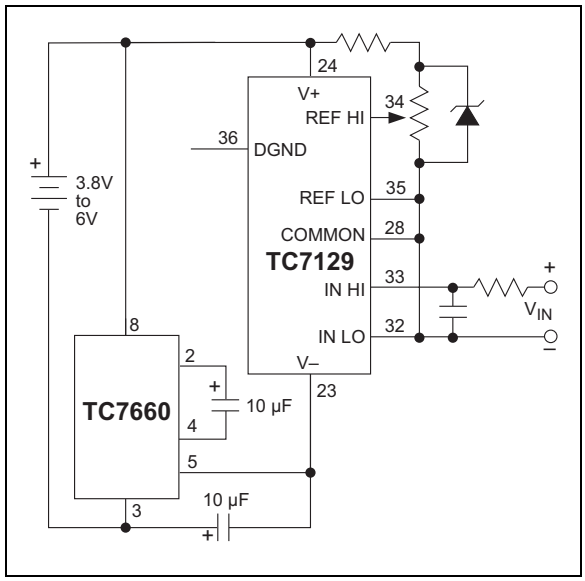


Figure 4-2: *Powering the TC7129 From a Low-Voltage Battery.*

4.2.3 +5V Power Supply

Measurements are made with respect to power supply ground. COMMON (pin 28) is connected to REF LO (pin 35). A voltage doubler is needed, since the supply voltage is less than the 6V minimum needed by the TC7129. DGND (pin 36) must be isolated from power supply ground (see Figure 4-3).

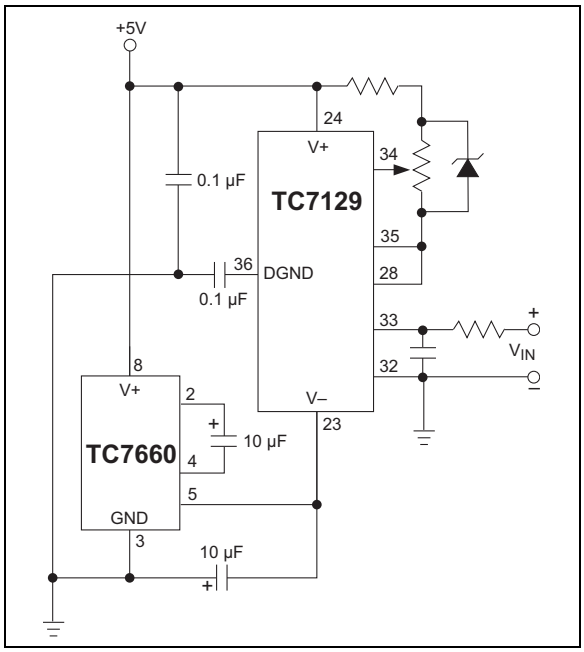


Figure 4-3: *Powering the TC7129 From a +5V Power Supply.*

4.3 Connecting to External Logic

External logic can be directly referenced to DGND (pin 36), provided that the supply current of the external logic does not exceed the sink current of DGND (Figure 4-4). A safe value for DGND sink current is 1.2 mA. If the sink current is expected to exceed this value, a buffer is recommended (see Figure 4-5).

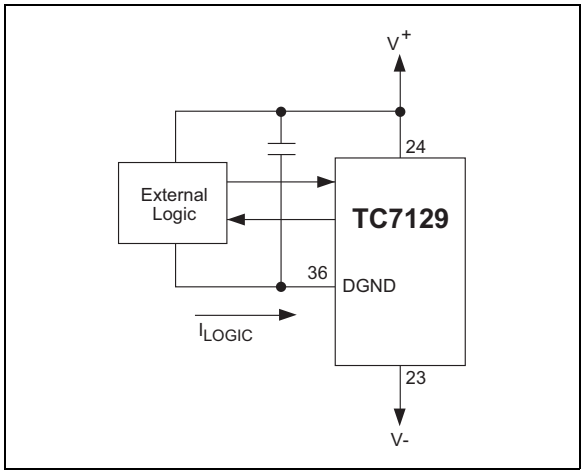


Figure 4-4: *External Logic Referenced Directly to DGND.*

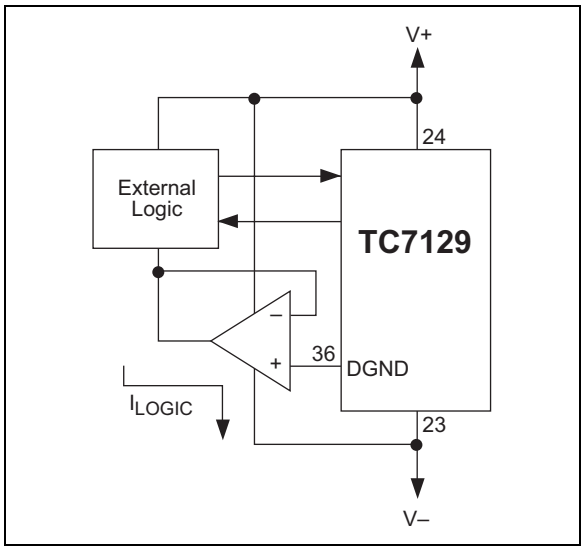


Figure 4-5: *External Logic Referenced to DGND with Buffer.*

4.4 Temperature Compensation

For most applications, V_{DISP} (pin 19) can be connected directly to DGND (pin 36). For applications with a wide temperature range, some LCDs require that the drive levels vary with temperature to maintain good viewing angle and display contrast. Figure 4-6 shows two circuits that can be adjusted to give temperature compensation of about 10 mV/°C between V+ (pin 24) and V_{DISP}. The diode between DGND and V_{DISP} should have a low turn-on voltage because V_{DISP} cannot exceed 0.3V below DGND.

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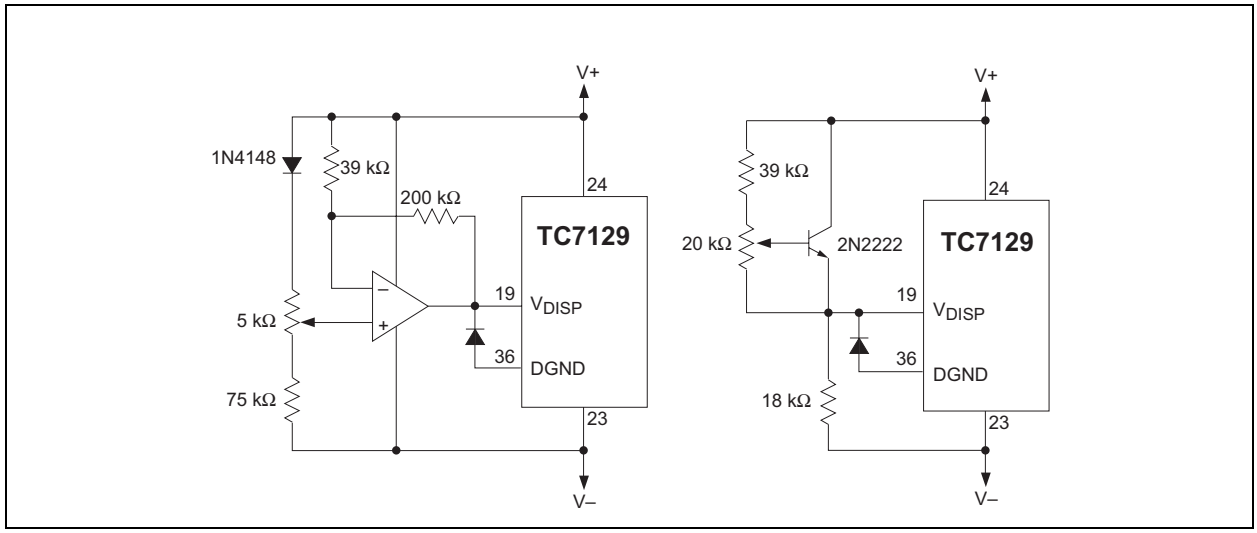


Figure 4-6: *Temperature Compensating Circuits.*

4.5 RC Oscillator

For applications in which 3-1/2 digit (100 µV) resolution is sufficient, an RC oscillator is adequate. A recommended value for the capacitor is 51 pF. Other values can be used as long as they are sufficiently larger than the circuit parasitic capacitance. The resistor value is calculated as:

EQUATION 4-1:

$$R = \frac{0.45}{Freq * C}$$

For 120 kHz frequency and C = 51 pF, the calculated value of R is 75 kΩ. The RC oscillator and the crystal oscillator circuits are shown in Figure 4-7.

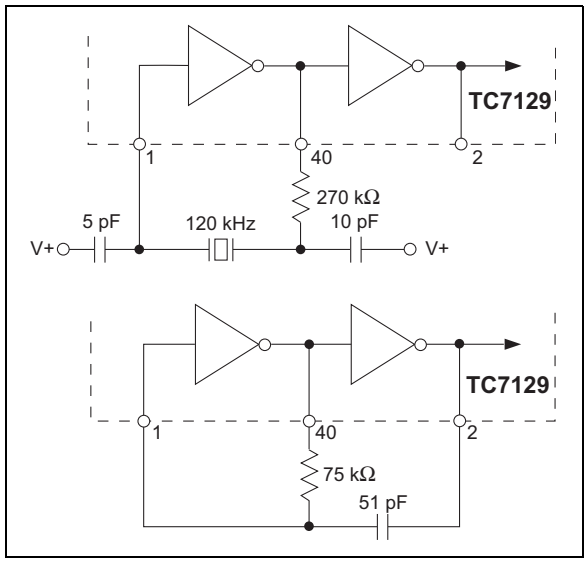


Figure 4-7: *Oscillator Circuits.*

4.6 Measuring Techniques

Two important techniques are used in the TC7129: successive integration and digital auto-zeroing. Successive integration is a refinement to the traditional dual-slope conversion technique.

4.7 Dual-Slope Conversion

A dual-slope conversion has two basic phases: integrate and de-integrate. During the integrate phase, the input signal is integrated for a fixed period of time; the integrated voltage level is thus proportional to the input voltage. During the de-integrate phase, the integrated voltage is ramped down at a fixed slope, and a counter counts the clock cycles until the integrator voltage crosses zero. The count is a measurement of the time to ramp the integrated voltage to zero and is, therefore, proportional to the input voltage being measured. This count can then be scaled and displayed as a measurement of the input voltage. Figure 4-8 shows the phases of the dual-slope conversion.

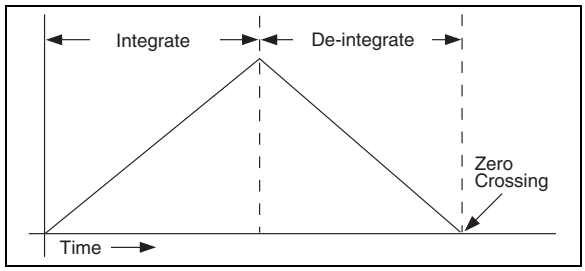


Figure 4-8: *Dual-Slope Conversion.*

The dual-slope method has a fundamental limitation. The count can only stop on a clock cycle, so that measurement accuracy is limited to the clock frequency. In addition, a delay in the zero-crossing comparator can add to the inaccuracy. Figure 4-9 shows these errors in an actual measurement.

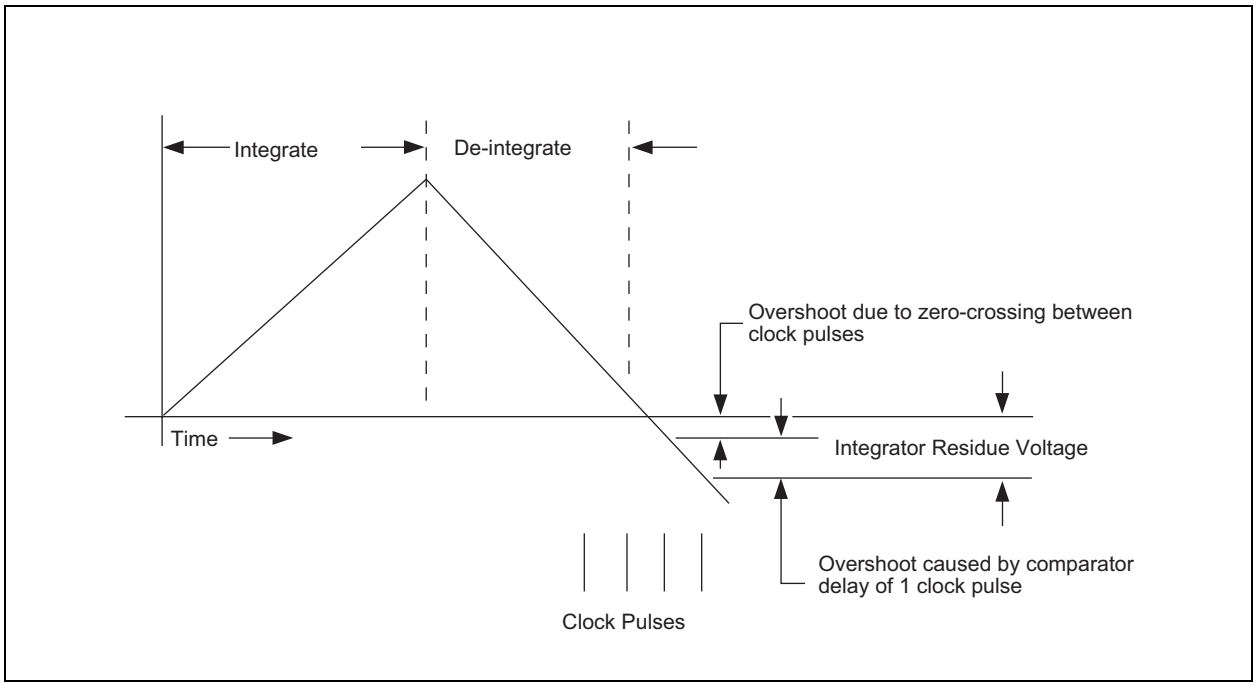


Figure 4-9: *Accuracy Errors in Dual-Slope Conversion.*

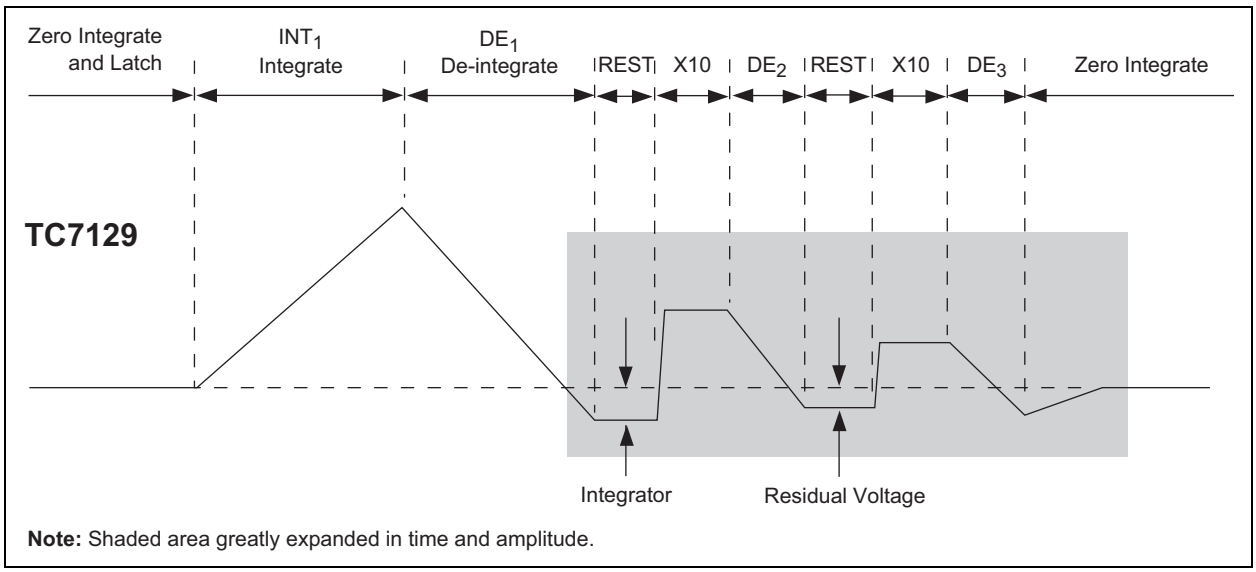


Figure 4-10: *Integration Waveform.*

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4.8 Successive Integration

The successive integration technique picks up where dual-slope conversion ends. The overshoot voltage shown in Figure 4-9 (called the “integrator residue voltage”) is measured to obtain a correction to the initial count. Figure 4-10 shows the cycles in a successive integration measurement.

The waveform shown is for a negative input signal. The sequence of events during the measurement cycle is shown in Table 4-1.

TABLE 4-1: MEASUREMENT CYCLE SEQUENCE

Phase	Description
INT_1	Input signal is integrated for fixed time (1000 clock cycles on 2V scale, 10,000 on 200 mV).
DE_1	Integrator voltage is ramped to zero. Counter counts up until zero-crossing to produce reading accurate to 3-1/2 digits. Residue represents an overshoot of the actual input voltage.
REST	Rest; circuit settles.
X10	Residue voltage is amplified 10 times and inverted.
DE_2	Integrator voltage is ramped to zero. Counter counts down until zero-crossing to correct reading to 4-1/2 digits. Residue represents an undershoot of the actual input voltage.
REST	Rest; circuit settles.
X10	Residue voltage is amplified 10 times and inverted.
DE_3	Integrator voltage is ramped to zero. Counter counts up until zero-crossing to correct reading to 5-1/2 digits. Residue is discarded.

4.9 Digital Auto-Zeroing

To eliminate the effect of amplifier offset errors, the TC7129 uses a digital auto-zeroing technique. After the input voltage is measured as described above, the measurement is repeated with the inputs shorted internally. The reading with inputs shorted is a measurement of the internal errors and is subtracted from the previous reading to obtain a corrected measurement. Digital auto-zeroing eliminates the need for an external auto-zeroing capacitor used in other ADCs.

4.10 Inside the TC7129

Figure 4-11 shows a simplified block diagram of the TC7129.

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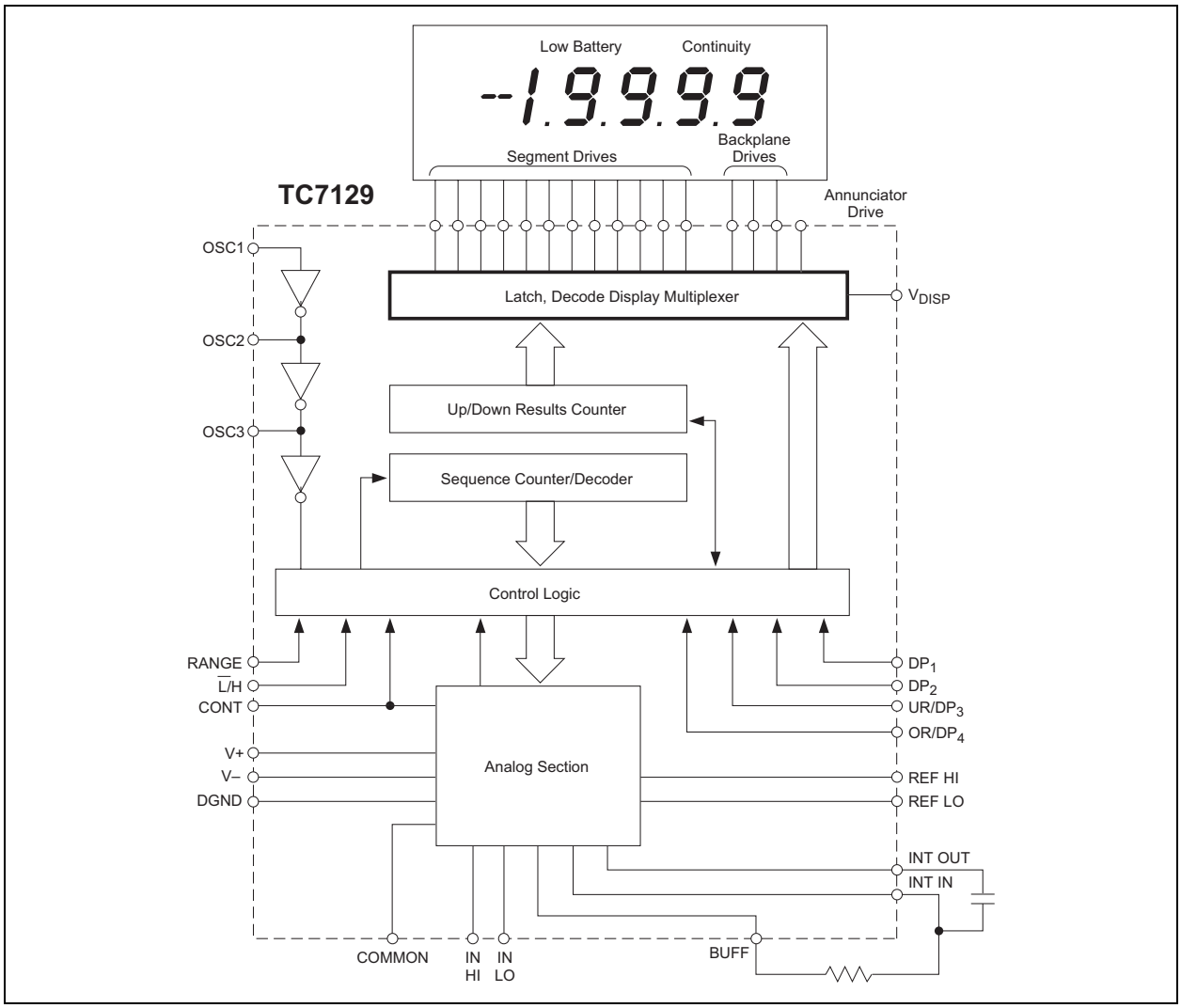


Figure 4-11: *TC7129 Functional Block Diagram.*

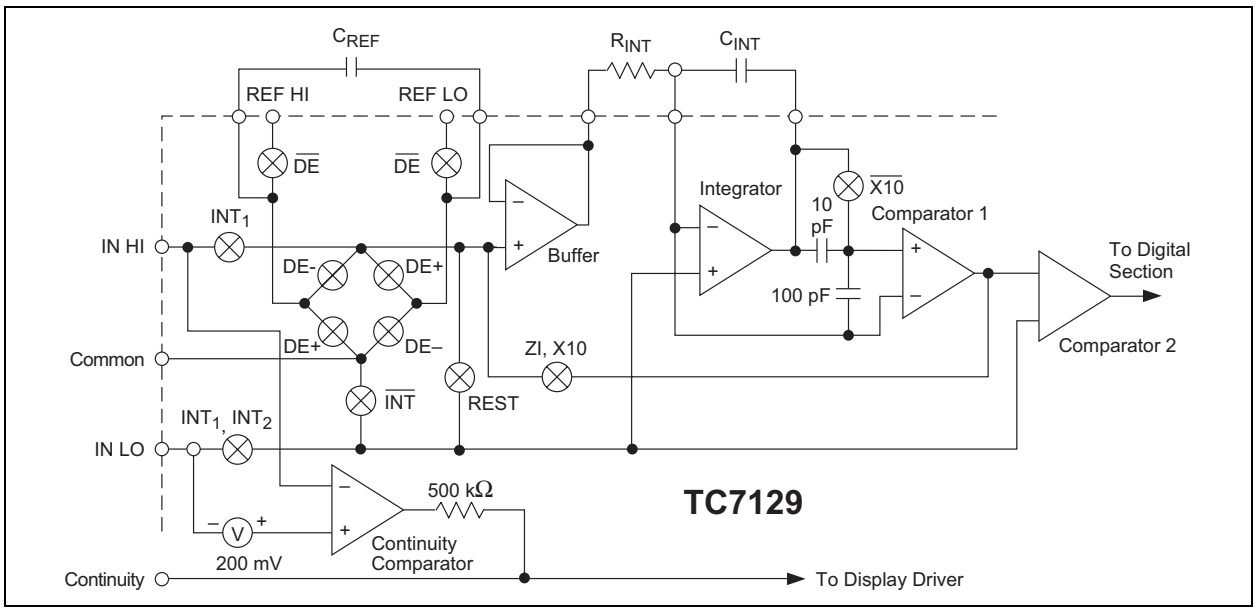


Figure 4-12: *Integrator Block Diagram.*

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4.11 Integrator Section

The integrator section includes the integrator, comparator, input buffer amplifier and analog switches (see Table 4-2) used to change the circuit configuration during the separate measurement phases described earlier. (See Figure 4-12).

TABLE 4-2: SWITCH LEGENDS

Label	Description
Label	Meaning.
DE	Open during all de-integrate phases.
DE–	Closed during all de-integrate phases when input voltage is negative.
DE+	Closed during all de-integrate phases when input voltage is positive.
INT_1	Closed during the first integrate phase (measurement of the input voltage).
INT_2	Closed during the second integrate phase (measurement of the amplifier offset).
INT	Open during both integrate phases.
REST	Closed during the rest phase.
ZI	Closed during the zero integrate phase.
X10	Closed during the X10 phase.
X10	Open during the X10 phase.

The buffer amplifier has a common mode input voltage range from 1.5V above V– to 1V below V+. The integrator amplifier can swing to within 0.3V of the rails. However, for best linearity, the swing is usually limited to within 1V. Both amplifiers can supply up to 80 µA of output current, but should be limited to 20 µA for good linearity.

4.12 Continuity Indicator

A comparator with a 200 mV threshold is connected between IN HI (pin 33) and IN LO (pin 32). Whenever the voltage between inputs is less than 200 mV, the CONTINUITY output (pin 27) will be pulled high, activating the continuity annunciator on the display. The continuity pin can also be used as an input to drive the continuity annunciator directly from an external source (see Figure 4-13).

A schematic of the input/output nature of this pin is also shown in Figure 4-14.

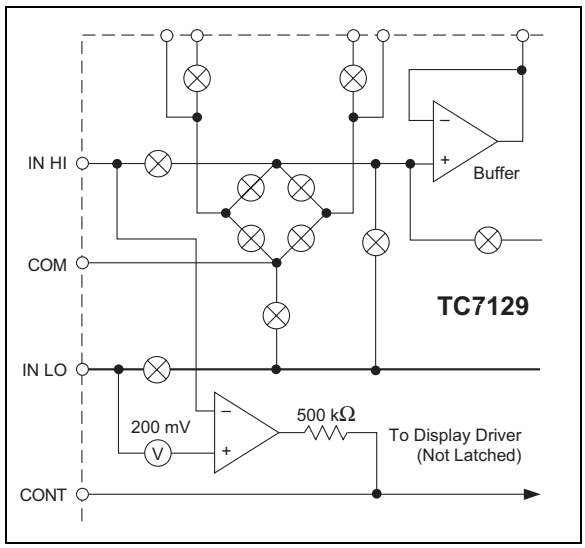


Figure 4-13: *Continuity Indicator Circuit.*

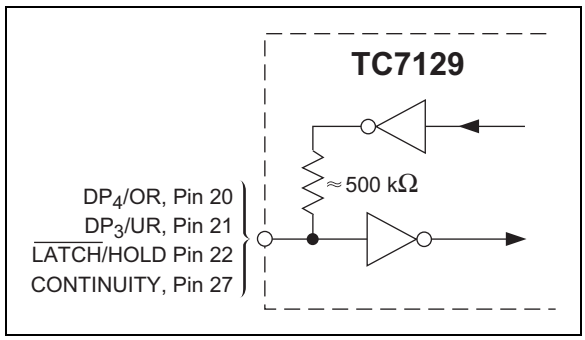


Figure 4-14: *Input/Output Pin Schematic.*

4.13 Common and Digital Ground

The common and digital ground (DGND) outputs are generated from internal Zener diodes. The voltage between V+ and DGND is the internal supply voltage for the digital section of the TC7129. Common can source approximately 12 µA; DGND has essentially no source capability (see Figure 4-15).

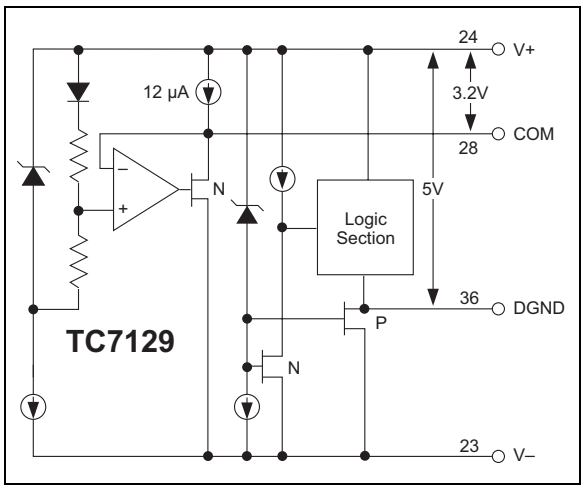


Figure 4-15: *Digital Ground (DGND) and Common Outputs.*

4.14 Low Battery

The low battery annunciator turns on when supply voltage between V– and V+ drops below 6.8V. The internal zener diode has a threshold of 6.3V. When the supply voltage drops below 6.8V, the transistor tied to V– turns off pulling the “Low Battery” point high.

4.15 Sequence and Results Counter

A sequence counter and associated control logic provide signals that operate the analog switches in the integrator section. The comparator output from the integrator gates the results counter. The results counter is a six-section up/down decade counter that holds the intermediate results from each successive integration.

4.16 Overrange and Underrange Outputs

When the results counter holds a value greater than ±19,999, the DP_4/OR output (Pin 20) is driven high. When the results counter value is less than ±1000, the DP_3/UR output (Pin 21) is driven high. Both signals are valid on the falling edge of $\overline{\text{LATCH}}$/HOLD ($\overline{\text{L}}$/H) and do not change until the end of the next conversion cycle. The signals are updated at the end of each conversion, unless the $\overline{\text{L}}$/H input (Pin 22) is held high. Pins 20 and 21 can also be used as inputs for external control of decimal points 3 and 4. Figure 4-14 shows a schematic of the input/output nature of these pins.

4.17 $\overline{\text{LATCH}}$/Hold

The $\overline{\text{L}}$/H output goes low during the last 100 cycles of each conversion. This pulse latches the conversion data into the display driver section of the TC7129. This pin can also be used as an input. When driven high, the display will not be updated; the previous reading is displayed. When driven low, the display reading is not latched; the sequence counter reading will be displayed. Since the counter is counting much faster than the backplanes are being updated, the reading shown in this mode is somewhat erratic.

4.18 Display Driver

The TC7129 drives a triplexed LCD with three backplanes. The LCD can include decimal points, polarity sign and annunciators for continuity and low battery. Figure 4-16 shows the assignment of the display segments to the backplanes and segment drive lines. The backplane drive frequency is obtained by dividing the oscillator frequency by 1200. This results in a backplane drive frequency of 100 Hz for 60 Hz operation (120 kHz crystal) and 83.3 Hz for 50 Hz operation (100 kHz crystal).

Backplane waveforms are shown in Figure 4-17. These appear on outputs BP_1, BP_2, BP_3 (pins 16, 17 and 18). They remain the same, regardless of the segments being driven.

Other display output lines (pins 4 through 15) have waveforms that vary depending on the displayed values. Figure 4-18 shows a set of waveforms for the A, G, D outputs (pins 5, 8, 11 and 14) for several combinations of “ON” segments.

The ANNUNCIATOR DRIVE output (pin 3) is a square wave, running at the backplane frequency (100 Hz or 83.3 Hz) with a peak-to-peak voltage equal to DGND voltage. Connecting an annunciator to pin 3 turns it on; connecting it to its backplane turns it off.

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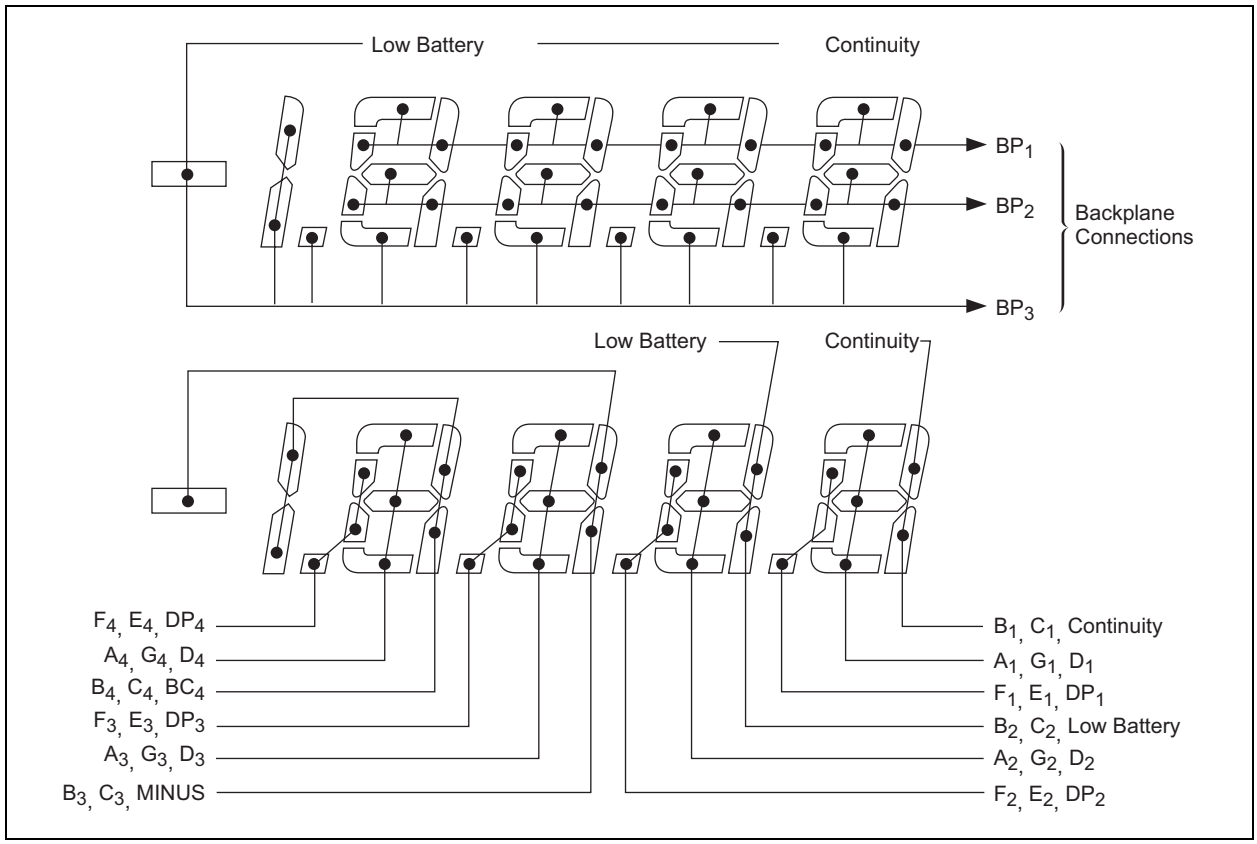


Figure 4-16: *Display Segment Assignments.*

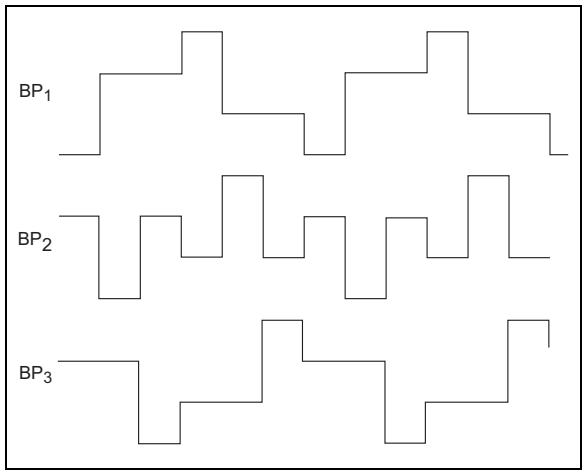


Figure 4-17: *Backplane Waveforms.*

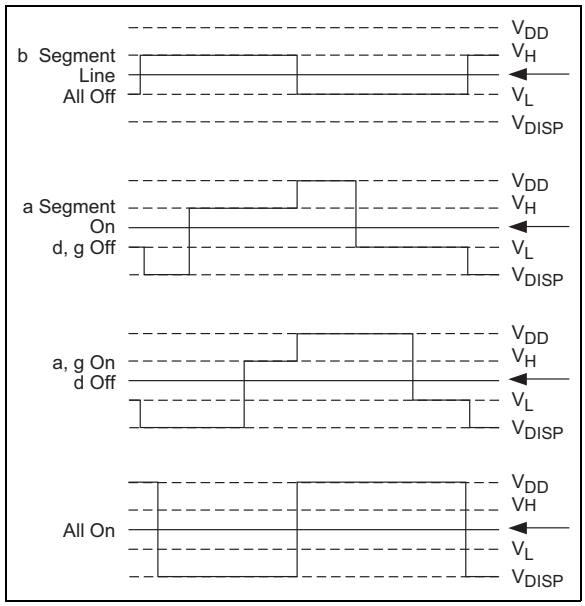


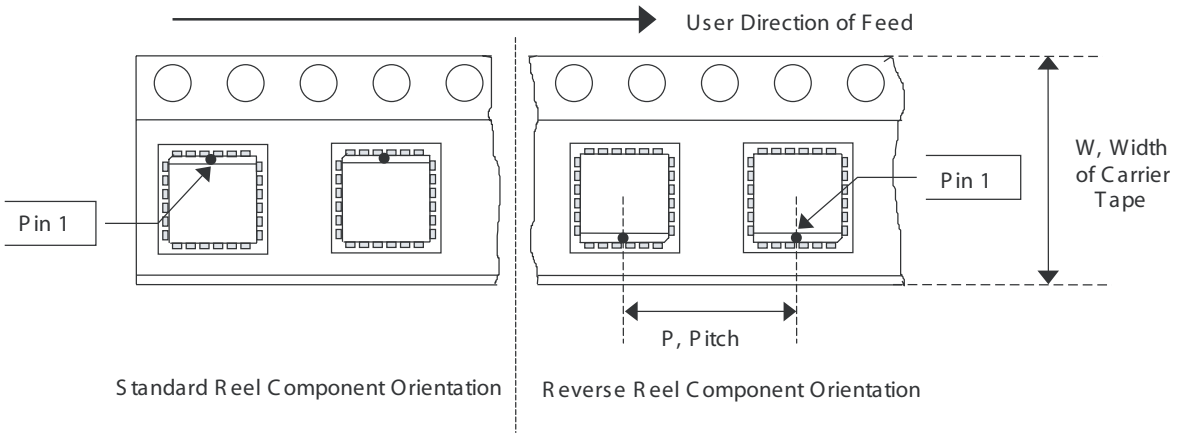
Figure 4-18: *Typical Display Output Waveforms.*

5.0 PACKAGING INFORMATION

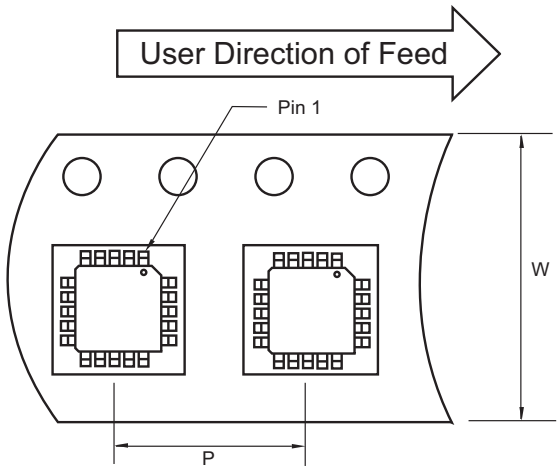
5.1 Package Marking Information

Package marking data not available a this time.

5.2 Taping Forms



Component Taping Orientation for 44-Pin PQFP Devices



Standard Reel Component Orientation
for 713 Suffix Device

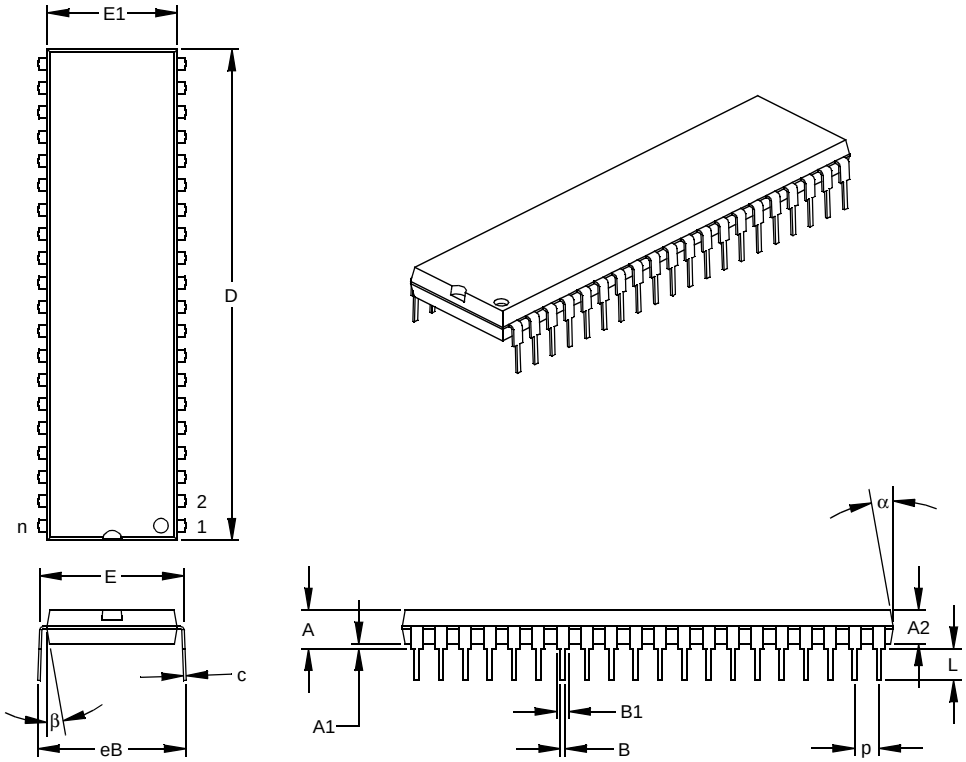
Carrier Tape, Number of Components Per Reel and Reel Size

Package	Carrier Width (W)	Pitch (P)	Part Per Full Reel	Reel Size
44-Pin PQFP	24 mm	16 mm	500	13 in

Note: Drawing does not represent total number of pins.

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40-Lead Plastic Dual In-line (P) – 600 mil Body (PDIP)



Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		40			40	
Pitch	p		.100			2.54	
Top to Seating Plane	A	.160	.175	.190	4.06	4.45	4.83
Molded Package Thickness	A2	.140	.150	.160	3.56	3.81	4.06
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.595	.600	.625	15.11	15.24	15.88
Molded Package Width	E1	.530	.545	.560	13.46	13.84	14.22
Overall Length	D	2.045	2.058	2.065	51.94	52.26	52.45
Tip to Seating Plane	L	.120	.130	.135	3.05	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.030	.050	.070	0.76	1.27	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing §	eB	.620	.650	.680	15.75	16.51	17.27
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

***** Controlling Parameter

§ Significant Characteristic

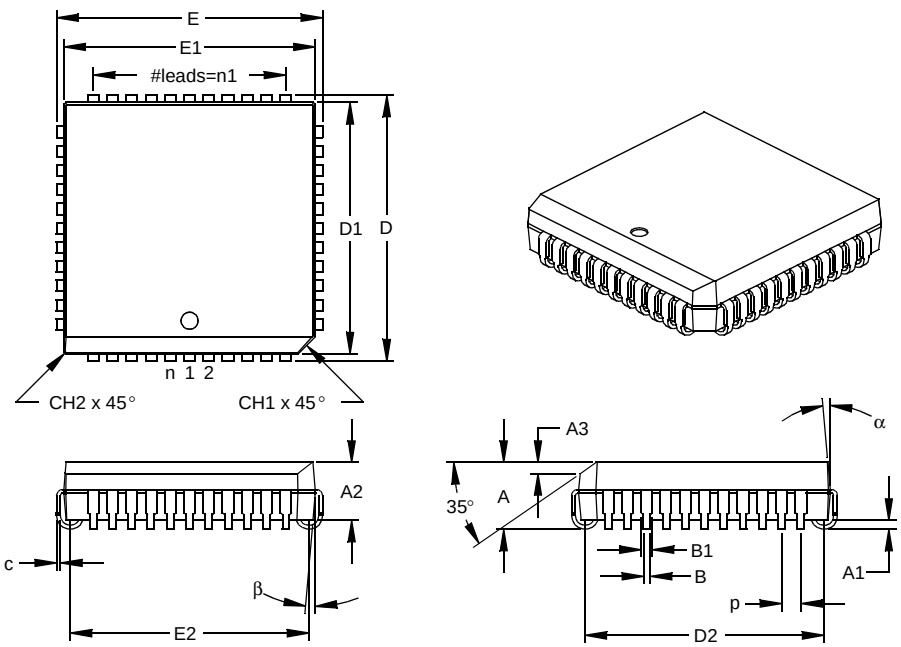
Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.

JEDEC Equivalent: MO-011

Drawing No. C04-016

44-Lead Plastic Leaded Chip Carrier (LW) – Square (PLCC)

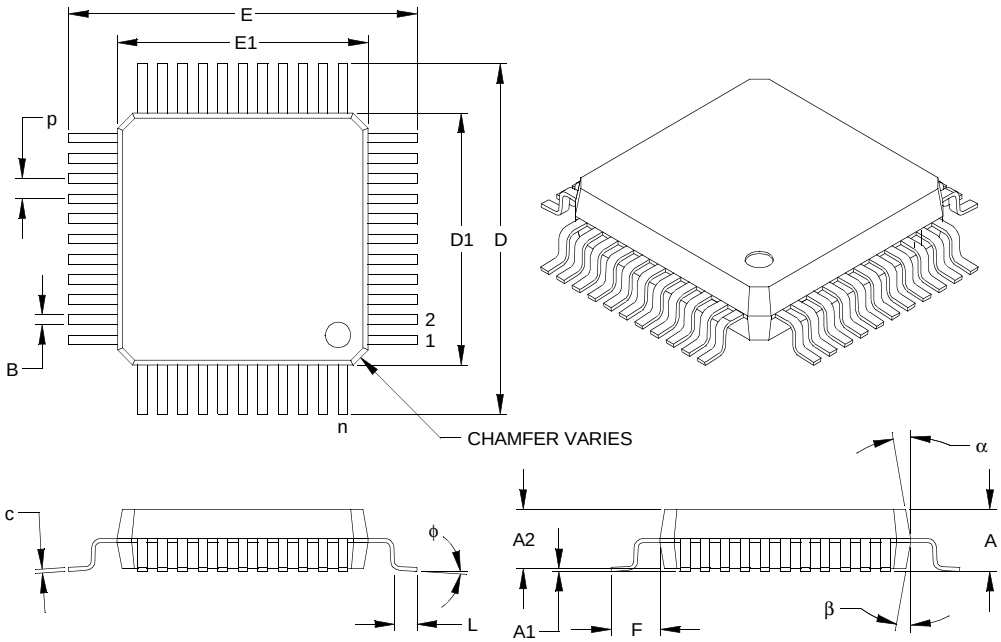


Units		INCHES*			MILLIMETERS		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		44			44	
Pitch	p		.050			1.27	
Pins per Side	n1		11			11	
Overall Height	A	.165	.173	.180	4.19	4.39	4.57
Molded Package Thickness	A2	.145	.153	.160	3.68	3.87	4.06
Standoff §	A1	.020	.028	.035	0.51	0.71	0.89
Side 1 Chamfer Height	A3	.024	.029	.034	0.61	0.74	0.86
Corner Chamfer 1	CH1	.040	.045	.050	1.02	1.14	1.27
Corner Chamfer (others)	CH2	.000	.005	.010	0.00	0.13	0.25
Overall Width	E	.685	.690	.695	17.40	17.53	17.65
Overall Length	D	.685	.690	.695	17.40	17.53	17.65
Molded Package Width	E1	.650	.653	.656	16.51	16.59	16.66
Molded Package Length	D1	.650	.653	.656	16.51	16.59	16.66
Footprint Width	E2	.590	.620	.630	14.99	15.75	16.00
Footprint Length	D2	.590	.620	.630	14.99	15.75	16.00
Lead Thickness	c	.008	.011	.013	0.20	0.27	0.33
Upper Lead Width	B1	.026	.029	.032	0.66	0.74	0.81
Lower Lead Width	B	.013	.020	.021	0.33	0.51	0.53
Mold Draft Angle Top	α	0	5	10	0	5	10
Mold Draft Angle Bottom	β	0	5	10	0	5	10

***** Controlling Parameter
§ Significant Characteristic
Notes:
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010” (0.254mm) per side.
JEDEC Equivalent: MO-047
Drawing No. C04-048

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44-Lead Plastic Quad Flatpack (KW) 10x10x2.0 mm Body, 1.95/0.25 mm Lead Form (PQFP)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		44			44	
Pitch	p		.031 BSC			0.80 BSC	
Overall Height	A	-	-	.096	-	-	2.45
Molded Package Thickness	A2	.077	.079	.083	1.95	2.00	2.10
Standoff §	A1	.010	-	-	0.25	-	-
Foot Length	L	.029	.035	.041	0.73	0.88	1.03
Footprint	F		.077 REF.			1.95 REF.	
Foot Angle	φ	0°	3.5°	7°	0°	3.5°	7°
Overall Width	E		.547 BSC			13.90 BSC	
Overall Length	D		.547 BSC			13.90 BSC	
Molded Package Width	E1		.394 BSC			10.00 BSC	
Molded Package Length	D1		.394 BSC			10.00 BSC	
Lead Thickness	c	.004	-	.009	0.11	-	0.23
Lead Width	B	.012	-	.018	0.30	-	0.45
Mold Draft Angle Top	α	5°	-	16°	5°	-	16°
Mold Draft Angle Bottom	β	5°	-	16°	5°	-	16°

***** Controlling Parameter

§ Significant Characteristic

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
See ASME Y14.5M

REF: Reference Dimension, usually without tolerance, for information purposes only.
See ASME Y14.5M

JEDEC Equivalent: MO-112 AA-1

Drawing No. C04-119

Revised 07-21-05

NOTES:

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PART NO.	X	XX	XX
Device	Temp.	Pkg	Taping Direction

Device:	TC7129: 4-1/2 Digit Analog-to-Digital Converter
Temperature:	C = 0°C to +70°C I = -25°C to +85°C
Package:	PL = 40-Pin PDIP KW = 40-Pin PQFP LW = 44-Pin PLCC JL = 40-Pin CDIP
Taping Direction:	713 = Standard Taping

Examples:

a) TC7129CPL: 40-Pin PDIP

b) TC7129CKW713: 44-Pin PQFP Tape and Reel

c) TC7129CLW: 44-Pin PLCC

NOTES:

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