TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74HC166AP, TC74HC166AF, TC74HC166AFN

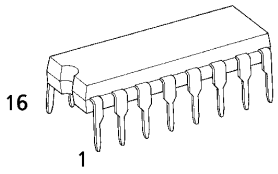
8 – BIT SHIFT REGISTER (P – IN, S – OUT)

(Note) The JEDEC SOP (FN) is not available in Japan.

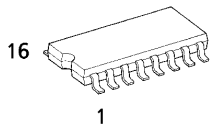
The TC74HC166A is a high speed CMOS 8-BIT PARALLEL/SERIAL-IN, SERIAL-OUT SHIFT REGISTER fabricated with silicon gate C^2MOS technology.
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.
It consists of parallel-in or serial-in, serial-out 8 - bit shift register with a gated clock input and an overriding clear input. The parallel-in or serial-in modes are controlled by the SHIFT/$\overline{\text{LOAD}}$ input. When the SHIFT/$\overline{\text{LOAD}}$ input is held high, the serial data input is enabled and the eight flip-flops perform serial shifting on each clock pulse. When held low, the parallel data inputs are enabled and synchronous loading occurs on the next clock pulse. Clocking is accomplished on the low-to-high transition of the clock pulse. The CK-INH input should be shifted high only while the CK input is held high. A direct clear input overrldes all other inputs, includng the clock, and sets all the flip-flops to zero. Functional details are shown in the truth table and the timing chrts.
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES :

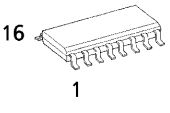
- High Speed ····· f_{MAX} = 57MHz(typ.)at V_{CC} = 5V
- Low Power Dissipation ····· I_{CC} = 4μA(Max.)at Ta = 25°C
- High Noise Immunity ····· $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min.)
- Output Drive Immunity ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}| = I_{OL}$ = 4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \simeq t_{pHL}$
- Wide Operating Voltage Range ···· V_{CC} (opr.) = 2V ~ 6V
- Pin and Function Compatible with 74LS166



P (DIP16-P-300-2.54A)
Weight : 1.00g (Typ.)

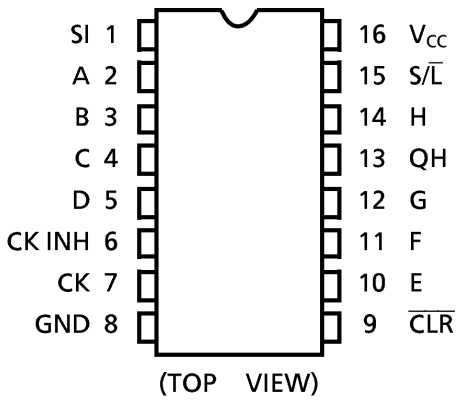


F (SOP16-P-300-1.27)
Weight : 0.18g (Typ.)

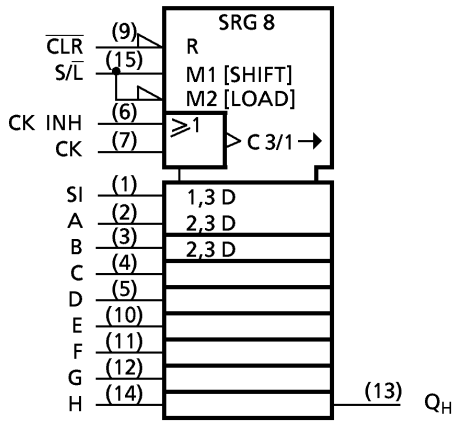


FN (SOL16-P-150-1.27)
Weight : 0.13g (Typ.)

PIN ASSIGNMENT



IEC LOGIC SYMBOL



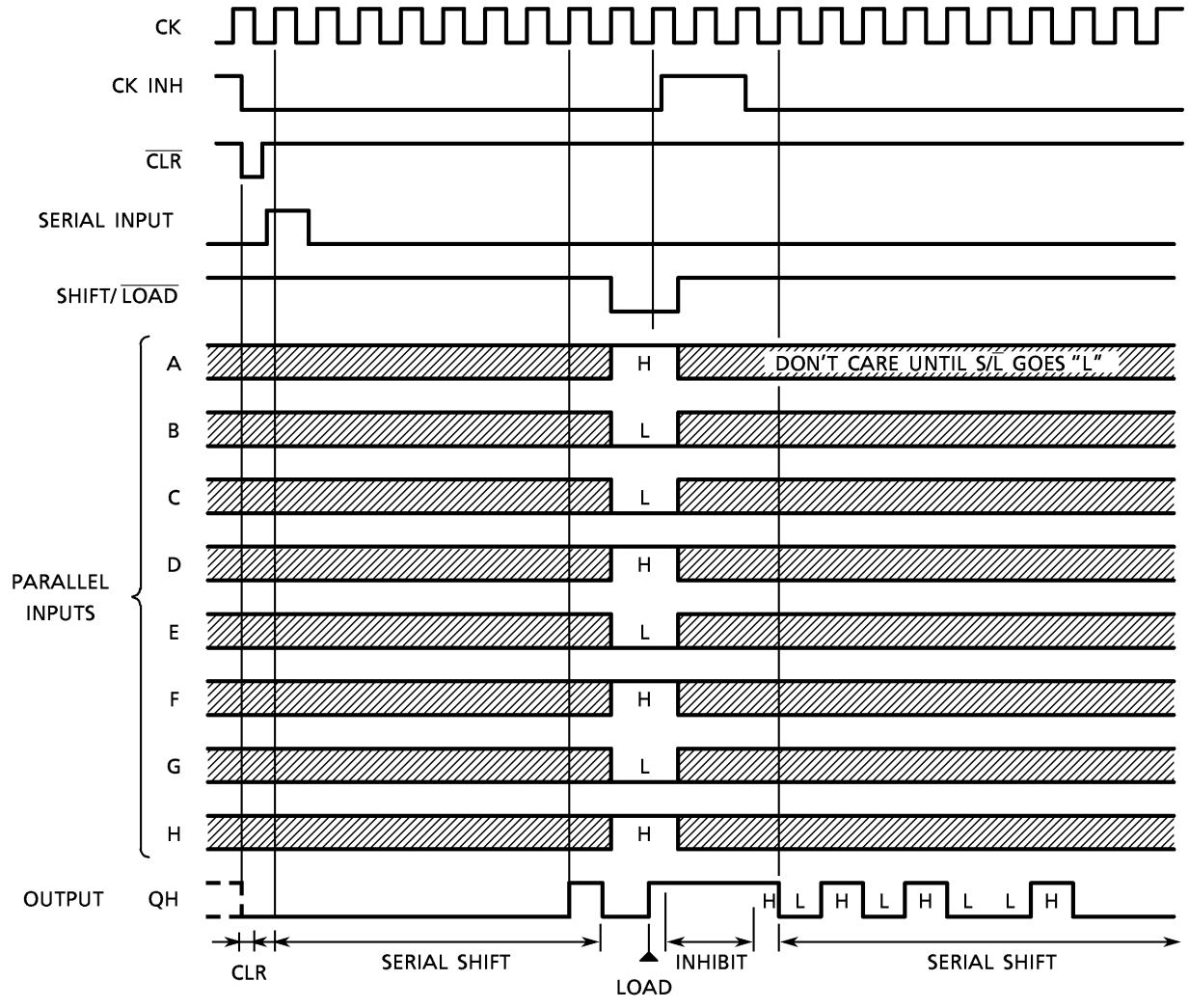
TRUTH TABLE

INPUTS						INTERNAL OUTPUTS	OUTPUT
$\overline{CLR}$	SHIFT/ $\overline{LOAD}$	CK INH.	CK	SERIAL IN	PARALLEL A ····· H	QA QB	QH
L	X	X	X	X	X	L L	L
H	X	X	↓	X	X	NO CHANGE	
H	L	L	↑	X	a ····· h	a b	h
H	H	L	↑	H	X	H QAn	QGn
H	H	L	↑	L	X	L QAn	QGn
H	X	H	X	X	X	NO CHANGE	

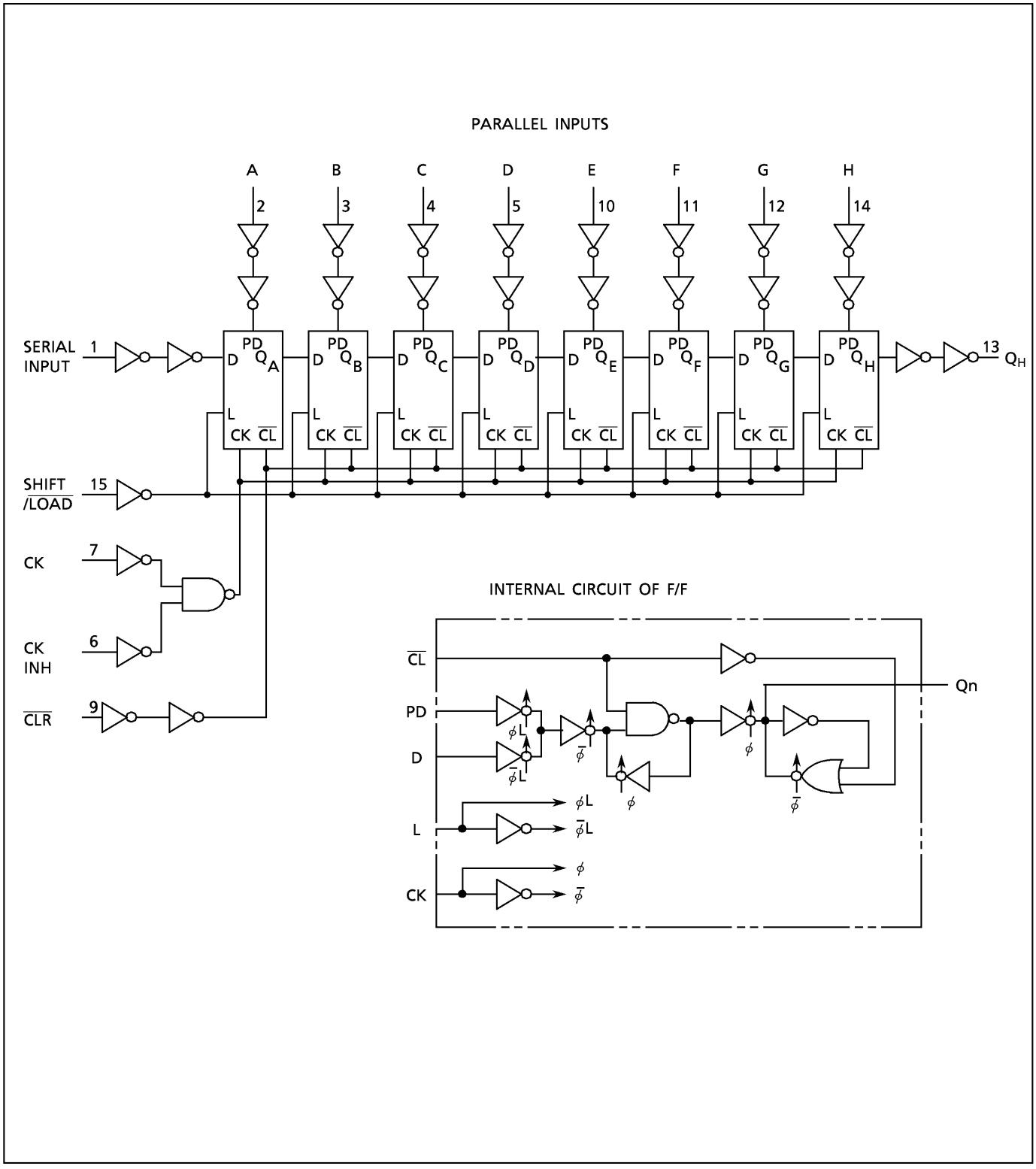
X : Don't Care

a ····· h : The level of steady state input voltage at inputs A through H respectively

TIMING CHART



SYSTEM DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5~7	V
DC Input Voltage	V_{IN}	−0.5~V_{CC} + 0.5	V
DC Output Voltage	V_{OUT}	−0.5~V_{CC} + 0.5	V
Input Diode Current	I_{IK}	± 20	mA
Output Diode Current	I_{OK}	± 20	mA
DC Output Current	I_{OUT}	± 25	mA
DC V_{CC} / Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	T_{stg}	−65~150	°C

*500mW in the range of Ta = −40°C~65°C. From Ta = 65°C to 85 °C a derating factor of −10mW/ °C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2~6	V
Input Voltage	V_{IN}	0~V_{CC}	V
Output Voltage	V_{OUT}	0~V_{CC}	V
Operating Temperature	T_{opr}	−40~85	°C
Input Rise and Fall Time	t_r, t_f	0~ 1000 (V_{CC} = 2.0V) 0~ 500 (V_{CC} = 4.5V) 0~ 400 (V_{CC} = 6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC} (V)	Ta = 25°C MIN.	Ta = 25°C TYP.	Ta = 25°C MAX.	Ta = −40~85°C MIN.	Ta = −40~85°C MAX.	UNIT
High - Level Input Voltage	V_{IH}			2.0 4.5 6.0	1.50 3.15 4.20	− − −	− − −	1.50 3.15 4.20	− − −	V
Low - Level Input Voltage	V_{IL}			2.0 4.5 6.0	− − −	− − −	0.50 1.35 1.80	− − −	0.50 1.35 1.80	V
High - Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −20μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	− − −	1.9 4.4 5.9	− − −	V
			I_{OH} = −4 mA I_{OH} = −5.2mA	4.5 6.0	4.18 5.68	4.31 5.80	− −	4.13 5.63	− −	
Low - Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20μA	2.0 4.5 6.0	− − −	0.0 0.0 0.0	0.1 0.1 0.1	− − −	0.1 0.1 0.1	V
			I_{OL} = 4 mA I_{OL} = 5.2mA	4.5 6.0	− −	0.17 0.18	0.26 0.26	− −	0.33 0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	−	−	± 0.1	−	± 1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	−	−	4.0	−	40.0	

TIMING REQUIREMENTS (Input $t_r = t_f = 6ns$)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C		Ta = −40~85°C	UNIT
			V_{CC} (V)	TYP.	LIMIT	LIMIT	
Minimum Pulse Width (CK)	$t_{W(H)}$ $t_{W(L)}$		2.0 4.5 6.0	— — —	75 15 13	95 19 16	ns
Minimum Pulse Width ($\overline{CLR}$)	$t_{W(L)}$		2.0 4.5 6.0	— — —	75 15 13	95 19 16	
Minimum Set−up Time (SI, PI)	t_s		2.0 4.5 6.0	— — —	75 15 13	95 19 16	
Minimum Set−up Time (S/$\overline{L}$)	t_s		2.0 4.5 6.0	— — —	75 15 13	95 19 16	
Minimum Hold Time (SI, PI)	t_h		2.0 4.5 6.0	— — —	0 0 0	0 0 0	
Minimum Hold Time (S/$\overline{L}$)	t_h		2.0 4.5 6.0	— — —	0 0 0	0 0 0	
Minimum Removal Time ($\overline{CLR}$)	t_{rem}		2.0 4.5 6.0	— — —	50 10 9	65 13 11	
Clock Frequency	f		2.0 4.5 6.0	— — —	6 31 36	5 25 29	MHz

AC ELECTRICAL CHARACTERISTICS ($C_L = 15pF$, $V_{CC} = 5V$, Ta = 25°C, Input $t_r = t_f = 6ns$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		—	4	8	ns
Propagation Delay Time (CK−QH)	t_{pLH} t_{pHL}		—	16	26	
Propagation Delay Time ($\overline{CLR}$−QH)	t_{pHL}		—	15	24	
Maximum Clock Frequency	f_{MAX}		33	57	—	MHz

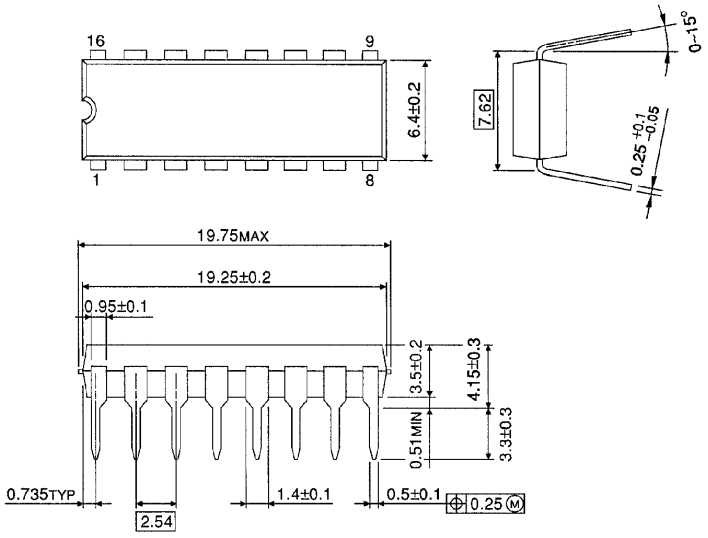
AC ELECTRICAL CHARACTERISTICS (C_L = 50pF, Input $t_r = t_f$ = 6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta = 25°C			Ta = −40~85°C		UNIT
			V_{CC} (V)	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0 4.5 6.0	— — —	30 8 7	75 15 13	— — —	95 19 16	ns
Propagation Delay Time (CK−QH)	t_{pLH} t_{pHL}		2.0 4.5 6.0	— — —	70 20 16	150 30 26	— — —	190 38 32	
Propagation Delay Time ($\overline{CLR}$−QH)	t_{pHL}		2.0 4.5 6.0	— — —	60 18 14	135 27 23	— — —	170 34 29	
Maximum Clock Frequency	f_{MAX}		2.0 4.5 6.0	6 31 36	14 50 63	— — —	5 25 29	— — —	MHz
Input Capacitance	C_{IN}			—	5	10	—	10	pF
Power Dissipation Capacitance	C_{PD} (1)			—	60	—	—	—	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

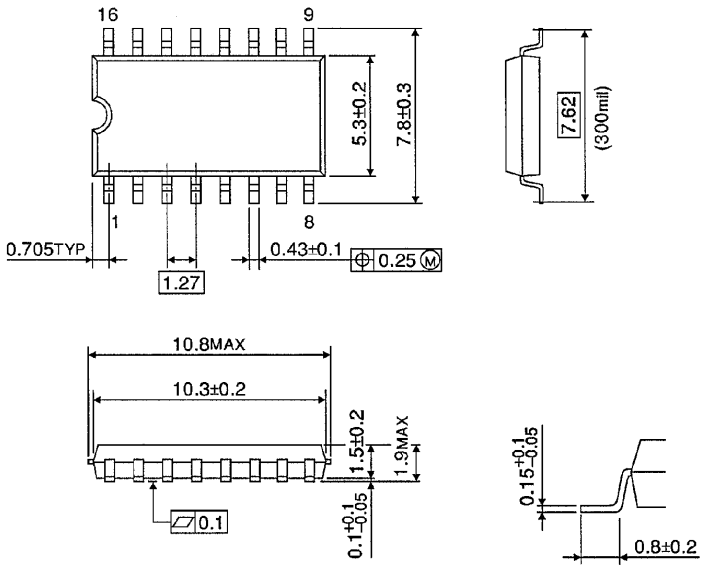
$$I_{CC}(opr) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

DIP 16PIN PACKAGE DIMENSIONS (DIP16-P-300-2.54A) Unit in mm



Weight : 1.00g (Typ.)

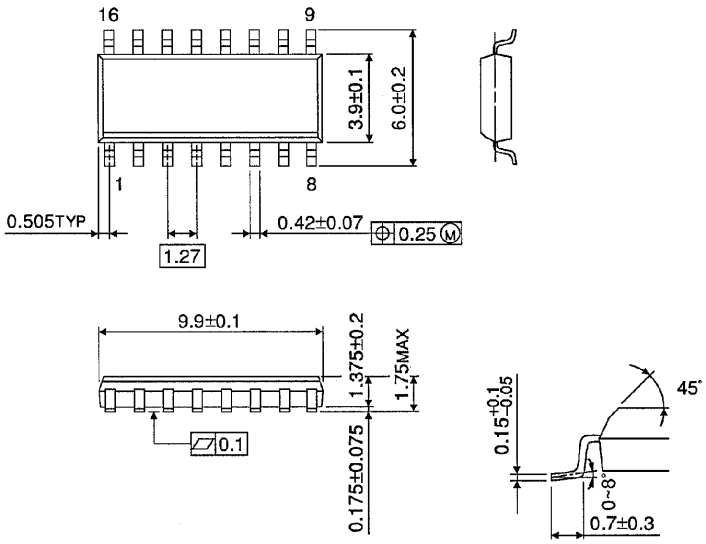
SOP 16PIN (200mil BODY) PACKAGE DIMENSIONS (SOP16-P-300-1.27) Unit in mm



Weight : 0.18g (Typ.)

SOP 16PIN (150mil BODY) PACKAGE DIMENSIONS (SOL16-P-150 -1.27) Unit in mm

(Note) This package is not available in Japan.



Weight : 0.13g (Typ.)

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