4-Kb Microwire Serial CMOS EEPROM

FEATURES

- **High speed operation: 2MHz**
- **1.8V to 5.5V supply voltage range**
- **Selectable x8 or x16 memory organization**
- **Sequential read**
- **Software write protection**
- **Power-up inadvertant write protection**
- **Low power CMOS technology**
- **1,000,000 Program/erase cycles**
- **100 year data retention**
- **Industrial temperature ranges**
- **RoHS-compliant 8-pin PDIP, SOIC, TSSOP and 8-pad TDFN packages**

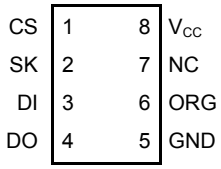
DESCRIPTION

The CAT93C66 is a 4-Kb CMOS Serial EEPROM device which is organized as either 256 registers of 16 bits (ORG pin at V_{CC}) or 512 registers of 8 bits (ORG pin at GND). Each register can be written (or read) serially by using the DI (or DO) pin. The CAT93C66 features sequential read and self-timed internal write with auto-clear. On-chip Power-On Reset circuitry protects the internal logic against powering up in the wrong state.

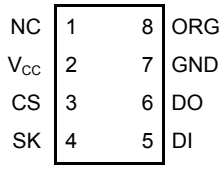
For Ordering Information details, see page 15.

PIN CONFIGURATION

PDIP (L)
SOIC (V, X)
TSSOP (Y)
TDFN (VP2, ZD4)*

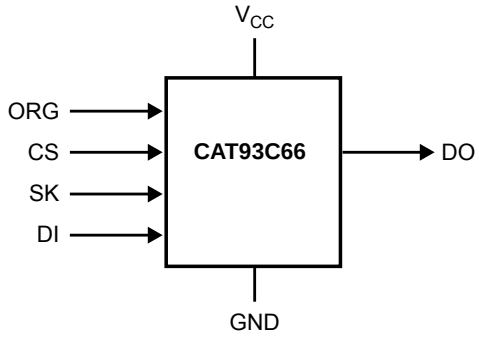


SOIC (W)



* TDFN 3x3mm (ZD4) package is available only for Die Rev E (not recommended for new designs)

FUNCTIONAL SYMBOL



PIN FUNCTION

Pin Name	Function
CS	Chip Select
SK	Clock Input
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	Power Supply
GND	Ground
ORG	Memory Organization
NC	No Connection

Note: When the ORG pin is connected to VCC, the x16 organization is selected. When it is connected to ground, the x8 organization is selected. If the ORG pin is left unconnected, then an internal pullup device will select the x16 organization

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ABSOLUTE MAXIMUM RATINGS[1]

Parameters	Ratings	Units
Storage Temperature	-65 to +150	°C
Voltage on Any Pin with Respect to Ground[2]	-0.5 to +6.5	V

RELIABILITY CHARACTERISTICS[3]

Symbol	Parameter	Min	Units
NEND[4]	Endurance	1,000,000	Program/ Erase Cycles
TDR	Data Retention	100	Years

D.C. OPERATING CHARACTERISTICS (NEW PRODUCT, DIE REV. G)

V_{CC} = +1.8V to +5.5V, T_A=-40°C to +85°C unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Max	Units
I_{CC1}	Power Supply Current (Write)	f_{SK} = 1MHz, V_{CC} = 5.0V		1	mA
I_{CC2}	Power Supply Current (Read)	f_{SK} = 1MHz, V_{CC} = 5.0V		500	µA
I_{SB1}	Power Supply Current (Standby) (x8 Mode)	V_{IN} = GND or V_{CC}, CS = GND ORG = GND		2	µA
I_{SB2}	Power Supply Current (Standby) (x16 Mode)	V_{IN} = GND or V_{CC}, CS = GND ORG = Float or V_{CC}		1	µA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}		1	µA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}, CS = GND		1	µA
V_{IL1}	Input Low Voltage	4.5V ≤ V_{CC} < 5.5V	-0.1	0.8	V
V_{IH1}	Input High Voltage	4.5V ≤ V_{CC} < 5.5V	2	V_{CC} + 1	V
V_{IL2}	Input Low Voltage	1.8V ≤ V_{CC} < 4.5V	0	V_{CC} x 0.2	V
V_{IH2}	Input High Voltage	1.8V ≤ V_{CC} < 4.5V	V_{CC} x 0.7	V_{CC} + 1	V
V_{OL1}	Output Low Voltage	4.5V ≤ V_{CC} < 5.5V, I_{OL} = 2.1mA		0.4	V
V_{OH1}	Output High Voltage	4.5V ≤ V_{CC} < 5.5V, I_{OH} = -400µA	2.4		V
V_{OL2}	Output Low Voltage	1.8V ≤ V_{CC} < 4.5V, I_{OL} = 1mA		0.2	V
V_{OH2}	Output High Voltage	1.8V ≤ V_{CC} < 4.5V, I_{OH} = -100µA	V_{CC} - 0.2		V

Notes:

(1) Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

(2) The DC input voltage on any pin should not be lower than -0.5V or higher than V_{CC} + 0.5V. During transitions, the voltage on any pin may undershoot to no less than -1.5V or overshoot to no more than V_{CC} + 1.5V, for periods of less than 20 ns.

(3) These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.

(4) Block Mode, V_{CC} = 5V, 25°C

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D.C. OPERATING CHARACTERISTICS (MATURE PRODUCT, DIE REV. E – Not Recommended for New Designs)

V_{CC} = +1.8V to +5.5V, unless otherwise specified.

Symbol	Parameter	Test Conditions	Min	Max	Units
I_{CC1}	Power Supply Current (Write)	f_{SK} = 1MHz, V_{CC} = 5.0V		3	mA
I_{CC2}	Power Supply Current (Read)	f_{SK} = 1MHz, V_{CC} = 5.0V		500	µA
I_{SB1}	Power Supply Current (Standby) (x8 Mode)	V_{IN} = GND or V_{CC}, CS = GND ORG = GND		10	µA
I_{SB2}	Power Supply Current (Standby) (x16 Mode)	V_{IN} = GND or V_{CC}, CS = GND ORG = Float or V_{CC}		10	µA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}		1	µA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}, CS = GND		1	µA
V_{IL1}	Input Low Voltage	4.5V ≤ V_{CC} < 5.5V	-0.1	0.8	V
V_{IH1}	Input High Voltage	4.5V ≤ V_{CC} < 5.5V	2	V_{CC} + 1	V
V_{IL2}	Input Low Voltage	1.8V ≤ V_{CC} < 4.5V	0	V_{CC} x 0.2	V
V_{IH2}	Input High Voltage	1.8V ≤ V_{CC} < 4.5V	V_{CC} x 0.7	V_{CC} + 1	V
V_{OL1}	Output Low Voltage	4.5V ≤ V_{CC} < 5.5V, I_{OL} = 2.1mA		0.4	V
V_{OH1}	Output High Voltage	4.5V ≤ V_{CC} < 5.5V, I_{OH} = -400µA	2.4		V
V_{OL2}	Output Low Voltage	1.8V ≤ V_{CC} < 4.5V, I_{OL} = 1mA		0.2	V
V_{OH2}	Output High Voltage	1.8V ≤ V_{CC} < 4.5V, I_{OH} = -100µA	V_{CC} - 0.2		V

PIN CAPACITANCE

T_A = 25°C, f = 1MHz, V_{CC} = 5V

Symbol	Test	Conditions	Min	Typ	Max	Units
C_{OUT}(1)	Output Capacitance (DO)	V_{OUT} = 0V			5	pF
C_{IN}(1)	Input Capacitance (CS, SK, DI, ORG)	V_{IN} = 0V			5	pF

Notes:

(1) These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.

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A.C. CHARACTERISTICS[1] (NEW PRODUCT, DIE REV. G)

V_{CC} = +1.8V to +5.5V, T_A = -40°C to +85°C, unless otherwise specified.

Symbol	Parameter	Limits		Units
		Min	Max	
t_{CSS}	CS Setup Time	50		ns
t_{CSH}	CS Hold Time	0		ns
t_{DIS}	DI Setup Time	100		ns
t_{DIH}	DI Hold Time	100		ns
t_{PD1}	Output Delay to 1		0.25	µs
t_{PD0}	Output Delay to 0		0.25	µs
t_{HZ}[2]	Output Delay to High-Z		100	ns
t_{EW}	Program/Erase Pulse Width		5	ms
t_{CSMIN}	Minimum CS Low Time	0.25		µs
t_{SKHI}	Minimum SK High Time	0.25		µs
t_{SKLOW}	Minimum SK Low Time	0.25		µs
t_{SV}	Output Delay to Status Valid		0.25	µs
SK_{MAX}	Maximum Clock Frequency	DC	2000	kHz

A.C. CHARACTERISTICS [1] (MATURE PRODUCT, DIE REV E – Not Recommended for New Design)

Symbol	Parameter	Limits						Units
		V_{CC} = 1.8V - 5.5V		V_{CC} = 2.5V - 5.5V		V_{CC} = 4.5V - 5.5V		
		Min	Max	Min	Max	Min	Max	
t_{CSS}	CS Setup Time	200		100		50		ns
t_{CSH}	CS Hold Time	0		0		0		ns
t_{DIS}	DI Setup Time	400		200		100		ns
t_{DIH}	DI Hold Time	400		200		100		ns
t_{PD1}	Output Delay to 1		1		0.5		0.25	µs
t_{PD0}	Output Delay to 0		1		0.5		0.25	µs
t_{HZ}[2]	Output Delay to High-Z		400		200		100	ns
t_{EW}	Program/Erase Pulse Width		10		10		10	ms
t_{CSMIN}	Minimum CS Low Time	1		0.5		0.25		µs
t_{SKHI}	Minimum SK High Time	1		0.5		0.25		µs
t_{SKLOW}	Minimum SK Low Time	1		0.5		0.25		µs
t_{SV}	Output Delay to Status Valid		1		0.5		0.25	µs
SK_{MAX}	Maximum Clock Frequency	DC	250	DC	500	DC	1000	kHz

Notes:

(1) Test conditions according to "A.C. Test Conditions" table.

(2) These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.

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POWER-UP TIMING[1] [2]

Symbol	Parameter	Max	Units
t_{PUR}	Power-up to Read Operation	1	ms
t_{PUW}	Power-up to Write Operation	1	ms

Notes:

(1) These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC-Q100 and JEDEC test methods.

(2) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated.

A.C. TEST CONDITIONS

Input Rise and Fall Times	≤ 50 ns	
Input Pulse Voltages	0.4V to 2.4V	4.5V ≤ V_{CC} ≤ 5.5V
Timing Reference Voltages	0.8V, 2.0V	4.5V ≤ V_{CC} ≤ 5.5V
Input Pulse Voltages	0.2V_{CC} to 0.7V_{CC}	1.8V ≤ V_{CC} ≤ 4.5V
Timing Reference Voltages	0.5V_{CC}	1.8V ≤ V_{CC} ≤ 4.5V
Output Load	Current Source I_{OLmax}/I_{OHmax}; CL=100pF	

DEVICE OPERATION

The CAT93C66 is a 4096-bit nonvolatile memory intended for use with industry standard micropro–cessors. The CAT93C66 can be organized as either registers of 16 bits or 8 bits. When organized as X16, seven 11-bit instructions control the reading, writing and erase operations of the device. When organized as X8, seven 12-bit instructions control the reading, writing and erase operations of the device. The CAT93C66 operates on a single power supply and will generate on chip, the high voltage required during any write operation.

Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the ready/busy status after a write operation. The serial communication protocol follows the timing shown in Figure 1.

The ready/busy status can be determined after the start of internal write cycle by selecting the device (CS high) and polling the DO pin; DO low indicates that the write operation is not completed, while DO high indicates that the device is ready for the next instruction. If necessary, the DO pin may be placed back into a high impedance state during chip select by shifting a dummy “1” into the DI pin. The DO pin will enter the high impedance state on the rising edge of the clock (SK). Placing the DO pin into the high impedance state is recommended in applications where the DI pin and the DO pin are to be tied together to form a common DI/O pin.

The format for all instructions sent to the device is a logical “1” start bit, a 2-bit (or 4-bit) opcode, 8-bit address (an additional bit when organized X8) and for write operations a 16-bit data field (8-bit for X8 organizations). The instruction format is shown in Instruction Set table.

INSTRUCTION SET

Instruction	Start Bit	Opcode	Address		Data		Comments
			x8	x16	x8	x16	
READ	1	10	A8-A0	A7-A0			Read Address AN – A0
ERASE	1	11	A8-A0	A7-A0			Clear Address AN – A0
WRITE	1	01	A8-A0	A7-A0	D7-D0	D15-D0	Write Address AN – A0
EWEN	1	00	11XXXXXX	11XXXXX			Write Enable
EWDS	1	00	00XXXXXX	00XXXXX			Write Disable
ERAL	1	00	10XXXXXX	10XXXXX			Clear All Addresses
WRAL	1	00	01XXXXXX	01XXXXX	D7-D0	D15-D0	Write All Addresses

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Read

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the CAT93C66 will come out of the high impedance state and, after sending an initial dummy zero bit, will begin shifting out the data addressed (MSB first). The output data bits will toggle on the rising edge of the SK clock and are stable after the specified time delay (t_{PD0} or t_{PD1}).

For the CAT93C66, after the initial data word has been shifted out and CS remains asserted with the SK clock continuing to toggle, the device will automatically increment to the next address and shift out the next data word in a sequential READ mode. As long as CS is continuously asserted and SK continues to toggle, the device will keep incrementing to the next address automatically until it reaches to the end of the address space, then loops back to address 0. In the sequential READ mode, only the initial data word is preceeded by a dummy zero bit. All subsequent data words will follow without a dummy zero bit. The READ instruction timing is illustrated in Figure 2.

Erase/Write Enable and Disable

The CAT93C66 powers up in the write disable state. Any writing after power-up or after an EWDS (erase/write disable) instruction must first be preceded by the EWEN (erase/write enable) instruction. Once the write instruction is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all CAT93C66 write and erase instructions, and will prevent any accidental writing or clearing of the device. Data can be read normally from the device regardless of the write enable/disable status. The EWEN and EWDS instructions timing is shown in Figure 3.

Figure 1. Sychronous Data Timing

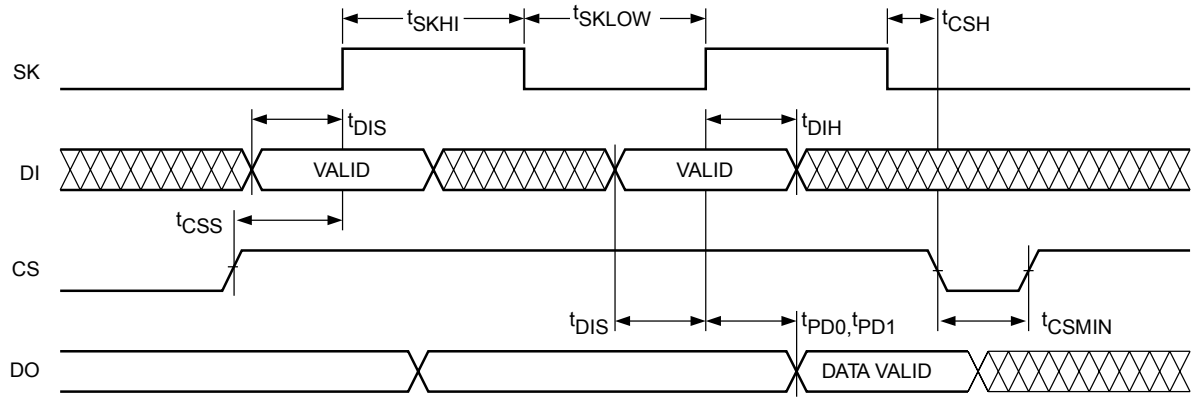
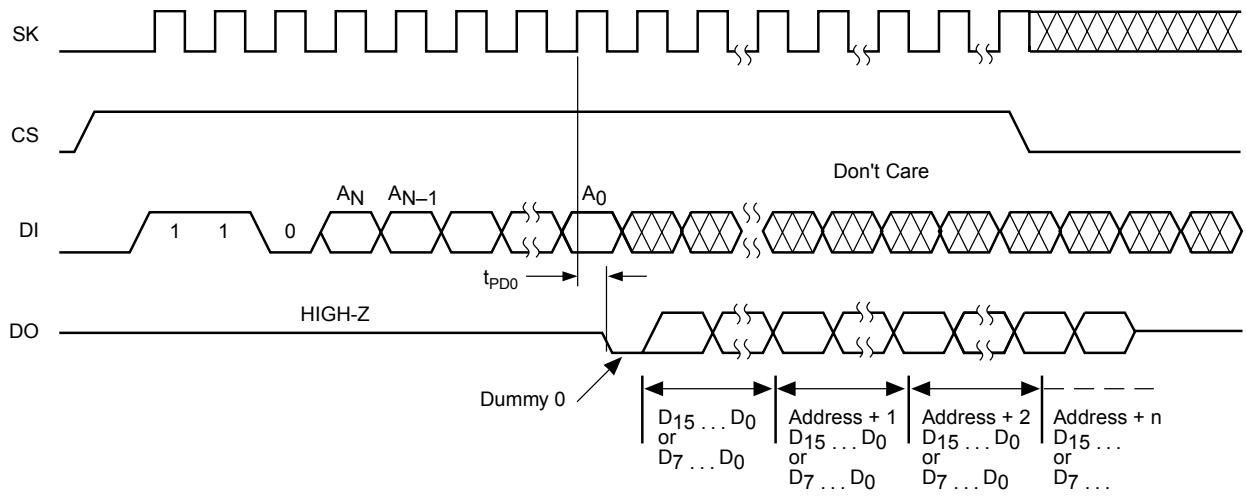


Figure 2. READ Instruction Timing



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Write

After receiving a WRITE command (Figure 4), address and the data, the CS (Chip Select) pin must be deselected for a minimum of t_{CSMIN}. The falling edge of CS will start the self clocking clear and data store cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C66 can be determined by selecting the device and polling the DO pin. Since this device features Auto-Clear before write, it is NOT necessary to erase a memory location before it is written into.

Erase

Upon receiving an ERASE command and address, the CS (Chip Select) pin must be deasserted for a minimum of t_{CSMIN} (Figure 5). The falling edge of CS will start the self clocking clear cycle of the selected memory location. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/ busy status of the CAT93C66 can be determined by selecting the device and polling the DO pin. Once cleared, the content of a cleared location returns to a logical “1” state.

Figure 3. EWEN/EWDS Instruction Timing

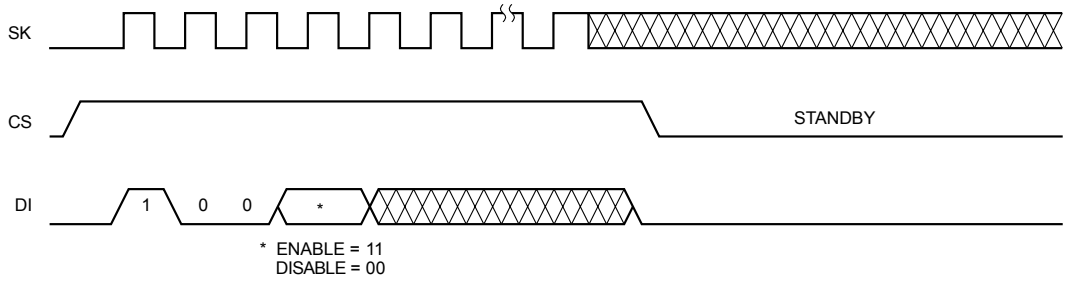


Figure 4. Write Instruction Timing

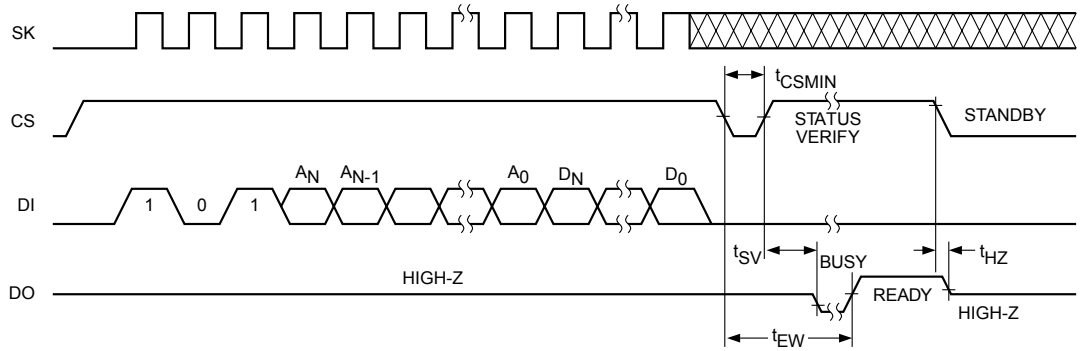
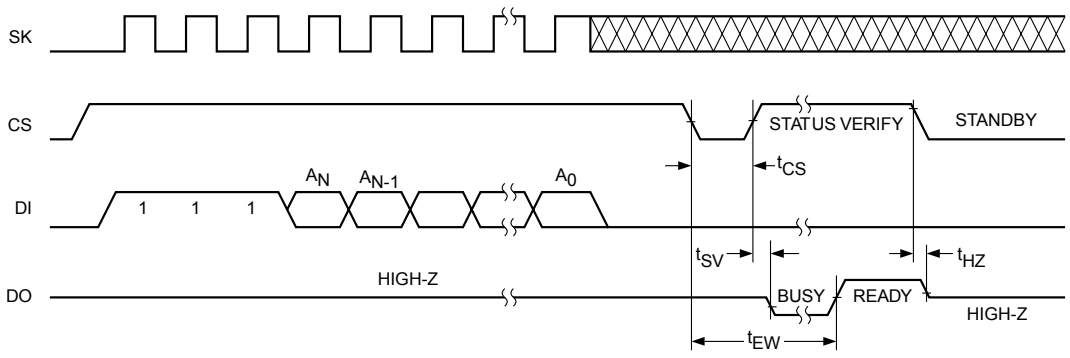


Figure 5. Erase Instruction Timing



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Erase All

Upon receiving an ERAL command (Figure 6), the CS (Chip Select) pin must be deselected for a minimum of t_{CSMIN}. The falling edge of CS will start the self clocking clear cycle of all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C66 can be determined by selecting the device and polling the DO pin. Once cleared, the contents of all memory bits return to a logical “1” state.

Write All

Upon receiving a WRAL command and data, the CS (Chip Select) pin must be deselected for a minimum of t_{CSMIN} (Figure 7). The falling edge of CS will start the self clocking data write to all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C66 can be determined by selecting the device and polling the DO pin. It is not necessary for all memory locations to be cleared before the WRAL command is executed.

Figure 6. ERAL Instruction Timing

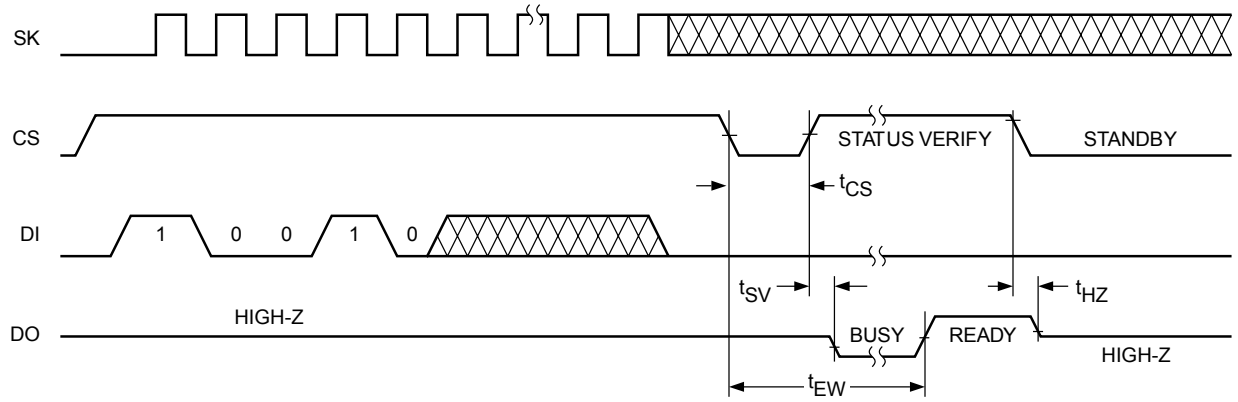
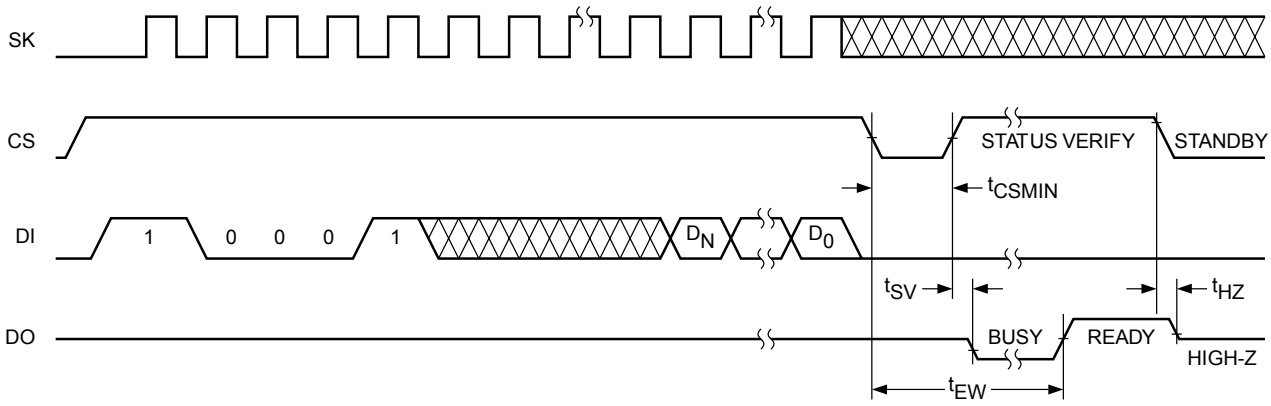


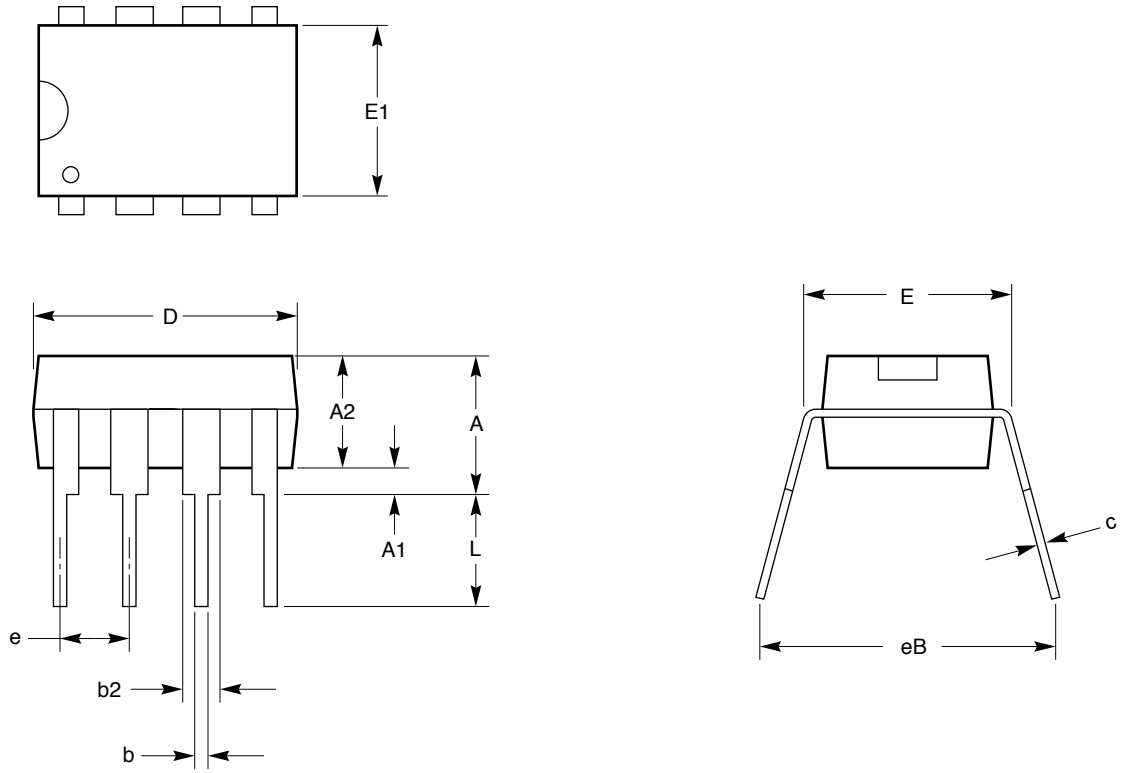
Figure 7. WRAL Instruction Timing



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PACKAGE OUTLINES

8-LEAD 300MIL WIDE PLASTIC DIP (L)



SYMBOL	MIN	NOM	MAX
A			4.57
A1	0.38		
A2	3.05		3.81
b	0.36	0.46	0.56
b2	1.14		1.77
c	0.21	0.26	0.35
D	9.02		10.16
E	7.62	7.87	8.25
E1	6.09	6.35	7.11
e		2.54 BSC	
eB	7.87		9.65
L	2.92		3.81

For current Tape and Reel information, download the PDF file from: http://www.catsemi.com/documents/tapeandreel.pdf.

Notes:

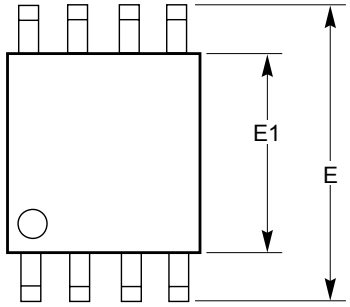
(1) All dimensions are in millimeters.

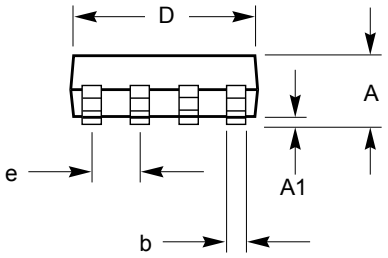
(2) Complies with JEDEC specification MS001

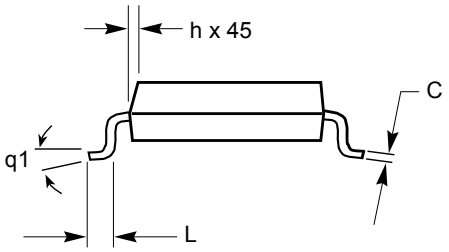
(3) Dimensioning and tolerancing per ANSI Y14.5M-1982.

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8-LEAD 150 MIL SOIC (V, W)







SYMBOL	MIN	NOM	MAX
A1	0.10		0.25
A	1.35		1.75
b	0.33		0.51
C	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e		1.27 BSC	
h	0.25		0.50
L	0.40		1.27
q1	0°		8°

For current Tape and Reel information, download the PDF file from: http://www.catsemi.com/documents/tapeandreel.pdf.

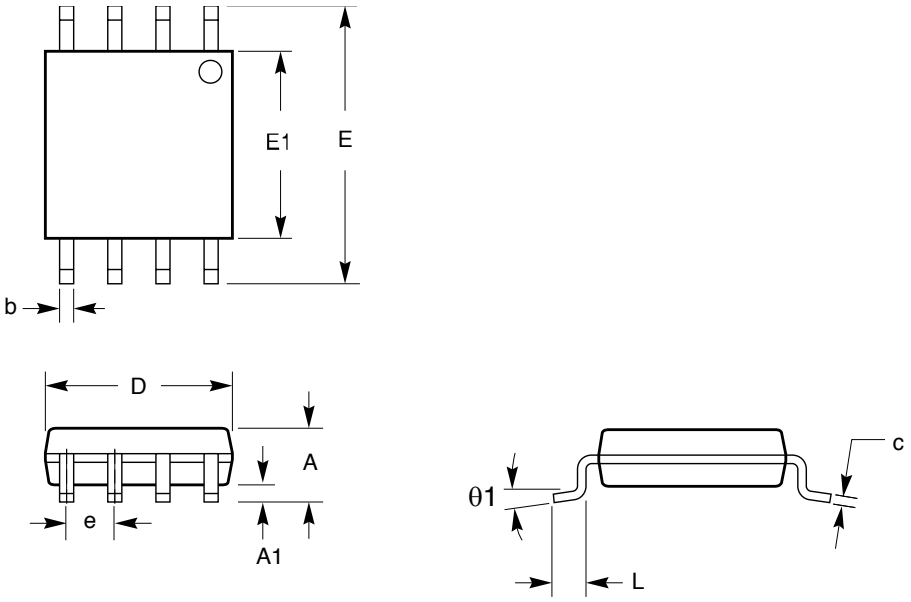
Notes:

(1) All dimensions are in millimeters.

(2) Complies with JEDEC specification MS-012.

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8-LEAD 208 MIL SOIC (X)



SYMBOL	MIN	NOM	MAX
A1	0.05		0.25
A			2.03
b	0.36		0.48
c	0.19		0.25
D	5.13		5.33
E	7.75		8.26
E1	5.13		5.38
e		1.27 BSC	
L	0.51		0.76
θ1	0°		8°

For current Tape and Reel information, download the PDF file from: http://www.catsemi.com/documents/tapeandreel.pdf.

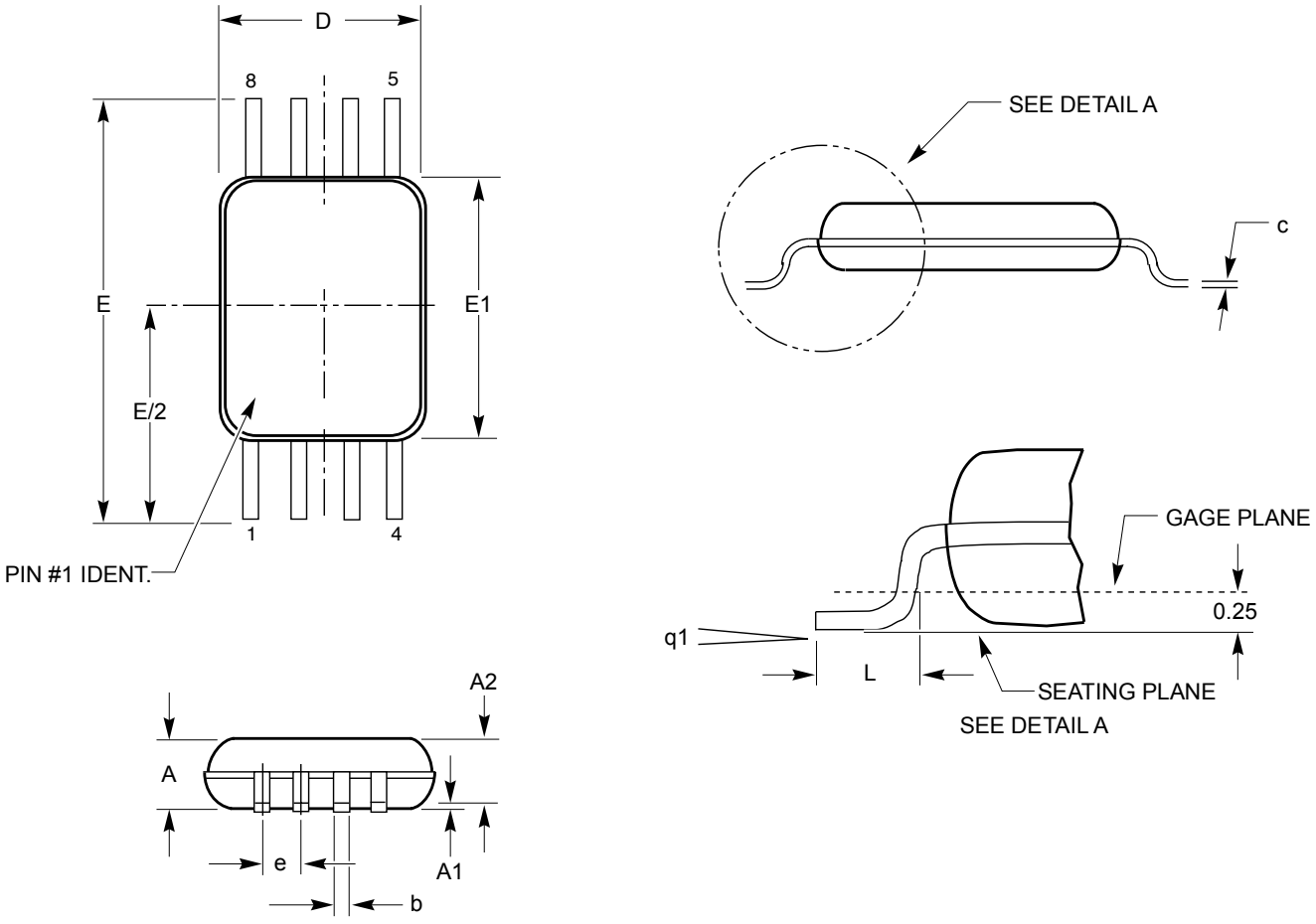
Notes:

(1) All dimensions are in millimeters.

(2) Complies with EIAJ specification EDR-7320.

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8-LEAD TSSOP (Y)



SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80	0.90	1.05
b	0.19		0.30
c	0.09		0.20
D	2.90	3.00	3.10
E	6.30	6.4	6.50
E1	4.30	4.40	4.50
e		0.65 BSC	
L	0.50	0.60	0.75
q1	0.00		8.00

For current Tape and Reel information, download the PDF file from: http://www.catsemi.com/documents/tapeandreel.pdf.

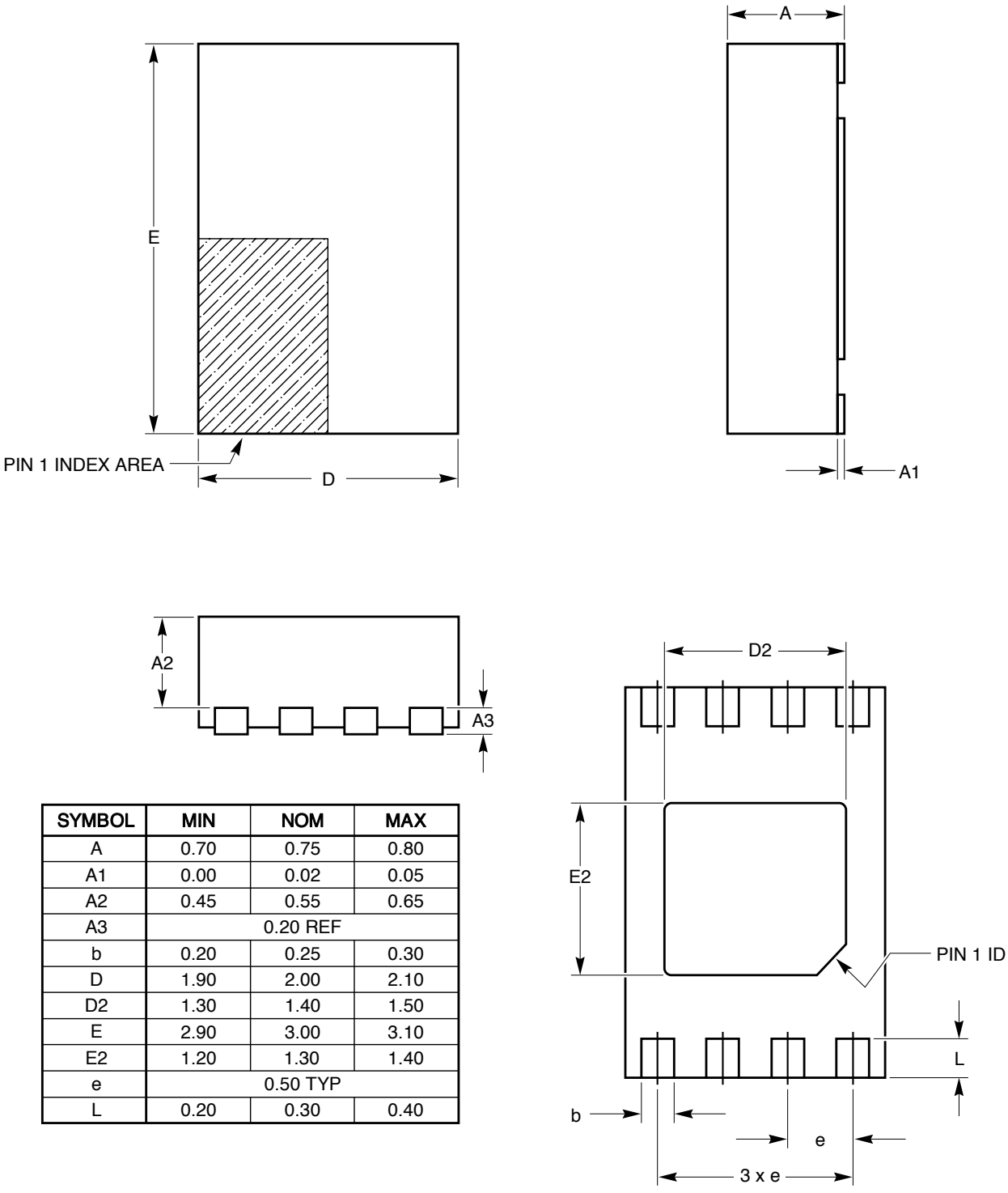
Notes:

(1) All dimensions are in millimeters.

(2) Complies with JEDEC Standard MO-153

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8-PAD TDFN 2X3 PACKAGE (VP2)



SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.45	0.55	0.65
A3		0.20 REF	
b	0.20	0.25	0.30
D	1.90	2.00	2.10
D2	1.30	1.40	1.50
E	2.90	3.00	3.10
E2	1.20	1.30	1.40
e		0.50 TYP	
L	0.20	0.30	0.40

For current Tape and Reel information, download the PDF file from: http://www.catsemi.com/documents/tapeandreel.pdf.

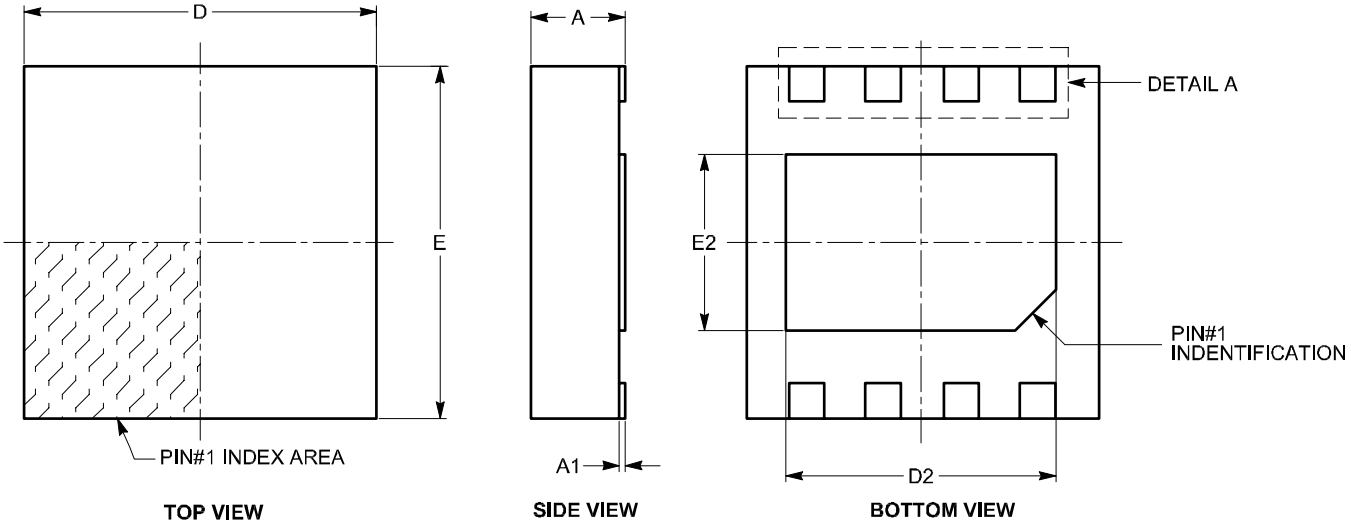
Notes:

(1) All dimensions are in millimeters.

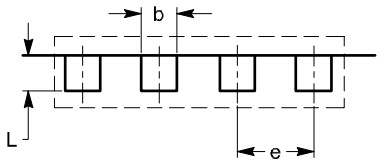
(2) Complies with JEDEC specification MO-229.

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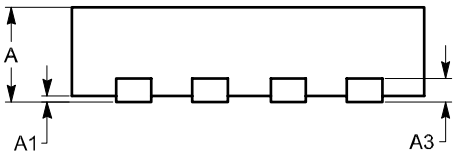
8-PAD TDFN 3X3 PACKAGE (ZD4)



SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.50	0.55	0.60
A3		0.20 REF	
b	0.23	0.30	0.37
D	2.90	3.00	3.10
D2	2.20	2.30	2.40
E	2.90	3.00	3.10
E2	1.40	1.50	1.60
e		0.65 TYP	
L	0.20	0.30	0.40



DETAIL A



FRONT VIEW

For current Tape and Reel information, download the PDF file from: http://www.catsemi.com/documents/tapeandreel.pdf.

Notes:

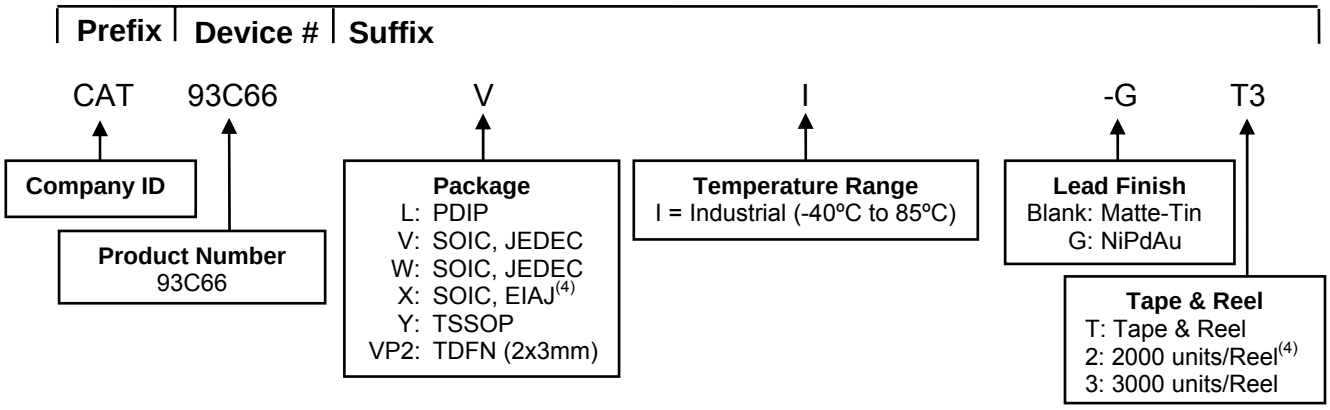
(1) All dimensions are in millimeters.

(2) Complies with JEDEC specification MO-229.

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ORDERING INFORMATION

CAT93C66, DIE REV. G (NEW PRODUCT)*



Notes:

(1) All packages are RoHS-compliant (Lead-free, Halogen-free).

(2) The standard lead finish is NiPdAu.

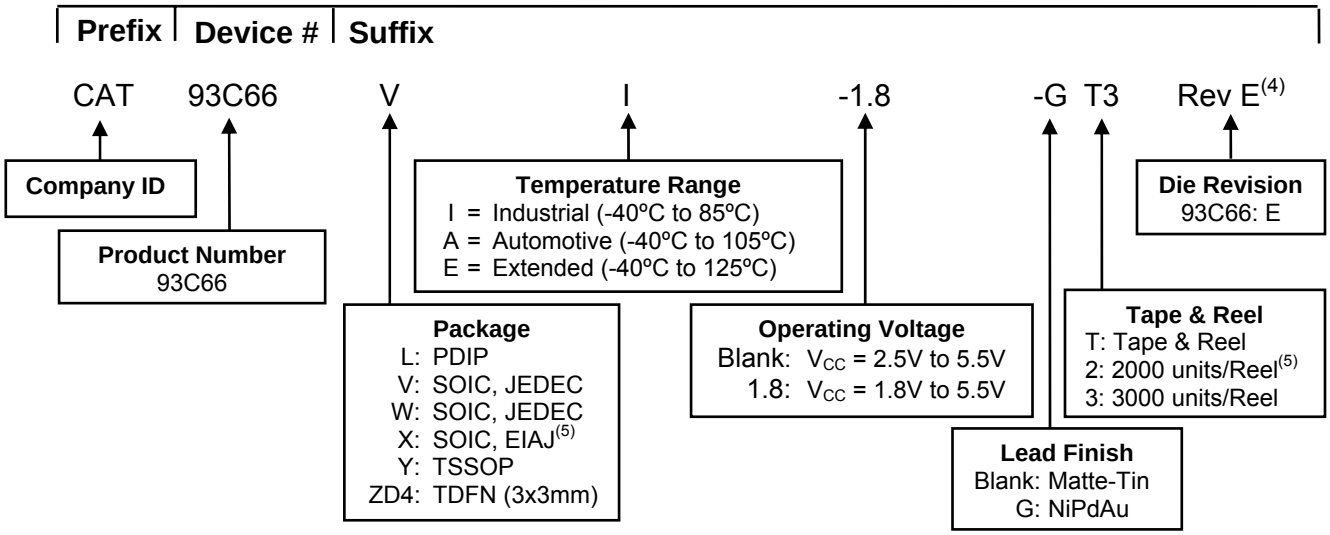
(3) The device used in the above example is a CAT93C66VI-GT3 (SOIC, Industrial Temperature, NiPdAu, Tape & Reel).

(4) For SOIC, EIAJ (X) package the standard lead finish is Matte-Tin. This package is available in 2000 pcs/reel, i.e. CAT93C66XI-T2.

(5) For additional package and temperature options, please contact your nearest Catalyst Semiconductor Sales office.

* For CAT93C66, Die Rev. G (all packages) availability, please contact factory.

CAT93C66, DIE REV. E, MATURE PRODUCT (Not Recommended for New Design)



Notes:

(1) All packages are RoHS-compliant (Lead-free, Halogen-free).

(2) The standard finish is NiPdAu.

(3) The device used in the above example is a CAT93C66VI-1.8-GT3 (SOIC green package, Industrial Temperature, 1.8 Volt to 5.5 Volt Operating Voltage, NiPdAu finish, Tape & Reel.)

(4) Product die revision letter is marked on top of the package as a suffix to the production date code (e.g., AYWWE.) For additional information, please contact your Catalyst sales office.

(5) For SOIC, EIAJ (X) package the standard lead finish is Matte-Tin. This package is available in 2000 pcs/reel, i.e. CAT93C66XI-T2.

(6) For additional package and temperature options, please contact your nearest Catalyst Semiconductor Sales office.

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REVISION HISTORY

Date	Rev.	Comments
05/14/04	L	New Data Sheet Created From CAT93C46/56/57/66/86. Parts CAT93C56, CAT93C56, CAT93C57, CAT93C66, CAT93C76 and CAT93C86 have been separated into single data sheets Add Die Revision ID Letter Update Features Update Description Update Pin Condition Add Functional Diagram Update Pin Function Update D.C. Operating Characteristics Update Pin Capacitance Update Instruction Set Update Device Operation Update Ordering Information Update Revision History Update Rev Number
10/13/06	M	Update Features Update Pin Configuration / Packages Update Functional Symbol Update Pin Functions Update D.C. Operating Characteristics (V_{CC} Range) Add Package Drawings Update Example of Ordering Information
11/17/06	N	Remove "Die Rev E" from the title Update Pin Configuration / Packages Update Absolute Maximum Rating Update Reliability Characteristics Update D.C. Operating Characteristics Added A.C. Characteristics for Die Rev G Rearrange / Format Text and Figures Added Example of Ordering Information for Die Rev G
12/07/06	O	Update separate DC Characteristics for Die Rev. G and Die Rev. E. Updated Example of Ordering Information
04/03/07	P	Update note on page 1 Update D.C. Operating Characteristics (New Product, Die Rev. G) Update Ordering Information – CAT93C66, Die Rev. G (New Product)

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Document No: 1089
Revision: P
Issue date: 04/03/07