Ordering number : ENA1928A

SANYO Semiconductors
DATA SHEET

An ON Semiconductor Company

CMOS LSI

LC01707PLF — FM multiple tuner IC

Overview

LC01707PLF is a vehicle-mounted FM multiple tuner IC with FM-FE, IF, IF-Filter, PLL, FM-DEMO and LPF incorporated. An FM multiple tuner can be developed with this one chip. It makes up a small-sized FM multiple tuners which can be mounted on PND.

Functions

- It is the FM tuner IC exclusively for the FM multiple.
- LNA is incorporated
- Image reduction complex BPF is incorporated
- Wide / Narrow Band RF AGC is incorporated
- Narrow Band IF AGC is incorporated
- Image rejection is adopted
- DLL detection method is adopted for the FM detection circuit, and it is not necessary to adjust.
- LPF for the carrier removal is incorporated.
- IC requires fewer external components.
- It is a BUS control tuner IC which can be controlled by controlled by I^2C BUS.

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD} max		4.3	V
Maximum input voltage	V_{DD} H		4.3	V
Maximum output voltage	V_{DD} L		4.3	V
Power dissipation	Pd max	Ta = 85°C *1	700	mW
Operating ambient	Topr		-40 to 85	°C
Storage temperature	Tstg		-55 to 150	°C
Maximum junction temperature	Tj max		150	°C

*1: Board size: 80mm × 70mm × 1.6mm Glass epoxy double-sided board

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Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage range	V_{DD}		3.0 to 3.6	V
Recommended supply temperature	V_{DD}		3.3	V

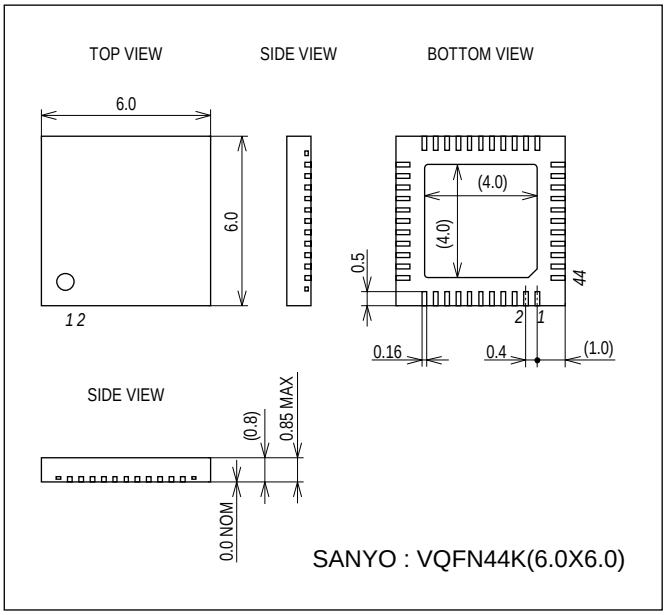
Electrical Characteristics at Ta = 25°C, V_{DD} = 3.3V,
fc = 83MHz, VIN=60dBμVEMF, fm=1kHz, Audio filter: HPF=100Hz, LPF=15kHz
Resister setting: IF AGC (02h) =6(110), RF AGC (00h) =0(0000)
DLL demodulator loop gain setting (09h) =1(01), Mono multi center setting (09h) =7(0111)

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Practical sensitivity 1 (S/N30dB)	SN30	22.5kHz dev, fm=1kHz, S/N=30dB input level		12	20	dBμEMF
Practical sensitivity 2 (S/N10dB)	SN10	7.5kHz dev, fm=76kHz, S/N=10dB input level *1		27		dBμEMF
S/N1	SN1	22.5kHz dev, fm=1kHz	34	44		dB
S/N2	SN2	7.5kHz dev, fm=76kHz *1		21		dB
Total harmonic distortion rate 1	THD_1	22.5kHz dev, fm=1kHz		0.5		%
Total harmonic distortion rate 2	THD_2	75.0kHz dev, fm=1kHz		0.5		%
AM suppression ratio	AMR	AM 30% mod	34	44		dB
Image rejection ratio	IMR	22.5k\Hz dev, fm=1kHz		32		dB
Audio output level 1	AD01	7.5kHz dev, fm=1kHz *1	26	39	70	mVrms
Audio output level 2	AD02	7.5kHz dev, fm=76kHz *1	15	23	41	mVrms
Consumption current	IDD	No signal input		106	170	mA

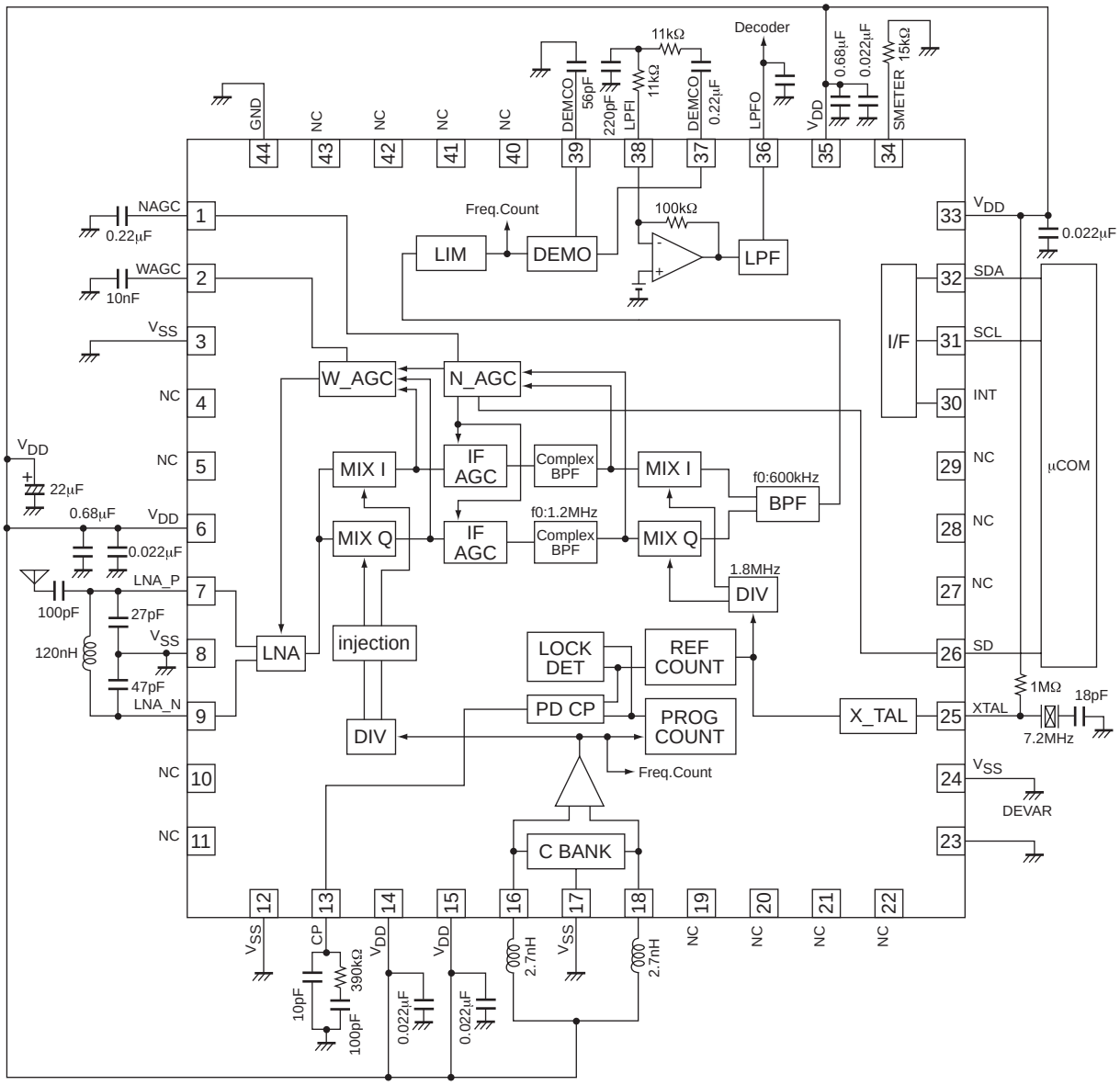
*1: Audio filter: HPF=100Hz, LPF=OFF

Package Dimensions

unit : mm (typ)
3408



Example of applied circuit (constant is tentative)



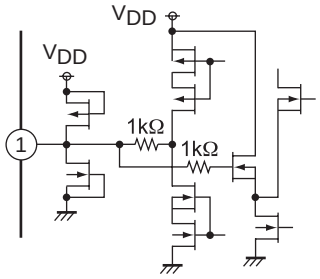
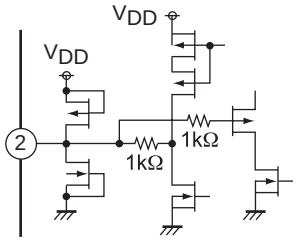
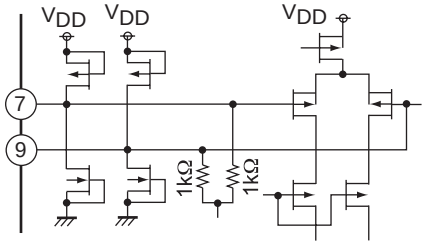
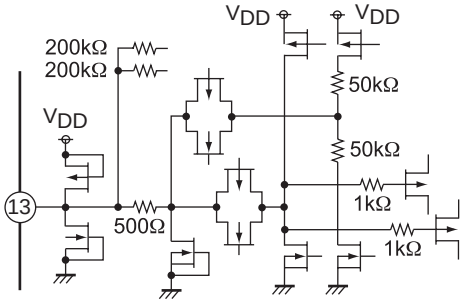
* Culprits oscillation circuit is used in this IC as a crystal oscillation circuit. Caution is required for layout of the board because oscillation between pin25 and power source and GND line.
* The margin of crystal oscillation changes due to the combination of the IC, a crystal oscillator and a board layout. This independent IC does not quarantine the oscillation operation.
* This IC uses the signal of FM band frequency (VCO divided into 1/4) which leaks into ANT pin. If the VCO leakage affects the performance of the system, make sure to connect an isolator on ANT pin path.

Component	Parameter	Value	Type	Supplier
L1/L2	Local OSC coil	2.7nH	C2012H-2N7D-RD	SAGAMI
L3	Differential input coil	120nH	C2012H-R12G-RC	SAGAMI
X1	Crystal	7.2MHz	SMD-49	KDS
			AT-49	KDS
			EXS00A-A01145	NDK
			EXS00A-A01146	NDK

Pin Description

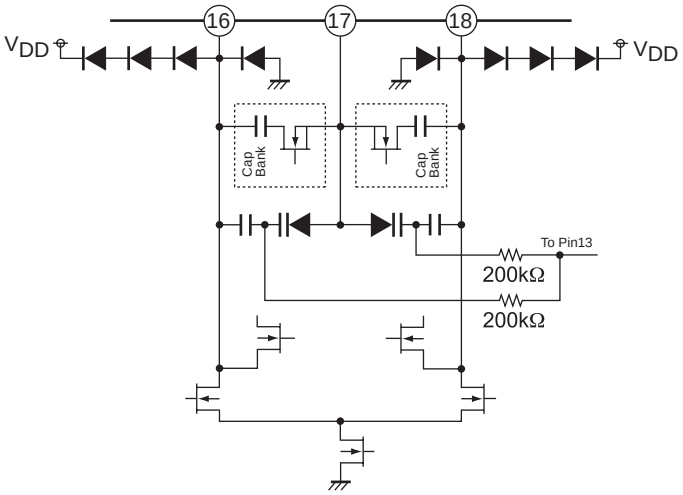
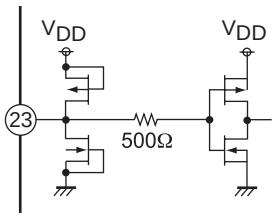
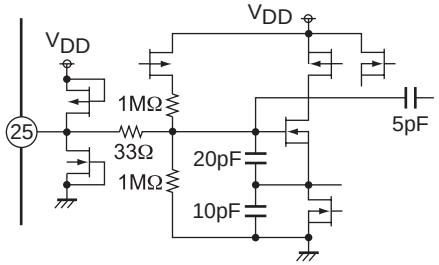
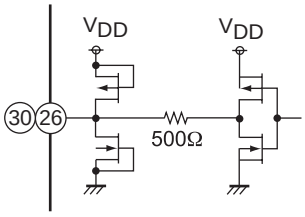
Pin No.	Pin name	I/O	Function
1	NAGC	O	Narrow band AGC detection capacitance connecting pin
2	WAGC	O	Wide band AGC detection capacitance connecting pin
3	V_{SS}	P	GND pin for IF
4	NC	-	
5	NC	-	
6	V_{DD}	P	Supply pin for LNA
7	LNA_A	I	LNA +input pin
8	V_{SS}	P	GND pin for LNA
9	LNA_N	I	LNA –input pin
10	NC	-	
11	NC	-	
12	V_{SS}	P	GND pin for 1st Mixer
13	CP	O	PLL charge pump capacitance connecting pin
14	V_{DD}	P	Supply pin 1st Mixer
15	V_{DD}	P	Supply pin for local oscillation
16	LO_1	O	Inductor connecting pin for local oscillation
17	V_{SS}	P	GND pin for local oscillation
18	LO_2	O	Inductor connecting pin for local oscillation
19	NC	-	
20	NC	-	
21	NC	-	
22	NC	-	
23	DEVER	I	Device address setting pin
24	V_{SS}	P	GND pin for PLL and logic
25	XTAL	I	Crystal resonator connecting pin (Clock input pin)
26	SD	O	Station detector pin
27	NC	-	
28	NC	-	
29	NC	-	
30	INT	O	Test pin
31	SCL	I	Serial data clock input
32	SDA	I	serial data input-output
33	V_{DD}	P	Supply pin for PLL and logic
34	SMETER	O	S-meter output
35	V_{DD}	P	Supply pin for IF
36	LPFO	O	Demodulation output (after band limitation)
37	DEMOO	O	Demodulation output
38	LPFI	I	Demodulation signal input pin
39	DEMOC	O	Capacitance connecting pin for demodulation detection
40	NC	-	
41	NC	-	
42	NC	-	
43	NC	-	
44	GND	P	GND pin

Pin Function

Pin No.	Pin name	Function	Equivalent circuit
1	NAGC	Narrow band AGC detection capacitor connection pin.	
2	WAGC	Wide band AGC detection capacitor connection pin.	
3	V_{SS}	GND pin for IF.	
4	NC	No connection.	
5	NC	No connection.	
6	V_{DD}	Supply pin for LNA.	
7 8 9	LNA_P V_{SS} LNA_N	Pin 7 is + input pin for LNA. Pin 8 is GND pin for LNA. Pin 9 is - input pin for LNA.	
10	NC	No connection.	
11	NC	No connection.	
12	V_{SS}	GND pin 1st mixer for the 1st mixer.	
13	CP	PLL charge pump capacitor connection pin.	
14	V_{DD}	Supply pin for the 1st mixer.	
15	V_{DD}	Supply pin for local oscillator.	

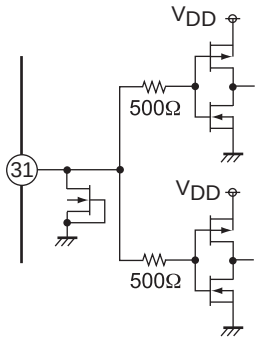
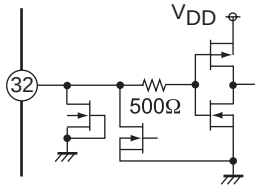
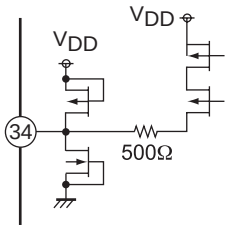
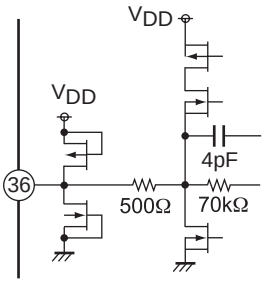
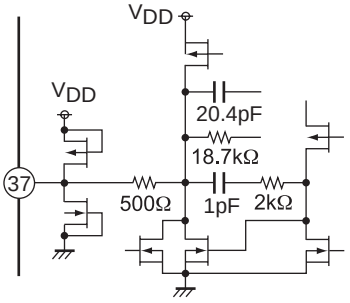
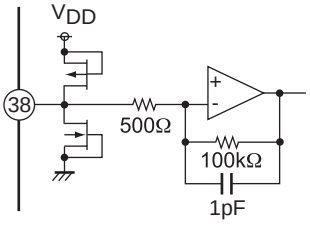
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Pin No.	Pin name	Function	Equivalent circuit
16 17 18	LO_1 V_{SS} LO_2	Pin 16 is inductor connection pin for local oscillator. Pin 17 is GND pin for local oscillator. Pin 18 is inductor connection pin for local oscillator.	
19	NC	No connection.	
20	NC	No connection.	
21	NC	No connection.	
22	NC	No connection.	
23	DEVAR	Device address setting pin.	
24	V_{SS}	PLL_logic GND pin.	
25	XTAL	Crystal oscillator connection pin (clock input pin).	
26 30	SD INT	Station detector pin. Test monitor pin.	
27	NC	No connection.	
28	NC	No connection.	
29	NC	No connection.	

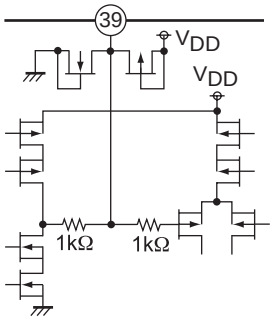
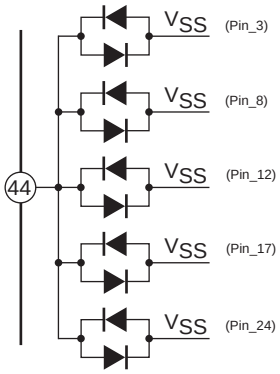
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Pin No.	Pin name	Function	Equivalent circuit
31	SCL	Serial data clock input.	
32	SDA	Serial data input/ output.	
33	V_{DD}	PLL_logic supply voltage pin.	
34	SMETER	S-meter output.	
35	V_{DD}	IF supply voltage pin	
36	LPFO	Demodulator output (After band limit).	
37	DEMOO	Demodulator output.	
38	LPFI	Demodulator signal input pin.	

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Pin No.	Pin name	Function	Equivalent circuit
39	DEMOC	Capacitor connection pin for demodulator detection.	
40	NC	No connection.	
41	NC	No connection.	
42	NC	No connection.	
43	NC	No connection.	
44	GND	GND pin.	

Communication specification

Communication specifications are indicated as below:

Serial Interface (I^2C-bus);

Sending and receiving data through I^2C-bus that consists of two bus lines of a serial data line (SDA) and a serial clock line (SCL). This bus enables 8-bit bi-directional serial data to transmit at the maximum speed of 400kbits (fast mode). This is not compatible with Hs mode.

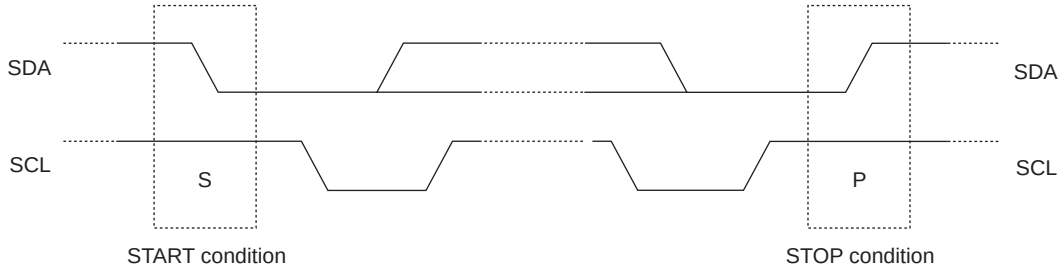
Terms used in I^2C

The following terms are used in I^2C

Terms	Description
Transmitter	Device to send data to the bus
Receiver	Device to receive from the bus
Master	Device to start data transmission, generate signal, and terminate data transmission
Slave	Device of which address is designated master

[Start] and [Stop] conditions

[Start] condition is required at the start of data communication and [Stop] condition at the end of data communication. The condition in which the SDA line changes from [H] to [L] with SCL at [H] is called the [Start] condition. The condition in which the SDA line changes from [L] to [H] with SCL at [H] is called the [Start] condition.



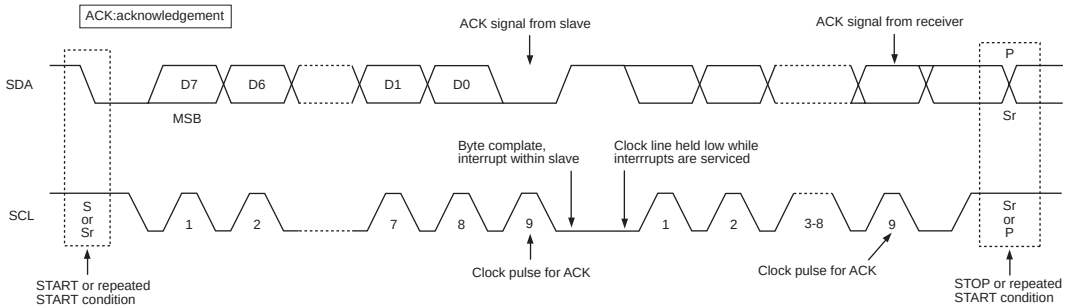
Data transmission

The length of each byte which is output to SDA line is always 8 bits. An acknowledge bit is needed after each byte.

Data is transmitted sequentially from the most significant bit (MSB).

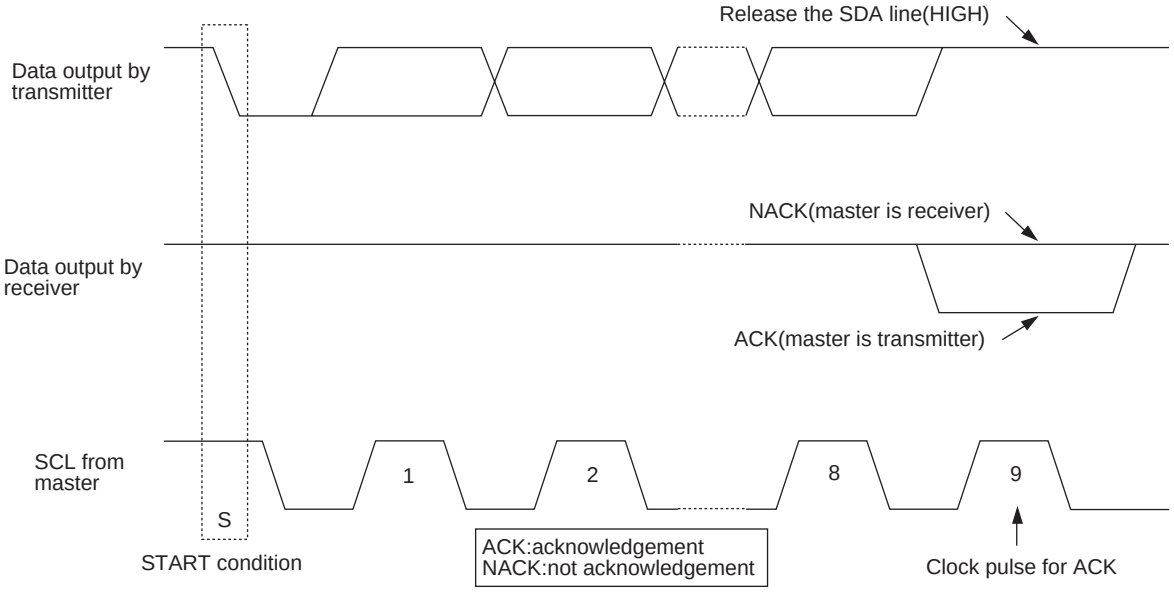
During the data transfer, the slave address is transmitted after the [Start] condition (S).

Data transfer is always ended by the [Stop] condition (P) generated by the master.



Acknowledge (Receive acknowledge)

When the master generates the acknowledge clock pulse, the transmitter opens the SDA line. (SDA line enters the [H] state.) When the acknowledge clock pulse is in the [H] state, the receiver sets the SDA line to [L] each time it receives one byte (eight bits) data. When the master works as a receiver, the master informs the slave of the end of data by omitting acknowledge at the end of data sent from the slave.

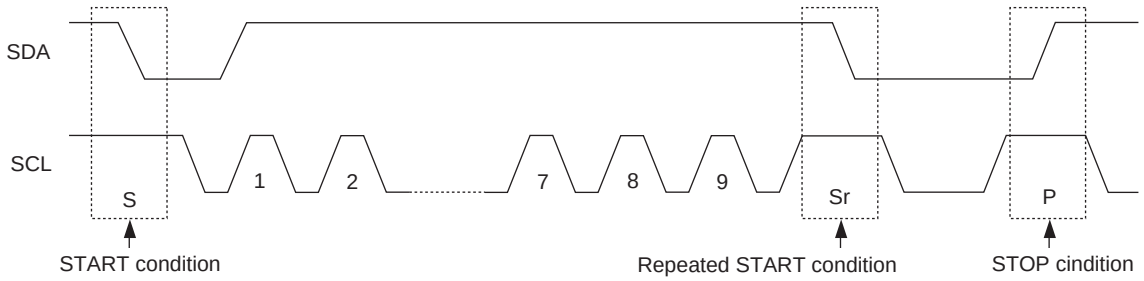


Software reset

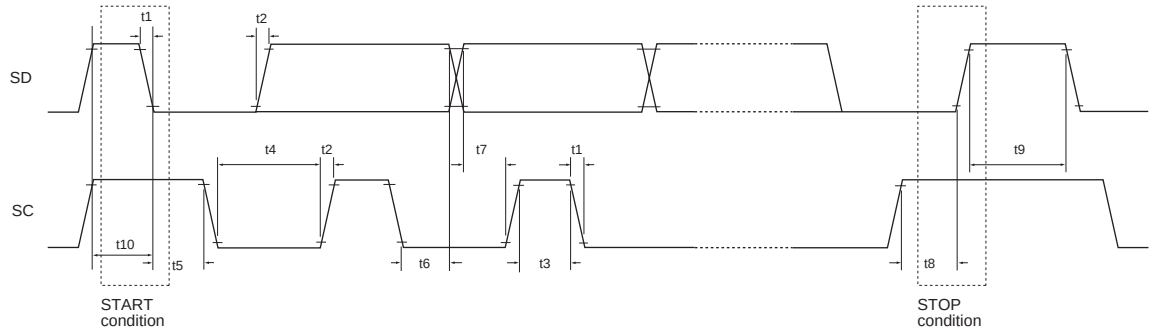
If the communication is interrupted (microcomputer reset, etc.), it is possible to communicate normally by entering the below signals and resetting the CPU in software.

*These signal timings restore the communication after its interruption. The register setting is never reset.

*Software reset command is incompatible with I^2C-bus format.



Electrical specification and timing for I/O stages



Bus line characteristics

Characteristic	Symbol	FAST-MODE		unit	Example at SCL = 100kHz
		min	max		
SCL clock frequency	fSCL		400	kHz	100
Fall time of SDA and SCL	t1	20+0.1Cb	300	ns	
Rise time of SDA and SCL	t2	20+0.1Cb	300	ns	
SCL “H” time	t3	0.6		μs	3
SCL “L” time	t4	1.3		μs	7
[Start] condition holding time	t5	0.6		μs	10
Data holding time for I^2C bus device	t6	0.3		μs	
Data setup time	t7	0.1		μs	3
[Stop] condition setup time	t8	0.6		μs	10
Bus free time between [Stop] and [Start]	t9	1.3		μs	20
[Start] condition setup time	t10	0.6		μs	
Bus line capacitive load	Cb		400	pF	

Serial interface voltage level V_{DD}: Communication bus voltage

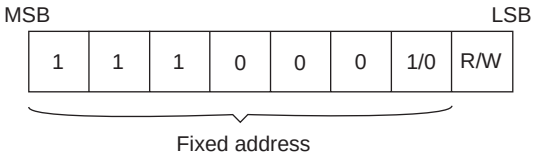
Characteristic	min	max	unit
High level input voltage	$0.7V_{DD}$	V_{DD}	V
Low level input voltage	0.0	$0.3V_{DD}$	V
High level output voltage (open drain)	V_{DD} *2		V
Low level output voltage (open drain)	0.0	$0.2V_{DD}$	V

*2: Output impedance of open drain becomes high at the high level output voltage.
Output voltage equals to V_{DD} (voltage =V_{DD}) since drain is pulled up to V_{DD}.

Definition of each bit

1) Slave address

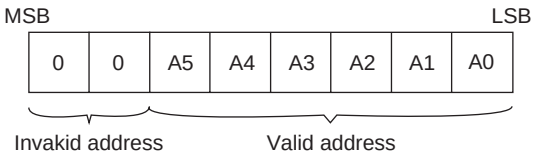
The slave address consists of seven-bit fixed address "1110000" or "1110001", which is unique to a chip, and the eighth-bit data direction bit(R/W). Sending (writing) is processed when the data direction bit is"0", and receiving (reading) is processed when it is "1". The fixed address is set to "1110001" at DEVAR=1 and it is set to "1110000" at DEVAR=0.



R/W	BIT
READ	1
WRITE	0

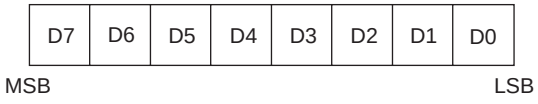
2) Register address

Since the total number of internal register is 34, 2-bit data set on the MSB side becomes invalid. 64 addresses are accepted 6 bits are used, but only 34 registers are used.



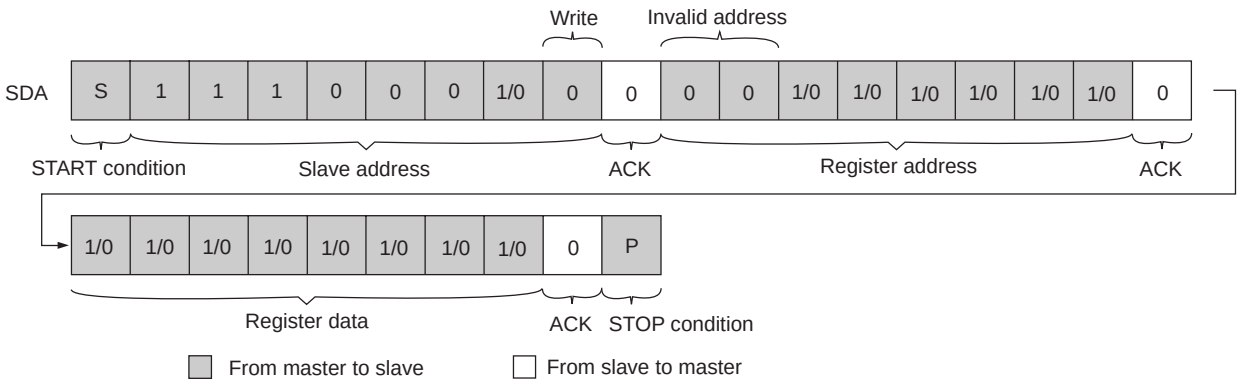
3) Register data

Each register data consists of eight bits.

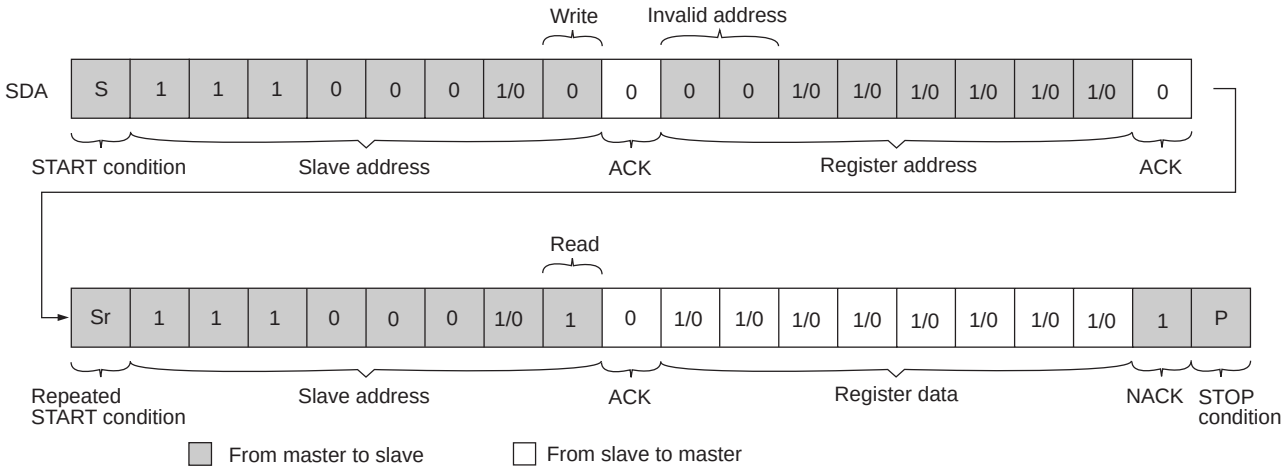


Command Format

1) Individual registers data writing



2) Individual registers data reading



Register Map 1

* HEX value is set by default. : Unused BIT

Register address	BIT	Bit name	Function	Bit operation	Read/ Write	Binary value	Hex value
00h	7					0	h'00
	6	SD_SL[2]	SD level detection setting	0:DRS0 1:DRS1 2:DRS2 3:DRS3 4:DRS4 5:DRS5 6:DRS6 7:DRS7	R/W	0	
	5	SD_SL[1]			R/W	0	
	4	SD_SL[0]			R/W	0	
	3	DWAG[3]	Wide band AGC level setting	0:15.6mVp-p 1:31.3mVp-p 2:46.9mVp-p 3:62.5mVp-p 4:78.1mVp-p 5:93.8mVp-p 6:109.4mVp-p 7:125.0mVp-p 8:140.6mVp-p 9:156.3mVp-p 10:171.9mVp-p 11:187.5mVp-p 12:203.1mVp-p 13:218.8mVp-p 14:234.4mVp-p 15:250mVp-p	R/W	0	
	2	DWAG[2]			R/W	0	
	1	DWAG[1]			R/W	0	
	0	DWAG[0]			R/W	0	
01h	7					0	h'00
	6					0	
	5					0	
	4					0	
	3					0	
	2					0	
	1	IMSD_SL[1]	Unused			0	
	0	IMSD_SL[0]				0	
02h	7	CLKIN	XTAL current setting	1:Normal 0:Twice	R/W	1	h'99
	6	DLOCKSEL	LOCKDET output waveform selection	1:Number of comparing 6 0:Munber of comparing 3	R/W	0	
	5	DFSEL[1]	Phase comparison frequency selection	0:100kHz 1:50kHz 2:50kHz 3:25kHz	R/W	0	
	4	DFSEL[0]			R/W	1	
	3	ENPE	Entire circuit enable	1:ON 0:OFF (Entire circuit OFF)	R/W	1	
	2	DNGA[2]	Narrow band AGC level setting	0:35mVp-p 1:111mVp-p 2:187mVp-p 3:263mVp-p 4:339mVp-p 5:415mVp-p 6:491mVp-p 7:567mVp-p (When the setting value is ether 0 or 1 and MSK=4%, error is detected in BER.)	R/W	0	
	1	DNGA[1]			R/W	0	
	0	DNGA[0]			R/W	1	
03h	7	ENCPLEVEL	Charge pump level comparison selection	1:ON 0:OFF	R/W	1	h'FF
	6	DENPRO	Program counter enable	1:ON 0:OFF	R/W	1	
	5	DENPD	Phase comparison enable	1:ON 0:OFF	R/W	1	
	4	DENCP	Charge pump enable	1:ON 0:OFF	R/W	1	
	3	DENREF	S-meter enable	1:ON 0:OFF	R/W	1	
	2	DENXTAL	XTAL enable	1:ON 0:OFF	R/W	1	
	1	DEBDEMO	Demodulator enable	1:ON 0:OFF	R/W	1	
	0	ENFST	Complex BPF block, IF AGC block enable	1:ON 0:OFF	R/W	1	
04h	7	DENLEVELDET	Capacitor bank control circuit enable	1:ON 0:OFF	R/W	0	h'7F
	6	ENRFMIX	RFMIX enable	1:ON 0:OFF	R/W	1	
	5	ENIFLPF	IF LPF enable	1:ON 0:OFF	R/W	1	
	4	ENDET	Wide band AGC, Narrow band AGC block enable	1:ON 0:OFF	R/W	1	
	3	ENLNA	LNA block enable	1:ON 0:OFF	R/W	1	
	2	DENSMETER	Reference counter enable	1:ON 0:OFF	R/W	1	
	1	DLOEN	Local oscillation enable	1:ON 0:OFF	R/W	1	
	0	DENPLL	PLL block enable	1:ON 0:OFF	R/W	1	
05h	7					0	h'03
	6					0	
	5					0	
	4					0	
	3					0	
	2					0	
	1	DNBAGC	IF AGC detection selector (Narrow band AGC)	1:ON 0:OFF	R/W	1	
	0	DWBAGC	RF AGC detection selector (Wide band AGC)	1:ON 0:OFF	R/W	1	
06h	7	DF0OSC[7]	Capacitor band value Oscillation frequency adjustment for master time constant setting		R/W	1	h'80
	6	DF0OSC[6]			R/W	0	
	5	DF0OSC[5]			R/W	0	
	4	DF0OSC[4]			R/W	0	
	3	DF0OSC[3]			R/W	0	
	2	DF0OSC[2]			R/W	0	
	1	DF0OSC[1]			R/W	0	
	0	DF0OSC[0]			R/W	0	
07h	7	DBPFO[7]	Capacitor bank value Complex BPF F0 adjustment		R/W	1	h'80
	6	DBPFO[6]			R/W	0	
	5	DBPFO[5]			R/W	0	
	4	DBPFO[4]			R/W	0	
	3	DBPFO[3]			R/W	0	
	2	DBPFO[2]			R/W	0	
	1	DBPFO[1]			R/W	0	
	0	DBPFO[0]			R/W	0	

Register Map 2

* HEX value is set by default. : Unused BIT

Register address	BIT	Bit name	Function	Bit operation	Read/ Write	Binary value	Hex value
08h	7	D2BPF[7]	Capacitor bank value 2nd IF BPF f0 adjustment		R/W	1	h'80
	6	D2BPF[6]			R/W	0	
	5	D2BPF[5]			R/W	0	
	4	D2BPF[4]			R/W	0	
	3	D2BPF[3]			R/W	0	
	2	D2BPF[2]			R/W	0	
	1	D2BPF[1]			R/W	0	
	0	D2BPF[0]			R/W	0	
09h	7					0	h'17
	6					0	
	5	DDEMOG[1]	DLL demodulator loop gain setting		R/W	0	
	4	DDEMOG[0]			R/W	1	
	3	DMONOC[3]	Mono multi center setting		R/W	0	
	2	DMONOC[2]			R/W	1	
	1	DMONOC[1]			R/W	1	
	0	DMONOC[0]			R/W	1	
0Ah	7					0	h'02
	6					0	
	5					0	
	4					0	
	3					0	
	2					0	
	1	ENIMRSSI	XTAL OSC FET size setting	1:Normal 0:Twice	R/W	1	
	0	DIQC	Complex BPF injection changeover	1:lower 0:upper	R/W	0	
0Bh	7					0	h'40
	6	DBL[6]	IQ balance adjustment		R/W	1	
	5	DBL[5]			R/W	0	
	4	DBL[4]			R/W	0	
	3	DBL[3]			R/W	0	
	2	DBL[2]			R/W	0	
	1	DBL[1]			R/W	0	
	0	DBL[0]			R/W	0	
0Ch	7					0	h'0A
	6					0	
	5					0	
	4					0	
	3	DCP1REF[3]	Charge pump output current value setting	0:0.1mA 1:0.2mA 2:0.3mA 3:0.4mA 4:0.5mA 5:0.6mA 6:0.7mA 7:0.8mA 8:0.9mA A:1mA B:1.1mA C:1.2mA D: unused E: unused F: unused	R/W	1	
	2	DCP1REF[2]			R/W	0	
	1	DCP1REF[1]			R/W	1	
	0	DCP1REF[0]			R/W	0	
0Dh	7	DPCNT_L[7]	N value of frequency divider (low 8 bits) N value of frequency divider = ((4 × received frequency)±(4 × 1st IF frequency)) / (4 channel × step frequency) * 1st IF frequency is 1.2MHz		R/W	*	h'**
	6	DPCNT_L[6]			R/W	*	
	5	DPCNT_L[5]			R/W	*	
	4	DPCNT_L[4]			R/W	*	
	3	DPCNT_L[3]			R/W	*	
	2	DPCNT_L[2]			R/W	*	
	1	DPCNT_L[1]			R/W	*	
	0	DPCNT_L[0]			R/W	*	
0Eh	7	DPCNT_H[7]	N value of frequency divider (high 8 bits)		R/W	*	h'**
	6	DPCNT_H[6]			R/W	*	
	5	DPCNT_H[5]			R/W	*	
	4	DPCNT_H[4]			R/W	*	
	3	DPCNT_H[3]			R/W	*	
	2	DPCNT_H[2]			R/W	*	
	1	DPCNT_H[1]			R/W	*	
	0	DPCNT_H[0]			R/W	*	
0Fh	7	DCBANK_L[7]	Local oscillator capacitor bank setting (low 8 bits)		R/W	0	h'00
	6	DCBANK_L[6]			R/W	0	
	5	DCBANK_L[5]			R/W	0	
	4	DCBANK_L[4]			R/W	0	
	3	DCBANK_L[3]			R/W	0	
	2	DCBANK_L[2]			R/W	0	
	1	DCBANK_L[1]			R/W	0	
	0	DCBANK_L[0]			R/W	0	

Register Map 3

* HEX value is set by default. : Unused BIT

Register address	BIT	Bit name	Function	Bit operation	Read/ Write	Binary value	Hex value
10h	7					0	h'01
	6					0	
	5					0	
	4					0	
	3					0	
	2					0	
	1					0	
	0	DCBANK_H[8]	Local oscillator capacitor bank setting (high 1 bit)		R/W	1	
11h	7					0	h'0F
	6					0	
	5					0	
	4	DCBEN	Unused			0	
	3	DLOALC[3]	Local oscillation level setting		R/W	1	
	2	DLOALC[2]			R/W	1	
	1	DLOALC[1]			R/W	1	
	0	DLOALC[0]			R/W	1	
12h	7					0	h'00
	6	DENIFCOUNT	Frequency counter (analog block) enable	1:ON 0:OFF	R/W	0	
	5	DENF0OSC	f0 detection oscillation circuit enable	1:ON 0:OFF	R/W	0	
	4	DENIFFREQ	Logic part reference clock enable	1:ON 0:OFF	R/W	0	
	3					0	
	2	DSCTCOUNT[2]	Count frequency selection	0:unused 1:IF frequency 2:prescaler frequency 3:freacaler frequency 4:f0 detection oscillation frequency 5:f0 detection oscillation frequency 6:unused 7:IF frequency	R/W	0	
	1	DSCTCOUNT[1]			R/W	0	
	0	DSCTCOUNT[0]			R/W	0	
13h	7					0	h'01
	6					0	
	5					0	
	4					0	
	3					0	
	2	CTE	Counter start trigger	1:ON (frequency counter start) Charge to 0 automatically	R/W	0	
	1	GT[1]	Frequency counter gate time selection	0:4ms 1:8ms 2:32ms 3:64ms	R/W	0	
	0	GT[0]			R/W	1	
14h	7	LOFQ_L[7]	LO_COUNT value (low 8 bits) Measurement frequency = counter value / GT[ms]		R	*	h'00
	6	LOFQ_L[6]			R	*	
	5	LOFQ_L[5]			R	*	
	4	LOFQ_L[4]			R	*	
	3	LOFQ_L[3]			R	*	
	2	LOFQ_L[2]			R	*	
	1	LOFQ_L[1]			R	*	
	0	LOFQ_L[0]			R	*	
15h	7	LOFQ_H[7]	LO_COUNT value (upper 8 bits)		R	*	h'00
	6	LOFQ_H[6]			R	*	
	5	LOFQ_H[5]			R	*	
	4	LOFQ_H[4]			R	*	
	3	LOFQ_H[3]			R	*	
	2	LOFQ_H[2]			R	*	
	1	LOFQ_H[1]			R	*	
	0	LOFQ_H[0]			R	*	
16h	7					0	h'10
	6					0	
	5	COUNTSEL				0	
	4	LOCKDETSEL				1	
	3	LOCKDET_DIG				0	
	2	LOCKDET	LOCK detection	1:LOCK 0:UNLOCK	R/W	0	
	1	PHLEVEL[1]	Charge pump voltage level detection	0:less than 0.5V 1:0.5V to 2.8V 2:Unused 3:more than 2.8V	R/W	0	
	0	PHLEVEL[0]			R/W	0	
17h	7					*	h'0*
	6					*	
	5					*	
	4					*	
	3	IMRSSI[3]	Reset detection circuit	0:reset 1:reset cancellation	R	*	
	2	IMRSSI[2]			R	*	
	1	IMRSSI[1]			R	*	
	0	IMRSSI[0]			R	*	

Register Map 4

* HEX value is set by default. : Unused BIT

Register address	BIT	Bit name	Function	Bit operation	Read/ Write	Binary value	Hex value
18h	7					0	
	6	DRS[6]	S-meter detection level	Detection range can be changed by setting to DNGA (02h)	R	*	
	5	DRS[5]			R	*	
	4	DRS[4]			R	*	
	3	DRS[3]			R	*	h'**
	2	DRS[2]			R	*	
	1	DRS[1]			R	*	
	0	DRS[0]			R	*	
19h	7	IFCOUNT_L[7]	IF count value (low 8 bits) 2nd IF frequency measurement results		R	*	
	6	IFCOUNT_L[6]			R	*	
	5	IFCOUNT_L[5]			R	*	
	4	IFCOUNT_L[4]			R	*	
	3	IFCOUNT_L[3]			R	*	h'**
	2	IFCOUNT_L[2]			R	*	
	1	IFCOUNT_L[1]			R	*	
	0	IFCOUNT_L[0]			R	*	
1Ah	7	IFCOUNT_H[7]	IF count value (high 8 bits)		R	*	
	6	IFCOUNT_H[6]			R	*	
	5	IFCOUNT_H[5]			R	*	
	4	IFCOUNT_H[4]			R	*	
	3	IFCOUNT_H[3]			R	*	h'**
	2	IFCOUNT_H[2]			R	*	
	1	IFCOUNT_H[1]			R	*	
	0	IFCOUNT_H[0]			R	*	
1Bh	7	IMCOUNT_L[7]	Unused		R	*	
	6	IMCOUNT_L[6]			R	*	
	5	IMCOUNT_L[5]			R	*	
	4	IMCOUNT_L[4]			R	*	
	3	IMCOUNT_L[3]			R	*	h'**
	2	IMCOUNT_L[2]			R	*	
	1	IMCOUNT_L[1]			R	*	
	0	IMCOUNT_L[0]			R	*	
1Ch	7	IMCOUNT_H[7]	Unused		R	*	
	6	IMCOUNT_H[6]			R	*	
	5	IMCOUNT_H[5]			R	*	
	4	IMCOUNT_H[4]			R	*	
	3	IMCOUNT_H[3]			R	*	h'**
	2	IMCOUNT_H[2]			R	*	
	1	IMCOUNT_H[1]			R	*	
	0	IMCOUNT_H[0]			R	*	
1Dh	7	F0_L[7]	f0 detection oscillation frequency count value (low 8 bits) Frequency measurement result for master time constant setting		R	*	
	6	F0_L[6]			R	*	
	5	F0_L[5]			R	*	
	4	F0_L[4]			R	*	
	3	F0_L[3]			R	*	h'**
	2	F0_L[2]			R	*	
	1	F0_L[1]			R	*	
	0	F0_L[0]			R	*	
1Eh	7	F0_H[7]	f0 detection oscillation frequency count value (high 8 bits)		R	*	
	6	F0_H[6]			R	*	
	5	F0_H[5]			R	*	
	4	F0_H[4]			R	*	
	3	F0_H[3]			R	*	h'**
	2	F0_H[2]			R	*	
	1	F0_H[1]			R	*	
	0	F0_H[0]			R	*	
1Fh	7					0	
	6					0	
	5					0	
	4					0	
	3					0	h'02
	2	DOUTSEL	Register for TEST		R/W	0	
	1	DCNTEST	Register for TEST		R/W	1	
	0	DOUTTEST	Register for TEST		R/W	0	

Continued on next page.

Continued from preceding page.

Register address	BIT	Bit name	Function	Bit operation	Read/ Write	Binary value	Hex value
20h	7					0	h'0A
	6	ERR2	Local oscillator capacitor bank control error flag 2		R/W	0	
	5	ERR1	Local oscillator capacitor bank control error flag 1		R/W	0	
	4	DCOSEL2	Local oscillator capacitor bank value changeover	1:cap bank control value 0:I²C input value	R/W	0	
	3	DCOSEL1	Local oscillator capacitor bank control process changeover	1:correcting process after sequential comparison 0:No correcting process after sequential comparison	R/W	1	
	2	DCOSEL0	Local oscillator capacitor bank control process changeover (micro alignment)	1:micro adjustment process 0:No micro adjustment process	R/W	0	
	1	DWAITSEL[1]	PLL operation check wait time after local oscillator capacitor bank adjustment	0:200µs 1: 400µs 2:800µs 3:1600µs	R/W	1	
	0	DWAITSEL[0]			R/W	0	
21h	7					0	h'0A
	6					0	
	5	DENINT	Register for TEST		R/W	0	
	4	MASKSEL	Register for TEST		R/W	0	
	3	LOSEL	Register for TEST		R/W	1	
	2	INTPH	Register for TEST		R/W	0	
	1	INTIM	Register for TEST		R/W	1	
	0	INTLO	Register for TEST		R/W	0	
22h	7	TESTSEL[2]	Register for TEST		R/W	0	h'15
	6	TESTSEL[1]	Register for TEST		R/W	0	
	5	TESTSEL[0]	Register for TEST		R/W	0	
	4	DSW	PLL loop filter ON/OFF	1:ON 0:OFF	R/W	1	
	3	TIMESEL2[1]	Local oscillator capacitor bank control correcting circuit operation clock setting	0:200µs 1: 400µs 2:800µs 3:1600µs	R/W	0	
	2	TIMESEL2[0]			R/W	1	
	1	TIMESEL[1]	Local oscillator capacitor bank control sequential comparison control operation clock setting	0:10µs 1: 20µs 2:40µs 3:80µs	R/W	0	
	0	TIMESEL[0]			R/W	1	

SD pin specification

SD voltage level V_{DD}: supply voltage

item	min	max	unit
High level output voltage	V_{DD}-0.8	V_{DD}	V
Low level output voltage	0	0.4	V

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