# MAS9181B/C

## OCTAL 8-BIT TRIMMER IC

- **Eight discrete DACs**
- **$I^2C$-bus slave receiver**
- **Voltage output**

## DESCRIPTION

The MAS9181 comprises eight digital to analog converters (DACs) each controlled by a two-wire $I^2C$ bus. The DACs are individually programmed using an 8-bit word to select an output from one of 256 voltage steps. The maximum output voltage of all DACs is set by Vmax and the resolution is Vmax/256. At power-on all outputs are set to their lowest value. The $I^2C$-bus slave receiver has 3 programmable address pins (2 for MAS9181 CS).

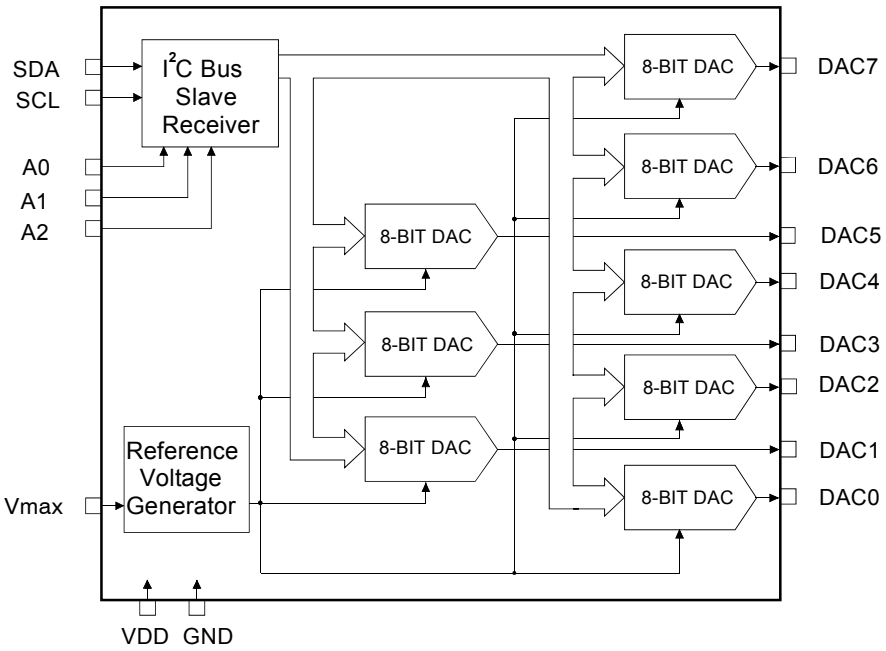
## FEATURES

- Rail to rail output stages
- Octal 8-bit DACs on a single monolithic chip
- Power supply range from +5 V to +12 V
- -20°C to +85°C temperature range
- 16-pin PDIL and SO package
- Power-up reset

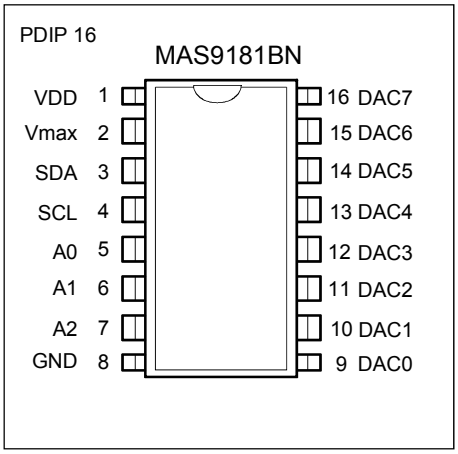
## APPLICATION

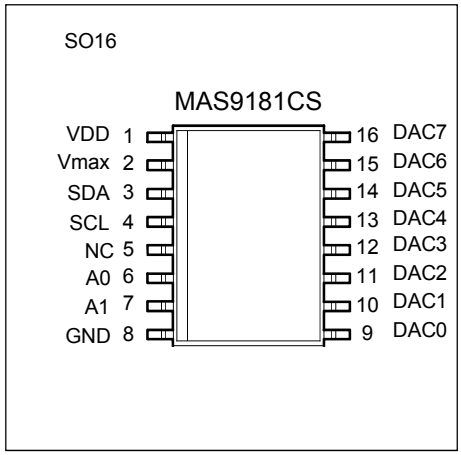
- Trimmer replacement
- AGC/AFT or TVs and VCRs
- Graphic equalizers
- High resolution monitors

## BLOCK DIAGRAM



## PIN CONFIGURATION




## PIN DESCRIPTION

| Pin name | Pin no. | | I/O | Function |
|---|---|---|---|---|
| | *1 | *2 | | |
| VDD | 1 | 1 | P | Positive supply voltage |
| Vmax | 2 | 2 | I | Control input for DAC maximum output voltage |
| SDA | 3 | 3 | I/O | $I^2C$ bus serial data input/output |
| SCL | 4 | 4 | I | $I^2C$ bus serial data clock |
| $A_0$ | 5 | 6 | I | Programmable address bits for $I^2C$ bus slave receiver |
| $A_1$ | 6 | 7 | I | Programmable address bits for $I^2C$ bus slave receiver |
| $A_2$ | 7 | NC | I | Programmable address bits for $I^2C$ bus slave receiver |
| GND | 8 | 8 | G | Ground |
| DAC0 | 9 | 9 | O | Analog voltage output |
| DAC1 | 10 | 10 | O | Analog voltage output |
| DAC2 | 11 | 11 | O | Analog voltage output |
| DAC3 | 12 | 12 | O | Analog voltage output |
| DAC4 | 13 | 13 | O | Analog voltage output |
| DAC5 | 14 | 14 | O | Analog voltage output |
| DAC6 | 15 | 15 | O | Analog voltage output |
| DAC7 | 16 | 16 | O | Analog voltage output |

*1 MAS9181BN (PDIP16)
*2 MAS9181CS (SO16)

## ABSOLUTE MAXIMUM RATINGS

(conditions)

| Parameter | Symbol | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| Supply Voltage | VDD | | -0.5 | 18 | V |
| Supply current | IDD | | -10 | 40 | mA |
| $I^2C$-bus line voltage | V(3),V(4) | | -0.5 | 5.9 | V |
| Input voltage | Vin | | -0.5 | VDD+0.5 | V |
| Output voltage | Vo | | -0.5 | VDD+0.5 | V |
| Maximum current on any pin | Imax | | | 10 | mA |
| total power dissipation | Ptot | | | 500 | mW |
| Operating ambient temperature range | Tamb | | -20 | +85 | $^oC$ |
| Storage temperature range | Tstg | | -65 | +150 | $^oC$ |

## RECOMMEDED OPERATION CONDITIONS

(All voltages are with respect to GND; Tamb = +25 $^oC$; VDD = 12V unless otherwise specified)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Supply Voltage | VDD | | 4.5 | 12 | 13.2 | V |
| Supply current | IDD | No loads, Vmax=VDD=12V, All data=$00_{OCT}$ | | 3.0 | 5.0 | mA |
| Total power dissipation | Ptot | No loads, Vmax=VDD=12V, All data=$00_{OCT}$ | | 40 | 60 | mW |

## ELECTRICAL CHARACTERISTICS

◆ **Inputs**
**SDA, SCL input (pins 3, 4)**

(All voltages are with respect to GND; Tamb = -20 $^oC$ to 85 $^oC$; VDD = 5V to 12V unless otherwise specified)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input voltage range | $V_I$ | | -0.5 | | 5.5 | V |
| Input low voltage | $V_{IL}$ | | | | 1.0 | V |
| Input high voltage | $V_{IH}$ | | 3.0 | | | V |
| Input leakage current | $I_{IL}$ | Vin = 0V or VDD | -1 | | +1 | µA |
| Power-up reset | | | | 3.5 | | V |

## ELECTRICAL CHARACTERISTICS

### Address Input (pins 5, 6, 7)

(All voltages are with respect to GND; Tamb = -20 °C to 85 °C; VDD = 5V to 12V unless otherwise specified)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input voltage range | $V_I$ | | 0 | | VDD | V |
| Input low voltage | $V_{IL}$ | | | | 1.0 | V |
| Input high voltage | $V_{IH}$ | | 3.0 | | | V |
| Input current low | $I_{IL}$ | | | -10 | -15 | μA |
| Input current high | $I_{IH}$ | | | | 1 | μA |

### Vmax Control Input for DAC maximum output voltage (pin 2)

(All voltages are with respect to GND; Tamb = -20 °C to 85 °C; VDD = 5V to 12V unless otherwise specified)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Pin 2 current | $I_2$ | | | 7 | 10 | μA |

### ◆ Outputs

(All voltages are with respect to GND; Tamb = -20 °C to 85 °C; VDD = 5V to 12V unless otherwise specified)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| DAC output (pin 9 to 16) Output voltage range | Vo | Io = +/- 100 μA | 0.1 | | VDD-0.1 | V |
| | | Io = +/- 500 μA | 0.2 | | VDD-0.2 | V |
| Output impedance | Zo | data = 7F | | 30 | | Ω |
| DAC output drive range | Io | Upper side saturation voltage= 0.2v<br>Low side saturation voltage = 0.2v | -1 | | 1 | mA |
| Output capacitive load | Co | | | | 2 | nF |

### SDA Output (pin 3)

(All voltages are with respect to GND; Tamb = -20 °C to 85 °C; VDD = 5V to 12V unless otherwise specified)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Output voltage low | $V_{OL}$ | $I_3$ = 3.0 mA | | | 0.4 | V |

### Linearity

(All voltages are with respect to GND; Tamb = -20 °C to 85 °C; VDD = 5V to 12V unless otherwise specified)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Differential nonlinearity | DNL | Io = 0 (without load)<br>Vmax = VDD-1.0 | -1 | | 1 | LSB |
| Integral nonlinearity | INL | Io = 0 (without load)<br>Vmax = VDD-1.0 | -1.5 | | 1.5 | LSB |
| Zero code error[1] | ZCE | data = 00 | | 10 | 30 | mV |
| Power supply rejection[1] | PSRR | | | | 5 | mV/V |
| Zero code temperature coefficient[1] | TCo | | -200 | | 200 | μV/°C |

Note 1: Guaranteed by design but not production tested

## FUNCTIONS

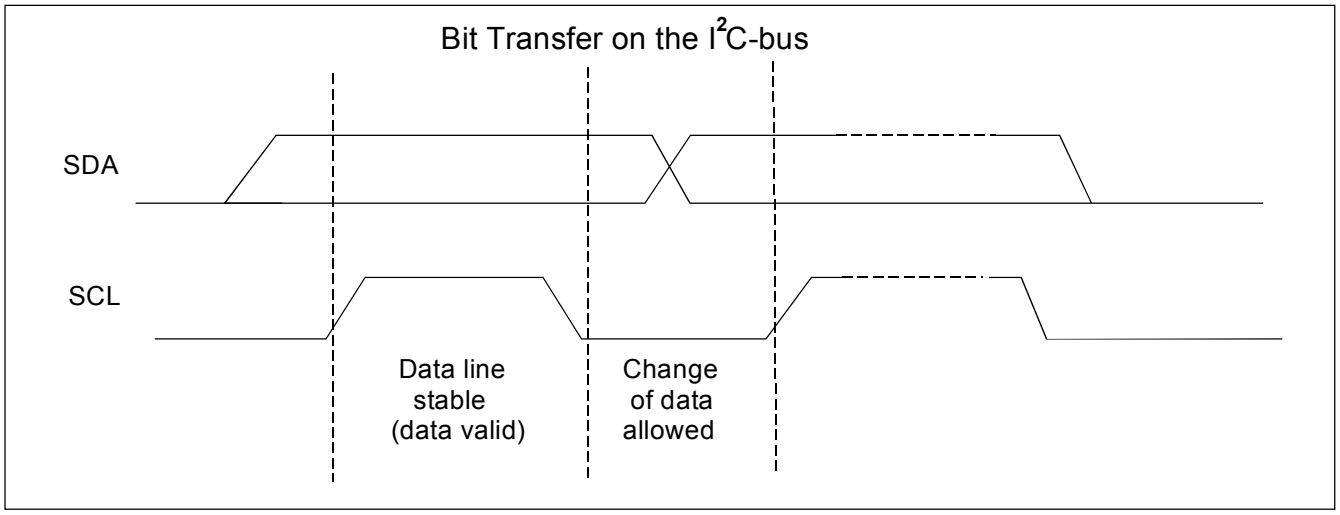
### ◆ I²C - bus

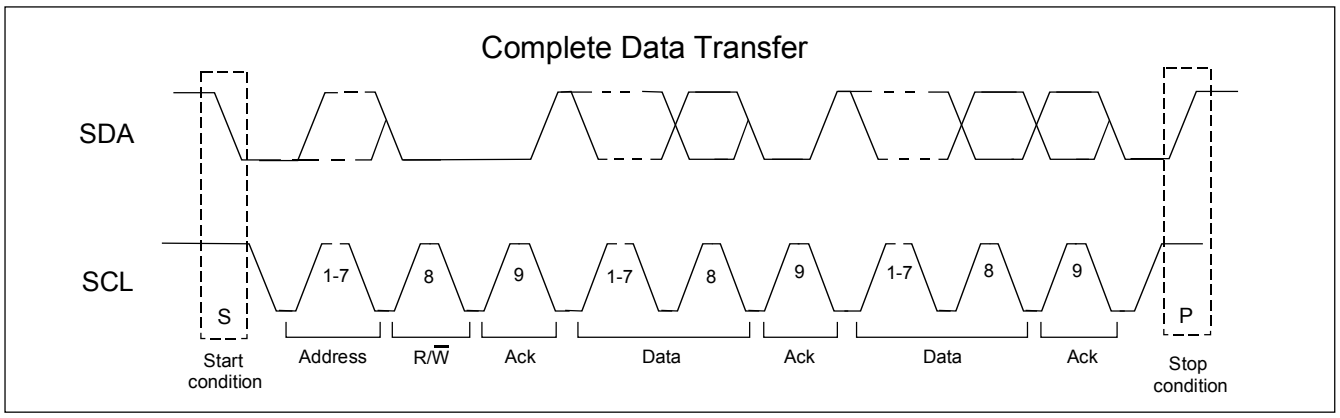
The MAS9181 I²C-bus interface is a receiver- only slave. Data is accepted from the I²C - bus in the following format.

| S | 0 1 0 0 A2 A1 A0 0 | A | I3 I2 I1 I0 SD SC SB SA | A | D7 D6 D5 D4 D3 D2 D1 D0 | A | P |
|---|---|---|---|---|---|---|---|
| | Address byte | | Instruction byte | | First data byte | | |

| | | | |
|---|---|---|---|
| S | Start condition | A2, A1, A0 | programmable address bits |
| P | Stop condition | I3, I2, I1, I0 | instruction bits |
| A | Acknowledgement | SD, SC, SB, SA | sub-address bits |
| | | D7, D6, D5, D4, D3, D2, D2, D1, D0 | data bits |

### ◆ I²C - bus timing



## FUNCTIONS

### ◆ Address Byte

Valid addresses are 40, 42, 44, 46, 48, 4A, 4C, 4E(hex), depending on the programming of bits A2, A1 and A0. With these addresses, up to eight MAS9181 ICs can be operated independently from one $I^2C$-bus. No other addresses are acknowledged by the MAS9181. The address inputs A0, A1 and A2 are programmed by connection to GND for An = 0 or to VDD for An = 1. If the inputs are left floating, An = 1 will result. For MAS9181CS, A2 is always 1.

### ◆ Instruction and data bytes

Valid instructions from 00 to 0F and F0 to FF (hex); MAS9181 will not respond to other instruction value, but will still generate an acknowledgement. Instructions 00 to0F cause auto-incrementing of the sub-address (bits SD to SA) when more than one data byte is sent within one transmission. With auto-incrementing, the first data byte is written into the DAC addessed by bits SD to SA and then the sub-address is automatically incremented by one position for the next databyte in the series. Auto-incrementing does not occur with instructions F0 to FF. The DAC addressed by the sub-address will always receive the data if more than one data byte is sent. Valid sub-addresses (bits SD to SA) are 0 to 7 (hex) relating numerically to DAC0 to DAC7. When the auto-incrementing function is used, the sub-address will sequence through all possible values (0 to F, 0 to F, etc.). While the sub-address is between 8 and F no DAC outputs change.

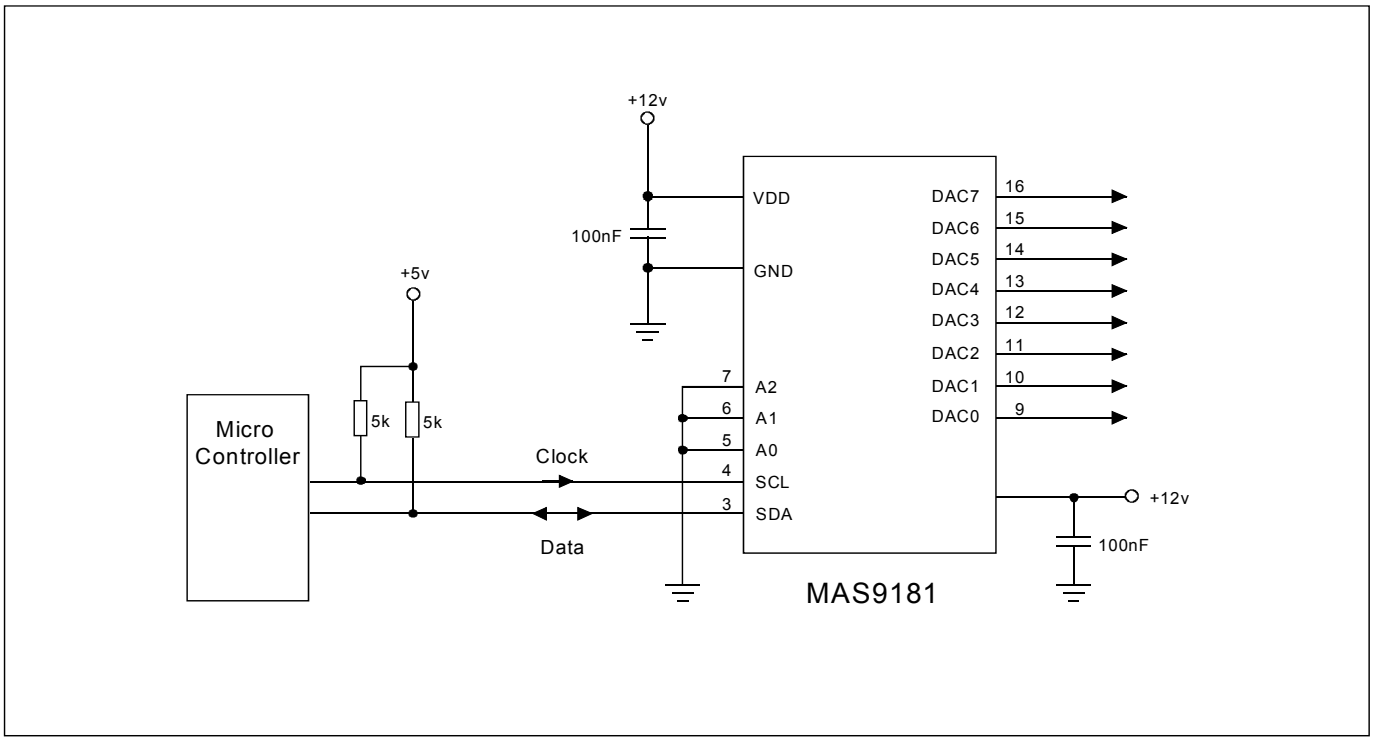
### ◆ $I^2C$ - bus

Input SCL (pin 4) and input/output SDA (pin 3) conform to $I^2C$-bus specifications. Pins 3 and 4 are protected against voltage pulses by internal zener diodes connected to the ground plane and therefore the normal bus line voltage shall not exceed 5.5V.

### ◆ Input Vmax

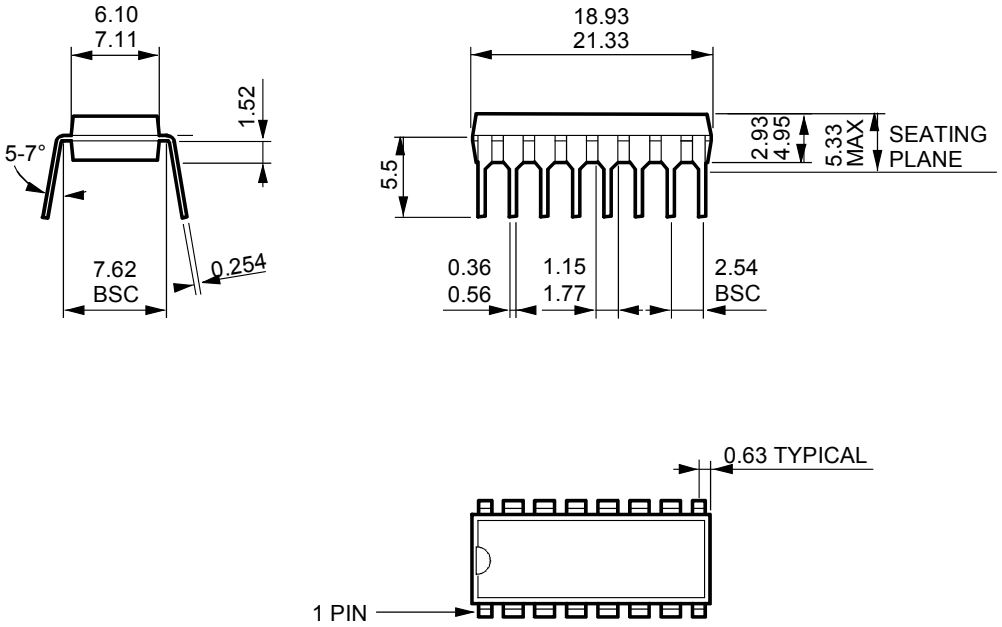
Input Vmax (pin 2) provides a means of comprising the output voltage swing of the DACs. The maximum DAC output voltage is restricted to approximately Vmax while the 8-bit resolution is maintained, therefore giving a finer voltage resolution of smaller output swings.

## APPLICATION INFORMATION

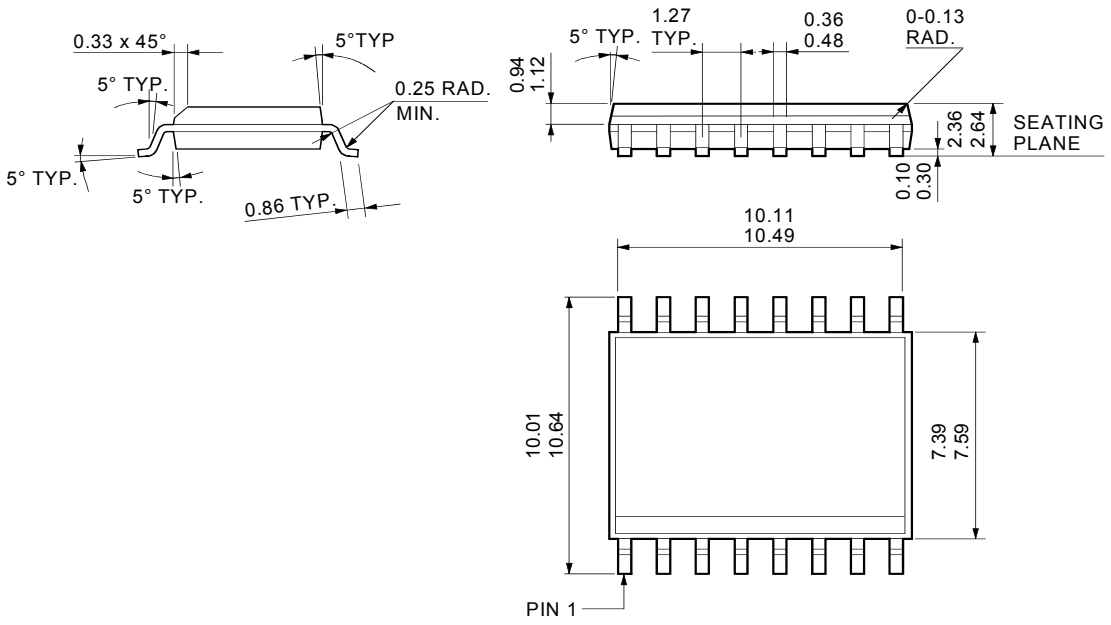


## PACKAGE OUTLINES

### 16 LEAD PDIP OUTLINE (300 MIL BODY)




### 16 LEAD SO OUTLINE (300 MIL BODY)




ALL MEASUREMENTS IN mm

## ORDERING INFORMATION

| Product Code | Product | Package | Comments |
|---|---|---|---|
| MAS9181BN | OCTAL 8-BIT TRIMMER-IC | 16 Pin PDIP 0.3" | |
| MAS9181CS | OCTAL 8-BIT TRIMMER-IC | 16 Pin SO 0.3" | 2 Address Pins |

## LOCAL DISTRIBUTOR

## MICRO ANALOG SYSTEMS OY CONTACTS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