

VTM® Current Multiplier

MIL-COTS
MVTM36 Series

High Efficiency, Sine Amplitude Converter™ (SAC™)

Features

- Family of MIL-COTs current multipliers covering output voltages from 1 to 50 Vdc
  - Operating from MIL-COTs PRM® modules
- High efficiency reduces system power consumption
- High density provides isolated regulated system and saves space
- VI Chip® package enables surface mount or through hole, low impedance interconnect to system board
- Contains built-in protection features against:
  - Overvoltage
  - Overcurrent
  - Short Circuit
  - Overtemperature
- ZVS/ZCS resonant Sine Amplitude Converter topology
- Less than 50°C temperature rise at full load in typical applications

Typical Applications

- Land/Air/Sea Unmanned Vehicles/Drones
- Scanning Equipment
- Radar
- Mobile Weapons
- Hybrid Vehicles

Product Ratings	
V_{IN} = 26.0 V to 50.0 V	P_{OUT} = up to 150 W
V_{OUT} = 1.0 V to 50.0 V (various models)	I_{OUT} = up to 80 A

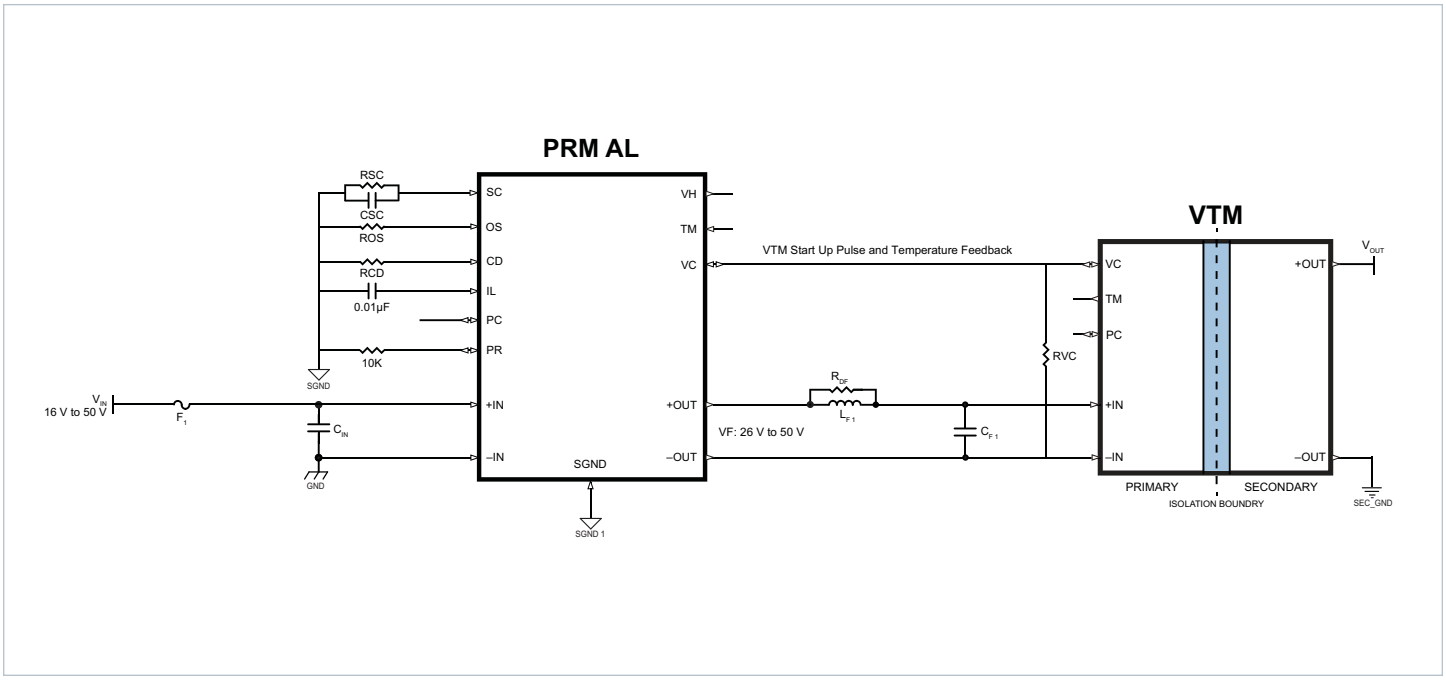
Product Description

The VI Chip® current multiplier is a high efficiency Sine Amplitude Converter™ (SAC™) operating from a 26 to 50 Vdc primary bus to deliver an isolated output. The Sine Amplitude Converter offers a low AC impedance beyond the bandwidth of most downstream regulators, which means that capacitance normally at the load can be located at the input to the Sine Amplitude Converter. This allows for a reduction in point of load capacitance of typically >100x which results in a saving of board area, materials and total system cost.

The VTM current multiplier is provided in a VI Chip package compatible with standard pick-and-place and surface mount assembly processes. The co-molded VI Chip package provides enhanced thermal management due to large thermal interface area and superior thermal conductivity. With high conversion efficiency the VTM current multiplier increases overall system efficiency and lowers operating costs compared to conventional approaches.

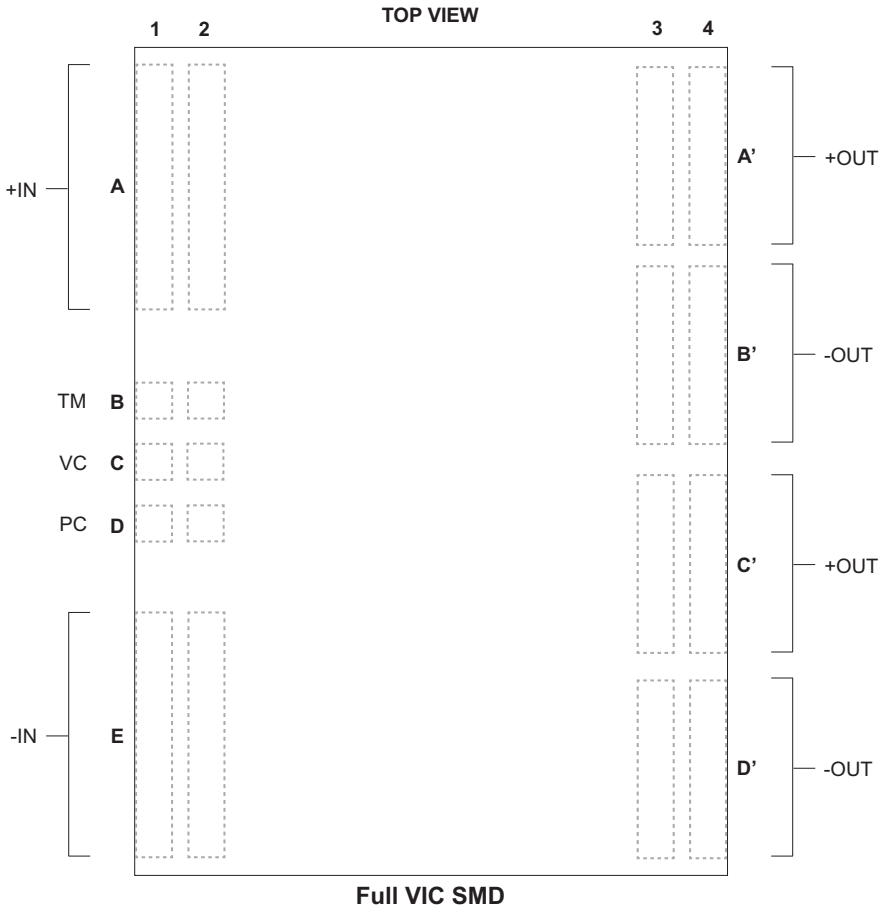
The VTM current multiplier enables the utilization of Factorized Power Architecture providing efficiency and size benefits by lowering conversion and distribution losses and promoting high density point of load conversion.

Typical Application



Using the MIL-COTs PRM, the output of the VTM is regulated over the load current range with only a single interconnect between the PRM and VTM and without the need for isolation in the feedback path.

Pin Configuration (Full)

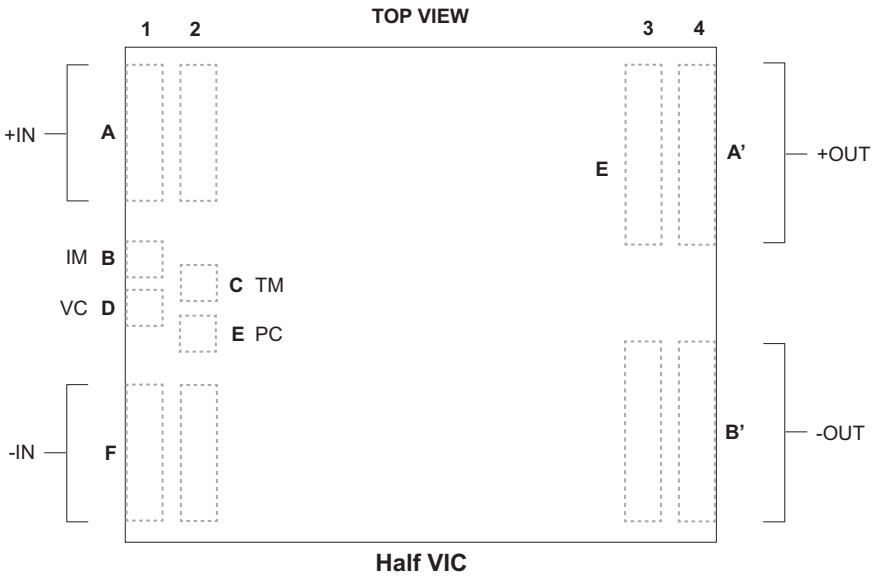


Full VIC SMD

Pin Description (Full)

Pin Number	Signal Name	Type	Function
A1, A2	+IN	INPUT POWER	Positive Input Power Terminal
B1, B2	TM	OUTPUT	Provides voltage proportional to internal VTM controller temperature. "Power Good" flag.
C1, C2	VC	INPUT	Connect to 12 V source to power internal VTM control circuits.
D1, D2	PC	BIDIR	Enables power supply when allowed to float high. 5 V during normal operation.
E1, E2	-IN	INPUT POWER RETURN	Negative Input Power Terminal
A'3, A'4, C'3, C'4	+OUT	OUTPUT POWER	Positive Output Power Terminal
B'3, B'4, D'3, D'4	-OUT	OUTPUT POWER RETURN	Positive Output Power Terminal

Pin Configuration (Half)



Pin Description (Half)

Pin Number	Signal Name	Type	Function
A1, A2	+IN	INPUT POWER	Positive Input Power Terminal
B1	IM	OUTPUT	Provides voltage proportional to load current.
C2	TM	OUTPUT	Provides voltage proportional to internal VTM controller temperature. “Power Good” flag.
D1	VC	INPUT	Connect to 12 V source to power internal VTM control circuits.
E2	PC	BIDIR	Enables power supply when allowed to float high. 5 V during normal operation.
F1, F2	-IN	INPUT POWER RETURN	Negative Input Power Terminal
A’3, A’4	+OUT	OUTPUT POWER	Positive Output Power Terminal
B’3, B’4	-OUT	OUTPUT POWER RETURN	Positive Output Power Terminal

Part Ordering Information

Device	Input Voltage Range	Package Type	Output Voltage x 10	Temperature Grade	Output Current	Revision	Version
VTM	36B	F	015	M	080	A	00
VTM = VTM	36B = 26.0 to 50.0 V	F = Full VIC SMD T = Full VIC Through Hole H = Half VIC SMD	015 = 1.5 V	M = -55 to 125°C	080 = 80 A	A	00 = Standard

All products shipped in JEDEC standard high profile (0.400" thick) trays (JEDEC Publication 95, Design Guide 4.10).

Standard Models

Part Number	Package Size	V_{IN}	K	V_{OUT}	Temperature	Current
MVTM36BF015M080A00	Full VIC SMD	26.0 V to 50.0 V	1/24	1.50 V (1.08 V to 2.08 V)	-55 to 125°C	80 A
MVTM36BT015M080A00	Full VIC TH					
MVTM36BF022M055A00	Full VIC SMD	26.0 V to 50.0 V	1/16	2.25 V (1.63 V to 3.13 V)	-55 to 125°C	55 A
MVTM36BT022M055A00	Full VIC TH					
MVTM36BF030M040B00	Full VIC SMD	26.0 V to 50.0 V	1/12	3.00 V (2.17 V to 4.17 V)	-55 to 125°C	40 A
MVTM36BT030M040B00	Full VIC TH					
MVTM36BF045M027A00	Full VIC SMD	26.0 V to 50.0 V	1/8	4.50 V (3.25 V to 6.25 V)	-55 to 125°C	27 A
MVTM36BT045M027A00	Full VIC TH					
MVTM36BF060M020A00	Full VIC SMD	26.0 V to 50.0 V	1/6	6.00 V (4.33 V to 8.33 V)	-55 to 125°C	20 A
MVTM36BT060M020A00	Full VIC TH					
MVTM36BF072M017A00	Full VIC SMD	26.0 V to 50.0 V	1/5	7.20 V (5.20 V to 10.0 V)	-55 to 125°C	17 A
MVTM36BT072M017A00	Full VIC TH					
MVTM36BF090M013A00	Full VIC SMD	26.0 V to 50.0 V	1/4	9.00 V (6.50 V to 12.5 V)	-55 to 125°C	13 A
MVTM36BT090M013A00	Full VIC TH					
MVTM36BF120M010A00	Full VIC SMD	26.0 V to 50.0 V	1/3	12.0 V (8.67 V to 16.7 V)	-55 to 125°C	10 A
MVTM36BT120M010A00	Full VIC TH					
MVTM36BF180M007A00	Full VIC SMD	26.0 V to 50.0 V	1/2	18.0 V (13.0 V to 25.0 V)	-55 to 125°C	7 A
MVTM36BT180M007A00	Full VIC TH					
MVTM36BF240M005A00	Full VIC SMD	26.0 V to 50.0 V	2/3	24.0 V (17.3 V to 33.3 V)	-55 to 125°C	5 A
MVTM36BT240M005A00	Full VIC TH					
MVTM36BF360M003A00	Full VIC SMD	26.0 V to 50.0 V	1	36.0 V (26.0 V to 50.0 V)	-55 to 125°C	3 A
MVTM36BT360M003A00	Full VIC TH					
MVTM36BH030M025A00	Half VIC SMD	26.0 V to 50.0 V	1/12	3.00 V (1.63 V to 3.13 V)	-55 to 125°C	25 A
MVTM36BH045M020A00	Half VIC SMD	26.0 V to 50.0 V	1/8	4.50 V (3.25 V to 6.25 V)	-55 to 125°C	20 A
MVTM36BH090M010A00	Half VIC SMD	26.0 V to 50.0 V	1/4	9.00 V (6.50 V to 12.5 V)	-55 to 125°C	10 A

Absolute Maximum Ratings

The absolute maximum ratings below are stress ratings only. Operation at or beyond these maximum ratings can cause permanent damage to the device.

Parameter	Comments	Min	Max	Unit
+IN to -IN		-1.0	60	V_{DC}
PC to -IN		-0.3	20	V_{DC}
TM to -IN		-0.3	7	V_{DC}
VC to -IN		-0.3	20	V_{DC}
IM to -IN	Half Chip only	0	3.15	V_{DC}
+IN / -IN to +OUT / -OUT (hipot)			2250	V_{DC}

General Electrical Characteristics

Specifications apply over all line and load conditions, unless otherwise noted; Boldface specifications apply over the temperature range of -55°C < T_J < 125°C (T-Grade); All other specifications are at T_J = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Input voltage range	V_{IN}	No external VC applied	**26**		**50**	V_{DC}
		VC applied	**0**		**50**	
V_{IN} slew rate	dV_{IN}/dt				**1**	V/µs
Output voltage ripple	V_{OUT_PP}	C_{OUT} = 0 F, I_{OUT} = Full Load, V_{IN} = 48 V, 20 MHz BW		5		% V_{OUT}
Protection						
Overvoltage lockout	V_{IN_OVLO+}	Module latched shutdown	**52.0**	56.0	**58.5**	V
Overvoltage lockout response time constant	t_{OVLO}	Effective internal RC filter		8		µs
Output overcurent trip	I_{OCP}			120		% I_{OUT_AVG}
Short circuit protection trip current	I_{SCP}			150		% I_{OUT_AVG}
Output overcurrent response time constant	t_{OCP}	Effective internal RC filter (Integrative)		3.8		ms
Short cicuit protection response time	t_{SCP}	From detection to cessation of switching (Instantaneous)		1		µs
Thermal shutdown setpoint	T_{J_OTP}		125	130	135	°C
Reverse inrush current protection		Reverse Inrush protection disabled for this product				

Model Specific Electrical Characteristics

Specifications apply over all line and load conditions, unless otherwise noted; Boldface specifications apply over the temperature range of -55°C < T_J < 125°C (T-Grade); All other specifications are at T_J = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
MVTM36BF015M080A00						
No load power dissipation	P_{NL}	V_{IN} = 26 V to 50 V			**7.5**	W
Transfer ratio	K	K = V_{OUT} / V_{IN}, I_{OUT} = 0 A		1/24		V/V
Ouput voltage	V_{OUT}	V_{OUT} = V_{IN} • K - I_{OUT} • R_{OUT}				V
Output current (average)	I_{OUT_AVG}				**80**	A
Output current (peak)	I_{OUT_PK}	t_{PEAK} < 10 ms, I_{OUT_AVG} ≤ 80 A			**120**	A
Efficiency (ambient)	η_{AMB}	V_{IN} = 36 V, I_{OUT} = 80 A	90.0	91.3		%
		V_{IN} = 26 V to 50 V, I_{OUT} = 80 A	87.3			
Output resistance (cold)	R_{OUT_COLD}	T_C = -40°C, I_{OUT} = 80 A	0.40	0.76	1.0	mΩ
Output resistance (ambient)	R_{OUT_AMB}	T_C = 25°C, I_{OUT} = 80 A	0.55	0.98	1.4	mΩ
Output resistance (hot)	R_{OUT_HOT}	T_C = 100°C, I_{OUT} = 80 A	0.65	1.18	1.5	mΩ
Switching frequency	f_{SW}		**1.50**	1.60	**1.70**	MHz
Output ripple frequency	f_{SW_RP}		**3.00**	3.20	**3.40**	MHz
MTBF		MIL-HDBK-217 Plus Parts Count; 25°C Ground Benign, Stationary, Indoors / Computer Profile		5.0		MHrs
		Telcordia Issue 2 - Method 1 Case 1; Ground Benign, Controlled		6.7		MHrs
VC internal resistor	$R_{VC\text{-}INT}$			2		kΩ
MVTM36BF022M055A00						
No load power dissipation	P_{NL}	V_{IN} = 26 V to 50 V			**8.6**	W
Transfer ratio	K	K = V_{OUT} / V_{IN}, I_{OUT} = 0 A		1/16		V/V
Ouput voltage	V_{OUT}	V_{OUT} = V_{IN} • K - I_{OUT} • R_{OUT}				V
Output current (average)	I_{OUT_AVG}				**55**	A
Output current (peak)	I_{OUT_PK}	t_{PEAK} < 10 ms, I_{OUT_AVG} ≤ 55 A			**82**	A
Efficiency (ambient)	η_{AMB}	V_{IN} = 36 V, I_{OUT} = 55 A	92.6	93.7		%
		V_{IN} = 26 V to 50 V, I_{OUT} = 55 A	88.8			
Output resistance (cold)	R_{OUT_COLD}	T_C = -40°C, I_{OUT} = 55 A	0.6	1.1	1.8	mΩ
Output resistance (ambient)	R_{OUT_AMB}	T_C = 25°C, I_{OUT} = 55 A	0.8	1.4	1.9	mΩ
Output resistance (hot)	R_{OUT_HOT}	T_C = 100°C, I_{OUT} = 55 A	1.0	1.7	2.2	mΩ
Switching frequency	f_{SW}		**1.36**	1.43	**1.50**	MHz
Output ripple frequency	f_{SW_RP}		**2.72**	2.86	**3.00**	MHz
MTBF		MIL-HDBK-217 Plus Parts Count; 25°C Ground Benign, Stationary, Indoors / Computer Profile		1.9		MHrs
		Telcordia Issue 2 - Method 1 Case 1; Ground Benign, Controlled		6.0		MHrs
VC internal resistor	$R_{VC\text{-}INT}$			1.0		kΩ

Model Specific Electrical Characteristics (Cont.)

Specifications apply over all line and load conditions, unless otherwise noted; Boldface specifications apply over the temperature range of -55°C < T_J < 125°C (T-Grade); All other specifications are at T_J = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
MVTM36BF030M040B00						
No load power dissipation	P_{NL}	V_{IN} = 26 V to 50 V			**12.0**	W
Transfer ratio	K	K = V_{OUT} / V_{IN}, I_{OUT} = 0 A		1/12		V/V
Ouput voltage	V_{OUT}	V_{OUT} = V_{IN} • K - I_{OUT} • R_{OUT}				V
Output current (average)	I_{OUT_AVG}				**40**	A
Output current (peak)	I_{OUT_PK}	t_{PEAK} < 10 ms, I_{OUT_AVG} ≤ 40 A			**60**	A
Efficiency (ambient)	η_{AMB}	V_{IN} = 36 V, I_{OUT} = 40 A	92.5	94.0		%
		V_{IN} = 26 V to 50 V, I_{OUT} = 40 A	90.2			
Output resistance (cold)	R_{OUT_COLD}	T_C = -40°C, I_{OUT} = 40 A	1.0	1.6	2.3	mΩ
Output resistance (ambient)	R_{OUT_AMB}	T_C = 25°C, I_{OUT} = 40 A	1.5	2.2	3.0	mΩ
Output resistance (hot)	R_{OUT_HOT}	T_C = 100°C, I_{OUT} = 40 A	2.0	2.6	3.3	mΩ
Switching frequency	f_{SW}		**1.36**	1.43	**1.50**	MHz
Output ripple frequency	f_{SW_RP}		**2.72**	2.86	**3.00**	MHz
MTBF		MIL-HDBK-217 Plus Parts Count; 25°C Ground Benign, Stationary, Indoors / Computer Profile		3.8		MHrs
		Telcordia Issue 2 - Method 1 Case 1; Ground Benign, Controlled		9.5		MHrs
VC internal resistor	$R_{VC\text{-}INT}$			1.0		kΩ
MVTM36BF045M027A00						
No load power dissipation	P_{NL}	V_{IN} = 26 V to 50 V			**7.0**	W
Transfer ratio	K	K = V_{OUT} / V_{IN}, I_{OUT} = 0 A		1/8		V/V
Ouput voltage	V_{OUT}	V_{OUT} = V_{IN} • K - I_{OUT} • R_{OUT}				V
Output current (average)	I_{OUT_AVG}				**27**	A
Output current (peak)	I_{OUT_PK}	t_{PEAK} < 10 ms, I_{OUT_AVG} ≤ 27 A			**40**	A
Efficiency (ambient)	η_{AMB}	V_{IN} = 36 V, I_{OUT} = 27 A	93.0	94.7		%
		V_{IN} = 26 V to 55 V, I_{OUT} = 27 A	89.3			
Output resistance (cold)	R_{OUT_COLD}	T_C = -40°C, I_{OUT} = 27 A	2.5	4.6	5.9	mΩ
Output resistance (ambient)	R_{OUT_AMB}	T_C = 25°C, I_{OUT} = 27 A	3.8	6.0	7.8	mΩ
Output resistance (hot)	R_{OUT_HOT}	T_C = 100°C, I_{OUT} = 27 A	4.5	7.1	9.0	mΩ
Switching frequency	f_{SW}		**1.10**	1.21	**1.30**	MHz
Output ripple frequency	f_{SW_RP}		**2.20**	2.42	**2.60**	MHz
MTBF		MIL-HDBK-217 Plus Parts Count; 25°C Ground Benign, Stationary, Indoors / Computer Profile		3.8		MHrs
		Telcordia Issue 2 - Method 1 Case 1; Ground Benign, Controlled		9.5		MHrs
VC internal resistor	$R_{VC\text{-}INT}$			1.0		kΩ

Model Specific Electrical Characteristics (Cont.)

Specifications apply over all line and load conditions, unless otherwise noted; Boldface specifications apply over the temperature range of -55°C < T_J < 125°C (T-Grade); All other specifications are at T_J = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
MVTM36BF060M020A00						
No load power dissipation	P_{NL}	V_{IN} = 26 V to 50 V			**14.0**	W
Transfer ratio	K	K = V_{OUT} / V_{IN}, I_{OUT} = 0 A		1/6		V/V
Ouput voltage	V_{OUT}	V_{OUT} = V_{IN} • K - I_{OUT} • R_{OUT}				V
Output current (average)	I_{OUT_AVG}				**20**	A
Output current (peak)	I_{OUT_PK}	t_{PEAK} < 10 ms, I_{OUT_AVG} ≤ 20 A			**30**	A
Efficiency (ambient)	η_{AMB}	V_{IN} = 36 V, I_{OUT} = 20 A	94.6	95.5		%
		V_{IN} = 26 V to 50 V, I_{OUT} = 20 A	92.0			
Output resistance (cold)	R_{OUT_COLD}	T_C = -40°C, I_{OUT} = 20 A	3.0	7.0	9.0	mΩ
Output resistance (ambient)	R_{OUT_AMB}	T_C = 25°C, I_{OUT} = 20 A	5.0	8.0	10.0	mΩ
Output resistance (hot)	R_{OUT_HOT}	T_C = 100°C, I_{OUT} = 20 A	6.0	12.0	15.0	mΩ
Switching frequency	f_{SW}		**1.47**	1.52	**1.57**	MHz
Output ripple frequency	f_{SW_RP}		**7.94**	3.04	**3.14**	MHz
MTBF		MIL-HDBK-217 Plus Parts Count; 25°C Ground Benign, Stationary, Indoors / Computer Profile		4.3		MHrs
		Telcordia Issue 2 - Method 1 Case 1; Ground Benign, Controlled		9.5		MHrs
VC internal resistor	$R_{VC\text{-}INT}$			0.56		kΩ
MVTM36BF072M017A00						
No load power dissipation	P_{NL}	V_{IN} = 26 V to 50 V			**14.0**	W
Transfer ratio	K	K = V_{OUT} / V_{IN}, I_{OUT} = 0 A		1/5		V/V
Ouput voltage	V_{OUT}	V_{OUT} = V_{IN} • K - I_{OUT} • R_{OUT}				V
Output current (average)	I_{OUT_AVG}				**17**	A
Output current (peak)	I_{OUT_PK}	t_{PEAK} < 10 ms, I_{OUT_AVG} ≤ 17 A			**25**	A
Efficiency (ambient)	η_{AMB}	V_{IN} = 36 V, I_{OUT} = 17 A	95.3	95.9		%
		V_{IN} = 26 V to 55 V, I_{OUT} = 17 A	92.0			
Output resistance (cold)	R_{OUT_COLD}	T_C = -40°C, I_{OUT} = 17 A	3.3	5.6	7.8	mΩ
Output resistance (ambient)	R_{OUT_AMB}	T_C = 25°C, I_{OUT} = 17 A	5.0	7.8	10.0	mΩ
Output resistance (hot)	R_{OUT_HOT}	T_C = 100°C, I_{OUT} = 17 A	7.0	9.1	12.0	mΩ
Switching frequency	f_{SW}		**1.50**	1.55	**1.60**	MHz
Output ripple frequency	f_{SW_RP}		**3.00**	3.10	**3.20**	MHz
MTBF		MIL-HDBK-217 Plus Parts Count; 25°C Ground Benign, Stationary, Indoors / Computer Profile		3.5		MHrs
		Telcordia Issue 2 - Method 1 Case 1; Ground Benign, Controlled		5.5		MHrs
VC internal resistor	$R_{VC\text{-}INT}$			0.56		kΩ

Model Specific Electrical Characteristics (Cont.)

Specifications apply over all line and load conditions, unless otherwise noted; Boldface specifications apply over the temperature range of -55°C < T_J < 125°C (T-Grade); All other specifications are at T_J = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
MVTM36BF090M013A00						
No load power dissipation	P_{NL}	V_{IN} = 26 V to 50 V			**14.0**	W
Transfer ratio	K	K = V_{OUT} / V_{IN}, I_{OUT} = 0 A		1/4		V/V
Ouput voltage	V_{OUT}	V_{OUT} = V_{IN} • K - I_{OUT} • R_{OUT}				V
Output current (average)	I_{OUT_AVG}				**13**	A
Output current (peak)	I_{OUT_PK}	t_{PEAK} < 10 ms, I_{OUT_AVG} ≤ 13 A			**19**	A
Efficiency (ambient)	η_{AMB}	V_{IN} = 36 V, I_{OUT} = 13 A	93.8	95.3		%
		V_{IN} = 26 V to 50 V, I_{OUT} = 13 A	93.5			
Output resistance (cold)	R_{OUT_COLD}	T_C = -40°C, I_{OUT} = 13 A	2.0	5.5	9.5	mΩ
Output resistance (ambient)	R_{OUT_AMB}	T_C = 25°C, I_{OUT} = 13 A	3.9	8.9	13.4	mΩ
Output resistance (hot)	R_{OUT_HOT}	T_C = 100°C, I_{OUT} = 13 A	5.0	10.6	15.9	mΩ
Switching frequency	f_{SW}		**1.85**	1.95	**2.05**	MHz
Output ripple frequency	f_{SW_RP}		**3.70**	3.90	**4.10**	MHz
MTBF		MIL-HDBK-217 Plus Parts Count; 25°C Ground Benign, Stationary, Indoors / Computer Profile		1.8		MHrs
		Telcordia Issue 2 - Method 1 Case 1; Ground Benign, Controlled		7.3		MHrs
VC internal resistor	$R_{VC\text{-}INT}$			0.51		kΩ
MVTM36BF120M010A00						
No load power dissipation	P_{NL}	V_{IN} = 26 V to 50 V			**10.5**	W
Transfer ratio	K	K = V_{OUT} / V_{IN}, I_{OUT} = 0 A		1/3		V/V
Ouput voltage	V_{OUT}	V_{OUT} = V_{IN} • K - I_{OUT} • R_{OUT}				V
Output current (average)	I_{OUT_AVG}				**10**	A
Output current (peak)	I_{OUT_PK}	t_{PEAK} < 10 ms, I_{OUT_AVG} ≤ 10 A			**15**	A
Efficiency (ambient)	η_{AMB}	V_{IN} = 36 V, I_{OUT} = 10 A	94.2	94.9		%
		V_{IN} = 26 V to 50 V, I_{OUT} = 10 A	90.0			
Output resistance (cold)	R_{OUT_COLD}	T_C = -40°C, I_{OUT} = 10 A	12.8	19.7	26.5	mΩ
Output resistance (ambient)	R_{OUT_AMB}	T_C = 25°C, I_{OUT} = 10 A	20.4	26.5	32.6	mΩ
Output resistance (hot)	R_{OUT_HOT}	T_C = 100°C, I_{OUT} = 10 A	23.1	29.2	35.2	mΩ
Switching frequency	f_{SW}		**1.56**	1.65	**1.74**	MHz
Output ripple frequency	f_{SW_RP}		**3.12**	3.30	**3.48**	MHz
MTBF		MIL-HDBK-217 Plus Parts Count; 25°C Ground Benign, Stationary, Indoors / Computer Profile		3.8		MHrs
		Telcordia Issue 2 - Method 1 Case 1; Ground Benign, Controlled		5.6		MHrs
VC internal resistor	$R_{VC\text{-}INT}$			2.0		kΩ

Model Specific Electrical Characteristics (Cont.)

Specifications apply over all line and load conditions, unless otherwise noted; Boldface specifications apply over the temperature range of -55°C < T_J < 125°C (T-Grade); All other specifications are at T_J = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
MVTM36BF180M007A00						
No load power dissipation	P_{NL}	V_{IN} = 26 V to 50 V			**13.5**	W
Transfer ratio	K	K = V_{OUT} / V_{IN}, I_{OUT} = 0 A		1/2		V/V
Ouput voltage	V_{OUT}	V_{OUT} = V_{IN} • K - I_{OUT} • R_{OUT}				V
Output current (average)	I_{OUT_AVG}				**7**	A
Output current (peak)	I_{OUT_PK}	t_{PEAK} < 10 ms, I_{OUT_AVG} ≤ 7 A			**10**	A
Efficiency (ambient)	η_{AMB}	V_{IN} = 36 V, I_{OUT} = 7 A	93.0	94.0		%
		V_{IN} = 26 V to 50 V, I_{OUT} = 7 A	92.0			
Output resistance (cold)	R_{OUT_COLD}	T_C = -40°C, I_{OUT} = 7 A	19.7	40.0	60.7	mΩ
Output resistance (ambient)	R_{OUT_AMB}	T_C = 25°C, I_{OUT} = 7 A	30.0	55.0	75.0	mΩ
Output resistance (hot)	R_{OUT_HOT}	T_C = 100°C, I_{OUT} = 7 A	35.0	60.0	90.0	mΩ
Switching frequency	f_{SW}		**1.68**	1.77	**1.86**	MHz
Output ripple frequency	f_{SW_RP}		**3.36**	3.54	**3.72**	MHz
MTBF		MIL-HDBK-217 Plus Parts Count; 25°C Ground Benign, Stationary, Indoors / Computer Profile		3.8		MHrs
		Telcordia Issue 2 - Method 1 Case 1; Ground Benign, Controlled		5.7		MHrs
VC internal resistor	$R_{VC\text{-}INT}$			0.51		kΩ
MVTM36BF240M005A00						
No load power dissipation	P_{NL}	V_{IN} = 26 V to 50 V			**8.5**	W
Transfer ratio	K	K = V_{OUT} / V_{IN}, I_{OUT} = 0 A		2/3		V/V
Ouput voltage	V_{OUT}	V_{OUT} = V_{IN} • K - I_{OUT} • R_{OUT}				V
Output current (average)	I_{OUT_AVG}				**5**	A
Output current (peak)	I_{OUT_PK}	t_{PEAK} < 10 ms, I_{OUT_AVG} ≤ 5 A			**7.5**	A
Efficiency (ambient)	η_{AMB}	V_{IN} = 36 V, I_{OUT} = 5 A	93.5	96.0		%
		V_{IN} = 26 V to 50 V, I_{OUT} = 5 A	93.0			
Output resistance (cold)	R_{OUT_COLD}	T_C = -40°C, I_{OUT} = 5 A	40.0	51.4	70.0	mΩ
Output resistance (ambient)	R_{OUT_AMB}	T_C = 25°C, I_{OUT} = 5 A	64.0	86.0	120.0	mΩ
Output resistance (hot)	R_{OUT_HOT}	T_C = 100°C, I_{OUT} = 5 A	85.0	102.0	135	mΩ
Switching frequency	f_{SW}		**1.57**	1.60	**1.63**	MHz
Output ripple frequency	f_{SW_RP}		**3.14**	3.20	**3.26**	MHz
MTBF		MIL-HDBK-217 Plus Parts Count; 25°C Ground Benign, Stationary, Indoors / Computer Profile		3.8		MHrs
		Telcordia Issue 2 - Method 1 Case 1; Ground Benign, Controlled		5.6		MHrs
VC internal resistor	$R_{VC\text{-}INT}$			2.0		kΩ

Model Specific Electrical Characteristics (Cont.)

Specifications apply over all line and load conditions, unless otherwise noted; Boldface specifications apply over the temperature range of -55°C < T_J < 125°C (T-Grade); All other specifications are at T_J = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
MVTM36BF360M003A00						
No load power dissipation	P_{NL}	V_{IN} = 26 V to 50 V			**9.0**	W
Transfer ratio	K	K = V_{OUT} / V_{IN}, I_{OUT} = 0 A		1		V/V
Ouput voltage	V_{OUT}	V_{OUT} = V_{IN} • K - I_{OUT} • R_{OUT}				V
Output current (average)	I_{OUT_AVG}				**3**	A
Output current (peak)	I_{OUT_PK}	t_{PEAK} < 10 ms, I_{OUT_AVG} ≤ 3 A			**4.5**	A
Efficiency (ambient)	η_{AMB}	V_{IN} = 36 V, I_{OUT} = 3 A	95.3	96.0		%
		V_{IN} = 26 V to 50 V, I_{OUT} = 3 A	93.3			
Output resistance (cold)	R_{OUT_COLD}	T_C = -40°C, I_{OUT} = 3 A	55.0	108.0	175.0	mΩ
Output resistance (ambient)	R_{OUT_AMB}	T_C = 25°C, I_{OUT} = 3 A	120.0	158.0	200.0	mΩ
Output resistance (hot)	R_{OUT_HOT}	T_C = 100°C, I_{OUT} = 3 A	175.0	205.0	235.0	mΩ
Switching frequency	f_{SW}		**1.64**	1.67	**1.70**	MHz
Output ripple frequency	f_{SW_RP}		**3.28**	3.34	**3.40**	MHz
MTBF		MIL-HDBK-217 Plus Parts Count; 25°C Ground Benign, Stationary, Indoors / Computer Profile		3.8		MHrs
		Telcordia Issue 2 - Method 1 Case 1; Ground Benign, Controlled		5.6		MHrs
VC internal resistor	$R_{VC\text{-}INT}$			2.0		kΩ

Model Specific Electrical Characteristics (Cont.)

Specifications apply over all line and load conditions, unless otherwise noted; Boldface specifications apply over the temperature range of -55°C < T_J < 125°C (T-Grade); All other specifications are at T_J = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
MVTM36BH030M025A00						
No load power dissipation	P_{NL}	V_{IN} = 26 V to 50 V			**5.0**	W
Transfer ratio	K	K = V_{OUT} / V_{IN}, I_{OUT} = 0 A		1/12		V/V
Ouput voltage	V_{OUT}	V_{OUT} = V_{IN} • K - I_{OUT} • R_{OUT}				V
Output current (average)	I_{OUT_AVG}				**25.0**	A
Output current (peak)	I_{OUT_PK}	t_{PEAK} < 10 ms, I_{OUT_AVG} ≤ 25 A			**37.5**	A
Efficiency (ambient)	η_{AMB}	V_{IN} = 36 V, I_{OUT} = 25 A	88.5	90.8		%
		V_{IN} = 26 V to 50 V, I_{OUT} = 25 A	85.5			
Output resistance (cold)	R_{OUT_COLD}	T_C = -40°C, I_{OUT} = 25 A	2.0	5.3	8.5	mΩ
Output resistance (ambient)	R_{OUT_AMB}	T_C = 25°C, I_{OUT} = 25 A	4.5	7.3	10.0	mΩ
Output resistance (hot)	R_{OUT_HOT}	T_C = 100°C, I_{OUT} = 25 A	5.0	8.0	12.0	mΩ
Switching frequency	f_{SW}		**1.50**	1.65	**1.80**	MHz
Output ripple frequency	f_{SW_RP}		**3.00**	3.30	**3.60**	MHz
MTBF		MIL-HDBK-217 Plus Parts Count; 25°C Ground Benign, Stationary, Indoors / Computer Profile		4.5		MHrs
VC internal resistor	$R_{VC\text{-}INT}$			8.87		kΩ

Current Monitor: IM

• The IM pin provides a DC analog voltage proportional to the output current of the VTM.

SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
ANALOG INPUT	**Steady**	IM voltage (no load)	V_{IM_NL}	T_C = 25°C, V_{IN} = 42 V, I_{OUT} = 0 A	0.30	0.32	0.38	V
		IM voltage (50%)	$V_{IM_50\%}$	T_C = 25°C, V_{IN} = 42 V, I_{OUT} = 12.5 A		0.94		V
		IM voltage (full load)	V_{IM_FL}	T_C = 25°C, V_{IN} = 42 V, I_{OUT} = 25 A		1.80		V
		IM gain	A_{IM}	T_C = 25°C, V_{IN} = 42 V, I_{OUT} > 12.5 A		69		mV/A
		IM resistance (external)	R_{IM_EXT}		**2.5**			MΩ

Model Specific Electrical Characteristics (Cont.)

Specifications apply over all line and load conditions, unless otherwise noted; Boldface specifications apply over the temperature range of -55°C < T_J < 125°C (T-Grade); All other specifications are at T_J = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
MVTM36BH045M020A00						
No load power dissipation	P_{NL}	V_{IN} = 26 V to 50 V			**5.6**	W
Transfer ratio	K	K = V_{OUT} / V_{IN}, I_{OUT} = 0 A		1/8		V/V
Ouput voltage	V_{OUT}	V_{OUT} = V_{IN} • K - I_{OUT} • R_{OUT}				V
Output current (average)	I_{OUT_AVG}				**20**	A
Output current (peak)	I_{OUT_PK}	t_{PEAK} < 10 ms, I_{OUT_AVG} ≤ 20 A			**30**	A
Efficiency (ambient)	η_{AMB}	V_{IN} = 48 V, I_{OUT} = 20 A	91.0	92.9		%
		V_{IN} = 26 V to 55 V, I_{OUT} = 20 A	89.5			
Output resistance (cold)	R_{OUT_COLD}	T_C = -40°C, I_{OUT} = 20 A	5.0	8.2	13.0	mΩ
Output resistance (ambient)	R_{OUT_AMB}	T_C = 25°C, I_{OUT} = 20 A	7.0	10.8	15.0	mΩ
Output resistance (hot)	R_{OUT_HOT}	T_C = 100°C, I_{OUT} = 20 A	9.0	13.2	18.0	mΩ
Switching frequency	f_{SW}		**1.37**	1.50	**1.63**	MHz
Output ripple frequency	f_{SW_RP}		**2.74**	3.00	**3.26**	MHz
MTBF		MIL-HDBK-217 Plus Parts Count; 25°C Ground Benign, Stationary, Indoors / Computer Profile		6.0		MHrs
VC internal resistor	$R_{VC\text{-}INT}$			4.64		kΩ

Current Monitor: IM

• The IM pin provides a DC analog voltage proportional to the output current of the VTM.

SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
ANALOG INPUT	**Steady**	IM voltage (no load)	V_{IM_NL}	T_C = 25°C, V_{IN} = 48 V, I_{OUT} = 0 A	0.27	0.33	0.37	V
		IM voltage (50%)	$V_{IM_50\%}$	T_C = 25°C, V_{IN} = 48 V, I_{OUT} = 10 A		1.0		V
		IM voltage (full load)	V_{IM_FL}	T_C = 25°C, V_{IN} = 48 V, I_{OUT} = 20 A		1.91		V
		IM gain	A_{IM}	T_C = 25°C, V_{IN} = 48 V, I_{OUT} > 10 A		91		mV/A
		IM resistance (external)	R_{IM_EXT}		**2.5**			MΩ

Model Specific Electrical Characteristics (Cont.)

Specifications apply over all line and load conditions, unless otherwise noted; Boldface specifications apply over the temperature range of -55°C < T_J < 125°C (T-Grade); All other specifications are at T_J = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
MVTM36BH090M010A00						
No load power dissipation	P_{NL}	V_{IN} = 26 V to 50 V			**5.2**	W
Transfer ratio	K	K = V_{OUT} / V_{IN}, I_{OUT} = 0 A		1/4		V/V
Ouput voltage	V_{OUT}	V_{OUT} = V_{IN} • K - I_{OUT} • R_{OUT}				V
Output current (average)	I_{OUT_AVG}				**10**	A
Output current (peak)	I_{OUT_PK}	t_{PEAK} < 10 ms, I_{OUT_AVG} ≤ 10 A			**15**	A
Efficiency (ambient)	η_{AMB}	V_{IN} = 36 V, I_{OUT} = 10 A	92.0	93.6		%
		V_{IN} = 26 V to 50 V, I_{OUT} = 10 A	90.0			
Output resistance (cold)	R_{OUT_COLD}	T_C = -40°C, I_{OUT} = 10 A	20.0	27.0	35.0	mΩ
Output resistance (ambient)	R_{OUT_AMB}	T_C = 25°C, I_{OUT} = 10 A	28.0	36.2	45.0	mΩ
Output resistance (hot)	R_{OUT_HOT}	T_C = 100°C, I_{OUT} = 10 A	35.0	44.4	55.0	mΩ
Switching frequency	f_{SW}		**1.60**	1.75	**1.90**	MHz
Output ripple frequency	f_{SW_RP}		**3.20**	3.50	**3.80**	MHz
MTBF		MIL-HDBK-217 Plus Parts Count; 25°C Ground Benign, Stationary, Indoors / Computer Profile		4.5		MHrs
VC internal resistor	$R_{VC\text{-}INT}$			2.05		kΩ

Current Monitor: IM

• The IM pin provides a DC analog voltage proportional to the output current of the VTM.

SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
ANALOG INPUT	**Steady**	IM voltage (no load)	V_{IM_NL}	T_C = 25°C, V_{IN} = 48 V, I_{OUT} = 0 A	0.28	0.35	0.42	V
		IM voltage (50%)	$V_{IM_50\%}$	T_C = 25°C, V_{IN} = 48 V, I_{OUT} = 5 A		0.90		V
		IM voltage (full load)	V_{IM_FL}	T_C = 25°C, V_{IN} = 48 V, I_{OUT} = 10 A		1.68		V
		IM gain	A_{IM}	T_C = 25°C, V_{IN} = 48 V, I_{OUT} > 5 A		156		mV/A
		IM resistance (external)	R_{IM_EXT}		**2.5**			MΩ

Signal Characteristics

Specifications apply over all line and load conditions, unless otherwise noted; Boldface specifications apply over the temperature range of -55°C < T_J < 125°C (T-Grade); All other specifications are at T_J = 25°C unless otherwise noted.

VTM Control: VC

- Used to wake up powertrain circuit.
- A minimum of 12 V must be applied indefinitely for V_{IN} ≤ 26 V to ensure normal operation.
- VC slew rate must be within range for a successful start.
- PRM® VC can be used as valid wake-up signal source.
- VC voltage may be continuously applied; there will be minimal VC current drawn when V_{IN} ≥ 26 V and VC ≤ 13.
- Internal resistance used in adaptive loop compensation

SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
ANALOG INPUT	Steady	External VC voltage	V_{VC_EXT}	Required for startup, and operation below 26 V.	**12**		**16.5**	V
		VC current draw threshold	V_{VC_TH}	Low VC current draw for Vin >26 V		13		V
		VC current draw	I_{VC}	VC = 13 V, V_{IN} = 0 V			**150**	mA
				VC = 13 V, V_{IN} > 26 V		0		
				VC = 16.5 V, V_{IN} > 26 V		0		
	Start Up	VC slew rate	dVC/dt	Required for proper startup	**0.02**		**0.25**	V/µs
		VC inrush current	I_{INR_VC}	VC = 16.5 V, dVC/dt = 0.25 V/µs			**750**	mA
	Transitional	VC output turn-on delay	t_{ON}	V_{IN} pre-applied, PC floating, VC enable; C_{PC} = 0 µF, C_{OUT} = 4000 µF			**500**	µs
		VC to PC delay	t_{VC_PC}	VC = 12 V to PC high, V_{IN} = 0 V, dVC/dt = 0.25 V/µs		10	**25**	µs

Primary Control: PC

- The PC pin enables and disables the VTM. When held below 2 V, the VTM will be disabled.
- PC pin outputs 5 V during normal operation. PC pin is equal to 2.5 V during fault mode given Vin ≥ 26 V and VC ≥ 12 V.
- After successful start-up and under no fault condition, PC can be used as a 5 V regulated voltage source with a 2 mA maximum current.
- Module will shutdown when pulled low with an impedance less than 400 Ω.
- In an array of VTMs, connect PC pin to synchronize startup.
- PC pin cannot sink current and will not disable other modules during fault mode.

SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
ANALOG INPUT	Steady	PC voltage	V_{PC}		**4.7**	5.0	**5.3**	V
		PC source current	I_{PC_OP}				2	mA
		PC resistance (internal)	R_{PC_INT}	Internal pull down resistor	**50**	150	**400**	kΩ
	Start Up	PC source current	I_{PC_EN}		**50**	100	**300**	µA
		PC capacitance (internal)	C_{PC_INT}				**50**	pF
		PC resistance (external)	R_{PC_EXT}		**60**			kΩ
DIGITAL INPUT / OUTPUT	Enable	PC voltage (enable)	V_{PC_EN}		**2**	2.5	**3**	V
	Disable	PC voltage (disable)	V_{PC_DIS}				**2**	V
		PC pull down current	I_{PC_PD}		**5.1**			mA
	Transitional	PC disable time	$t_{PC_DIS_T}$			4		µs
		PC fault response time	t_{FR_PC}	From fault to PC = 2 V		100		µs

Signal Characteristics (Cont.)

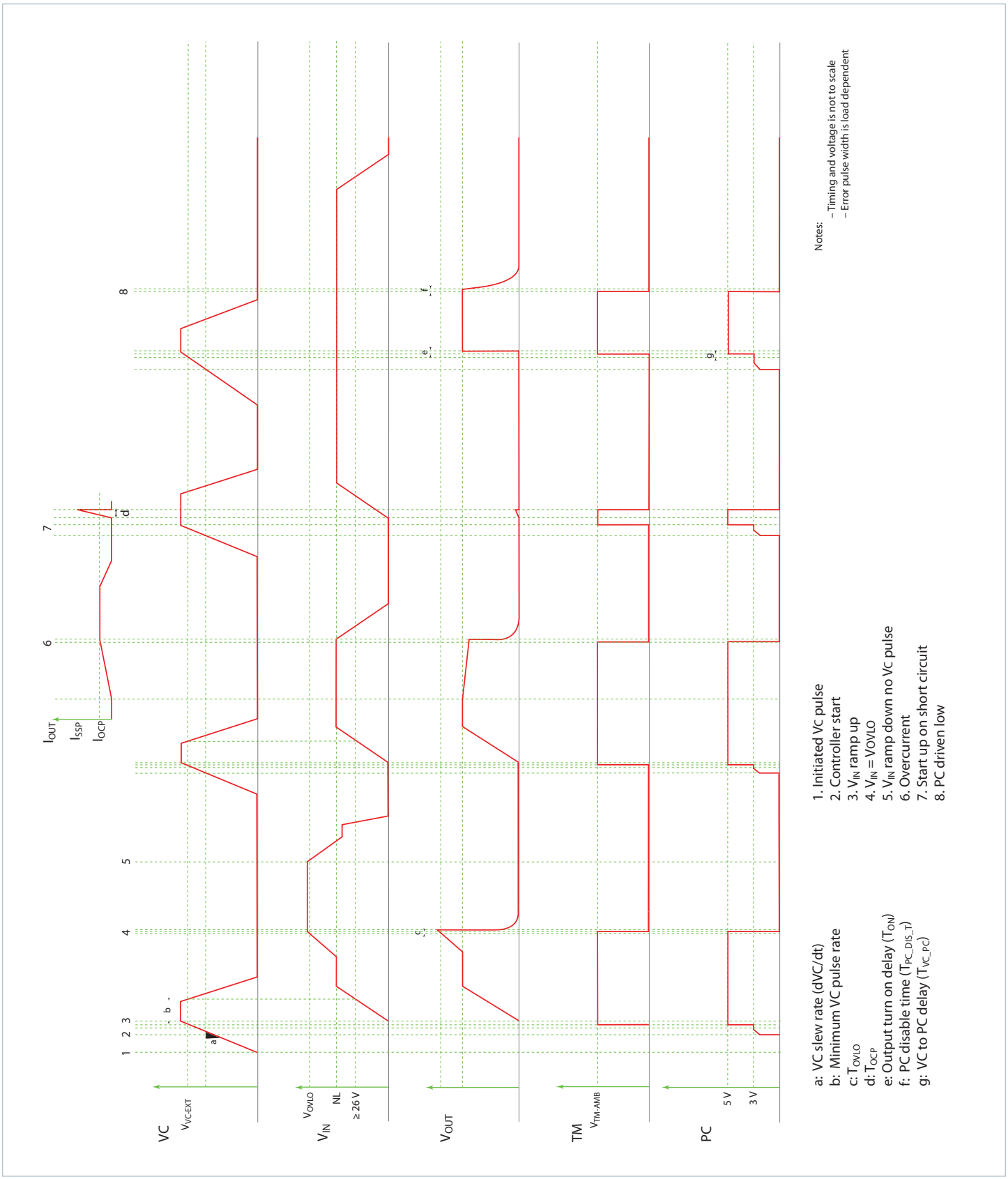
Specifications apply over all line and load conditions, unless otherwise noted; Boldface specifications apply over the temperature range of -55°C < T_J < 125°C (T-Grade); All other specifications are at T_J = 25°C unless otherwise noted.

Temperature Monitor: TM

- The TM pin monitors the internal temperature of the VTM controller IC within an accuracy of ±5°C.
- Can be used as a "Power Good" flag to verify that the VTM is operating.
- The TM pin has a room temperature setpoint of 3 V (@27°C) and approximate gain of 10 mV/ °C.

SIGNAL TYPE	STATE	ATTRIBUTE	SYMBOL	CONDITIONS / NOTES	MIN	TYP	MAX	UNIT
ANALOG OUTPUT	Steady	TM voltage	V_{TM_AMB}	T_J controller = 27°C	2.95	3.00	3.05	V
		TM source current	I_{TM}				**100**	µA
		TM gain	A_{TM}			10		mV/°C
DIGITAL OUTPUT (FAULT FLAG)	Disable	TM voltage	V_{TM_DIS}			0		V
	Transitional	TM resistance (internal)	R_{TM_INT}	Internal pull down resistor	**25**	40	**50**	kΩ
		TM capacitance (external)	C_{TM_EXT}				**50**	pF
		TM fault response time	t_{FR_TM}	From fault to TM = 1.5 V		10		µs

Timing diagram



General Characteristics

Specifications apply over all line and load conditions, unless otherwise noted; Boldface specifications apply over the temperature range of -55°C < T_J < 125°C (T-Grade); All other specifications are at T_J = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Mechanical						
(Full VIC)						
Length	L		32.25 / [1.270]	32.5 / [1.280]	32.75 / [1.289]	mm/[in]
Width	W		21.75 / [0.856]	22.0 / [0.866]	22.25 / [0.876]	mm/[in]
Height	H		6.48 / [0.255]	6.73 / [0.265]	6.98 / [0.275]	mm/[in]
Volume	Vol	No heat sink		4.81 / [0.294]		cm^3/[in^3]
Weight	W			15.0 / [0.53]		g/[oz]
(Half VIC)						
Length	L		21.7 / [0.85]	22.0 / [0.87]	22.3 / [0.88]	mm/[in]
Width	W		16.4 / [0.64]	16.5 / [0.65]	16.6 / [0.66]	mm/[in]
Height	H		6.48 / [0.255]	6.73 / [0.265]	6.98 / [0.275]	mm/[in]
Volume	Vol	No heat sink		2.44 / [0.150]		cm^3/[in^3]
Weight	W			8.0 / [0.28]		g/[oz]
Lead finish		Nickel	0.51		2.03	µm
		Palladium	0.02		0.15	
		Gold	0.003		0.051	
Thermal						
Operating temperature	T_J		-55		125	°C
Thermal Resistance (Full VIC)	Φ_{JC}	Isothermal heat sink and isothermal internal PCB		1		°C/W
Thermal Resistance (Half VIC)	Φ_{JC}	Isothermal heat sink and isothermal internal PCB		2.2		°C/W
Assembly						
Storage temperature	T_{ST}		-65		125	°C
ESD withstand	ESD_{HBM}	Human Body Model Component Level ANSI/ESDA/JEDEC JS-001-2012, Class 1C 1000 to <2000 V	1000			V_{DC}
	ESD_{CDM}	Field Induced Change Device Model JESD22-C101E, Class II 200 to <500 V	200			

General Characteristics Cont.

Specifications apply over all line and load conditions, unless otherwise noted; Boldface specifications apply over the temperature range of -55°C < T_J < 125°C (T-Grade); All other specifications are at T_J = 25°C unless otherwise noted.

Attribute	Symbol	Conditions / Notes	Min	Typ	Max	Unit
Soldering						
Peak temperature during reflow		MSL 4 (Datecode 1528 and later)			245	°C
Peak time above 217°C				60	90	s
Peak heating rate during reflow				1.5	3	°C/s
Peak cooling rate post reflow				1.5	6	°C/s
Safety						
Isolation voltage (hipot)	V_{HIPOT}		**2250**			V_{DC}
Isolation resistance	R_{IN_OUT}		**10**			MΩ
Agency approvals / standards		cTUVus				
		cURus				
		CE Marked for low voltage directive and RoHS recast directive, as applicable				

Using the control signals VC, PC, TM, IM

The VTM Control (VC) pin is an input pin which powers the internal VCC circuitry when within the specified voltage range of 12 V to 16.5 V. This voltage is required in order for the VTM module to start, and must be applied as long as the input is below 26 V. In order to ensure a proper start, the slew rate of the applied voltage must be within the specified range.

Some additional notes on the using the VC pin:

- In most applications, the VTM module will be powered by an upstream PRM® which provides a 10 ms VC pulse during startup. In these applications the VC pins of the PRM and VTM should be tied together.
- The VC voltage can be applied indefinitely allowing for continuous operation down to 0 V_{IN}.
- The fault response of the VTM module is latching. A positive edge on VC is required in order to restart the unit. If VC is continuously applied the PC pin may be toggled to restart the module.

Primary Control (PC) pin can be used to accomplish the following functions:

- Delayed start: Upon the application of VC, the PC pin will source a constant 100 µA current to the internal RC network. Adding an external capacitor will allow further delay in reaching the 2.5 V threshold for module start.
- Auxiliary voltage source: Once enabled in regular operational conditions (no fault), each VTM PC provides a regulated 5 V, 2 mA voltage source.
- Output disable: PC pin can be actively pulled down in order to disable the module. Pull down impedance shall be lower than 400 Ω.
- Fault detection flag: The PC 5 V voltage source is internally turned off as soon as a fault is detected. It is important to notice that PC doesn't have current sink capability. Therefore, in an array, PC line will not be capable of disabling neighboring modules if a fault is detected.
- Fault reset: PC may be toggled to restart the unit if VC is continuously applied.

Temperature Monitor (TM) pin provides a voltage proportional to the absolute temperature of the converter control IC.

It can be used to accomplish the following functions:

- Monitor the control IC temperature: The temperature in Kelvin is equal to the voltage on the TM pin scaled by 100. (i.e. 3.0 V = 300 K = 27ºC). If a heat sink is applied, TM can be used to thermally protect the system.
- Fault detection flag: The TM voltage source is internally turned off as soon as a fault is detected. For system monitoring purposes (microcontroller interface) faults are detected on falling edges of TM signal.

Current Monitor (IM) (half chip models only) pin provides a voltage proportional to the output current of the VTM module. The nominal voltage will vary between V_{IM_NL} to V_{IM_FL} over the output current range of the module. The accuracy of the IM pin will be within 25% under all line and temperature conditions between 50% and 100% load.

Startup behavior

Depending on the sequencing of the VC with respect to the input voltage, the behavior during startup will vary as follows:

- Normal Operation (VC applied prior to Vin): In this case the controller is active prior to ramping the input. When the input voltage is applied, the VTM output voltage will track the input. The inrush current is determined by the input voltage rate of rise and output capacitance. If the VC voltage is removed prior to the input reaching 26 V, the VTM module may shut down.
- Stand Alone Operation (VC applied after Vin): In this case the module output will begin to rise upon the application of the VC voltage. A soft-start circuit may vary the ouput rate of rise in order to limit the inrush current to it's maximum level. When starting into high capacitance, or a short, the output current will be limited for a maximum of 900 µsec. After this period, the adaptive soft start circuit will time out and the module may shut down. No restart will be attempted until VC is re-applied, or PC is toggled. To ensure a successful start in this mode of operation, additional capacitance on the output of the VTM should be kept to a minimum.

Thermal Considerations

VI Chip® products are multi-chip modules whose temperature distribution varies greatly for each part number as well as with the input / output conditions, thermal management and environmental conditions. Maintaining the top of the VTM case to less than 100ºC will keep all junctions within the VI Chip below 125ºC for most applications.

The percent of total heat dissipated through the top surface versus through the J-lead is entirely dependent on the particular mechanical and thermal environment. The heat dissipated through the top surface is typically 60%. The heat dissipated through the J-lead onto the PCB board surface is typically 40%. Use 100% top surface dissipation when designing for a conservative cooling solution.

It is not recommended to use a VI Chip module for an extended period of time at full load without proper heat sinking

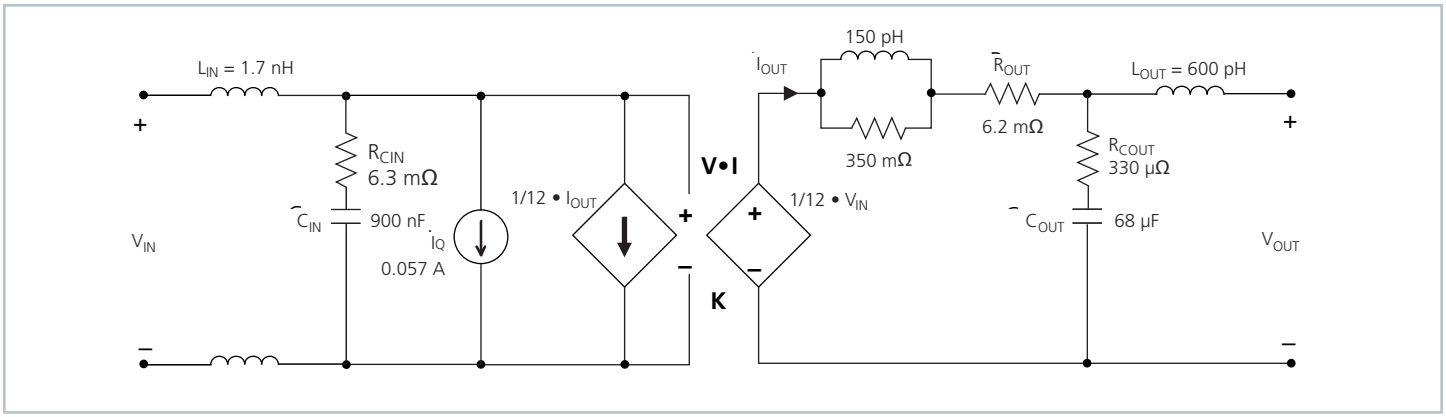


Figure 1 — *VI Chip® module AC model (MVTM48EH040M025A00 shown)*

Sine Amplitude Converter™ Point of Load Conversion

The Sine Amplitude Converter (SAC™) uses a high frequency resonant tank to move energy from input to output. The resonant LC tank, operated at high frequency, is amplitude modulated as function of input voltage and output current. A small amount of capacitance embedded in the input and output stages of the module is sufficient for full functionality and is key to achieving power density.

A typical SAC can be simplified into the model above.

At no load:

$$V_{OUT} = V_{IN} \bullet K \qquad (1)$$

K represents the "turns ratio" of the SAC. Rearranging Eq (1):

$$K = \frac{V_{OUT}}{V_{IN}} \qquad (2)$$

In the presence of load, Vout is represented by:

$$V_{OUT} = V_{IN} \bullet K - I_{OUT} \bullet R_{OUT} \qquad (3)$$

and Iout is represented by:

$$I_{OUT} = \frac{I_{IN} - I_Q}{K} \qquad (4)$$

R_{OUT} represents the impedance of the SAC, and is a function of the R_{DSON} of the input and output MOSFETs and the winding resistance of the power transformer. Iq represents the quiescent current of the SAC control and gate drive circuitry.

The use of DC voltage transformation provides additional interesting attributes. Assuming for the moment that $R_{OUT} = 0\ \Omega$ and $I_Q = 0$ A, Eq. (3) now becomes Eq. (1) and is essentially load independent. A resistor R is now placed in series with V_{IN} as shown in Figure 2.

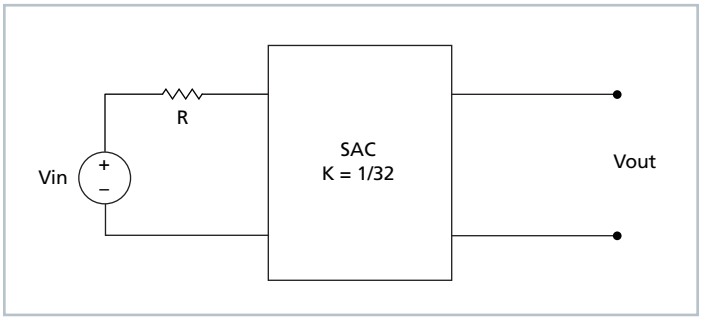


Figure 2 — *K = 1/32 Sine Amplitude Converter™ with series input resistor*

The relationship between V_{IN} and V_{OUT} becomes:

$$V_{OUT} = (V_{IN} - I_{IN} \bullet R) \bullet K \qquad (5)$$

Substituting the simplified version of Eq. (4) (I_Q is assumed = 0 A) into Eq. (5) yields:

$$V_{OUT} = V_{IN} \bullet K - I_{OUT} \bullet R \bullet K^2 \qquad (6)$$

This is similar in form to Eq. (3), where R_{OUT} is used to represent the characteristic impedance of the SAC™. However, in this case a real R on the input side of the SAC is effectively scaled by K^2 with respect to the output.

Assuming that R = 1 Ω, the effective R as seen from the secondary side is 0.98 mΩ, with K = 1/32 as shown in Figure 2.

A similar exercise should be performed with the additon of a capacitor, or shunt impedance, at the input to the SAC. A switch in series with V_{IN} is added to the circuit. This is depicted in Figure 3.

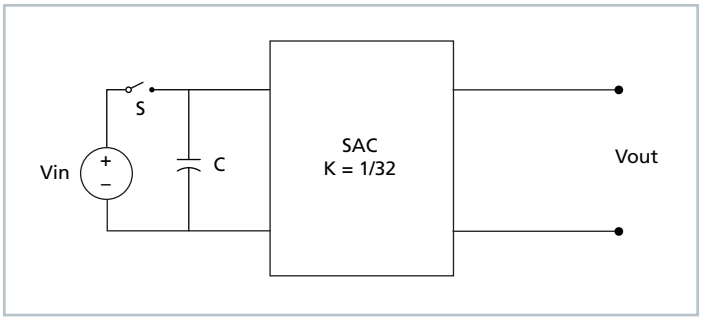


Figure 3 — *Sine Amplitude Converter™ with input capacitor*

A change in V_{IN} with the switch closed would result in a change in capacitor current according to the following equation:

$$I_C(t) = C\frac{dVin}{dt} \qquad (7)$$

Assume that with the capacitor charged to V_{IN}, the switch is opened and the capacitor is discharged through the idealized SAC. In this case,

$$I_C = I_{OUT} \bullet K \qquad (8)$$

Substituting Eq. (1) and (8) into Eq. (7) reveals:

$$I_{OUT} = \frac{C}{K^2} \bullet \frac{dV_{OUT}}{dt} \qquad (9)$$

Writing the equation in terms of the output has yielded a K^2 scaling factor for C, this time in the denominator of the equation. For a K factor less than unity, this results in an effectively larger capacitance on the output when expressed in terms of the input. With a K = 1/32 as shown in Figure 3, C = 1 µF would effectively appear as C = 1024 µF when viewed from the output.

Low impedance is a key requirement for powering a high-current, low-voltage load efficiently. A switching regulation stage should have minimal impedance, while simultaneously providing appropriate filtering for any switched current. The use of a SAC between the regulation stage and the point of load provides a dual benefit, scaling down series impedance leading back to the source and scaling up shunt capacitance (or energy storage) as a function of its K factor squared. However, these benefits are not useful if the series impedance of the SAC is too high. The impedance of the SAC must be low well beyond the crossover frequency of the system.

A solution for keeping the impedance of the SAC low involves switching at a high frequency. This enables magnetic components to be small since magnetizing currents remain low. Small magnetics mean small path lengths for turns. Use of low loss core material at high frequencies reduces core losses as well.

The two main terms of power loss in the VTM module are:

- No load power dissipation (Pnl): defined as the power used to power up the module with an enabled power train at no load.
- Resistive loss (R_{OUT}): refers to the power loss across the VTM current multiplier modeled as pure resistive impedance.

$$P_{DISSIPATED} = P_{NL} + P_{ROUT} \qquad (10)$$

Therefore,

$$P_{OUT} = P_{IN} - P_{DISSIPATED} = P_{IN} - P_{NL} - P_{ROUT} \qquad (11)$$

The above relations can be combined to calculate the overall module efficiency:

$$\eta = \frac{P_{OUT}}{P_{IN}} = \frac{P_{IN} - P_{NL} - P_{ROUT}}{P_{IN}} \qquad (12)$$

$$= \frac{V_{IN} \bullet I_{IN} - P_{NL} - (I_{OUT})^2 \bullet R_{OUT}}{V_{IN} \bullet I_{IN}}$$

$$= 1 - \left(\frac{P_{NL} + (I_{OUT})2 \bullet R_{OUT}}{V_{IN} \bullet I_{IN}}\right)$$

Input and Output Filter Design

A major advantage of a SAC™ system versus a conventional PWM converter is that the former does not require large functional filters. The resonant LC tank, operated at extreme high frequency, is amplitude modulated as a function of input voltage and output current and efficiently transfers charge through the isolation transformer. A small amount of capacitance embedded in the input and output stages of the module is sufficient for full functionality and is key to achieving high power density.

This paradigm shift requires system design to carefully evaluate external filters in order to:

1. Guarantee low source impedance.

   To take full advantage of the VTM module dynamic response, the impedance presented to its input terminals must be low from DC to approximately 5 MHz. Input capacitance may be added to improve transient performance or compensate for high source impedance.
2. Further reduce input and/or output voltage ripple without sacrificing dynamic response.

   Given the wide bandwidth of the VTM module, the source response is generally the limiting factor in the overall system response. Anomalies in the response of the source will appear at the output of the module multiplied by its K factor.
3. Protect the module from overvoltage transients imposed by the system that would exceed maximum ratings and cause failures.

   The VI Chip® module input/output voltage ranges must not be exceeded. An internal overvoltage lockout function prevents operation outside of the normal operating input range. Even during this condition, the powertrain is exposed to the applied voltage and power MOSFETs must withstand it.

Capacitive Filtering Considerations for a Sine Amplitude Converter

It is important to consider the impact of adding input and output capacitance to a Sine Amplitude Converter™ on the system as a whole. Both the capacitance value, and the effective impedance of the capacitor must be considered.

A Sine Amplitude Converter has a DC R_{OUT} value which has already been discussed in the previous section. The AC R_{OUT} of the SAC contains several terms:

- Resonant tank impedance
- Input lead inductance and internal capacitance
- Output lead inductance and internal capacitance

The values of these terms are shown in the behavioral model in the prior section. It is important to note on which side of the transformer these impedances appear and how they reflect across the transformer given the K factor.

The overall AC impedance varies from model to model but for most models it is dominated by DC Rout value from DC to beyond 500 KHz.

Any capacitors placed at the output of the VTM module reflect back to the input of the module by the square of the K factor (Eq. 9) with the impedance of the module appearing in series. It is very important to keep this in mind when using a PRM® regulator to power the VTM. Most PRM regulators have a limit on the maximum amount of capacitance that can be applied to the output. This capacitance includes both the regulator output capacitance and the current multiplier output capacitance reflected back to the input. In PRM regulator remote sense applications, it is important to consider the reflected value of VTM current multiplier output capacitance when designing and compensating the PRM regulator control loop.

Capacitance placed at the input of the VTM module appear to the load reflected by the K factor, with the impedance of the VTM module in series. In step-down VTM ratios, the effective capacitance is increased by the K factor. The effective ESR of the capacitor is decreased by the square of the K factor, but the impedance of the VTM module appears in series. Still, in most step-down VTM modules an electrolytic capacitor placed at the input of the module will have a lower effective impedance compared to an electrolytic capacitor placed at the output. This is important to consider when placing capacitors at the output of the current multiplier. Even though the capacitor may be placed at the output, the majority of the AC current will be sourced from the lower impedance, which in most cases will be the VTM current multiplier. This should be studied carefully in any system design using a VTM current multiplier. In most cases, it should be clear that electrolytic output capacitors are not necessary to design a stable, well-bypassed system.

Current Sharing

The SAC™ topology bases its performance on efficient transfer of energy through a transformer without the need of closed loop control. For this reason, the transfer characteristic can be approximated by an ideal transformer with some resistive drop and positive temperature coefficient.

This type of characteristic is close to the impedance characteristic of a DC power distribution system, both in behavior (AC dynamic) and absolute value (DC dynamic).

When connected in an array with the same K factor, the VTM module will inherently share the load current with parallel units, according to the equivalent impedance divider that the system implements from the power source to the point of load.

Some general recommendations to achieve matched array impedances:

- Dedicate common copper planes within the PCB to deliver and return the current to the modules.
- Provide the PCB layout as symmetric as possible.
- Apply same input / output filters (if present) to each unit.

For further details see AN:016 Using BCM® Bus Converters in High Power Arrays.

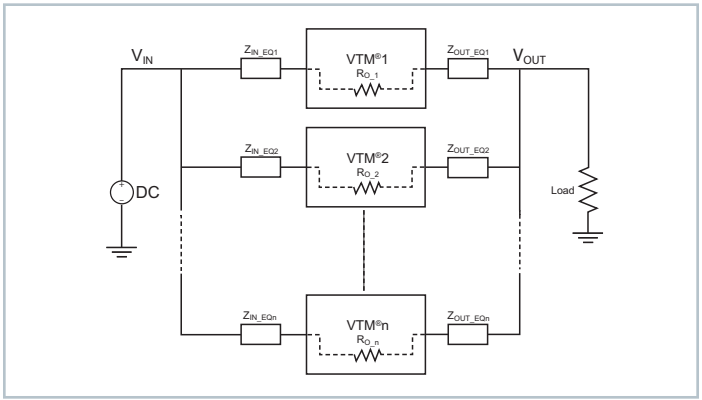


Figure 4 — *VTM module array*

Fuse Selection

In order to provide flexibility in configuring power systems VI Chip® products are not internally fused. Input line fusing of VI Chip products is recommended at system level to provide thermal protection in case of catastrophic failure.

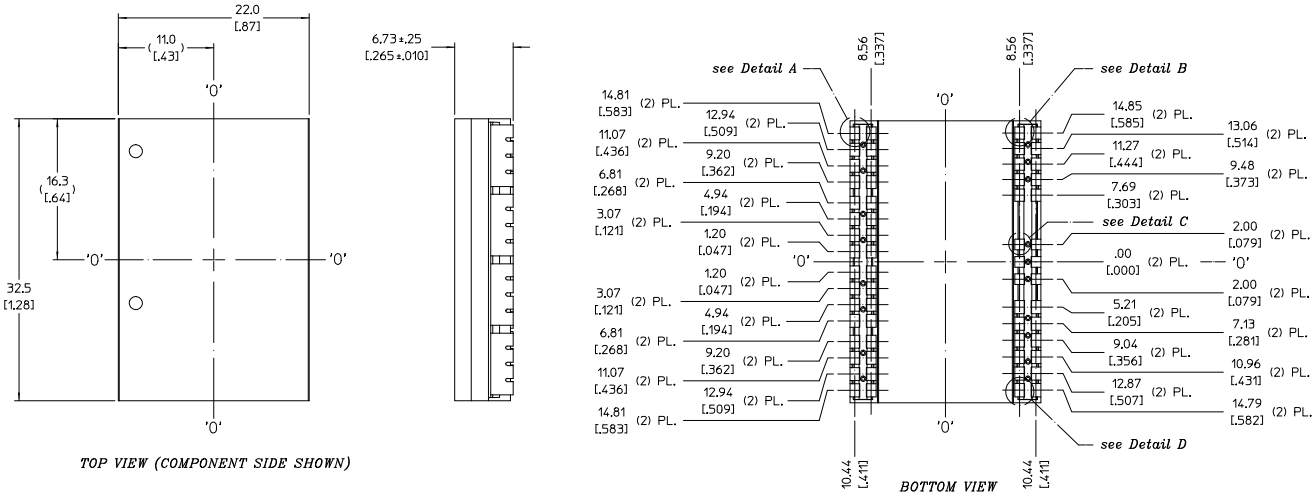
The fuse shall be selected by closely matching system requirements with the following characteristics:

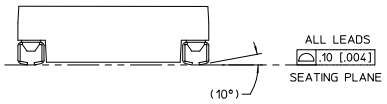
- Current rating (usually greater than maximum VTM module current)
- Maximum voltage rating (usually greater than the maximum possible input voltage)
- Ambient temperature
- Nominal melting I^2t

Reverse Operation

The MVTM is capable of reverse operation.
If a voltage is present at the output which satisfies the condition $V_{OUT} > V_{IN} \bullet K$ at the time the VC voltage is applied, or after the unit has started, then energy will be transferred from secondary to primary. The input to output ratio will be maintained. The MVTM will continue to operate in reverse as long as the input and output are within the specified limits. The MVTM has not been qualified for continuous operation (>10 ms) in the reverse direction.

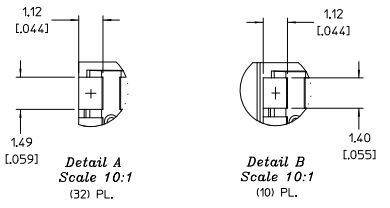
Product Outline & Recommended Land Pattern; Full VIC SMD, 18 pin

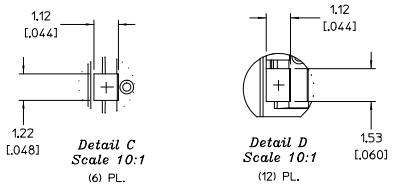


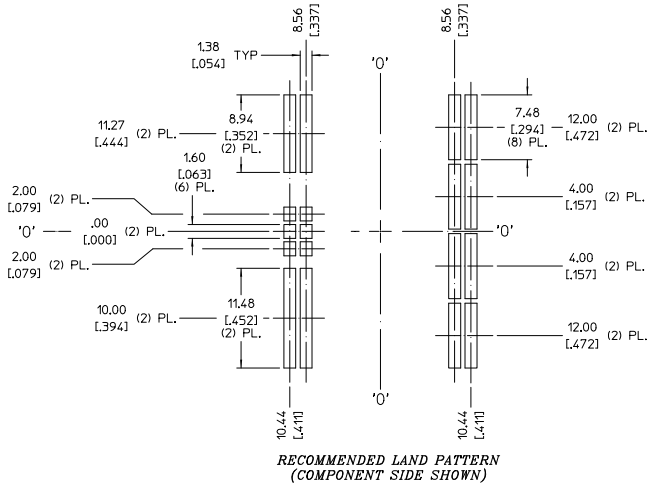


NOTE:

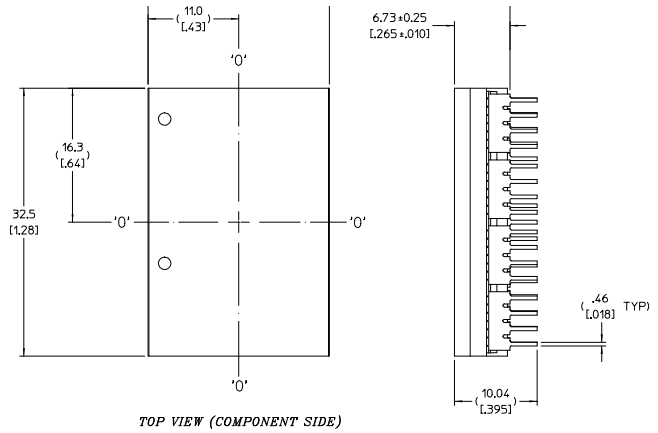
1. RoHS COMPLIANT PER CST-0001 LATEST REVISION.



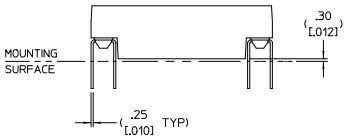




Product Outline & Recommended Land Pattern; Full VIC TH, 60 pin

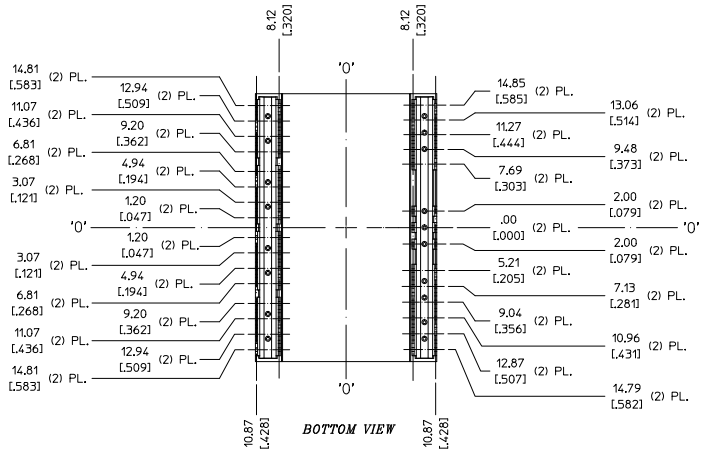


TOP VIEW (COMPONENT SIDE)

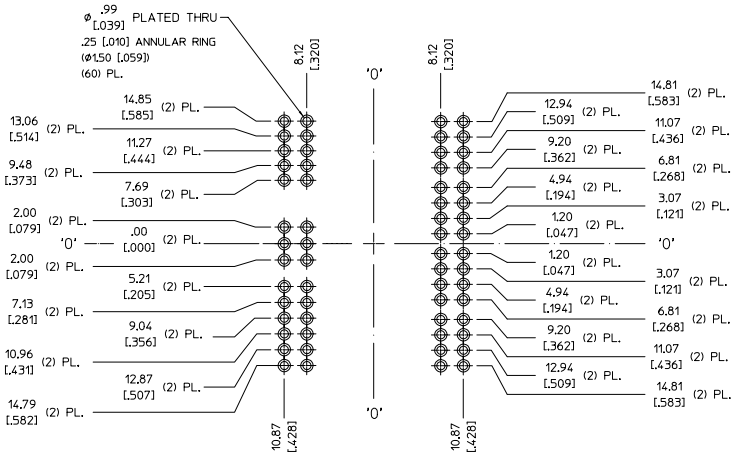


NOTE:

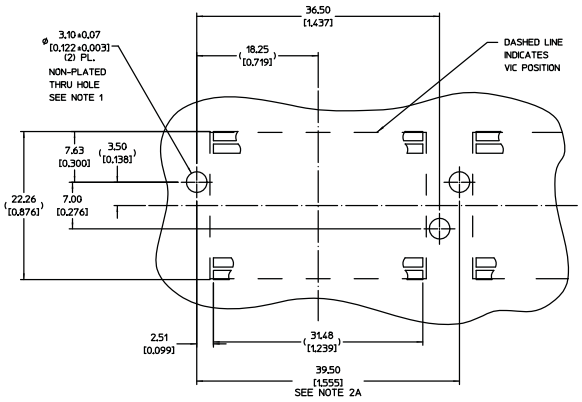
1. RoHS COMPLIANT PER CST-0001 LATEST REVISION.



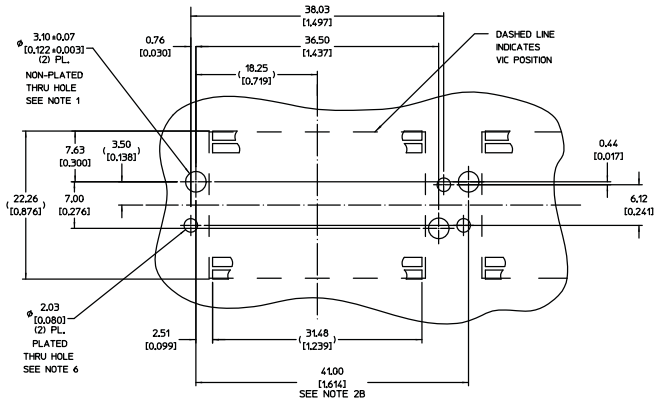
BOTTOM VIEW



Recommended Heat Sink Push Pin Location; Full



(NO GROUNDING CLIPS)

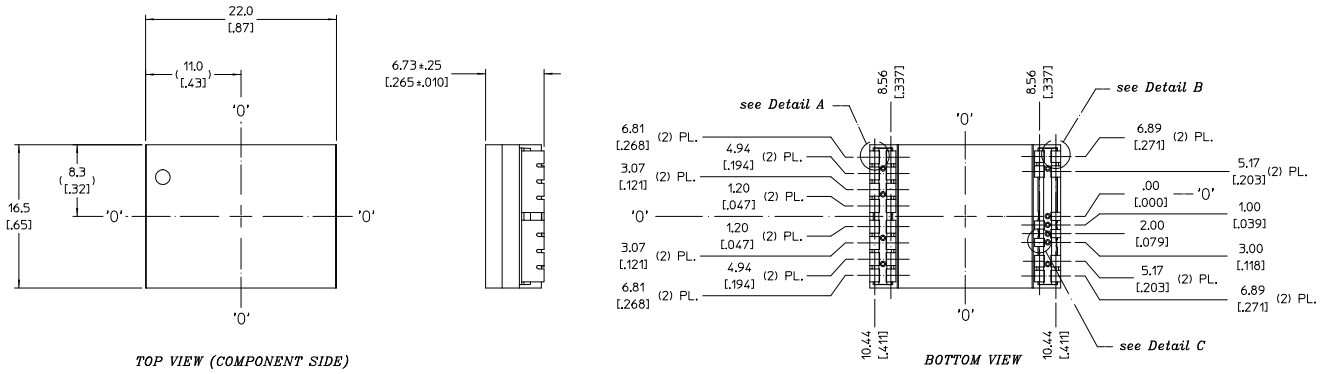


(WITH GROUNDING CLIPS)

Notes:

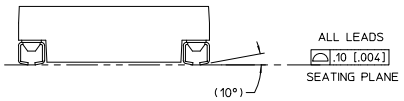
1. Maintain 3.50 (0.138) Dia. keep-out zone free of copper, all PCB layers.
2. (A) Minimum recommended pitch is 39.50 (1.555). This provides 7.00 (0.275) component edge-to-edge spacing, and 0.50 (0.020) clearance between Vicor heat sinks.
   (B) Minimum recommended pitch is 41.00 (1.614). This provides 8.50 (0.334) component edge-to-edge spacing, and 2.00 (0.079) clearance between Vicor heat sinks.
3. VI Chip® module land pattern shown for reference only; actual land pattern may differ. Dimensions from edges of land pattern to push–pin holes will be the same for all full-size VI Chip® products.
4. RoHS compliant per CST–0001 latest revision.
5. Unless otherwise specified:
   Dimensions are mm (inches)
   tolerances are:
   x.x (x.xx) = ±0.3 (0.01)
   x.xx (x.xxx) = ±0.13 (0.005)
6. Plated through holes for grounding clips (33855) shown for reference, heat sink orientation and device pitch will dictate final grounding solution.

Mechanical Drawing; Half VIC SMT, 12 pin



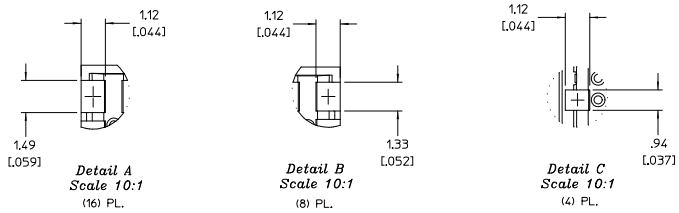
TOP VIEW (COMPONENT SIDE)

BOTTOM VIEW



NOTE:

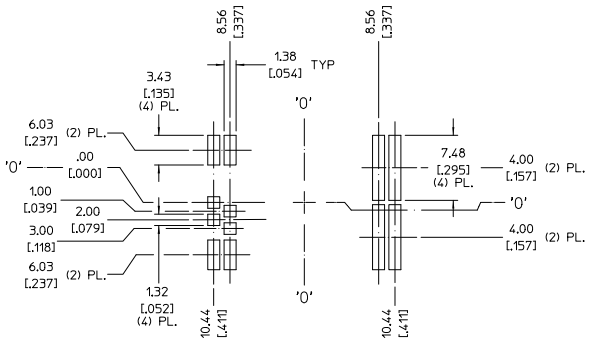
1. RoHS COMPLIANT PER CST-0001 LATEST REVISION.



Detail A
Scale 10:1
(16) PL.

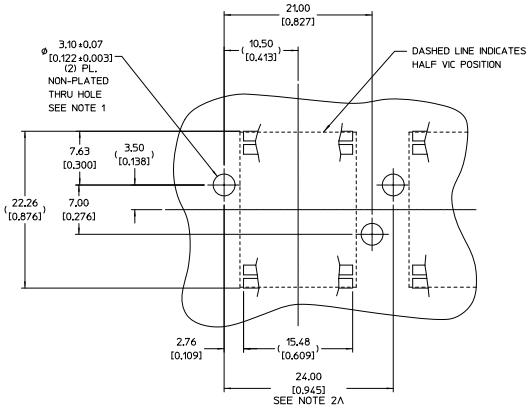
Detail B
Scale 10:1
(8) PL.

Detail C
Scale 10:1
(4) PL.

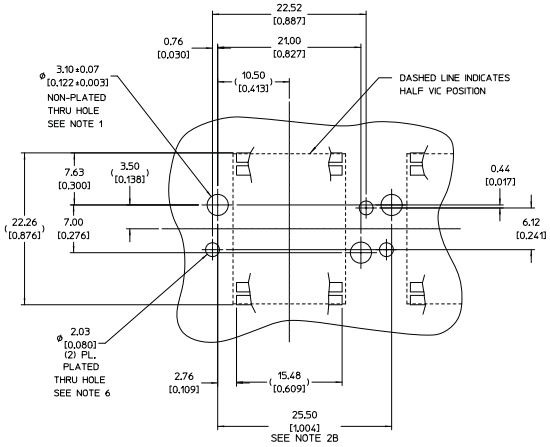


RECOMMENDED LAND PATTERN
(COMPONENT SIDE SHOWN)

Recommended Heat Sink Push Pin Location; Half



(NO GROUNDING CLIPS)



(WITH GROUNDING CLIPS)

Notes:

1. Maintain 3.50 (0.138) Dia. keep-out zone free of copper, all PCB layers.

2. (A) minimum recommended pitch is 24.00 (0.945) this provides 7.50 (0.295) component edge–to–edge spacing, and 0.50 (0.020) clearance between Vicor heat sinks.
(B) Minimum recommended pitch is 25.50 (1.004). This provides 9.00 (0.354) component edge–to–edge spacing, and 2.00 (0.079) clearance between Vicor heat sinks.

3. VI Chip® module land pattern shown for reference only, actual land pattern may differ. Dimensions from edges of land pattern to push–pin holes will be the same for all half size V•I Chip Products.

4. RoHS compliant per CST–0001 latest revision.

5. Unless otherwise specified:
Dimensions are mm (inches)
tolerances are:
x.x (x.xx) = ±0.13 (0.01)
x.xx (x.xxx) = ±0.13 (0.005)

6. Plated through holes for grounding clips (33855) shown for reference. Heat sink orientation and device pitch will dictate final grounding solution.

Revision History

Revision	Date	Description	Page Number(s)
1.0	3/2014	Initial Release	n/a
1.1	11/25/2014	Typ value of VC Internal Resistor	12
1.2	1/07/2015	Updated 3 V part to B version	5
1.3	07/??/15	What would you like to say here?	19 & 20

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