



Is Now Part of



ON Semiconductor®

To learn more about ON Semiconductor, please visit our website at
www.onsemi.com

ON Semiconductor and the ON Semiconductor logo are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

AN-9036

Guidelines for Using Fairchild's Power56

Dennis Lang, Staff Engineer

Introduction

The Power56 minimizes both Printed Wiring Board (PWB) space and $R_{DS(ON)}$ in a convenient, familiar SO-8 sized footprint, with the addition of a large drain tab for improving thermal performance. The Power56 offers a footprint widely used in the industry for enhanced performance SO-8 sized packages. This packaging technology requires mounting techniques, which are slightly different from a conventional SO-8; however, those familiar with mounting packages with large planar areas will find the techniques similar. This note will examine techniques for mounting the Power56 in both prototype and manufacturing environments using eutectic and lead free solder pastes.



Figure 1: Power56 Mounted on PWB

Component Mounting

The process of attaching an electronic component to the PWB is *the* critical process in determining performance *and* reliability of a MOSFET. Proper stencil and PWB design is essential in getting the most out of a component, especially for a device utilizing an advanced performance package like the Power56. Proper design of the process is also important for reducing defects improving throughput and profitability of the assembly line. It has been proposed that the "10x" rule applies to assembly defects. The implication is that as you progress through the steps of the assembly, from printing solder to the end customer, the cost of a defect rises tenfold per process step.

Board Layout

When designing a board for Power56, the designer should remember that the drain is the most efficient at dissipating heat. Because of this there is the largest potential for gain by focusing on

the drain heat sink and its heat path. Because of the unique design of the Power56 it is possible to run copper traces from 3 sides of the die as seen below in figure 2. For best thermal performance it is recommended that the user put as much copper on the drain as possible, while keeping the thermal path short by keeping the area around the drain tab open. Pins 1-3 are Source and pin 4 is the Gate. Pins 5-8 are part of the drain tab and make one continuous solder joint with the drain tab. See the applicable data sheet for the specific pin out.

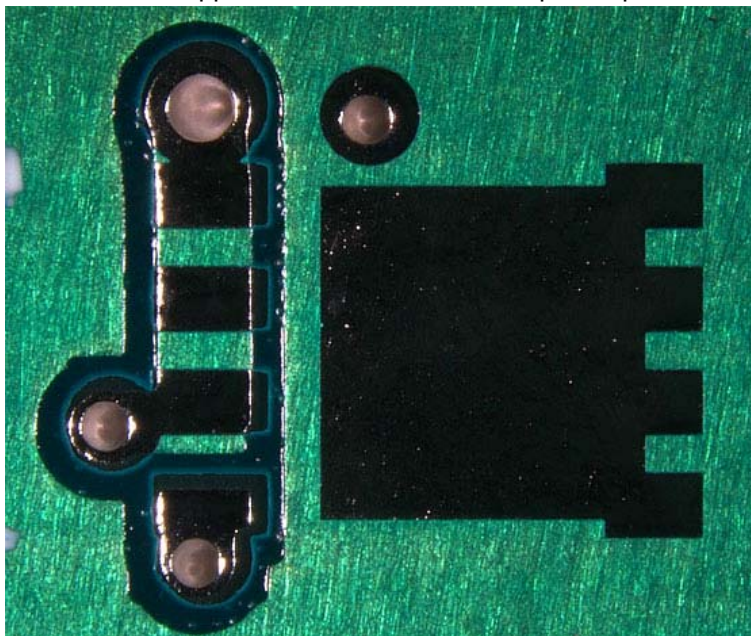


Figure 2: Power56 PWB footprint showing area around drain lead allowing copper pour area for heat dissipation.

Via Usage with Power56

Note: This data was taken for the Fairchild FLMP package. It is applicable to the Power56 as well. Customers frequently wish to use vias in their design to improve thermal performance by using copper for heat dissipation on multiple layers of the PWB. Some papers suggest placing vias in the drain pad for devices like TO-220. This is not recommended by the author. This practice creates unpredictable solder joint formation as the wetting of solder into vias is random; sometimes all of the vias will fill, sometimes none. Placing solder mask over the vias to keep solder from wetting into the vias also creates voiding and is not recommended. It has been proven through Finite Element Analysis and supporting laboratory experimentation that placing the vias just outside the pad will not cause an appreciable reduction in thermal performance, and yield superior manufacturability. Figure 3 is a proven recommendation.

Solder Process

It has been estimated that 60% of all manufacturing defects are created at the solder deposition phase. In modern surface mount electronics manufacturing, this means problems at stencil printing. The design of the stencil is critical for the creation of a solder joint that exhibits superior electrical and mechanical performance. As all designers involved in the design of stencils know there is not one design that will work for all applications. Differences in PWB finish, design, solder paste and flux, reflow profile and dimensional accuracies for all of the related equipment and machinery means ideally all stencils should be optimized for the specific application. Because the stencil designer needs a “starting” point, it is recommended to focus on printing a

volume of solder paste that after reflow will be thick enough to cover the entire drain pad to a thickness matching the maximum seating plane tolerance of the component. For the Fairchild Power56, this tolerance is 0.06mm. A broad assumption used in the industry is that the volume of solder paste will reduce by 50% due to reflow.

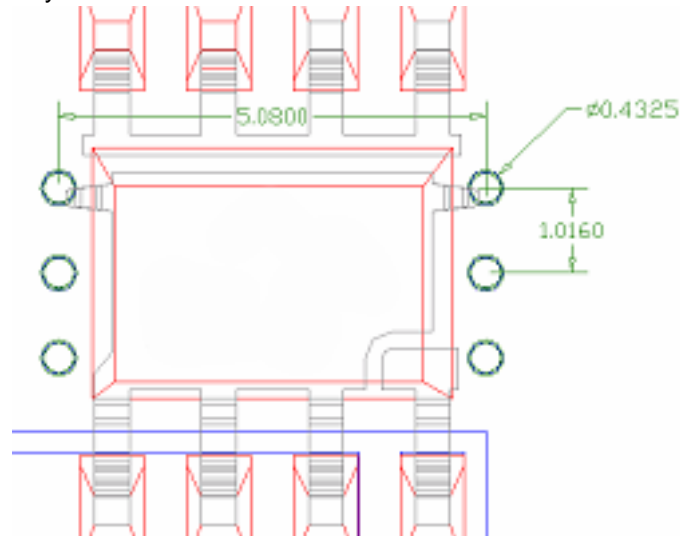


Figure 3: Recommended Via Size and Placement

Through testing in Fairchild's SMT Apps Lab, it has been found that the stencil apertures described below, and pictured in the appendix, are a good starting point, balancing adequate solder volume to ensure a good joint, with concerns of excess solder volume and related defects such as beading. Both stencil designs were found to be good places for the stencil designer to start with. IPC-7525, *Stencil Design Guidelines* is also a good reference for all component types. These stencil apertures were tested with Type 3 solder paste in eutectic tin lead and Lead Free SAC 305 alloy compositions and found to deliver good performance with appropriate reflow settings. (Though lead free paste is more "sticky" and as such care should be taken to verify the process parameters such as rate of stencil separation and prints between cleaning if a stencil originally designed for eutectic paste is used.) It is important to note that lead free paste solders will not deliver wetting across the pad that process engineers have come to expect from eutectic tin lead paste due to the high surface tension of tin present in high quantity in many lead free alloys. The appearance of the solder joint itself is also frequently less shiny, even with good process parameters.

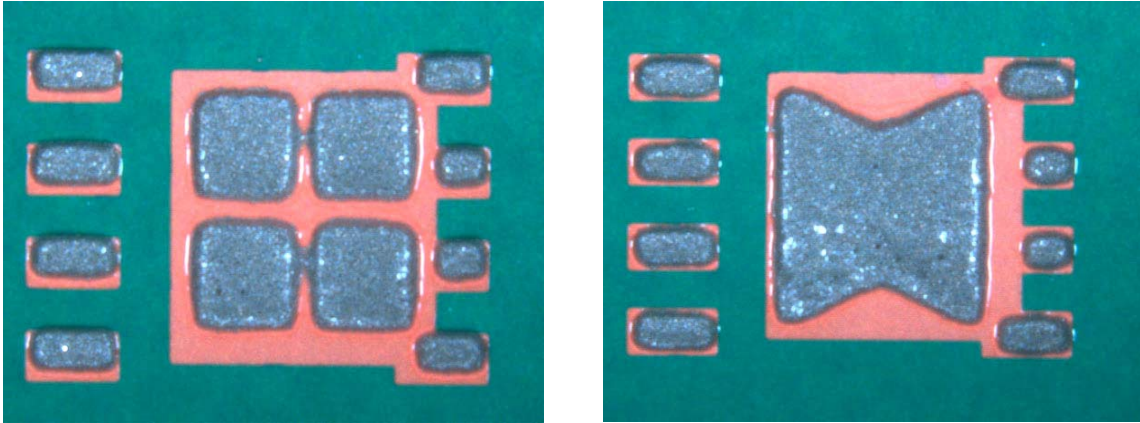
Stencil Printing

The parameters used for printing in this study were, 5 mil thick electroformed stencil, 60° steel squeegee, 1 psi squeegee pressure, and 25mm/s print speed. The solder paste vendor should supply initial set-up information for your particular paste composition as speed and pressure is paste dependant. The dimensioned stencil openings can be found in the appendix.

Solder Paste

Power56 components are normally used with one of the SAC tin/silver/copper lead free solder paste alloys. IPC-9502, PWB Assembly Soldering Process Guideline for Electronic Components, is a helpful reference for surface mount guidelines. Fairchild tests its components to 3 pass reflow using a modified IPC/JEDEC J-STD-020B reflow profile, with the peak temp tested to 260°C by Fairchild instead of the 250°C of the standards committee. Further information on Fairchild's lead free effort can be found at:

http://www.fairchildsemi.com/products/lead_free/



Figures 4 and 5: Printed solder of different geometries, both are proven to work well. Dimensioned stencil apertures can be found in the appendix.

Lead Termination, Exposed Copper and Solder Fillet

Questions have arisen with this type of package and the fact that the lead ends show exposed copper due to the singulation process in manufacturing. This exposed copper is specifically permitted in JEDEC JESD22-102D 5.3.3.2, "Exposed terminal base metal is allowable on the end toe of surface mount components."

A solder fillet to this exposed copper is not guaranteed. Due to various storage environments, the oxidation on the copper may be such that a fillet cannot be formed. It has been found in testing that a fillet does normally form when a reflow profile following the standards of the solder paste vendor is used. A proper profile allows the flux is able to properly prepare the surface for solder adhesion.

Using Power56 in Production

Standard pick and place equipment can be used with Power56 components, utilizing standard methods with the stencil and solder recommendations above. The manufacturing engineer should center the component on the PWB pad on the Power56 to the pad on the board for best performance on pick and place equipment. Organic Surface Protectant or an immersion metal plated PWB is recommended. Due to the planar nature of all QFN and MLP type packages, including Power56, a Hot Air Solder Leveled PWB may cause the components to shift in reflow.

Rework and Prototype Component Removal

If it becomes necessary to rework a Power56 package, the correct way to remove the component is by hot air. Use of a hot air rework station with a vacuum chuck, is the preferred method. A heat gun that produces enough heat to melt the solder is an acceptable alternative. Heat up the component until the solder has melted and allows the Power56 to be easily removed using tweezers and a gentle twisting motion. Take care not to destroy the plastic molding compound on the component if failure analysis is desired. Remove the solder from the PWB using either a solder vacuum or solder braid making sure to clean the area of solder and flux thoroughly. If a hot air rework station is available, use this tool to place the new component. Below are several methods for using Power56 in a prototyping or laboratory environment. If the component is to be returned to Fairchild for a failure analysis, special care must be taken not to overheat the Power56 during removal as the initial failure signature(s) may be lost due to this damage.

Prototype Mounting Using a Hot Air Gun

It is possible to mount a Power56 using a hot air gun, and it is the preferred prototyping method. Apply paste to the drain pad of the PWB using solder paste and place the component, properly oriented, with tweezers. Use a hot air gun (recommend setting air temperature to approximately

300°C) directly above the part to reflow the paste. Once the paste has reflowed, apply heat for approximately 5 more seconds with the hot air gun and follow by soldering the leads with a soldering iron and solder wire.

Things to Watch For

There are a couple of common errors when mounting Power56 components, especially in a prototype environment. If too much solder is placed on the board it can cause shorts during mounting. When the part is placed into solder paste, the solder is displaced outward. If there is an overabundance of solder, the solder can wick onto the leads and cause shorts between the gate, source and/or drain. Solder beading is also a possible problem due to this. Another common mistake is the use of too much heat. Within approximately 5 seconds of solder reflow with the hot air gun the application of heat must be stopped. Some discoloring of the PWB may result if too much heat is applied to the board.

X-Ray Inspection

When using a component like an Power56, x-ray inspection may be used to verify initial process control or as an ongoing quality check. Wetting to all 4 corners of the Power56 drain tab is necessary for reliability. Acceptable overall voiding is 25% provided the voids are dispersed throughout the drain connection.

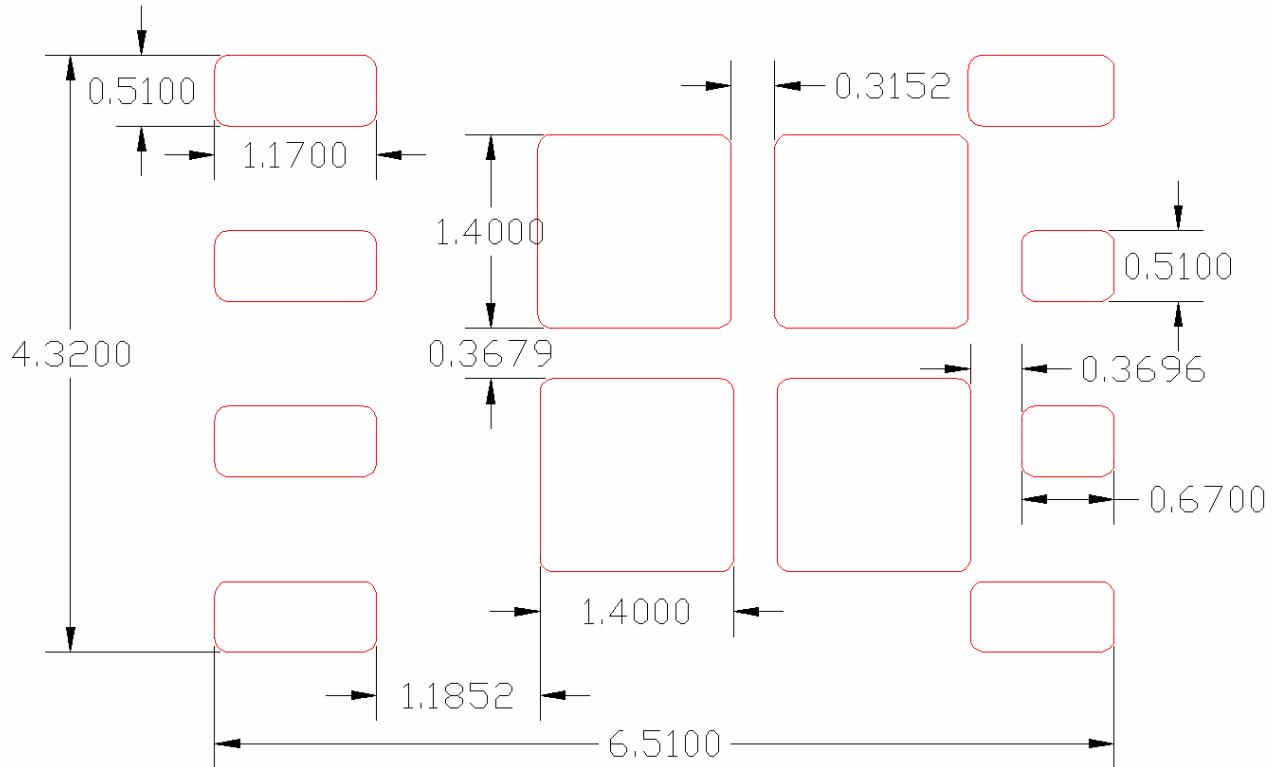
References

- [1] B. Bear, "Real Time Statistical Process Control of the Screen Print Process", Raytheon
- [2] J. Belamonte et al, "Step 4: Printing", Surface Mount Technology (SMT), April, 2005
- [3] IPC, IPC-7525 "Stencil Design Guidelines", IL, May, 2000
- [4] IPC/JEDEC, J-Std-020B, "Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices", July, 2002
- [5] JEDEC, JESD22-102D, "Solderability", September, 2004
- [6] J.H. Lau and Y.H. Pao, Solder Joint Reliability of BGA, CSP, Flip Chip and Fine Pitch SMT Assemblies, McGraw-Hill, NY, 1997
- [7] D. Lang and CL Wu, "Impact of Vias on Printed Circuit Board Thermal Performance", IMAPS 2004, 37th International Symposium on Microelectronics November, 2004
- [8] E. Strafstrom, "Unraveling the Final Finishing Mystery", Circuits Assembly, November, 2000, pp. 56-62

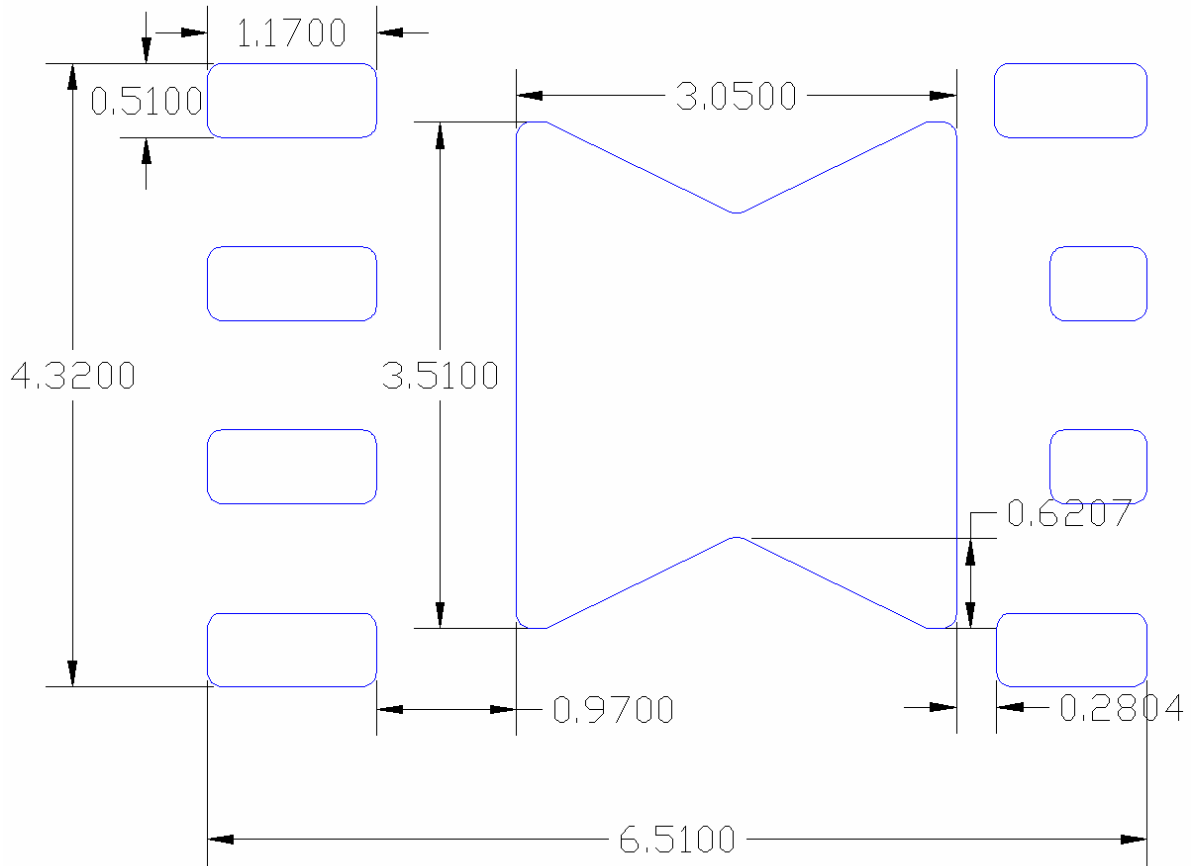
Applicable FSIDs: FDMS8460, FDMS8660AS, FDMS8660S, FDMS8662, FDMS8670AS, FDMS8670S, FDMS8672AS, FDMS8672S, FDMS8674, FDMS8680, FDMS8692, FDMS3500, FDMS3662, FDMS5352, FDMS8670, and FDMS3572.

APPENDIX

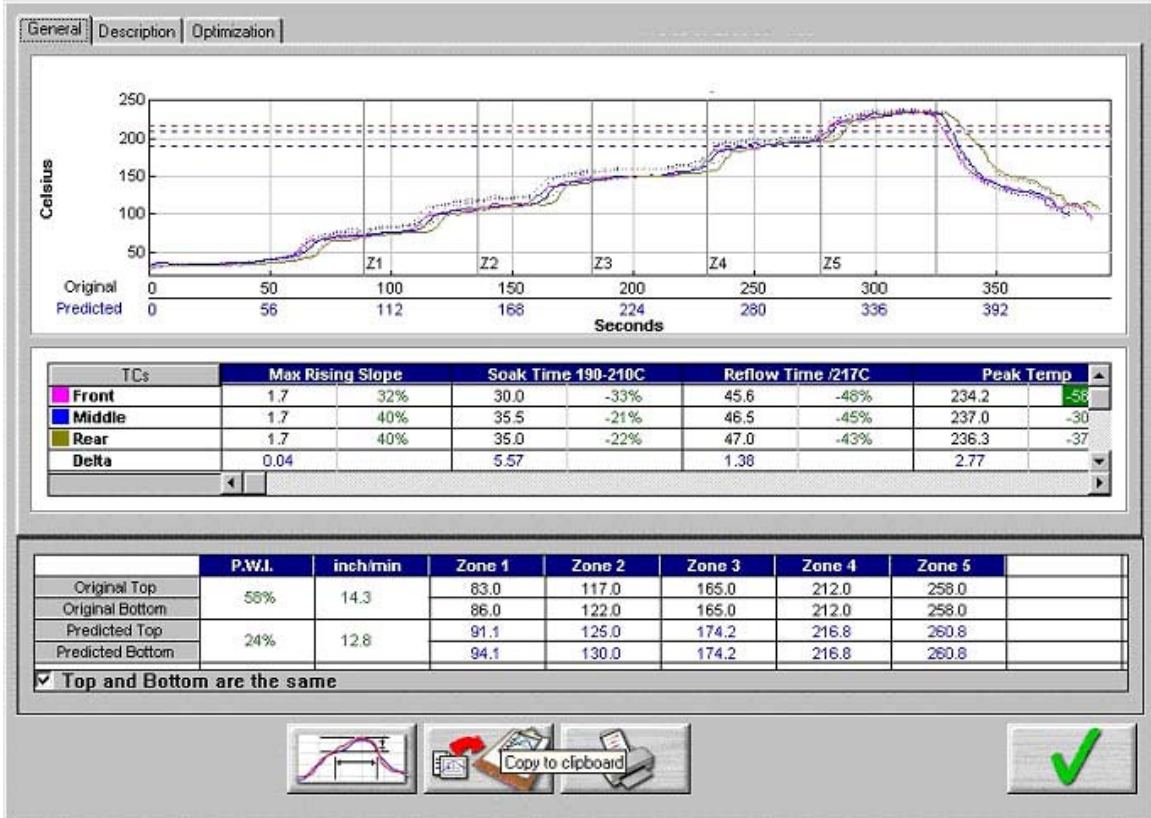
Stencil pattern for waffle type drain pad.



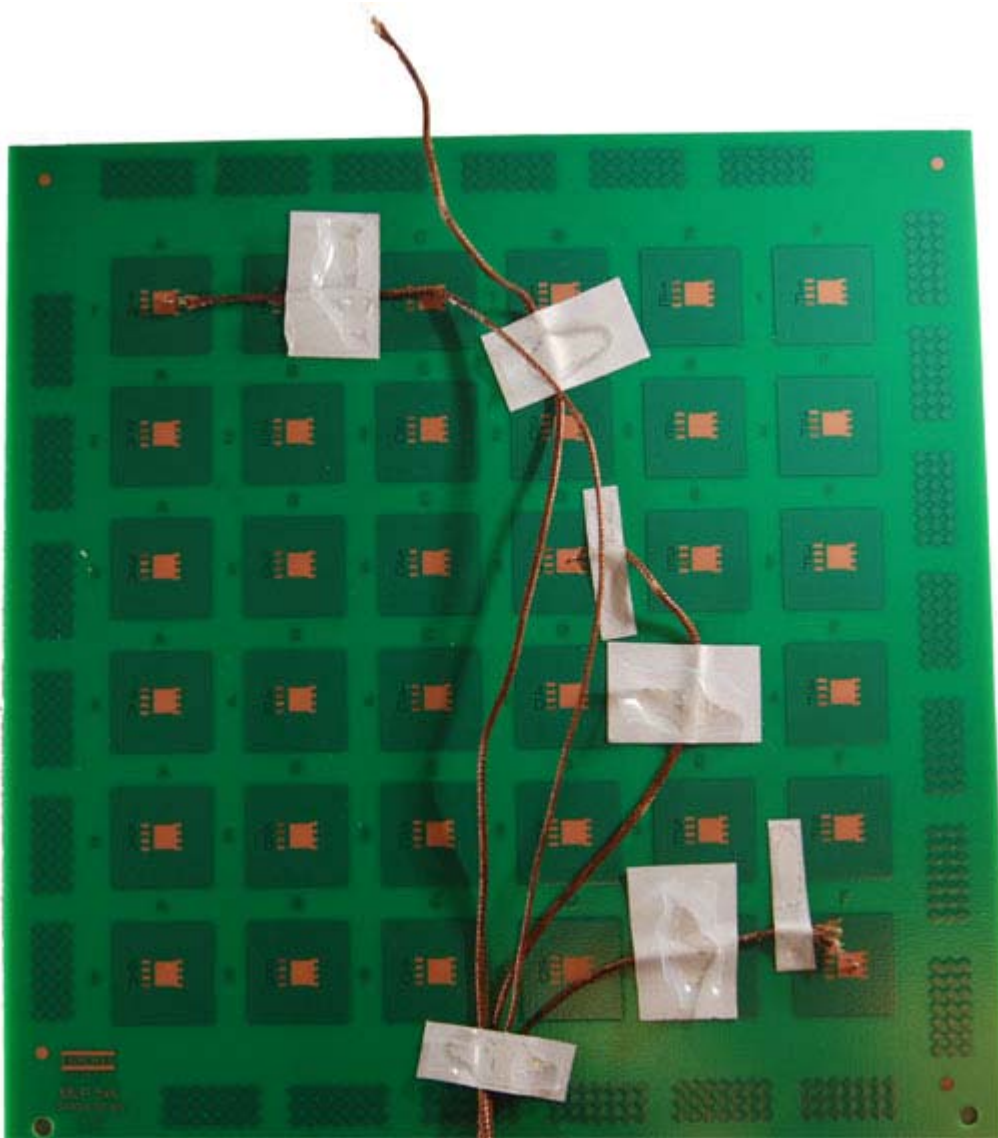
Stencil aperture for “bowtie” type stencil.



This is a typical Reflow profile useful as a baseline for using a SAC305 alloy, no clean paste. Oven zone settings are noted under the “Original Top” and “Original Bottom” rows. All ovens and PWB designs will require individualized settings created with a profiler.



Profiler thermocouples attached to test PWB with high temperature tape.



ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>
For additional information, please contact your local
Sales Representative