OKI Semiconductor

This version: Nov. 1997
Previous version: Mar. 1996

MSM6262-xx

DOT MATRIX LCD CONTROLLER WITH 48-DOT COMMON DRIVER

GENERAL DESCRIPTION

The MSM6262-xx is a dot matrix LCD controller which is fabricated by OKI's low power consumption CMOS silicon gate technology. In combination with 8-bit microcontroller, the MSM6262-xx can control the dot matrix character type LCD module.

The MSM6262-xx is provided with a serial data transfer output. So, a maximum of 160 characters can be controlled by combining this device with the MSM5259, MSM5839C, or MSM5260.
The MSM6262-xx is recommended for use in an LCD panel which is capable of displaying 81 to 160 characters. If an LCD panel of which display capacity is 80 characters or less is used, the MSM6222B-xx is recommended.
The MSM6262-xx is best suited to be used as an LCD controller for applications such as electronic typewriters, POS system terminals, and data banks.

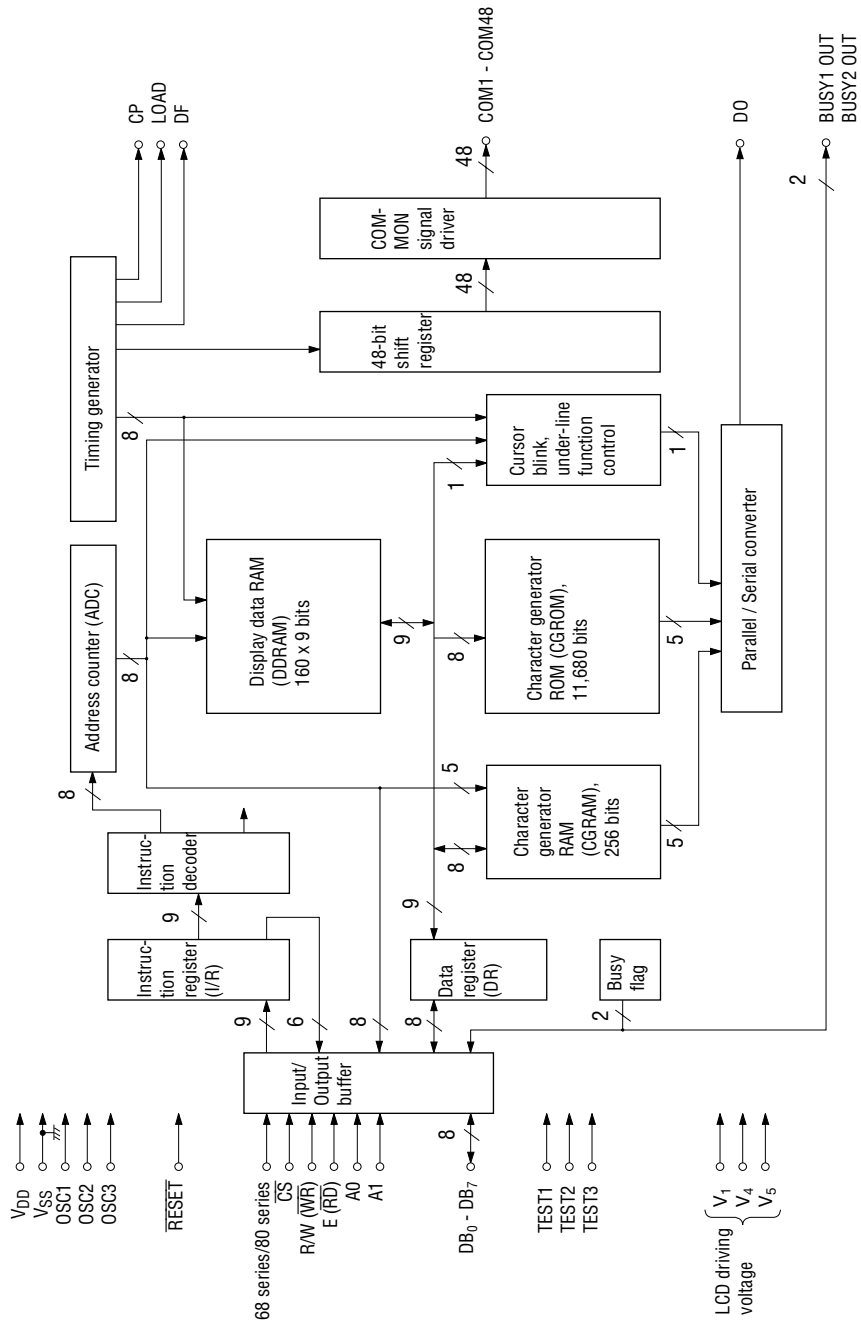
FEATURES

- Dot matrix LCD controller/driver for three different font configuration
  (5 x 7 dots, 5 x 11 dots and 5 x 12 dots)
- Up to 160 characters can be controlled
  (Display data RAM ... 160 x 9-bit)
- On-chip character generator ROM (CGROM) for 256 different characters
  - 5 x 7 dots ... 128 characters
  - 5 x 11 dots ... 96 characters
  - 5 x 12 dots ... 32 characters
- On-chip character generator RAM (CGRAM) (32 x 8-bit)
  - 5 x 8 dots ... 4 kinds
  - 5 x 12 dots ... 2 kinds
- Easy interface with Z80, 6809, 80C49, and 80C51
- Underline function
- Shift function for g, i, p, q and y
- Selectable driving duty

Duty	Font Configuration (dots)	Cursor Display	Display (characters x lines)
1/16	5 x 7	Available	80 x 2
1/24	5 x 11	Available	80 x 2
1/32	5 x 7	Available	40 x 4
1/48	5 x 11	Available	40 x 4

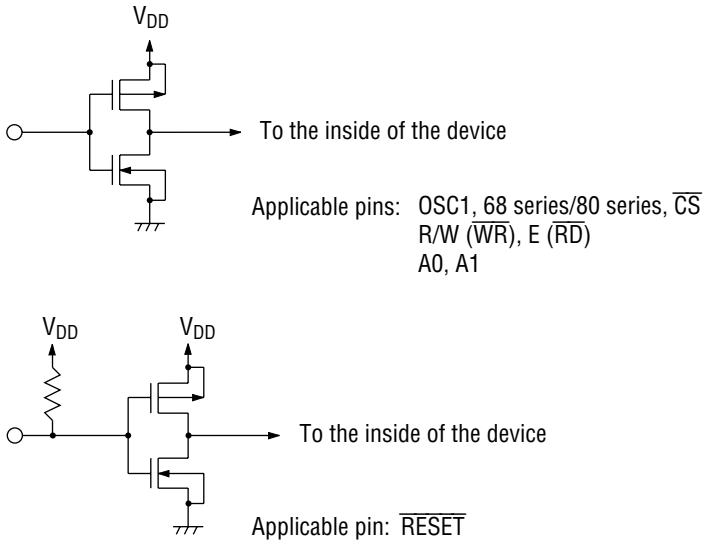
- Package :
  80-pin plastic QFP (QFP80-P-1420-0.80-BK) (Product name : MSM6262-xxGS-BK)
  xx indicates code number.

BLOCK DIAGRAM

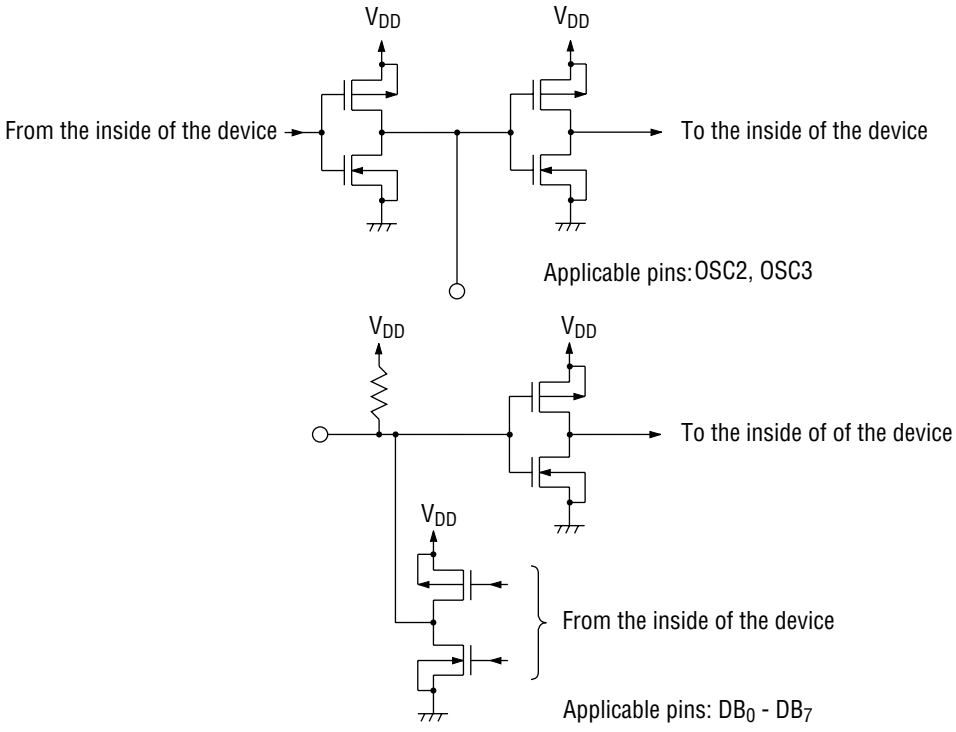


INPUT AND OUTPUT CONFIGURATION

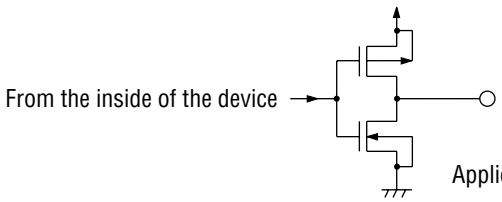
Input pin



Input /Output pin

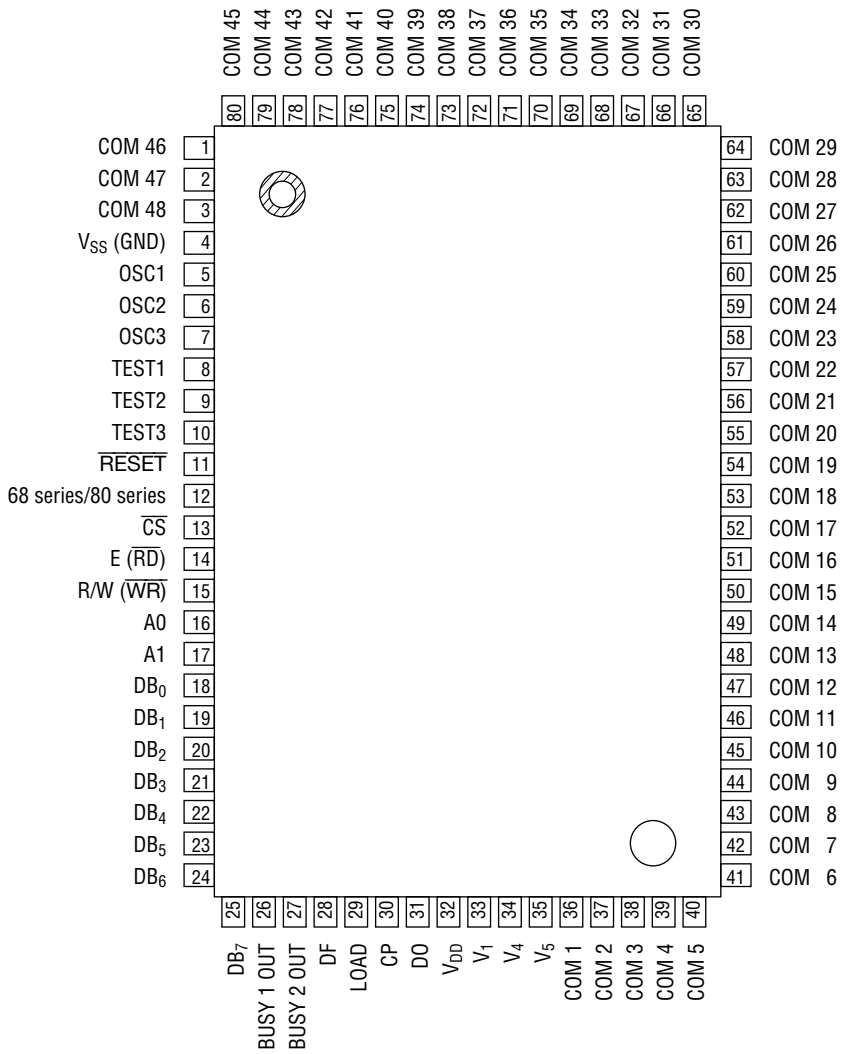


Output pin



Applicable pins: CP, LOAD, DF, DO,
BUSY1 OUT, BUSY2 OUT

PIN CONFIGURATION (TOP VIEW)



80-Pin Plastic QFP

PIN DESCRIPTIONS

Symbol	Type	Description
OSC1 OSC2, OSC3	I/O	Clock oscillating pins required for internal operation upon receipt of the LCD drive signal and CPU instruction.
$\overline{\text{RESET}}$	I	Reset pin
68 series/80 series	I	Selection pin for either 68 series CPU or 80 series CPU
$\overline{\text{CS}}$	I	Chip select pin. By setting $\overline{\text{CS}}$ at "L" level, MSM6262-xx is set at selecting condition.
R/W ($\overline{\text{WR}}$)	I	R/W pin of 68 series CPU shall be connected to this pin, while $\overline{\text{WR}}$ pin shall be connected to this pin in the case of 80 series CPU.
E ($\overline{\text{RD}}$)	I	E pin of 68 series CPU shall be connected to this pin, while $\overline{\text{RD}}$ pin shall be connected to this pin in the case of 80 series CPU.
A0, A1	I	The address bus of CPU shall be connected to these pins. Instruction code is set by these pins.
DB_0 - DB_7	I/O	The data bus of CPU shall be connected to these pins. These pins are used to set the data of the instruction or to read the data.
TEST1 - TEST3	I	Test pins. Normally these pins should be set at V_{SS} or open.
V_{DD}, V_{SS}	—	Voltage supply pins. V_{DD} is also used for the common bias voltage level to drive the LCD.
V_1, V_4, V_5	—	Common bias voltage input pins to drive the LCD
DO	O	Serial data output pin for SEGMENT drivers
CP	O	Clock pulse output pin. The clock output from this pin enables the character pattern data, which is output from DO, to input to the SEGMENT drivers (MSM5839C or MSM5259).
LOAD	O	Load signal output pin. The character pattern data to the SEGMENT drivers, which was output from DO and CP, is loaded to the LCD output of the SEGMENT drivers, synchronized with the COMMON signal.
DF	O	B-type AC signal output pin to drive the LCD
COM1 - COM48	O	COMMON signal output pins to drive the LCD
BUSY1 OUT	O	This pin shows the internal condition of MSM6262-xx. "H" shows that MSM6262-xx is in internal operation, while "L" shows that MSM6262-xx is ready to receive the instruction from the CPU.
BUSY2 OUT	O	This pin shows that MSM6262-xx is in internal operation based on the instruction from the CPU, or MSM6262-xx is in display revising operation based on the instruction from the CPU. "H" shows that MSM6262-xx is in internal operation, while "L" shows that the display on the LCD has been established and the MSM6262-xx is ready to receive an instruction.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit	Applicable Pin
Supply Voltage	V_{DD}	Ta = 25°C, V_{DD}–V_{SS}	–0.3 to +7.0	V	V_{DD}, V_{SS}
Supply Voltage for Driving LCD	V_1, V_4, V_5	Ta = 25°C	V_{DD} – 12 to V_{DD} + 0.3	V	V_1, V_4, V_5
Input Voltage	V_{IN}	Ta = 25°C	–0.3 to V_{DD} + 0.3	V	OSC1, $\overline{RESET}$ 68 series / 80 series $\overline{CS}$, A0, A1, R/W ($\overline{WR}$) E ($\overline{RD}$), DB_0 - DB_7
Power Dissipation	P_D	Ta = 25°C	500	mW	—
Storage Temperature	T_{STG}	—	–55 to +125	°C	—

RECOMMENDED OPERATING CONDITOINS

Parameter	Symbol	Condition	Range	Unit	Applicable Pin
Supply Voltage	V_{DD}	—	4.5 to 5.5	V	V_{DD}, GND
LCD Driving Voltage	V_{LCD}	1/5 bias, V_{DD}–V_5	3.0 to 11	V	V_{DD}, V_1, V_4, V_5
		1/6, 1/7 bias, V_{DD}–V_5	4.0 to 11	V	
		1/8 bias, V_{DD}–V_5	4.5 to 11	V	
Operating Temperature	T_{op}	—	–20 to +75	°C	—

Note: For bias, refer to *3 in the section "DC Characteristics".

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD} = 4.5 to 5.5 V , Ta = –20 to +75°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable Pin
"H" Input Voltage	V_{IH1}	—	2.2	—	V_{DD}	V	$\overline{CS}$, R/W ($\overline{WR}$) E ($\overline{RD}$), A0, A1 DB_0 - DB_7
"L" Input Voltage	V_{IL1}	—	–0.3	—	0.7	V	
"H" Output Voltage	V_{OH1}	I_O = –250 µA	2.4	—	—	V	DB_0 - DB_7
"L" Output Voltage	V_{OL1}	I_O = 1.8 mA	—	—	0.4	V	
"H" Input Voltage	V_{IH2}	—	V_{DD}–0.8	—	V_{DD}	V	OSC1, $\overline{RESET}$ 68series/80series
"L" Input Voltage	V_{IL2}	—	–0.3	—	0.8	V	
"H" Output Voltage	V_{OH2}	I_O = –500 µA	0.85 V_{DD}	—	—	V	DO, LOAD, DF
"L" Output Voltage	V_{OL2}	I_O = 500 µA	—	—	0.15 V_{DD}	V	
"H" Output Voltage	V_{OH3}	I_O = –1 mA	0.85 V_{DD}	—	—	V	CP
"L" Output Voltage	V_{OL3}	I_O = 1 mA	—	—	0.15 V_{DD}	V	
"H" Output Voltage	V_{OH4}	I_O = –100 µA	2.4	—	—	V	BUSY1 OUT BUSY2 OUT
"L" Output Voltage	V_{OL4}	I_O = 1.6 mA	—	—	0.4	V	
COM Voltage Drop	V_{COM}	I_O = ± 50 µA *1	—	—	2.9	V	COM1 - COM48
"H" Input Current	I_{ILH1}	V_{IN} = V_{DD}	—	—	1	µA	$\overline{CS}$, R/W ($\overline{WR}$) E ($\overline{RD}$), A0, A1 OSC1, 68series/ 80series
"L" Input Current	I_{ILL1}	V_{IN} = V_{SS}	—	—	–1	µA	
Supply Current	I_{DD1}	V_{DD} = 5 V, *2 f_{OSC} = 500 kHz (RC oscillation)	—	—	1.5	mA	V_{DD}
	I_{DD2}	V_{DD} = 5 V, *2 f_{IN} = 500 kHz (external oscillation)	—	—	1.5	mA	
LCD Driving Voltage	V_{LCD}	V_{DD}–V_5 *3 1/5 bias	3.0	—	11	V	V_1 , V_4, V_5
		V_{DD}–V_5 *3 1/6-1/7 bias	4.0	—	11	V	
		V_{DD}–V_5 *3 1/8 bias	4.5	—	11	V	
"H" Input Current	I_{ILH2}	V_{IN} = V_{DD}	—	—	2	µA	$\overline{RESET}$
"L" Input Current	I_{ILL2}	V_{IN} = V_{SS}, V_{DD} = 5 V	–8	–20	–60	µA	

*1. This is applicable to the voltage drop which is caused between V_{DD}, V_1, V_4, V_5 and COM1 - COM48 when a current of 50 µA is flowed in/out to/from all of COM1 - COM48. (When the output level is either V_{DD} or V_1, it should be applied only when the current flows in. When the output level is either V_4 or V_5, it should be applied only when the current flows in.
In this case, +5V is applied to V_{DD} and V_1, while –6 V is applied to V_4 and V_5.)

*2. This is applicable to the current which flows in to V_{DD} under following conditions.
V_{DD} = 5 V, V_{SS} = 0 V, V_1 = 2.8 V, V_4 = -3.8 V, V_5 = –6 V, No load, No interface with CPU

*3. V_1 to V_5 should be set at as follows.

No. of lines (N) / Font configuration / Pin	2 lines		4 lines	
	5 x 8	5 x 12	5 x 8	5 x 12
V_1	$V_{DD} - \frac{1}{5} V_{LCD}$	$V_{DD} - \frac{1}{6} V_{LCD}$	$V_{DD} - \frac{1}{7} V_{LCD}$	$V_{DD} - \frac{1}{8} V_{LCD}$
V_4	$V_{DD} - \frac{4}{5} V_{LCD}$	$V_{DD} - \frac{5}{6} V_{LCD}$	$V_{DD} - \frac{6}{7} V_{LCD}$	$V_{DD} - \frac{7}{8} V_{LCD}$
V_5	$V_{DD} - V_{LCD}$	$V_{DD} - V_{LCD}$	$V_{DD} - V_{LCD}$	$V_{DD} - V_{LCD}$

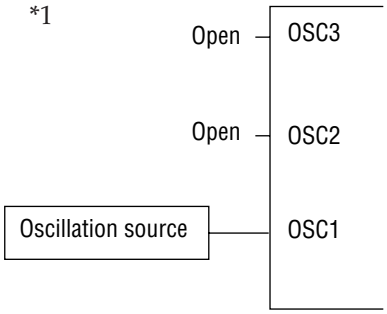
V_{LCD} = LCD driving voltage

AC Characteristics

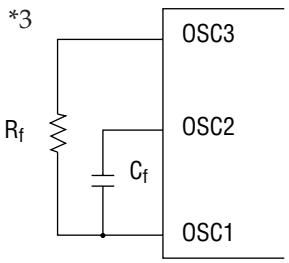
(V_{DD} = 4.5 to 5.5V , Ta = –20 to +75°C)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Applicable Pin
Input Frequency	f_{IN}	*1, *2	300	500	700	kHz	OSC1
Input Clock Duty	f_{DUTY}	*2	45	50	55	%	
Input Clock Rise Time	t_r	*2	—	—	100	ns	
Input Clock Fall Time	t_f	*2	—	—	100	ns	
RC Oscillation Frequency	f_{CR}	*3	300	500	700	kHz	OSC1, OSC2, OSC3
"H" Input Current	I_{ILH3}	$V_{IN} = V_{DD}$	—	—	1	µA	DB_0 - DB_7
"L" Input Current	I_{ILL3}	$V_{IN} = V_{SS}$ V_{DD} = 5 V	–45	–120	–250	µA	

*1

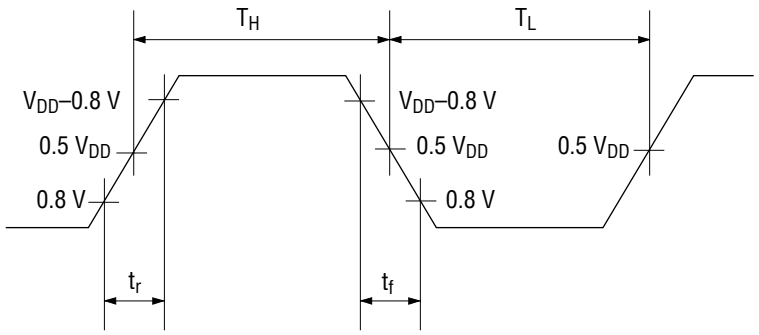


*3



R_f = 39 kΩ ± 5%
C_f = 22 pF ± 10%
(Keep the wiring from OSC1, OSC2, and OSC3 to R_f and C_f as short as possible.)

*2



$$f_{DUTY} = \frac{T_H}{T_H + T_L} \times 100\%$$

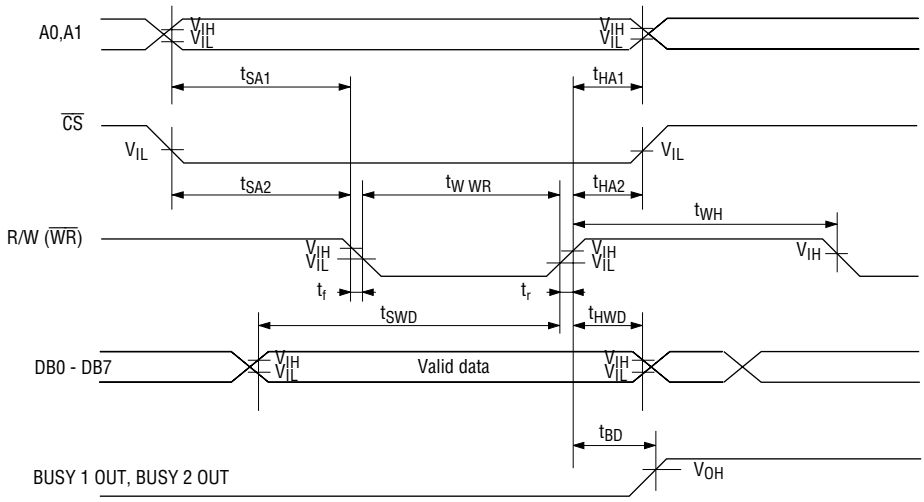
TIMING DIAGRAM

Interface with 80 Series CPU

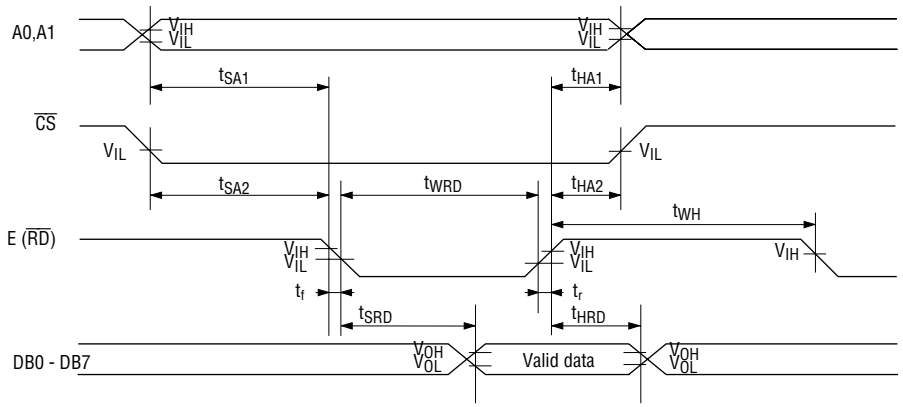
(V_{DD} = 4.5 to 5.5V, Ta = –20 to +75°C)

Parameter	Symbol	Min.	Max.	Unit
Address Set-up Time	t_{SA1}	110	—	ns
$\overline{CS}$ Set-up Time	t_{SA2}	100	—	ns
$\overline{WR}$ "L" Pulse Width	t_{WWR}	320	—	ns
$\overline{RD}$ "L" Pulse Width	t_{WRD}	320	—	ns
$\overline{WR}$, $\overline{RD}$ "H" Pulse Width	t_{WH}	210	—	ns
Address Hold Time	t_{HA1}	25	—	ns
$\overline{CS}$ Hold Time	t_{HA2}	25	—	ns
Data Set-up Time	t_{SWD}	300	—	ns
Data Hold Time (Write operation)	t_{HWD}	20	—	ns
$\overline{WR}$, $\overline{RD}$ Fall Time	t_f	—	25	ns
$\overline{WR}$, $\overline{RD}$ Rise Time	t_r	—	25	ns
Data Delay Time	t_{SRD}	—	190	ns
Data Hold Time (Read operation)	t_{HRD}	0	—	ns
Busy Output Delay Time	t_{BD}	—	410	ns

Write operation

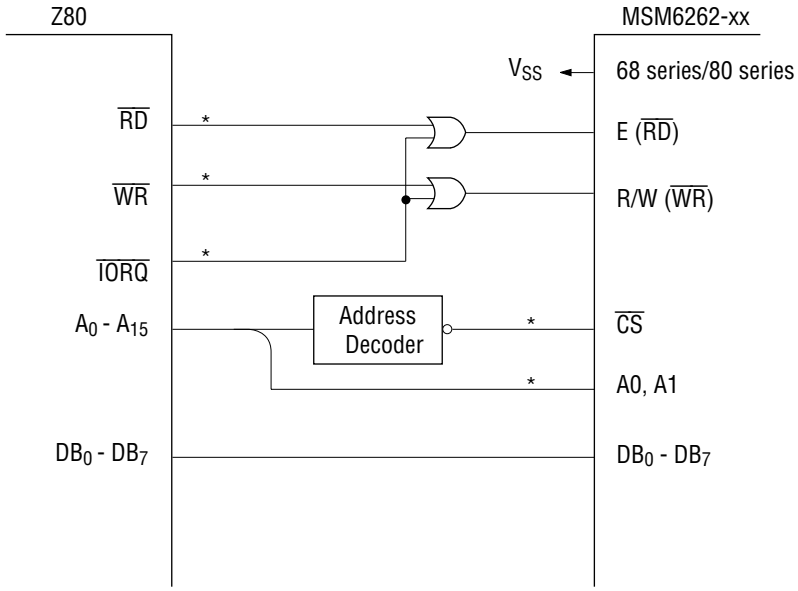


Read operation



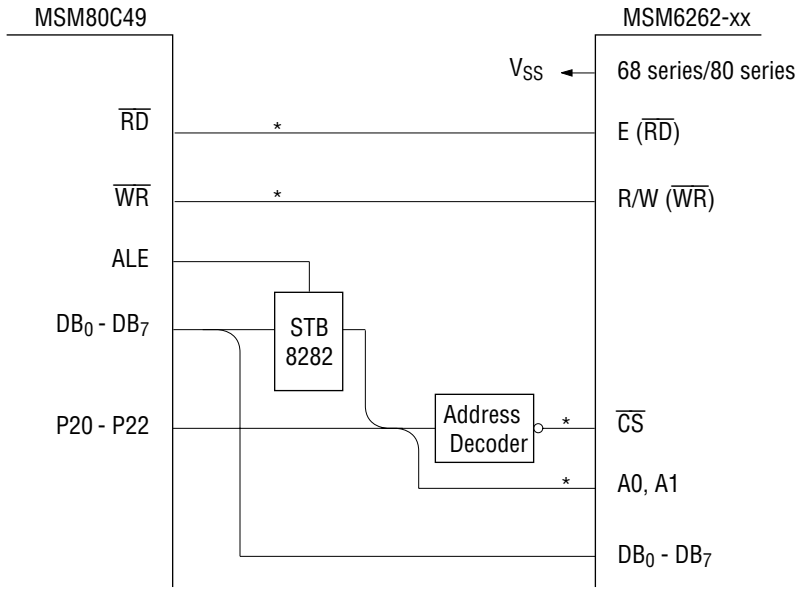
Refer to the DC Characteristics for the definition of V_{IH}, V_{IL}, V_{OH} and V_{OL}.

• Interface with Z80



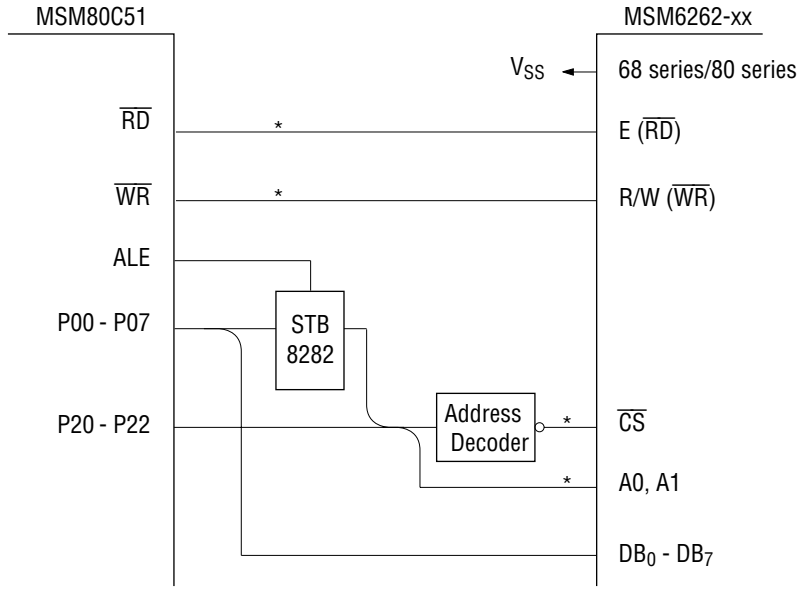
* A pull-up resistor of about 50 kΩ is required when the output of CPU becomes high impedance.

• Interface with 80C49



* A pull-up resistor of about 50 kΩ is required when the output of CPU becomes high impedance.

• Interface with 80C51



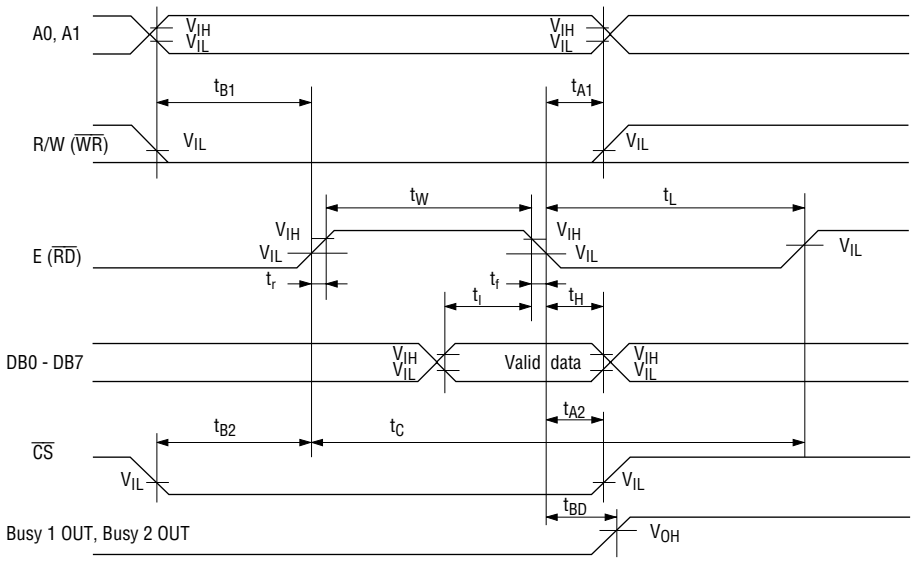
* A pull-up resistor of about 50 kΩ is required when the output of CPU becomes high impedance.

Interface with 68 Series CPU

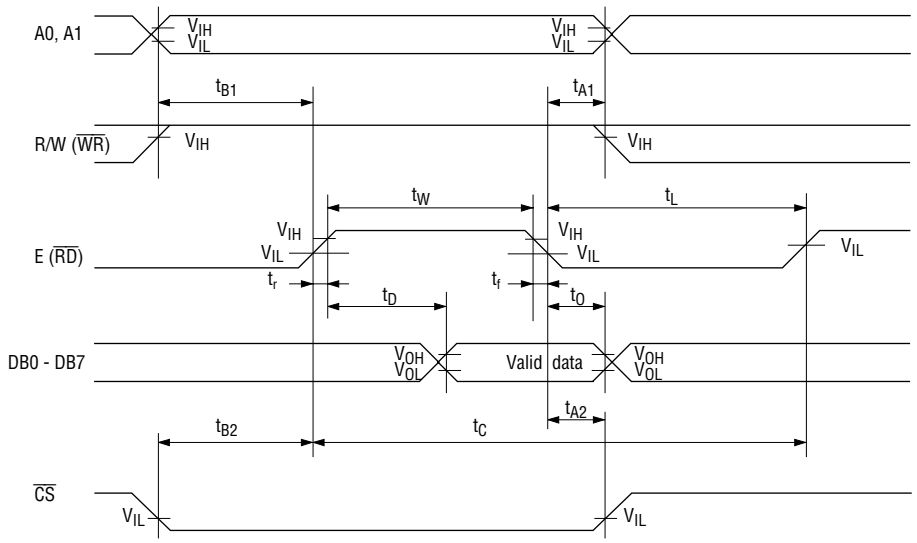
(V_{DD} = 4.5 to 5.5 V, Ta = –20 to +75°C)

Parameter	Symbol	Min.	Max.	Unit
Cycle Time	t_C	500	—	ns
Address, R/W Set-up Time	t_{B1}	100	—	ns
$\overline{CS}$ Set-up Time	t_{B2}	90	—	ns
E signal "H" Pulse Width	t_W	220	—	ns
E signal "L" Pulse Width	t_L	210	—	ns
Address, R/W Hold Time	t_{A1}	20	—	ns
$\overline{CS}$ Hold Time	t_{A2}	20	—	ns
Data Set-up Time	t_I	225	—	ns
Data Hold Time (Write operation)	t_H	30	—	ns
E signal Rise Time	t_r	—	25	ns
E signal Fall Time	t_f	—	25	ns
Data Delay Time	t_D	—	180	ns
Data Hold Time (Read operation)	t_O	10	—	ns
Busy Output Delay Time	t_{BD}	—	410	ns

Write operation

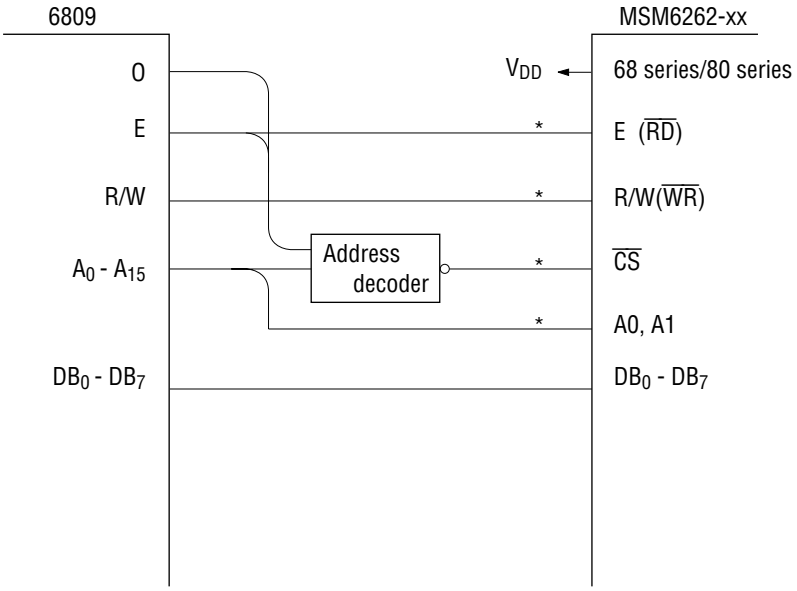


Read operation



Refer to the DC Characteristics for the definition of V_{IH}, V_{IL}, V_{OH}, and V_{OL}.

• Interface with 6809

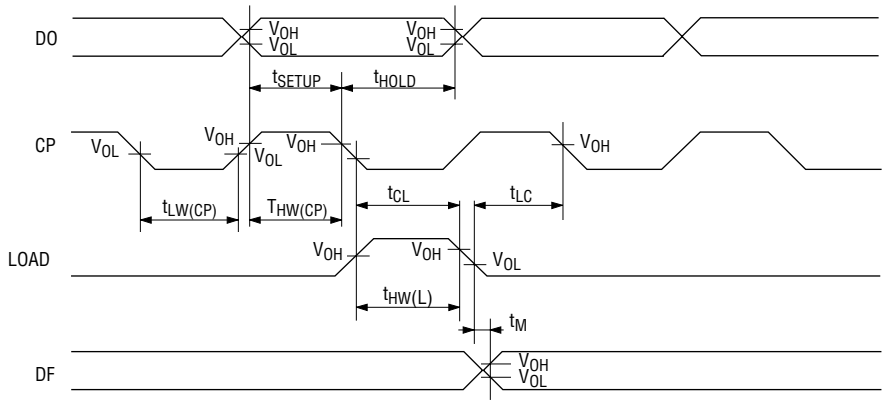


* A pull-up resistor of about 50 kΩ is required when the output of CPU becomes high impedance.

Interface with Segment Driver

(V_{DD} = 4.5 to 5.5 V, Ta = –20 to +75°C, f_{OSC} = 500 kHz)

Parameter	Symbol	Min.	Max.	Unit
Clock "L" Pulse Width	$t_{LW(CP)}$	400	—	ns
Clock "H" Pulse Width	$t_{HW(CP)}$	400	—	ns
Do Set-up Time	t_{SETUP}	200	—	ns
Do Hold Time	t_{HOLD}	200	—	ns
LOAD, Clock Set-up Time	t_{CL}	200	—	ns
LOAD, Clock Hold Time	t_{LC}	100	—	ns
LOAD, "H" Pulse Width	$t_{HW(L)}$	400	—	ns
DF Delay Time	t_M	–500	500	ns

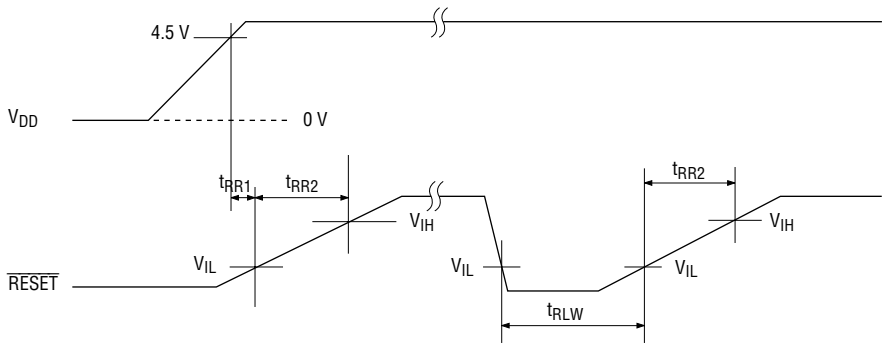


Refer to the DC Characteristics for the definition of V_{IH}, V_{IL}, V_{OH}, and V_{OL}.

Reset Waveform

(V_{DD} = 4.5 to 5.5 V, Ta = –20 to +75°C)

Parameter	Symbol	Min.	Max.	Unit
"L" Input Time upon power on	t_{RR1}	0.25	—	ms
"L" Input Width when in operation	t_{RLW}	0.5	—	ms
Rise Time	t_{RR2}	0.1	200	ms



Refer to the DC Characteristics for the definition of V_{IH}, V_{IL}, V_{OH}, and V_{OL}.

FUNCTIONAL DESCRIPTION

1. Instruction Register (IR) and Data Register (DR)

   The MSM6262-xx has two registers, instruction register (IR) and data register (DR).
   IR is used to store the address code or instruction code of display data RAM (DD RAM) or character generator RAM (CG RAM).
   This register can be written by the CPU, but cannot be read out by the CPU.
   DR is used to store the data to write into (or read out) the data to/from DD RAM or CG RAM.
   The data written into DR by the CPU is automatically written into the DD RAM or CG RAM.
   When an address code is written into IR, the data of the specified address is automatically transferred to the DR from either DD RAM or CG RAM. By having the CPU subsequently read the DR, it is possible to verify DD RAM or CG RAM data.
   After the writing of DR by the CPU, the DD RAM or CG RAM of the next address is selected to be ready for the next CPU writing.
   Likewise, after the reading operation of the CPU, DD RAM or CG RAM data of the next address is transferred to the DR, when CPU is ready for the next reading operation.

2. Busy Flag (BF)

   When the output of BUSY 1 OUT is "H", MSM6262-xx is engaged in internal operation.
   When the output of BUSY 2 OUT is "H", it indicates that MSM6262-xx is engaged in internal operation or MSM6262-xx is engaged in the revising of the display starting line on the LCD. (Refer to the instruction table.)
   When the output of BUSY 1 OUT is "H", any input of new instruction is ignored. So, before setting a new instruction, it is necessary to check whether BUSY 1 OUT and BUSY 2 OUT are at "L".

3. Address Counter (ADC)

   The address counter (ADC) allocates the address for the DD RAM and CG RAM write/read and also for the cursor display.
   When the instruction code for a DD RAM address or CG RAM address setting is input to IR, after deciding whether it is DD RAM or CG RAM, the address counter code is transferred from IR to ADC. After writing (reading) the display data to (from) the DD RAM or CG RAM, the ADC increments (or decrements) by 1 automatically as its internal operation.

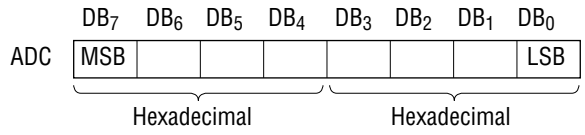
4. Timing Generator Circuit

This circuit generates the timing signal for the internal operation by CPU's instruction as well as to operate the internal circuit of DD RAM, CG RAM, CG ROM and so forth. It also generates the transfer signal to the SEGMENT driver (MSM5839C or MSM5259).
The internal operation accessed by the CPU and internal operation for LCD display is independent.
So, a manipulation such as writing data from CPU to DD RAM will not have an influence such as display flickering upon any part other than the display part to which the data is written.

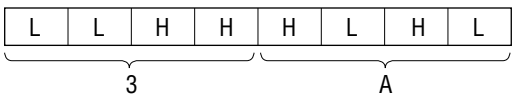
5. Display Data RAM (DD RAM)

DD RAM is used to store the 8-bit character code (refer to Table 1) and 1-bit under-line data. The address of DD RAM corresponds to the display position on the LCD. The correspondence is described below.

DD RAM address (set to ADC) is described as hexadecimal.



Example: When DD RAM address is 3A



(1) Relation between DD RAM and display position in 2-line display mode

	Digit 1	2	3	4	5	– – –	79	80	Display position
1st line	00	01	02	03	04	– – –	4E	4F	DD RAM address (hexadecimal)
2nd line	80	81	82	83	84	– – –	CE	CF	

Note: The address of the last digit of the first line and the first digit of the second line does not have any continuity.

(2) When 2 pieces of MSM5389C(or MSM5259) are connected to MSM6262-xx, 32 characters can be displayed from the first digit to yhe 16th degit.

	Digit 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1st line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
2nd line	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F

{ or MSM5839C (1) MSM5259 (1)

MSM5839C (2) MSM5259 (2) }

When the display is shifted by an instruction, the relation between the DD RAM address and the display position becomes as follows.

(Shift to the right)

	Digit 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1st line	4F	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E
2nd line	CF	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E

{ or MSM5839C (1) MSM5259 (1) — MSM5839C (2) MSM5259 (2) }

1st line	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10
2nd line	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F	90

(Shift to the left)

(3) The maximum DD RAM capacity of MSM6262-xx is for 160 characters. So, up to 10 pieces of MSM5839C (or MSM5259) can be connected in the case of 2-line display mode.

	Digit 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	– – –	73	74	75	76	77	78	79	80
1st line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	– – –	48	49	4A	4B	4C	4D	4E	4F
2nd line	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F	90	91	– – –	C8	C9	CA	CB	CC	CD	CE	CF

{ or MSM5839C (1) MSM5259 (1) — MSM5839C (2) MSM5259 (2) — MSM5839C (3)-(9) MSM5259 (3)-(9) — MSM5839C (10) MSM5259 (10) }

(4) Relation between the DD RAM and display position in 4-line display mode

	Digit 1	2	3	4	5	– – –	39	40	Display position
1st line	00	01	02	03	04	– – –	26	27	DD RAM address (hexadecimal)
2nd line	40	41	42	43	44	– – –	66	67	
3rd line	80	81	82	83	84	– – –	A6	A7	
4th line	C0	C1	C2	C3	C4	– – –	E6	E7	

Note: The address of the last digit of the previous line and the first digit of the next line does not have any continuity.

(5) When 2 pieces of MSM5839C (or MSM5259) are connected to MSM6262-xx, 64 characters can be displayed from the first digit to the 16th digit.

Digit	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1st line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
2nd line	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F
3rd line	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F
4th line	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CB	CF

{ or MSM5839C (1) MSM5259 (1)　　MSM5839C (2) MSM5259 (2) }

When the display is shifted by an instruction, the relation between the DD RAM address and the display position becomes as follows.

(shift to right direction)

Digit	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
1st line	27	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E
2nd line	67	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E
3rd line	A7	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E
4th line	E7	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE

{ or MSM5839C (1) MSM5259 (1)　　MSM5839C (2) MSM5259 (2) }

1st line	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10
2nd line	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50
3rd line	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F	90
4th line	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF	D0

(shift to left direction)

(6) The maximum DD RAM capacity of MSM6262-xx is for 160 characters. So, up to 5pieces of MSM5839C (or MSM5259) can be connected in the case of 4-line display mode.

Digit	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	– – –	33	34	35	36	37	38	39	40
1st line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	– – –	20	21	22	23	24	25	26	27
2nd line	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	– – –	60	61	62	63	64	65	66	67
3rd line	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F	90	91	– – –	A0	A1	A2	A3	A4	A5	A6	A7
4th line	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF	D0	D1	– – –	E0	E1	E2	E3	E4	E5	E6	E7

or MSM5839C (1) MSM5259 (1)　MSM5839C (2) MSM5259 (2)　MSM5839C (3),(4) MSM5259 (3),(4)　MSM5839C (5) MSM5259 (5)

6. Cursor/Blink Control Circuit

This is the circuit to control the generation of cursor and its blinking. This circuit is controlled by the program of the CPU.
The position of the cursor and its blink appears on the position according to the ADC contents, which correspond to the address of DD RAM. For example, when the ADC is set as "07" (hex.), the position of cursor and its blinking becomes as follows.

	DB7			– – –				DB0
ADC	0	0	0	0	0	1	1	1
				0				7

2-line display

Cursor and its blinking position

Digit	1	2	3	4	5	6	7	8	9		79	80
	00	01	02	03	04	05	06	07	08	– – –	4E	4F
	80	81	82	83	84	85	86	87	88	– – –	CE	CF

4-line display

Cursor and its blinking position

Digit	1	2	3	4	5	6	7	8	9		39	40
	00	01	02	03	04	05	06	07	08	– – –	26	27
	40	41	42	43	44	45	46	47	48	– – –	66	67
	80	81	82	83	84	85	86	87	88	– – –	A6	A7
	C0	C1	C2	C3	C4	C5	C6	C7	C8	– – –	E6	E7

Note: Cursor display and blinking can be performed even when the CG RAM address is set in the ADC. So, it is necessary to disable the cursor display and blinking when the CG RAM address is set in the ADC.

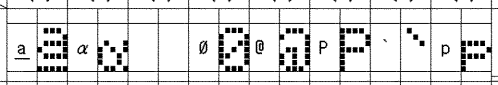
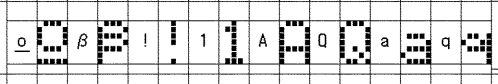
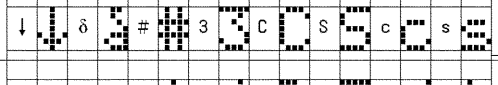
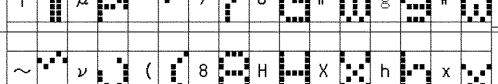
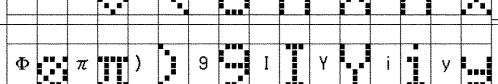
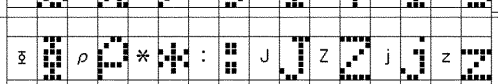
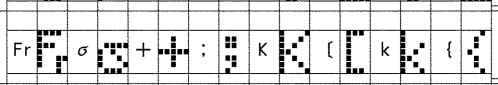
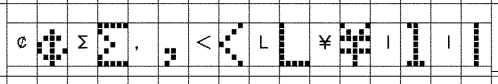
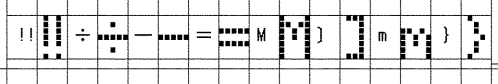
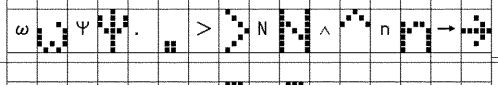
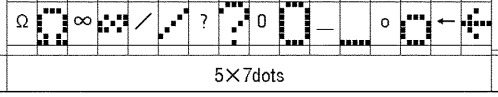
7. Underline Control Circuit

First, either underline display mode or underline blinking mode has to be set by the CPU. When an instruction to enable the underline function is input from the CPU, the cursor display shifts to the right direction (increment) or left direction (decrement). Display of underline appears (or disappears) on the same position where cursor was displayed.
An input of "H" data enables the underline display, while an input of "L" data deletes the underline.

8. Character Generator ROM (CG ROM)

CG ROM stores the character pattern. MSM6262-xx has 128 kinds of 5 x 7-dot patterns, 96 kinds of 5 x 11-dot patterns and 32 kinds of 5 x 12-dot patterns. The character pattern corresponds to the character code which is written into the DD RAM.
The relation between 8-bit character code and character pattern is described in Table 1.
When the 8-bit character code of CG ROM is written into the DD RAM, the character pattern of the corresponding character code of the CG ROM is displayed on the LCD position corresponding to the DD RAM address.
When all of the upper 4 bits of CG ROM code are "L", CG ROM can be switched to CG RAM.

Table 1 Character code and character pattern of Standard Code (MSM6262-04)

Upper 4 bits / Lower 4 bits	0000 (0)	0001 (1)	0010 (2)	0011 (3)	0100 (4)	0101 (5)	0110 (6)	0111 (7)	1000 (8)	1001 (9)	1010 (A)	1011 (B)	1100 (C)	1101 (D)	1110 (E)	1111 (F)
0000 (0)																
0001 (1)																
0010 (2)																
0011 (3)																
0100 (4)																
0101 (5)																
0110 (6)																
0111 (7)																
1000 (8)																
1001 (9)																
1010 (A)																
1011 (B)																
1100 (C)																
1101 (D)																
1110 (E)																
1111 (F)																
Configuration	5×7dots								5×11dots						5×12dots	

9. Character Generator RAM (CG RAM)

The CG RAM is used to display user's original character pattern other than CG ROM.
The CG RAM has capacity (32 bytes = 256 bits) to write 4 kinds of 5 x 8 dots and 2 kinds of 5 x 12 dots.
In displaying the character pattern stored in the CG RAM, CG RAM has to be enabled by an instruction. When CG RAM is enabled, CG ROM code for 16 characters cannot be read out since the CGROM code with all "L" on the upper 4 bits is used as CG RAM code.
The following describes how to write character patterns into the CG RAM and how to display them on the LCD.

(1) When the character pattern is 5 x 8 dots (See Table 2-1)

- A method to write character pattern into the CG RAM by the CPU

  The lower 3 bits (0 - 2) of the CG RAM address correspond to the line position of the character pattern. The upper 2 bits (3, 4) of the CG RAM address correspond to the lower 2 bits (0, 1) of the character code.
  First, set increment of decrement by the CPU, and then input CG RAM address. After this, write character pattern data into CG RAM through DB0 to DB7 line by line.
  DB0 - DB7 correspond to CG RAM data 0 - 7 in Table 2-1.
  Display is turned on when "H" is set as input data and turned off when "L" is set as input data.
  Since the ADC is automatically incremented or decremented by 1 after the writing of data to the CG RAM, it is not necessary to set the CG RAM address again.
  To enable cursor display, set all input data on the line where the lower 3 bits of the CG RAM (0-2) are all "H" to "L".
  0 - 4 bits of CG RAM data are output to the LCD as the display data; however, 5 - 7 bits of CG RAM data are not. But it can be used as the data RAM because the data can be written/read through DB0 to DB7.

- A method to display the CG RAM character pattern to the LCD

  First, an instruction to enable the CG RAM has to be input from the CPU. CG RAM is selected only when all of the upper 4 bits of the character code is "L".
  So, the character pattern of CG RAM is displayed on the LCD position that corresponds to the DD RAM address, when the character code shown in Table 2-1 is written into DD RAM.
  Since the bits 2 and 3 of the character code are regarded as invalid, "K" is displayed when the character codes "01", "05", "'09", and "0D" are selected.

(2) When the character pattern is 5 x 12 dots (See Table 2-2)

- A method to write character pattern into the CG RAM by the CPU

  The lower 4 bits of CG RAM address (0 - 3) correspond to the line position of the character pattern.
  The upper 1 bit of CG RAM address bit 4 corresponds to the bit 1 of the character code.
  First, set increment or decrement by the CPU, and then input CG RAM address.
  After this, write the character pattern data into CG RAM through DB_0 to DB_7 line by line.
  DB_0 - DB_7 correspond to CG RAM data 0 - 7 in Table 2-2.
  Display is turned on when "H" is set as the input data and turned off when "L" is set

as the input data.
Since the ADC is automatically incremented or decremented by 1 after the writing of data to the CG RAM, it is not necessary to set the CG RAM address again.
To enable cursor display, set all input data on the line where the CG RAM address is "0B" or "1B" (hex.) to "L".
The addresses "0" to "B" (hexadecimal) in the bits 0 to 4 of the CG RAM data are output on the LCD as the display data. However, the addresses "C" to "F" (hexadecimal) in the bits 0 to 4, and 5 to 7 of the CG RAM data are not output on the LCD. But these CG RAM data can be used as the data RAM so that they can be written into or read out through DB0 to DB7.

- A method to display the CG RAM character pattern on the LCD

First, an instruction to enable the CG RAM has to be input from the CPU. CG RAM is selected only when all of the upper 4 bits of the character code is "L".
So, the character pattern of CG RAM is displayed on the LCD position corresponding to the DD RAM address, when the character code shown in Table 2-2 is written into the DD RAM.
Since bits 0, 2 and 3 of the character code are regarded as invalid, the character of "μ" is displayed when the character codes "00", "01", "04", "05", "08", "09", "0C" and "0D" are selected.

(3) A method to read out the CG RAM data

First, set the CG RAM address by inputting a CG RAM address set instruction from the CPU.

Then, execute the CG RAM/DD RAM data read instruction. The set data of CG RAM address is output from the DB0 to DB7. The 8-bit data, read out from the MSM6262-xx, corresponds to the data which is written into the CG RAM. Since the CG RAM address is automatically incremented or decremented by 1, the CG RAM read out instruction can be successfully input. It is necessary, however, to set the DD RAM at data transferring condition by executing the DD RAM address set instruction after all of CG RAM data are read out.

Table 2-1 Relation between CG RAM data (character pattern) vs. CGRAM address and DDRAM data vs. character pattern when the character pattern is 5 × 8 dots.

CG RAM ADDRESS	CG RAM DATA (Character Pattern)	DD RAM DATA (Character Code)
4 3 2 1 0 LSB	7 6 5 4 3 2 1 0 MSB LSB	7 6 5 4 3 2 1 0 MSB LSB
L L L L L L L H L H L L H H H L L H L H H H L H H H	X X X L H H H L H L L L H H L L L H H L L L H H L L L H H L L L H L H H H L L L L L L	L L L L X X L L
L H L L L L L H L H L L H H H L L H L H H H L H H H	X X X H L L L H H L L H L H L H L L H H L L L H L H L L H L L H L H L L L H L L L L L	L L L L X X L H
H H L L L L L H L H L L H H H L L H L H H H L H H H	X X X L H H H L L L H L L L L H L L L L H L L L L H L L L L H L L L H H H L L L L L L	L L L L X X H H

X: Don't care

Table 2-2 Relation between CGRAM data (character pattern) vs. CGRAM address and DDRAM data vs. character pattern when the character pattern is 5 × 12 dots.

CG RAM ADDRESS	CG RAM DATA (Character Pattern)	DD RAM DATA (Character Code)
4 3 2 1 0 LSB	7 6 5 4 3 2 1 0 MSB LSB	7 6 5 4 3 2 1 0 MSB LSB
L L L L L	X X X L L L L L	
L L L L H	L L L L L	
L L H L L	L L L L L	
L L H H	L H L L L	
L H L L	L H H H H	
L H L H	H L L H L	L L L L X X L X
L H H L	L H H H H	
L H H H	L H L H L	
H L L L	H H H H H	
H L L H	L L L H L	
H L H L	L L L L L	
H L H H	L L L L L	← B
H H L L	X X X X X	
H H L H		
H H H L		
H H H H		
H L L L L	X X X L L L L L	
L L L H	L L L L L	
L L H L	L L L L L	
L L H H	L L L L L	
L H L L	L L L L L	
L H L H	H L L L H	L L L L X X H X
L H H L	H L L L H	
L H H H	L H L H L	
H L L L	L L H L L	
H L L H	L H L L L	
H L H L	H L L L L	
H L H H	L L L L L	← B
H H L L	X X X X X	
H H L H		
H H H L		
H H H H		

X: Don't care

9. LCD Display Circuit (COM1 to COM48, DO, CP, LOAD, DF)

The MSM6262-xx is provided with COMMON signal output. So, maximum 160 characters can be displayed when it is used together with SEGMENT drivers (MSM5259 or MSM5839C). Interface between MSM6262-xx and SEGMENT drivers can be done by using DO, CP, LOAD and DF.
The SEGMENT data is serially output from DO pin, synchronized with the pulse which is output from the CP pin.
This data, input to the SEGMENT driver, is converted from serial data to parallel data by the latch pulse which is output from the LOAD pin of MSM6262-xx and this converted data is used as the display data. This parallel/serial conversion is performed synchronized with the COMMON signal of MSM6262-xx and LCD display AC signal which is output from DF pin. So, this signal can drive dot matrix LCD panel.

10. Reset Circuit

Power-on-reset is required for MSM6262-xx when it is powered-on. So, a capacitor has to be connected between $\overline{\text{RESET}}$ pin and V_{SS} pin.
It is also advisable to connect a diode between $\overline{\text{RESET}}$ pin and V_{DD} pin when it is required to connect a capacitor of more than 3.3 µF to $\overline{\text{RESET}}$ pin.
When the power-on reset circuit normally operates, the busy flags 1 and 2 become at "H" level for about 10 ms after the power-on. During this period, a initialization of MSM6262-xx is performed by following procedures.

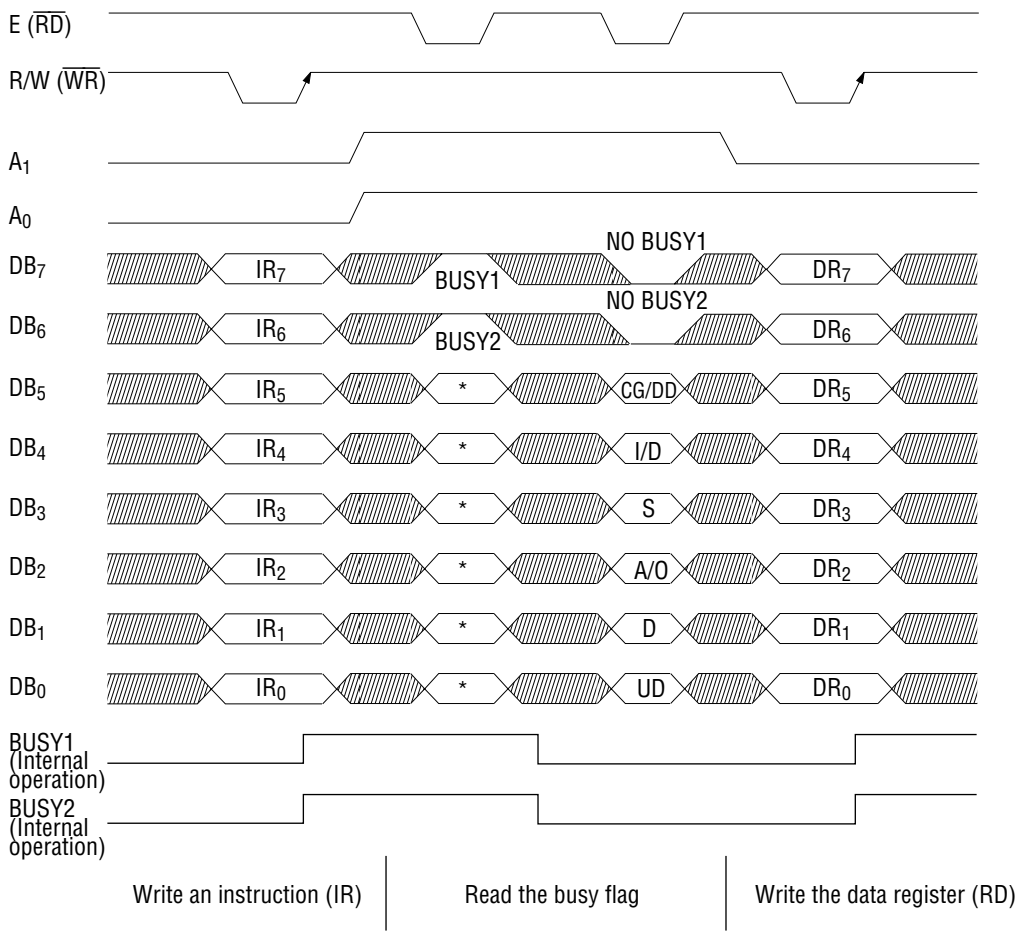
1 Display is cleared
2 CG ROM becomes enabled
3 No display shift
4 ADC is incremented
5 2-line display mode
6 5 x 8 dots font configuration
7 No display shift for "g", "j", "p", "q" and "y"
8 Display off
9 No display of cursor, blinking and underline

11. Data Bus with CPU

MSM6262-xx can be interfaced with 8-bit CPU, such as 6809, Z80, 80C49 and 80C51. When MSM6262-xx is connected with 6809, the 68 series/80 series pin has to be connected to V_{DD}. When MSM6262-xx is connected with Z80, 80C49 or 80C51, the 68 series/80 series pin has to be connected to V_{SS}. The level at 68 series/80 series cannot be switched during MSM6262-xx's operation. It must be connected with either V_{DD} or V_{SS} before MSM6262-xx is turned on.

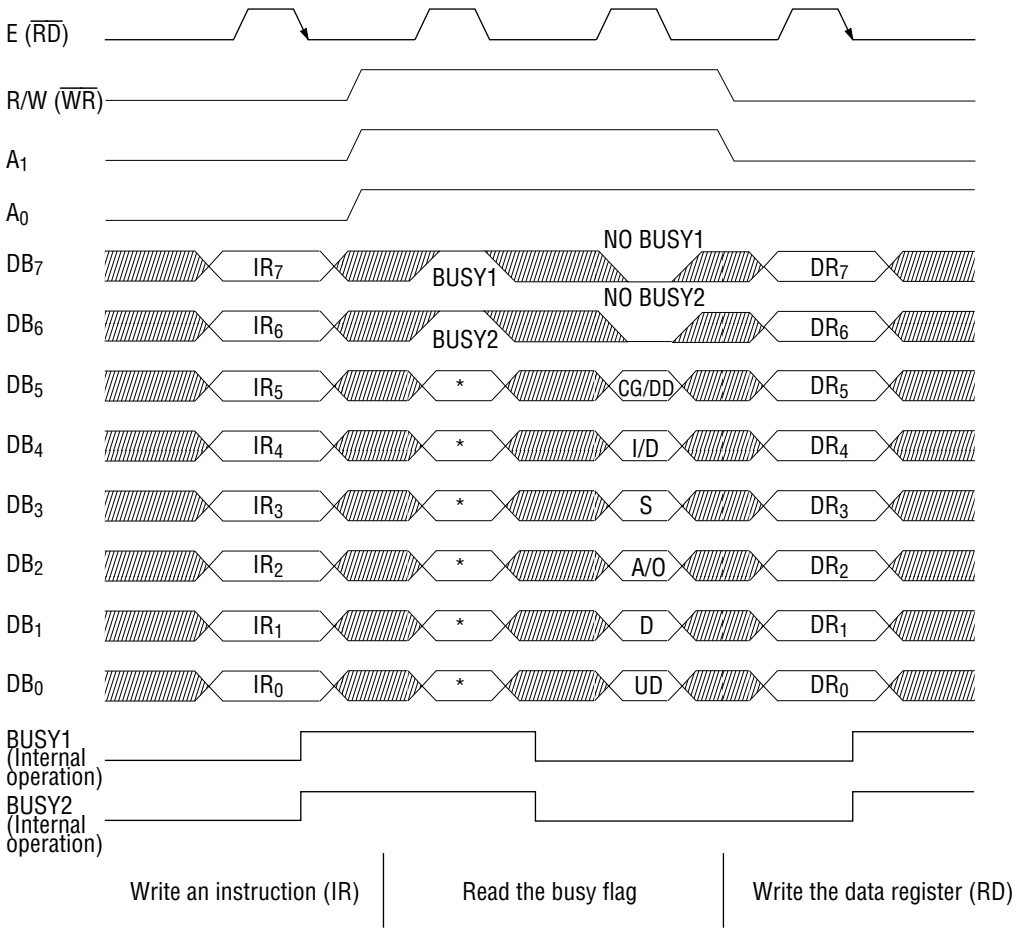
Note: It is possible, indeed, to change the 68 series/ 80 series pin's level when a reset signal is being input to $\overline{\text{RESET}}$ pin. However, the 68 series /80 series pin does not have characteristics to have an interface with MCU, nor does it have an antichattering circuit.
Further, if a reset signal is input, the MSM6262-xx is initialized as described above. So, in this case, changing the 68 series/80 series pin level is not recommended.

80 series CPU data transfer



* : Don't care

68 series CPU data transfer



* : Don't care

Instruction Table

* : DON'T CARE

80series CPU / 68series CPU	Note 1	A_1	A_0	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	Explanation	Execution Time (MAX), When fosc = 500kHz
	R/W	A_1	A_0	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0		
Display Clear	L	L	L	L	L	L	L	L	L	L	H	Clears all of the display. and sets address 0 of DD RAM in the address counter.	3.22 ms
Return	L	L	L	L	L	L	L	L	L	H	CR/C	CR/C = L: Cursor home CR/C = H: Carriage Return	1.62 ms
Under Line	L	L	L	L	L	L	L	L	H	UL	*	UL = H: Writes the underline in the cursor part before executing this instruction. UL = L : Erases the underline in the cursor part before executing this instruction.	20 µs
Entry Mode Set	L	L	L	L	L	L	L	H	I/D	S	A/O	Sets whether the display of the direction of cursor (I/D) move should be shifted or not. When the data is being written or read, this operation is performed. This instruction also sets whether the character code of DD RAM is used as CG ROM or CG RAM.(A/O)	20 µs
Display/Cursor Shift	L	L	L	L	L	L	H	S/C	UD/RL	D_2 (UR/DL)	D_1 (*)	Shifts the cursor and display without changing the DD RAM contents. (S/C, UD/RL,UR/DL) The line to be displayed in the uppermost position can be set.	20 µs
CG RAM address Set	L	L	L	L	L	H	A_{CG}					Sets the CG RAM address. The dara, which will be sent/received after the CG RAM address is set, is CG RAM data.	20 µs
Function Set	L	L	L	L	H	N	*	F_1	F_2	F_3	*	Sets the following: No. of display digits (N), Character font (F_1), Cursor line font (F_2), Font shift of "g, j, p, q, y" (F_3)	20 µs
Display Control	L	L	L	H	D	C	B	UC	UB	*	*	Sets the following: All display on/off (D), Cursor display on/off (C), Character on the cursor position blink on/off (B), Underline display on/off (UC), Character, on the underline, blink on/off (UB)	20 µs
CG RAM/DD RAM Data Write	L	L	H	WRITE DATA								Writes a data in either DD RAM or CG RAM.	20 µs
DD RAM Address Set	L	H	L	A_{DD}								Sets DD RAM address. The data which is sent/received after that is DD RAM data.	20 µs
Read the Underlined Data	H	L	L	ULD	READ DATA							Reads following data: Data on the underline, DD RAM or CG from RAM data.	20 µs
Read the CG RAM/ DD RAM Data	H	L	H	READ DATA								Reads the data either from DD RAM or from CG RAM.	20 µs
Read the Address Counter Content	H	H	L	A_{DC}								Reads the address counter contents.	0 µs
Read Busy Flag	H	H	H	B1F	B2F	CG/DD	I/D	S	A/O	D	UD	Busy 1 flag (B1F) shows that MSM6262-xx's internal operation is going on. Busy 2 flag (B2F) shows that the revising of display starting line is going on. CG/DD shows whether the data, being transmitted or received, is of CG RAM or DD RAM. I/D shows the direction in which cursor moves. S shows the display shift. A/O shows that the DD RAM character code is CG RAM character code or CG RAM character code. D shows the all display on/off. UD shows underline display on/off.	0 µs

CR/C = H : Carriage Return
UL = H : Write underline
I/D = H : Increment
S = H : Accompany display shift
A/O = L : CG ROM ENABLE
S/C = H : Display move
UD/RL = H: Up/Down move
D_2,D_1 : The bit to set the line to be displayed in the uppermost position. D_1 is LSB. D_2 is MSB.
UR/DL = H: Upper-right move
N = L : 2 lines
N = H : 4 lines
F_1 = H : 5 x 11 dots
F_2 = L : 5 x 12 dots or 5 x 8 dots
F_3 = H : Shift "g, j, p, q, y" to the lower position by 1 dot.
ULD = H : Underline data exists
B1F = H : Internal operation going on
B2F = H : Revising the display starting line or internal operation going on
CG/DD = H: Transmit /Receive CG RAM data

CR/C = L : Cursor home
UL = L : Underline erase
I/D = L : Decrement
A/O = H : CG RAM ENABLE
S/C = L : Cursor move
UD/RL = L : Left/Right move
UR/DL = L : Down-left move
F_1 = L : 5 x 7 dots
F_2 = H : 5 x 11 dots or 5 x 7 dots
F_3 = L : Disable character shift
ULD = L : No underline data
B1F = L : Ready to receive instruction
B2F = L : No revision on display starting line
CG/DD = L : Transmit/Receive of DD RAM data

DD RAM : Display data RAM
CG RAM : Character generator RAM
A_{CG} : CG RAM address
A_{DD} : DD RAM address
A_{DC} : Address counter which is used for both DD RAM and CG RAM

When fosc = 600 kHz, execution time becomes

$20\ \mu s \times \frac{500}{600}$

$\fallingdotseq 16.7\ \mu s$

Note 1: In the case of 80 series CPU, access to MSM6262-xx is done by $\overline{WR}$ and $\overline{RD}$. So, a bit for part of the read/write code is not required.

12. Instruction Code

The instruction code is defined as the signal through which the MSM6262-xx is accessed by the CPU. MSM6262-xx starts its operation upon receipt of the instruction code.
The internal processing operation starts with a timing that does not affect the LCD display, so, the busy condition is longer than that of cycle time.
In the busy condition, MSM6262-xx does not execute any instruction other than the reading of busy flag. Therefore, make certain that busy flag is set at "L" before inputting the instruction code.

(1) Display clear

	A_1	A_0	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	L	L	L	L	L	L	L	L	L	H

When this instruction is executed, the LCD display is cleared.
When cursor display and/or character blink is being performed, their display position moves to the left end of the LCD. (In the case of 2-line or 4-line display mode, it moves to the left end of the first line.)
All of the DD RAM data becomes "20" (hex), while ADC data becomes "00" (hex.). If the display is on a shifted position, it returns to the original position.
Data for underline is re-written as "L" and display turns off.

(2) Return

- CR/C = L (Cursor home)

	A_1	A_0	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	L	L	L	L	L	L	L	L	H	CR/C

When this instruction is executed, cursor and blinking position moves to the left end of the LCD. (In the case of 2-line or 4-line display mode, it moves to the left end of the first line.)
When display is being shifted, the display returns to its original position for both horizontally and vertically.
ADC becomes "00" (hex.).

- CR/C = H (Carriage return)
When this instruction is executed, cursor and blinking position moves to the left end of the line on which the cursor and brink were positioned before execution of instruction.
If the display is being shifted when this instruction was executed, the cursor and blinking position moves to the original position before it was shifted only concerning to the shift to the right and left.
All bits other than line specifying bit of ADC will be reset to "0" (hex.).

(3) Underline

	A_1	A_0	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	L	L	L	L	L	L	L	H	UL	*

*: Don't care

- UL = H (Write underline)
  When this instruction is executed, the underline appears on the cursor position. Cursor will move to the right or left if either increment or decrement is specified.

- UL = L (Erase underline)
  When this instruction is executed, the underline on the cursor position disappears. Cursor will move to the right or left if either increment or decrement is specified.
  When this instruction is executed, ADC will be automatically incremented by +1 or decremented by –1. Display is shifted accordingly.

(4) Entry mode set

	A_1	A_0	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	L	L	L	L	L	L	H	I/D	S	A/O

- I/D (Increment/Decrement)
  When this instruction is executed, DD RAM address will be incremented (I/D = "H") or decremented (I/D = "L") by 1, after the character code or underline code is written into (or read out from) the DD RAM.
  In the case of increment, cursor moves to the right, while the cursor moves to the left in the case of decrement.
  Processing for writing/reading the data into/from CG RAM is performed the same way.

- S (Display shift upon writing)
  When S = "H" and data is written into DD RAM, display is shifted either to the right or left. When I/D = "H", the whole display shifts to the left, while it shifts to the right when I/D = "L". So, display of cursor looks being stopped and display itself looks being shifted.
  In the case of reading the data from DD RAM, display is not shifted. Also in the case of reading/writing the data from/to CG RAM, display shall not be shifted.
  When S = "L", display is not be shifted.

- A/O (CG RAM ENABLE/CG ROM ENABLE)
  When A/O is "L", CG ROM will be enabled, and all CG ROM contets on Table 2 becomes selectable and CG RAM cannot be selected.
  CG RAM cannot be used as character code for display. But it can be used as data RAM.
  When A/O = "H", CG RAM is enabled.
  When the upper 4 bits of the character code in Table 1 are "00" (hex.), the bit pattern of CG RAM is displayed on the LCD. (CG RAM has a RAM area for 4 kinds of 5 x 8 dots and 2 kinds of 5 x 12 dots)
  CG ROM is selected when the upper 4 bits of the character code in Table 1 are "01" - "0F" (hex.).

(5) Display/Cursor move

	A_1	A_0	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	L	L	L	L	L	H	S/C	UD/RL	D_2 (UR/DL)	D_1 (*)

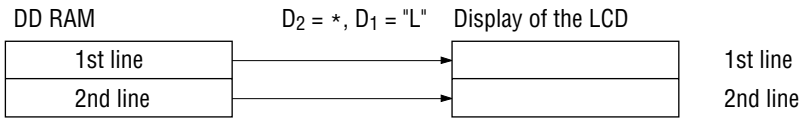
*: Don't care

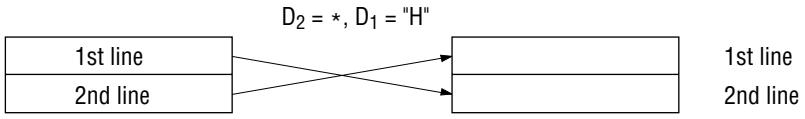
- S/C (Display move/Cursor move)
  This is the bit to select either display or cursor to move. S/C = "H" enables the display movement, while S/C = "L" enables the cursor movement.

- UD/RL (Upward or downward move/Right or left move)
  UD/RL = "H" enables upward or downward move. UD/RL = "L" enables right or left move.

- D_2, D_1 (Starting line of display)
  Upward or downward movement is enabled by setting the starting line of display. D_1 is LSB and D_2 is MSB. Both D_1 and D_2 are expressed in 2-bit binary data.
  Only D_1 is valid in 2-line mode. Both D_1 and D_2 are valid in 4-line mode.

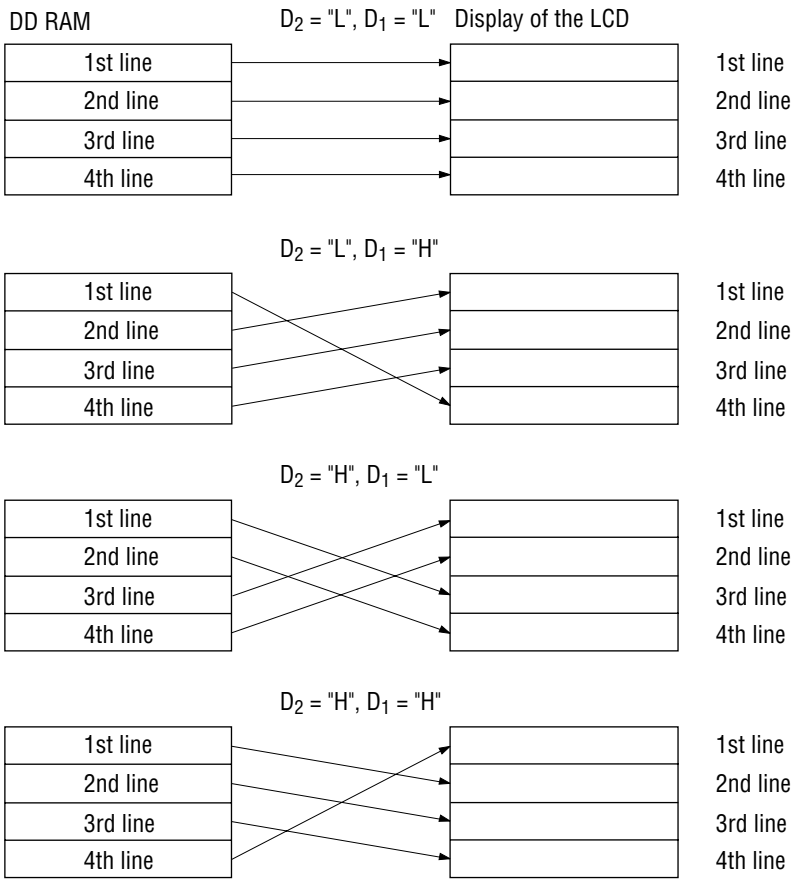
[2-line mode]





* : Don't care

[4-line mode]


DD RAM
D2 = "L", D1 = "L"
Display of the LCD
1st line
2nd line
3rd line
4th line
1st line
2nd line
3rd line
4th line
D2 = "L", D1 = "H"
1st line
2nd line
3rd line
4th line
1st line
2nd line
3rd line
4th line
D2 = "H", D1 = "L"
1st line
2nd line
3rd line
4th line
1st line
2nd line
3rd line
4th line
D2 = "H", D1 = "H"
1st line
2nd line
3rd line
4th line
1st line
2nd line
3rd line
4th line

- UR/DL (Up-right move/Down-left move)
  UR/DL = "H" enables up-right movement.
  UR/DL = "L" enables down-left movement.

  Combination of bit for Display/Cursor movement is as follwes

S/C	UD/ RL	D_2 (UR/ DR)	D_1 *	Explanation
L	L	L	*	Move the cursor to the left by 1 digit
L	L	H	*	Move the cursor to the right by 1 digit
L	H	L	*	Move the cursor downward by 1 digit
L	H	H	*	Move the cursor upward by 1 digit
H	L	L	*	Move the display to the left by 1 digit
H	L	H	*	Move the display to the right by 1 digit
H	H	L	L	Set the first line as the display starting line
H	H	L	H	Set the 2nd line as the display starting line
H	H	H	L	Set the 3rd line as the display starting line ▲
H	H	H	H	Set the 4th line as the display starting line ▲

* : Don't care

▲ : Invalid in 2-line mode

(6) CG RAM address set

	A_1	A_0	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	L	L	L	L	H	Ac_4	Ac_3	Ac_2	Ac_1	Ac_0

Set the CG RAM address which consists of 5 bits of Ac_4 - Ac_0. The data which will be transferred after this instruction is set will be limited to the CG RAM data (character font data).

(7) Function set

	A_1	A_0	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	L	L	L	H	N	*	F_1	F_2	F_3	*

*: Don't care

- N (Selection of LCD lines to be displayed)

N	LCD lines
L	2-line mode
H	4-line mode

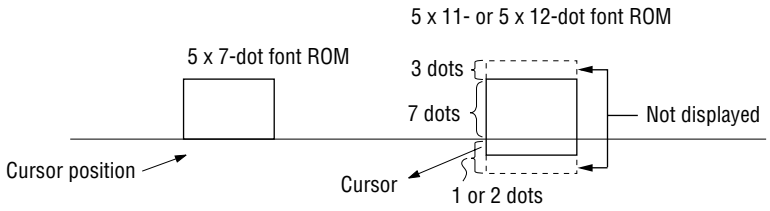
- F_1 (5 x 11 dots/5 x 7 dots)
  When F_1 = "H", 5 x 12-dot font is selected.
  When F_1 = "L", 5 x 8-dot font is selected.

- F_2 (Font assignment of cursor line)
  When F_2 = "L" and if character code, which has a display dot on the cursor position, is selected, it is displayed on the cursor line of LCD.
  When F_2 = "H" and if character code, which has a display dot on the cursor position, is selected, cursor is displayed but the bit on the cursor position is not displayed.
  However, this function does not apply to CG RAM and the bit on the cursor position is also displayed.

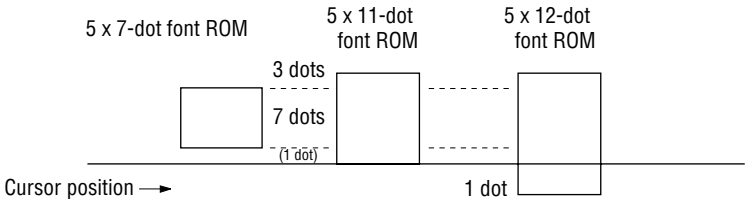
- F_3 (Character shift of "g, j, p, q, y")
  When F_3 = "H", each character of "g, j, p, q, y" is displayed shifted downward by 1 dot for the whole character.
  When F_3 = "L", display of these characters is the same as other characters, as shown in Table 1. This bit is valid only for 5 x 12-dot font.

  Example

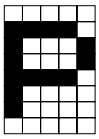
① F_1 = "L" (5 x 8-dot/font)



② F_1 = "H" (5 x 12-dot/font)

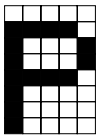


③ F_2 = "H"

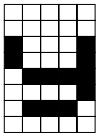


Cursor position

④ F_2 = "L"

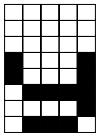


⑤ F_3 = "L"



Cursor position

⑥ F_3 = "H" (5 x 12-dot font only)



Shifted downward by 1 dot

(8) Display control

	A_1	A_0	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	L	L	H	D	C	B	UC	UB	*	*

*: Don't care

- D (All display on/off)
  When D = "H", display on the LCD is enabled.
  When D = "L", display is disabled.
  When display was disabled by setting D at "L", character code in the DD RAM does not change. So, when D becomes "H" again, display is enabled immediately.

- C (Cursor display on/off)
  C = "H", cursor display appears.
  When C = "L", cursor display disappears.

- B (Cursor blinking)
  When B = "H", blinking of character on the position corresponding to the cursor position, starts. Blinking of all-dot's-on and character (and cursor)-on is performed alternately for every 409.6 ms in case of fosc = 500 kHz and 5 x 8 dots font configuration (every 614.4 ms in case of 5 x 12 dots font configuration)
  When B = "L", blinking stops.
  Cursor and blinking can be set together.

- UC (Underline display)
  When UC = "H", underline is displayed on the cursor position.
  When UC = "L", underline display is disabled.

- UB (Underlined character blinking)
  When UB = "H", blinking of character on the position corresponding to the underline position, starts. Blinking of character stops when UB = "L".
  Cursor, blink, underline, and blinking of character on the underline can be set together.

(9) CG RAM and DD RAM data write

	A_1	A_0	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	L	H	DI_7	DI_6	DI_5	DI_4	DI_3	DI_2	DI_1	DI_0

Write the 8-bit data (DI_7 - DI_0) into either CG RAM or DD RAM. Determination of either CG RAM or DD RAM is made by the previously set CC RAM or DD RAM address set. After the data is written into the RAM, it is incremented or decremented by 1 according to the entry mode of the address. Display shift is also determined by the entry mode.

(10) DD RAM address set

	A_1	A_0	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	H	L	AI_7	AI_6	AI_5	AI_4	AI_3	AI_2	AI_1	AI_0

This instruction code sets the DD RAM address, which consists of 8 bits (A_{I7} to A_{I0}). The data which is received after this instruction is set is limited to the DD RAM data (character code data).
Do not input any address code other than those below.

2-line mode :	1st line	00 - 4F
	2nd line	80 - CF
4-line mode :	1st line	00 - 27
	2nd line	40 - 67
	3rd line	80 - A7
	4th line	C0 - E7

(11) Underline data read

	A_1	A_0	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	L	L	ULD	$D0_6$	$D0_5$	$D0_4$	$D0_3$	$D0_2$	$D0_1$	$D0_0$

This instruction reads underline data, and CG RAM or DD RAM data.
Determination of CG RAM or DD RAM is made by the previously set CG RAM or DD RAM address set.
The first data read by this instruction is an invalied data. Normal data is read out from the second instruction onward if the read instruction is executed continuously. This instruction address will be incremented or decremented by 1 according to the entry mode. Display shift is, however, not performed. Underline data is output to DB7 as either "H" (when display is on) or "L" (when display is off).
The MSB of RAM data is not read. RAM data consists of 7 bits (DB0 to DB6).

(12) CG RAM and DD RAM data read

	A_1	A_0	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	L	H	D_{07}	D_{06}	D_{05}	D_{04}	D_{03}	D_{02}	D_{01}	D_{00}

This instruction reads the 8-bit data (D_{O7} to D_{O0}) from either CG RAM or DD RAM. Determination of CG RAM or DD RAM is made by the previously set CG RAM or DD RAM address set.
The CG RAM address set instruction or DD RAM address set instruction has to be input just before executing this read instruction. If it is not input, the first output of the data becomes invalid. When this read instruction is performed continuously, normal data is output from the 2nd data onward.
In the case of DD RAM data read, normal data is output from the first data even if the address set is not input, provided that cursor is moved by the cursor shift instruction.
After reading the data, the address is incremented or decremented by 1 by the entry mode.
The shift of the display, however, is not performed.

(13) Address counter read

	A_1	A_0	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	H	L	A_{07}	A_{06}	A_{05}	A_{04}	A_{03}	A_{02}	A_{01}	A_{00}

This instruction reads the 8-bit data (A_{O7} to A_{O0}) . Address counter is determined by the previously set address set because it is used for both CG RAM and DD RAM.

(14) Busy flag read

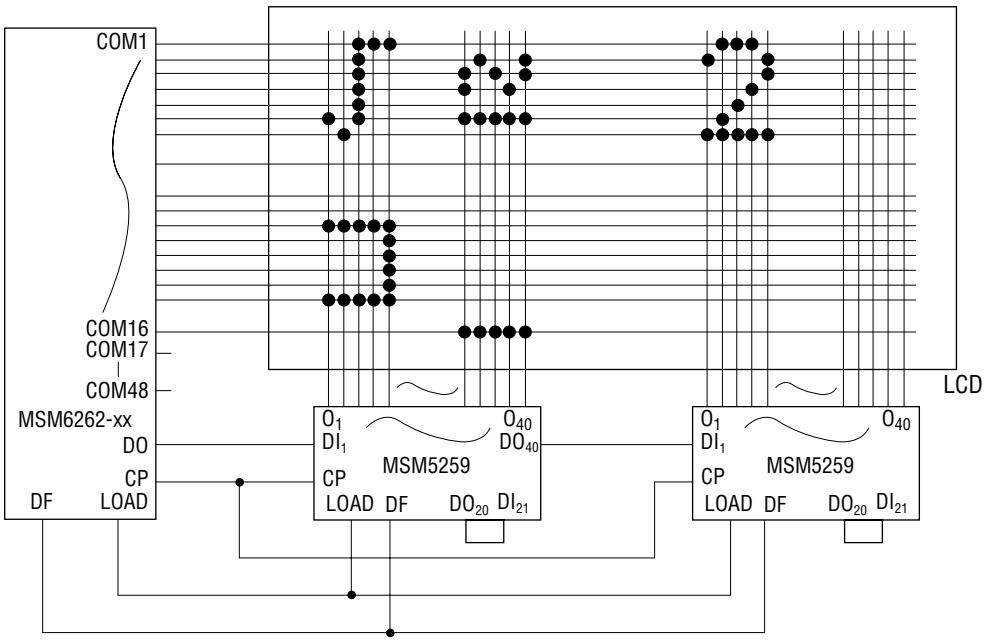
	A_1	A_0	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Instruction code	H	H	B1F	B2F	CG/ DD	I/D	S	A/O	D	UD

- B1F (Busy 1 flag)
  When B1F = "H", MSM6262-xx is engaged in internal operation and next instruction is not accepted until when B1F becomes "L". So, subsequent instruction has to be input after B1F is confirmed at "L". During B1F = "H", DB_5 to DB_0 are undefined.
- B2F (Busy 2 flag)
  B2F indicates that MSM6262-xx is engaged in its internal operation and it also indicates that the display starting line is under being revised.
  Instruction contents of B1F and B2F are the same except when setting the starting line of display.
  B2F = "H" indicates that MSM6262-xx is engaged in its internal operation. B2F = "L" indicates that MAM6262-xx is ready for accepting new instruction.
  Even when B2F = "H", new instruction can be accepted if B1F = "L". However, if the starting line of display is revised under this condition, the previous set data about starting line of display becomes invalid and the newly input data about starting line becomes valid.

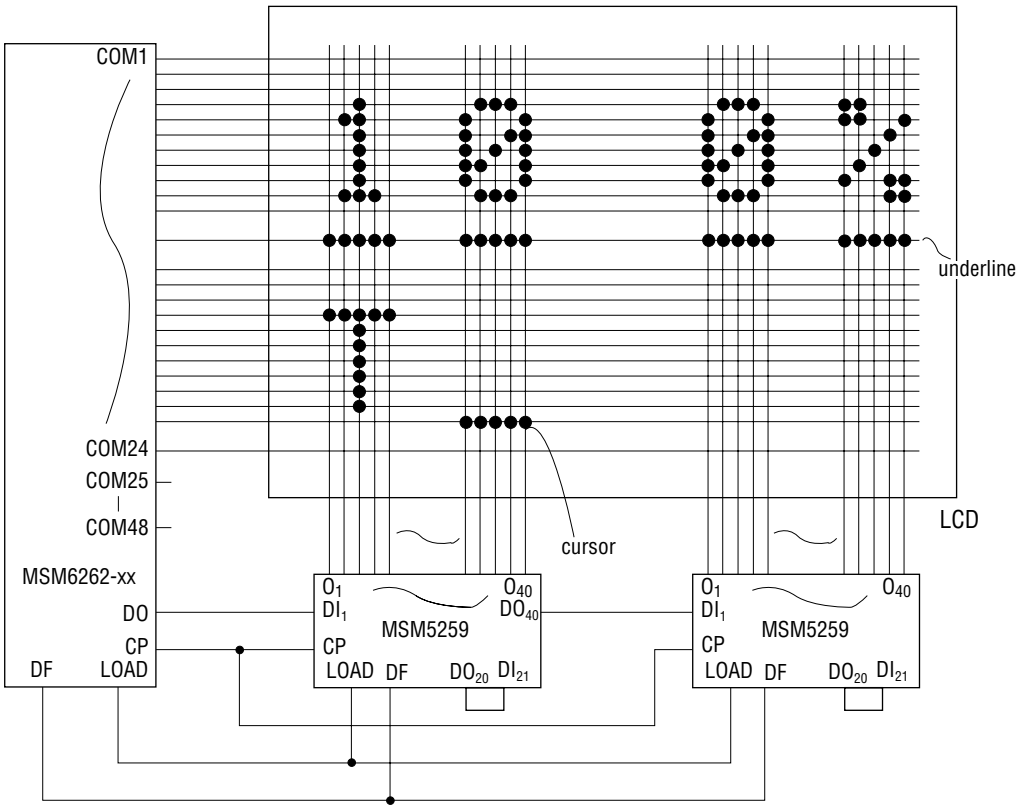
- CG/DD (CG RAM/DD RAM)
  This bit indicates whether the address counter contents are CG RAM or DD RAM when B1F = "L". It indicates that CG RAM data has been selected when CG/DD = "H" and that DD RAM data has been selected when CG/DD = "L".
- I/D (Increment/Decrement)
  This bit indicates which has been set in the entry mode set, increment or decrement, when B1F = "L". It indicates that increment has been set when I/D = "H" and that decrement has been set when I/D = "L".
- S (Shift)
  This bit reads the shift condition in the entry mode when B1F = "L". It indicates that shift is set when S = "H" and shift is disabled when S = "L".
- A/O (CG RAM ENABLE/CG ROM ENABLE)
  This bit indicates which has been selected in the entry mode, CG ROM or CG RAM, when BIF = "L".
  It indicates the CG ROM selected state when A/O = "L" and CG RAM selected state when A/O = "H".
- D (Display)
  This bit indicates which has been set by display control instruction, LCD display ON or OFF, when B1F = "L". It indicates that the display is on when D = "H" and the display is off when D = "L".
- UD (Underline)
  This is the bit to indicate the condition of underline or blinking on the underline, both of which were set by display control instruction, when B1F = "L".
  When UD = "H", either (or both of) underline display or blinking on the underline is being executed. When UD = "L", it indicates neither of underline display nor blinking on the underline is performed.

APPLICATION CIRCUITS

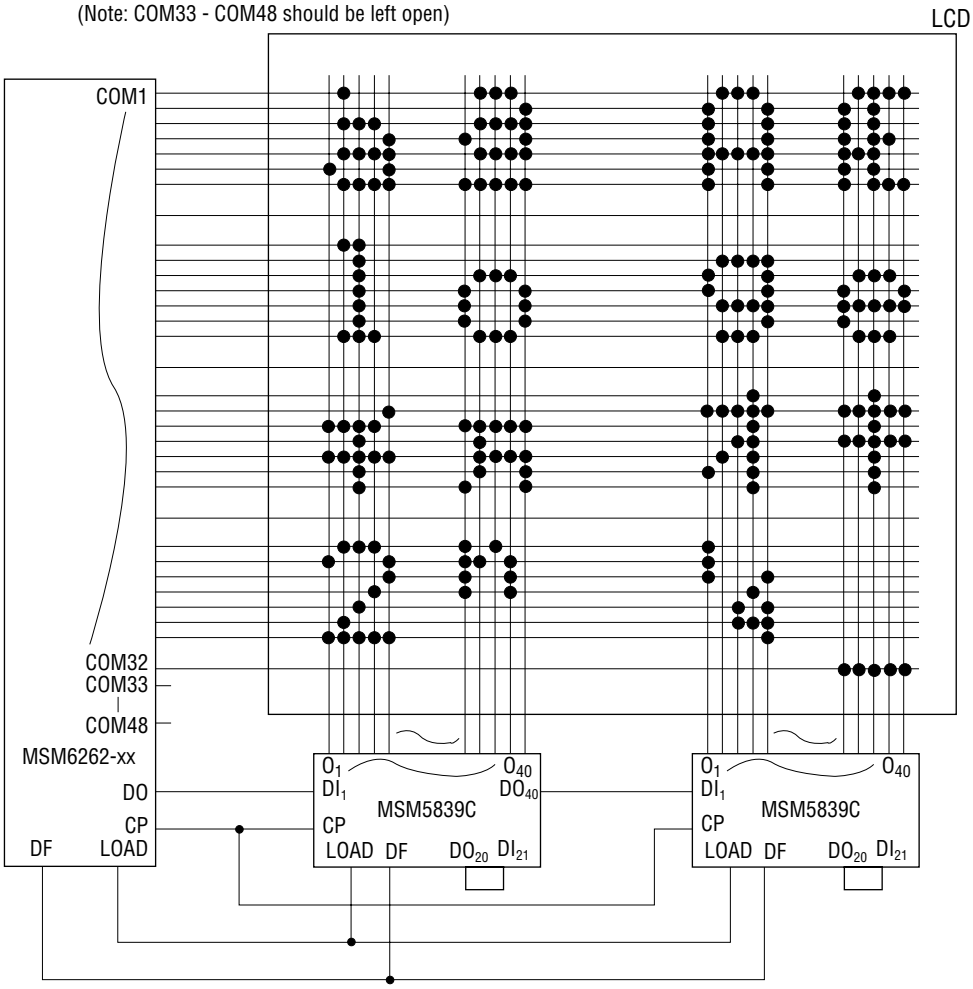
1 2-line display mode
5 x 7 dots, 2 lines × 16 characters
(Note: COM17 - COM48 should be left open)



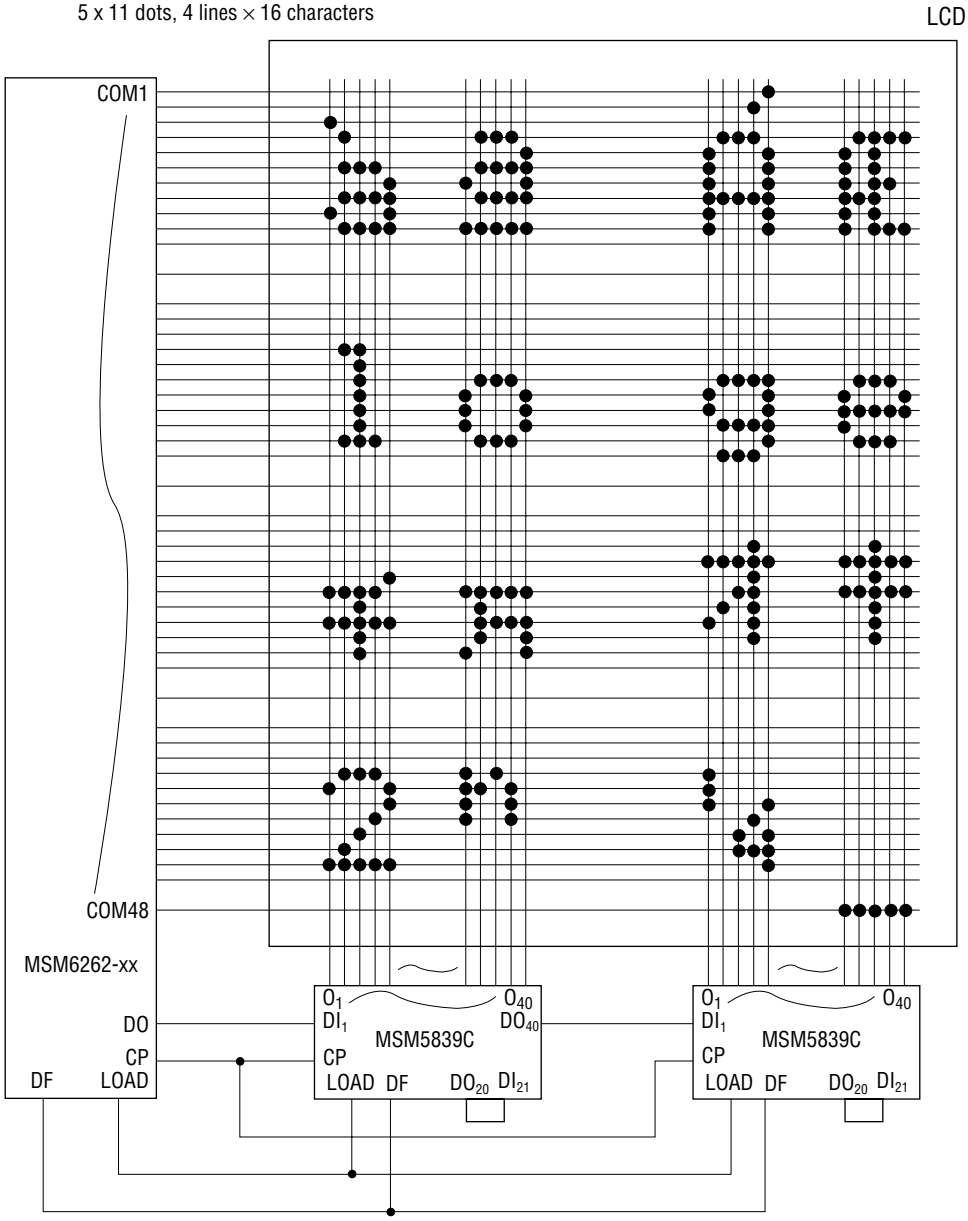
2 2-line display mode
5 x 11 dots, 2 lines × 16 characters
(Note: COM25 - COM48 should be left open)



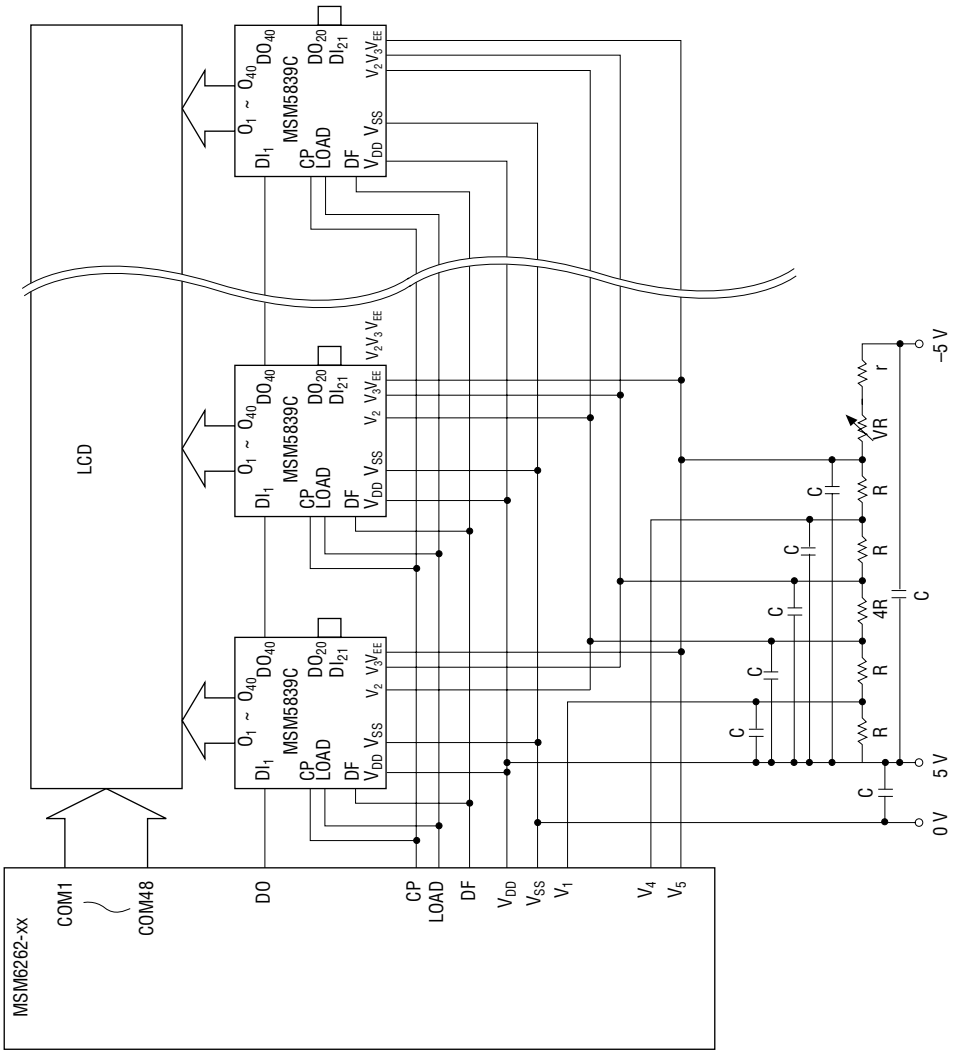
3 4-line display mode
5 x 7 dots, 4 lines × 16 characters
(Note: COM33 - COM48 should be left open)



4 4-line display mode
5 x 11 dots, 4 lines × 16 characters



- Example of connection with MSM5839C and bias circuit

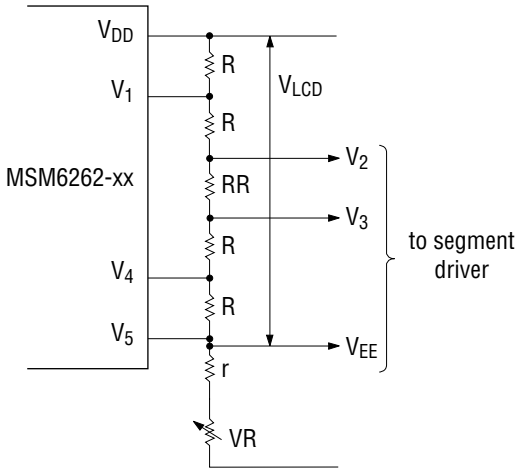


- Example of bias circuit

1/5 - 1/8 bias example 1.

Bias	1/5	1/6	1/7	1/8
RR	R	2R	3R	4R

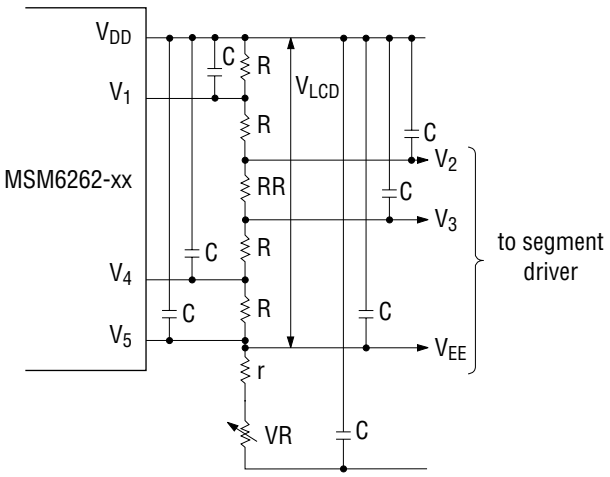
V_{LCD}: LCD driving voltage



1/5 - 1/8 bias example 2.

Bias	1/5	1/6	1/7	1/8
RR	R	2R	3R	4R

V_{LCD}: LCD driving voltage



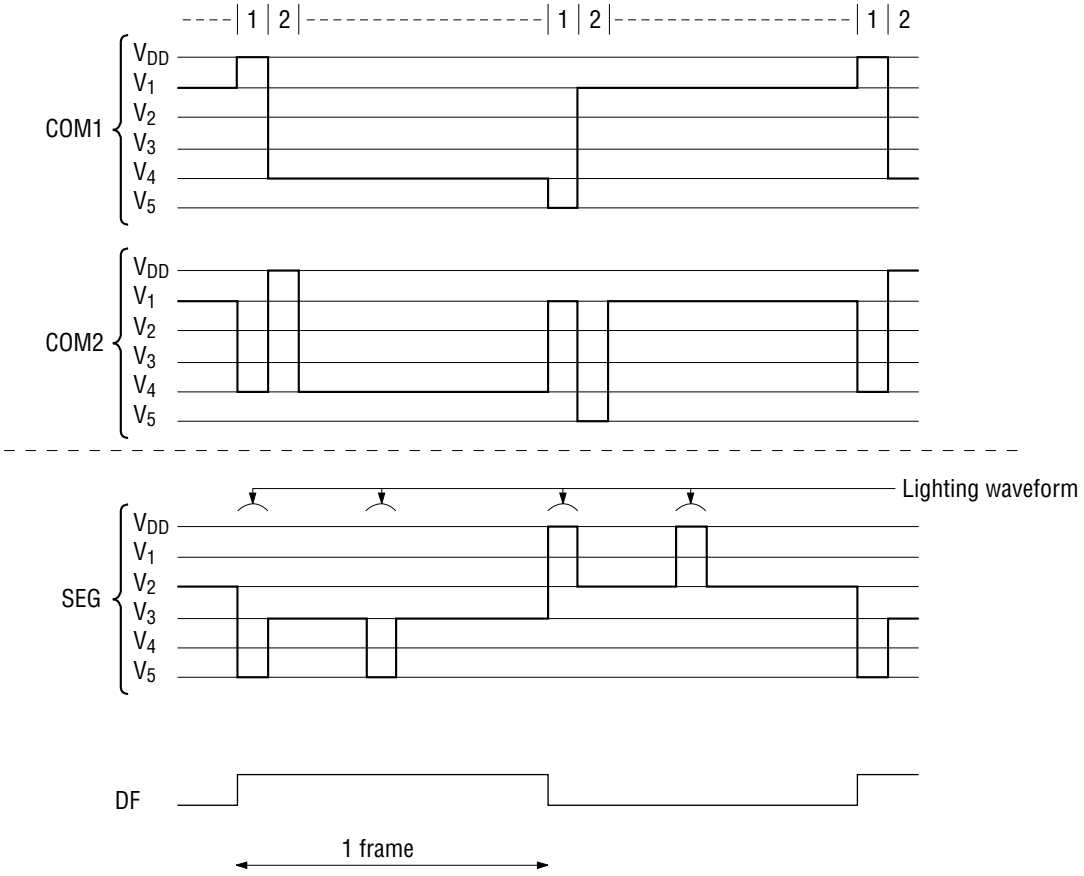
- LCD duty and bias

No. of lines	2 lines		4 lines	
Duty	1/16	1/24	1/32	1/48
Bias	1/5	1/6	1/7	1/8

Above are examples of relation between LCD duty and bias. Use these values for reference, for they vary depending on the characteristics of LCD panel.
The value of resistor on bias circuit is determined by the operational margin and power consumption. To make the power consumption lower, the value of resistor has to be larger, but it makes the LCD driving output impedance high and causes the distortion on the LCD driving waveform.
If a large LCD panel is used, the value of the resistor should be much lower because the LCD capacitance increases.
Connecting a bypass capacitor to the bias resistor in parallel can improve the distortion of LCD driving waveform. However, connecting a capacitor of too large value may cause a level shift of the bias voltage.
So, it has to be determined carefully after checking experimentally.
Followings are the reference values.

$R = 2$ to $10\ k\Omega$
$V_R = 10$ to $50\ k\Omega$
$r = 0.2$ to $2\ k\Omega$
$C = 0.0022$ to $0.047\ \mu F$

- LCD driving waveform (at 1/5 to 1/8 bias)



Duty	1/16	1/24	1/32	1/48
Frame frequency	78.125 Hz	52.08 Hz	78.125 Hz	52.08 Hz

Note: f_{osc} = 500 kHz

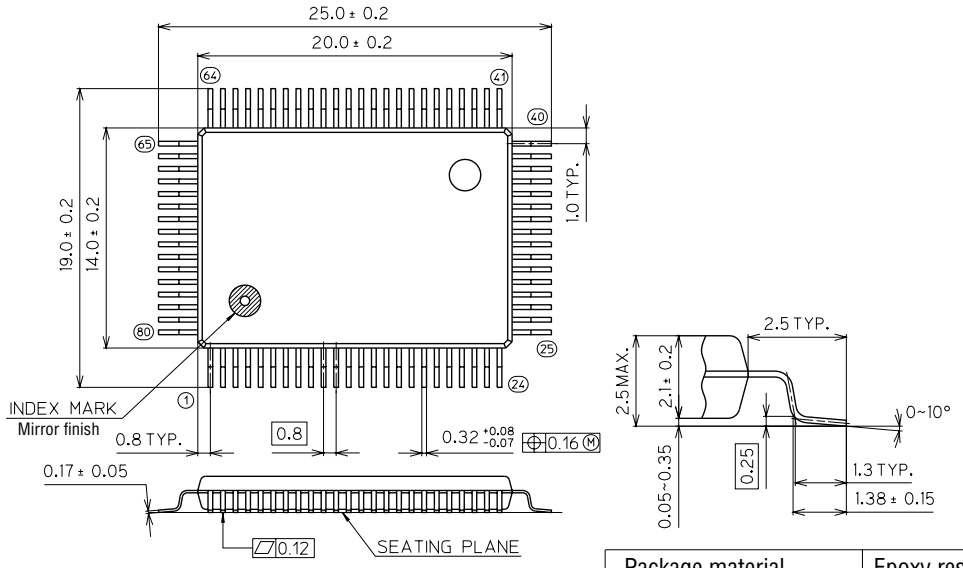
Selecting a SEGMENT driver IC

When V_{LCD} is within the voltage range of V_{DD} and that of V_{SS}, MSM5259 is recommendable as SEGMENT driver. When V_{LCD} is beyond the voltage range of V_{DD} and that of V_{SS}, MSM5839C or MSM5260 is recommendable as SEGMENT driver.

PACKAGE DIMENSIONS

(Unit : mm)

QFP80-P-1420-0.80-BK



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating
Solder plate thickness	5 μm or more
Package weight (g)	1.27 TYP.

Notes for Mounting the Surface Mount Type Package

The SOP, QFP, TSOP, SOJ, QFJ (PLCC), SHP and BGA are surface mount type packages, which are very susceptible to heat in reflow mounting and humidity absorbed in storage.
Therefore, before you perform reflow mounting, contact Oki's responsible sales person for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).