



REVISION HISTORY

<u>Revision</u>	<u>Description</u>	<u>Issue Date</u>
Rev. 1.0	Initial Issue	Jul.25.2004
Rev. 1.1	Delete Icc1/ I _{SB} Spec.	Sep.21.2004
Rev. 1.2	Adding Skinny P-DIP	Aug.18.2005
Rev. 1.3	Revised STSOP Package Outline Dimension	Mar.26.2008
Rev. 1.4	Revised V _{TERM} to V _{T1} and V _{T2} Revised Test Condition of I _{SB1} /I _{DR} Added LL Spec.	Feb.2.2009
Rev. 1.5	Revised Test Condition of I _{CC} Revised FEATURES & ORDERING INFORMATION <u>Lead free and green package available</u> to <u>Green package available</u> Deleted T _{SOLDER} in <u>ABSOLUTE MAXIMUN RATINGS</u> Added packing type in <u>ORDERING INFORMATION</u>	Apr.17.2009

FEATURES

- Fast access time : 8/10/12/15ns
- Low power consumption:
Operating current : 110/100/90/80mA (TYP.)
Standby current : 1mA (TYP.)
2μA (TYP.) LL-version
- Single 5V power supply
- All inputs and outputs TTL compatible
- Fully static operation
- Tri-state output
- Data retention voltage : 2.0V (MIN.)
- **Green package available**
- Package : 28-pin 300 mil SOJ
28-pin 300 mil Skinny P-DIP
28-pin 8mm x 13.4mm STSOP

GENERAL DESCRIPTION

The LY61256 is a 262,144-bit high speed CMOS static random access memory organized as 32,768 words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

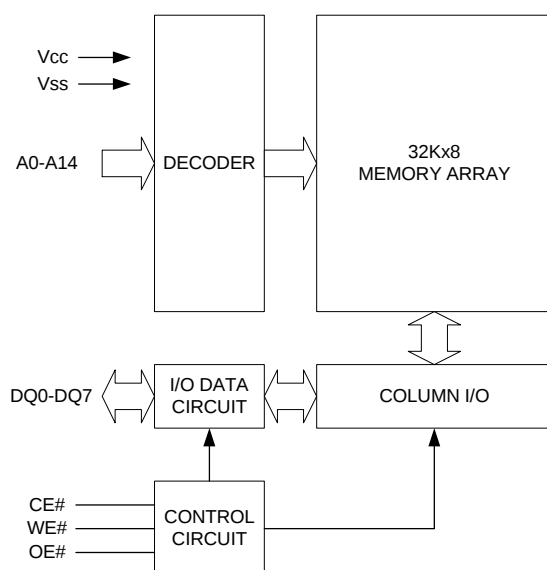
The LY61256 is well designed for high speed system application. Easy expansion is provided by using an active LOW Chip Enable(CE#). The active LOW Write Enable(WE#) controls both writing and reading of the memory.

The LY61256 operates from a single power supply of 5V and all inputs and outputs are fully TTL compatible

PRODUCT FAMILY

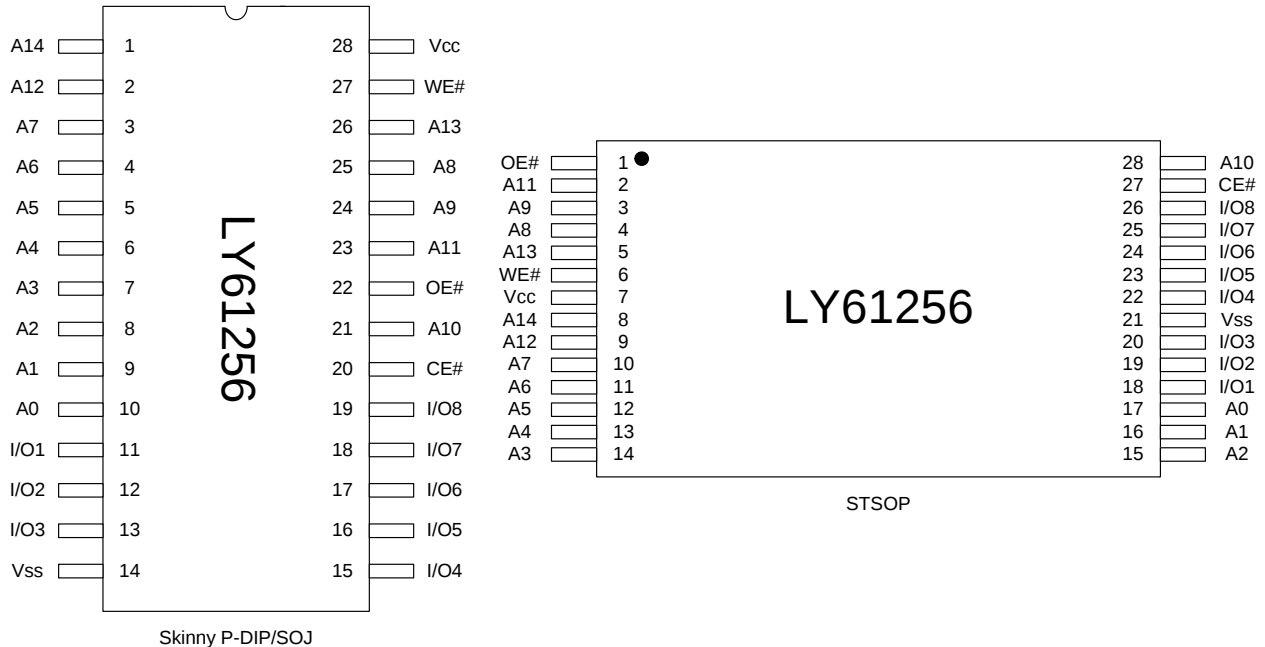
Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation	
				Standby(I _{SB1} ,TYP.)	Operating(I _{cc} ,TYP.)
LY61256	0 ~ 70°C	4.5 ~ 5.5V	8/10/12/15ns	1mA	110/100/90/80mA
LY61256(E)	-20 ~ 80°C	4.5 ~ 5.5V	8/10/12/15ns	1mA	110/100/90/80mA
LY61256(I)	-40 ~ 85°C	4.5 ~ 5.5V	8/10/12/15ns	1mA	110/100/90/80mA
LY61256(LL)	0 ~ 70°C	4.5 ~ 5.5V	8/10/12/15ns	2μA(LL)	110/100/90/80mA
LY61256(LLE)	-20 ~ 80°C	4.5 ~ 5.5V	8/10/12/15ns	2μA(LL)	110/100/90/80mA
LY61256(LLI)	-40 ~ 85°C	4.5 ~ 5.5V	8/10/12/15ns	2μA(LL)	110/100/90/80mA

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	DESCRIPTION
A0 - A14	Address Inputs
DQ0 – DQ7	Data Inputs/Outputs
CE#	Chip Enable Input
WE#	Write Enable Input
OE#	Output Enable Input
Vcc	Power Supply
Vss	Ground

PIN CONFIGURATION

ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on Vcc relative to Vss	V _{T1}	-0.5 to 6.5	V
Voltage on any other pin relative to Vss	V _{T2}	-0.5 to Vcc+0.5	V
Operating Temperature	T _A	0 to 70(C grade)	°C
		-20 to 80(E grade)	
		-40 to 85(I grade)	
Storage Temperature	T _{STG}	-65 to 150	°C
Power Dissipation	P _D	1	W
DC Output Current	I _{OUT}	50	mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE#	OE#	WE#	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	High-Z	I _{SB1}
Output Disable	L	H	H	High-Z	I _{CC}
Read	L	L	H	D _{OUT}	I _{CC}
Write	L	X	L	D _{IN}	I _{CC}

Note: H = V_{IH}, L = V_{IL}, X = Don't care.

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP. ^{*4}	MAX.	UNIT
Supply Voltage	V _{CC}		4.5	5.0	5.5	V
Input High Voltage	V _{IH} ^{*1}		2.4	-	V _{CC} +0.5	V
Input Low Voltage	V _{IL} ^{*2}		- 0.5	-	0.8	V
Input Leakage Current	I _{LI}	V _{CC} ≥ V _{IN} ≥ V _{SS}	- 1	-	1	μA
Output Leakage Current	I _{LO}	V _{CC} ≥ V _{OUT} ≥ V _{SS} , Output Disabled	- 1	-	1	μA
Output High Voltage	V _{OH}	I _{OH} = -4mA	2.4	-	-	V
Output Low Voltage	V _{OL}	I _{OL} = 8mA	-	-	0.4	V
Average Operating Power supply Current	I _{CC}	Cycle time = Min. CE# = V _{IL} , I _{I/O} = 0mA Others at V _{IL} or V _{IH}	-8	-	110	mA
			-10	-	100	mA
			-12	-	90	mA
			-15	-	80	mA
Standby Power Supply Current	I _{SB1}	CE# ≥ V _{CC} - 0.2V,	Normal	-	1	mA
		CE# ≥ V _{CC} - 0.2V, Others at 0.2V or V _{CC} -0.2V	LL	-	2	μA

Notes:

1. V_{IH}(max) = V_{CC} + 3.0V for pulse width less than 10ns.
2. V_{IL}(min) = V_{SS} - 3.0V for pulse width less than 10ns.
3. Over/Undershoot specifications are characterized, not 100% tested.
4. Typical values are included for reference only and are not guaranteed or tested.
Typical valued are measured at V_{CC} = V_{CC}(TYP.) and T_A = 25°C

CAPACITANCE (T_A = 25°C, f = 1.0MHz)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C _{IN}	-	6	pF
Input/Output Capacitance	C _{I/O}	-	8	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	0.2V to V _{CC} - 0.2V
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	C _L = 30pF + 1TTL, I _{OH} /I _{OL} = -4mA/8mA



AC ELECTRICAL CHARACTERISTICS

(1) READ CYCLE

PARAMETER	SYM.	LY61256-8		LY61256-10		LY61256-12		LY61256-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Read Cycle Time	t _{RC}	8	-	10	-	12	-	15	-	ns
Address Access Time	t _{AA}	-	8	-	10	-	12	-	15	ns
Chip Enable Access Time	t _{ACE}	-	8	-	10	-	12	-	15	ns
Output Enable Access Time	t _{OE}	-	4	-	5	-	6	-	7	ns
Chip Enable to Output in Low-Z	t _{CLZ} *	2	-	2	-	3	-	4	-	ns
Output Enable to Output in Low-Z	t _{OLZ} *	0	-	0	-	0	-	0	-	ns
Chip Disable to Output in High-Z	t _{CHZ} *	-	4	-	5	-	6	-	7	ns
Output Disable to Output in High-Z	t _{OHZ} *	-	4	-	5	-	6	-	7	ns
Output Hold from Address Change	t _{OH}	3	-	3	-	3	-	3	-	ns

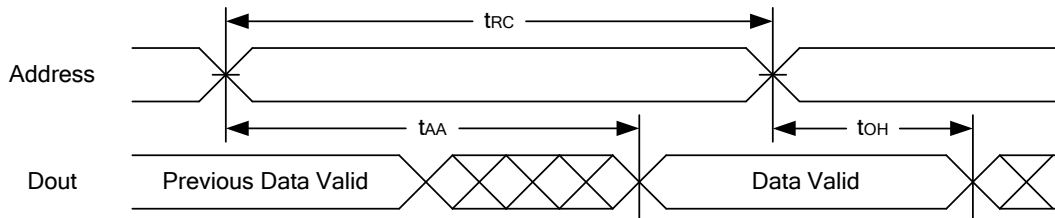
(2) WRITE CYCLE

PARAMETER	SYM.	LY61256-8		LY61256-10		LY61256-12		LY61256-15		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Write Cycle Time	t _{WC}	8	-	10	-	12	-	15	-	ns
Address Valid to End of Write	t _{AW}	6.5	-	8	-	10	-	12	-	ns
Chip Enable to End of Write	t _{CW}	6.5	-	8	-	10	-	12	-	ns
Address Set-up Time	t _{AS}	0	-	0	-	0	-	0	-	ns
Write Pulse Width	t _{WP}	6.5	-	8	-	9	-	10	-	ns
Write Recovery Time	t _{WR}	0	-	0	-	0	-	0	-	ns
Data to Write Time Overlap	t _{DW}	5	-	6	-	7	-	8	-	ns
Data Hold from End of Write Time	t _{DH}	0	-	0	-	0	-	0	-	ns
Output Active from End of Write	t _{OW} *	1.5	-	2	-	3	-	4	-	ns
Write to Output in High-Z	t _{WHZ} *	-	5	-	6	-	7	-	8	ns

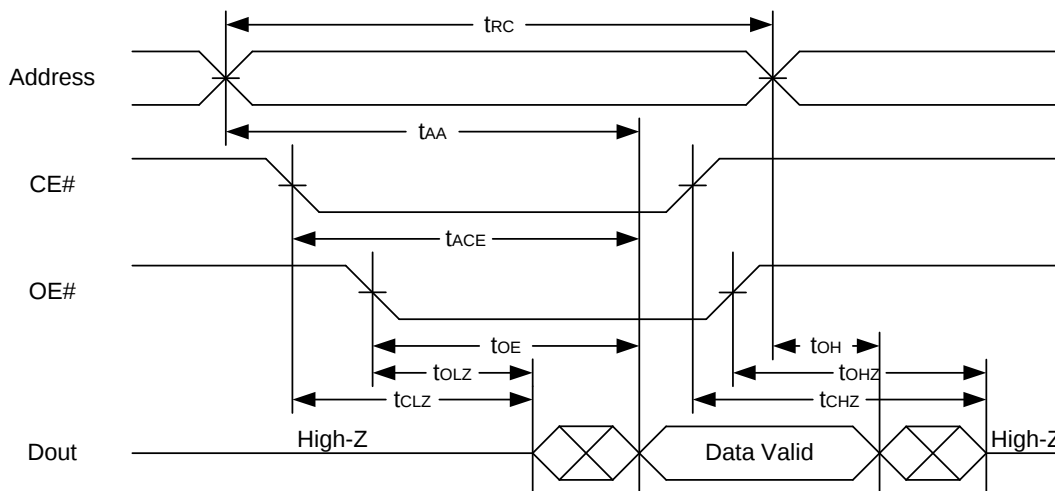
*These parameters are guaranteed by device characterization, but not production tested.

TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)



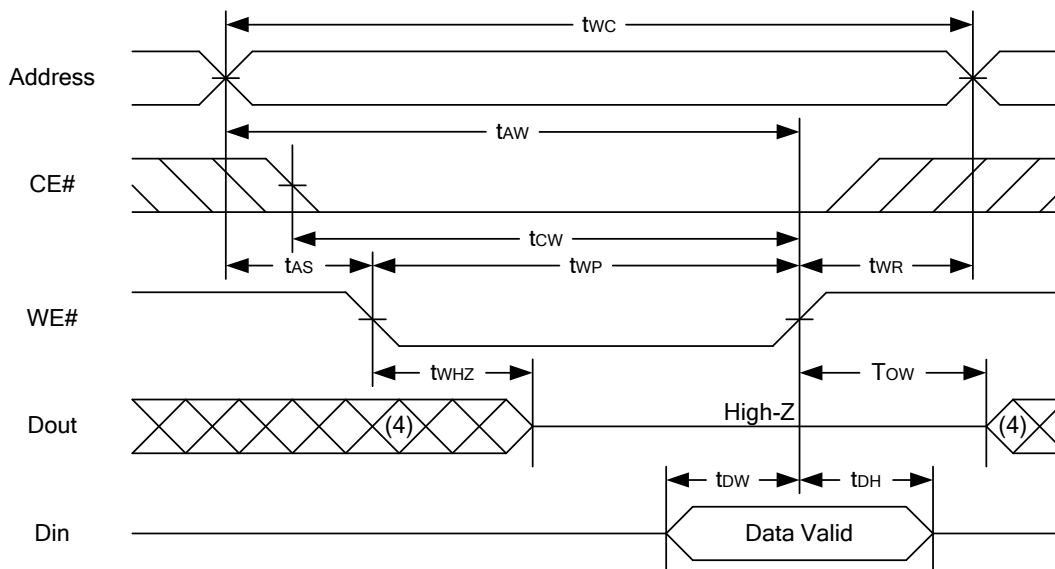
READ CYCLE 2 (CE# and OE# Controlled) (1,3,4,5)



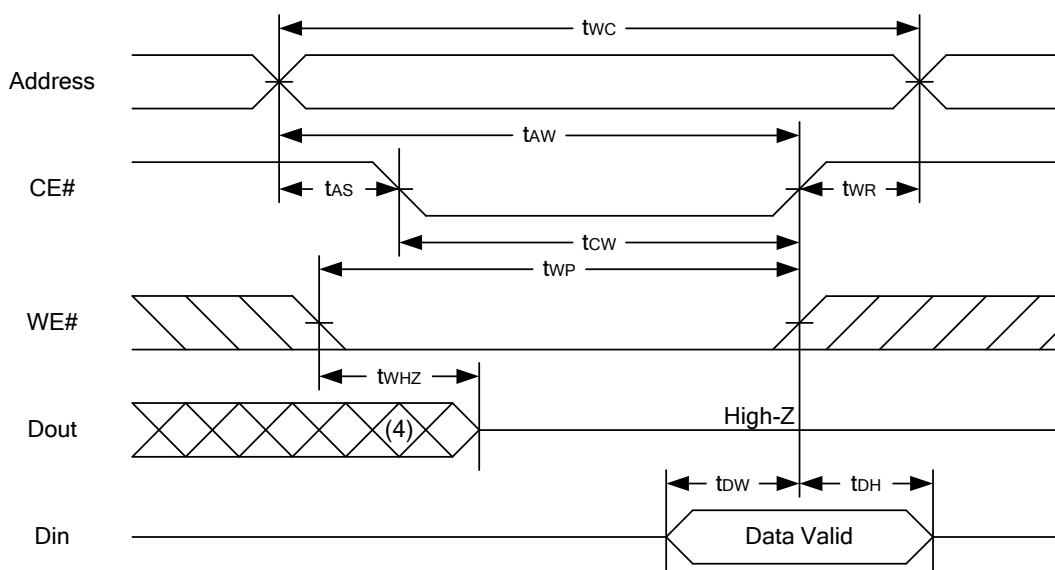
Notes :

1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low.
3. Address must be valid prior to or coincident with CE# = low; otherwise t_{AA} is the limiting parameter.
4. t_{CLZ} , t_{OLZ} , t_{CHZ} and t_{OHZ} are specified with $C_L = 5\text{pF}$. Transition is measured $\pm 500\text{mV}$ from steady state.
5. At any given temperature and voltage condition, t_{CHZ} is less than t_{CLZ} , t_{OHZ} is less than t_{OLZ} .

WRITE CYCLE 1 (WE# Controlled) (1,2,3,5,6)



WRITE CYCLE 2 (CE# Controlled) (1,2,5,6)



Notes :

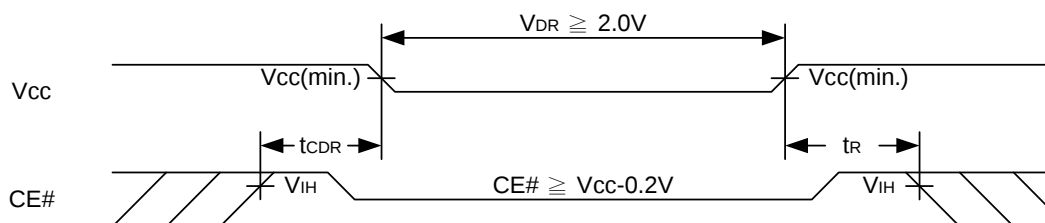
1. WE#, CE# must be high during all address transitions.
2. A write occurs during the overlap of a low CE#, low WE#.
3. During a WE# controlled write cycle with OE# low, t_{WP} must be greater than $t_{WHZ} + t_{DW}$ to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the CE# low transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
6. t_{OW} and t_{WHZ} are specified with $C_L = 5pF$. Transition is measured $\pm 500mV$ from steady state.

DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
V _{CC} for Data Retention	V _{DR}	CE# $\geq$ V _{CC} - 0.2V	2.0	-	5.5	V
Data Retention Current	I _{DR}	V _{CC} = 2.0V CE# $\geq$ V _{CC} - 0.2V	-	0.6	3	mA
		V _{CC} = 2.0V CE# $\geq$ V _{CC} - 0.2V Others at 0.2V or V _{CC} -0.2V	-	0.5	20	μ A
		LL	-	-	-	-
Chip Disable to Data Retention Time	t _{CDR}	See Data Retention Waveforms (below)	0	-	-	ns
Recovery Time	t _R		t _{RC*}	-	-	ns

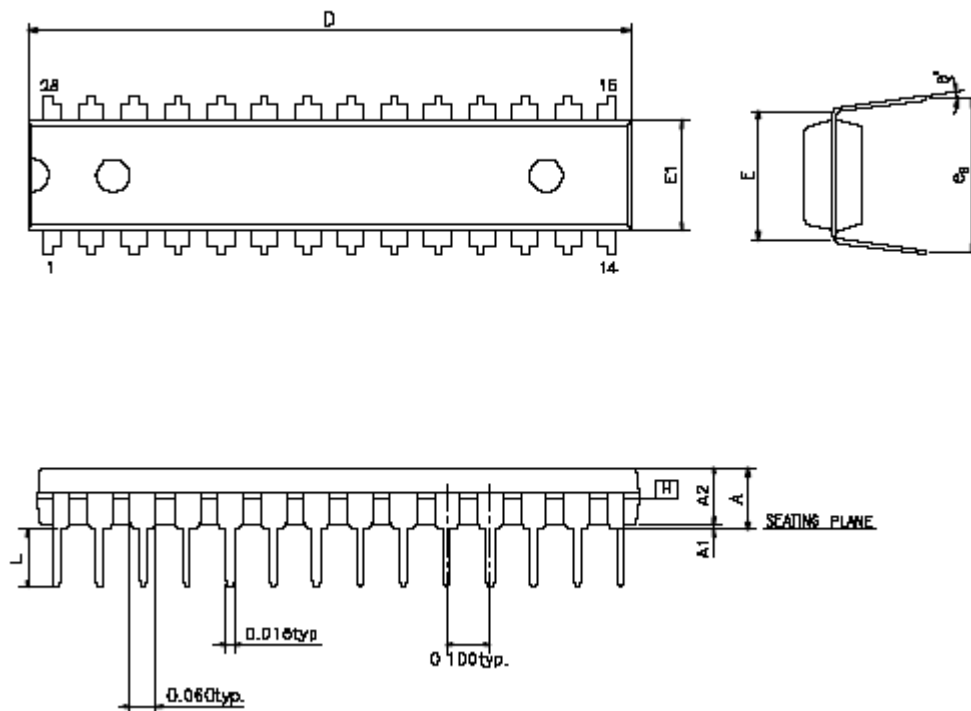
t_{RC*} = Read Cycle Time

DATA RETENTION WAVEFORM



PACKAGE OUTLINE DIMENSION

28 pin 300 mil PDIP Package Outline Dimension

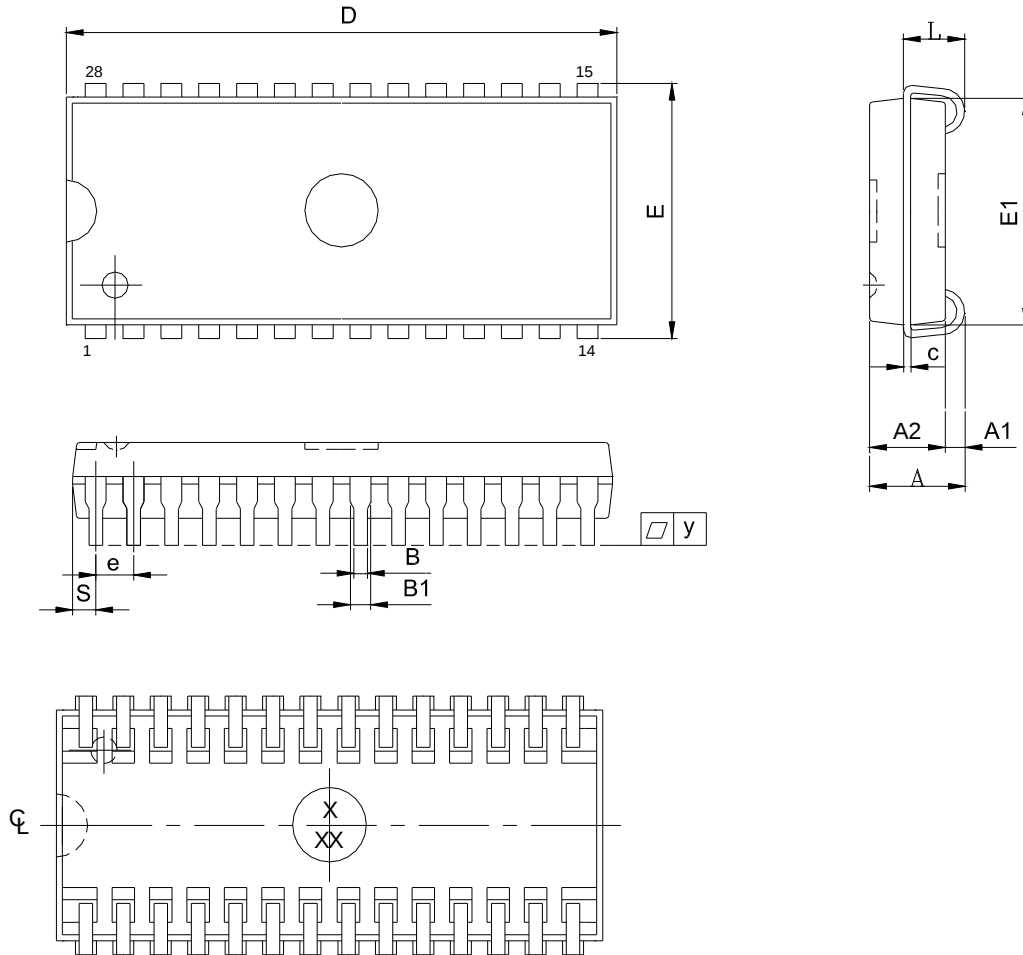


SYMBOLS	MIN.	NOR.	MAX.
A	—	—	0.210
A1	0.015	—	—
A2	0.125	0.130	0.135
D	1.385	1.390	1.400
E	0.310 BSC		
E1	0.283	0.288	0.293
L	0.115	0.130	0.150
E2	0.330	0.350	0.370
θ°	0	7	15

UNIT : INCH

NOTE:

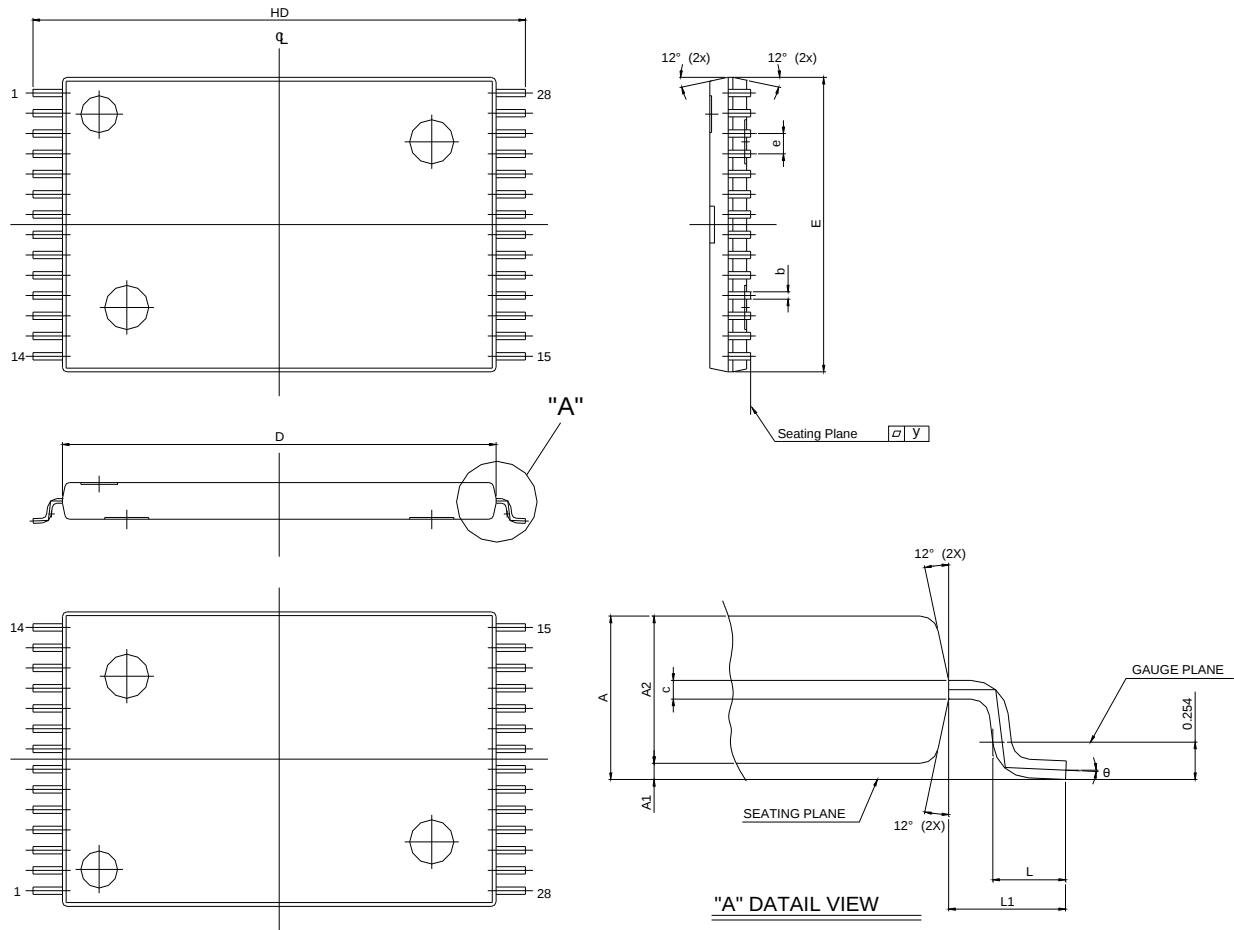
1. JEDEC OUTLINE : MS-D15 AH

28-pin 300 mil SOJ Package Outline Dimension


SYM. \ UNIT	INCH(REF)	MM(BASE)
A	0.140 (MAX)	3.556 (MAX)
A1	0.026 (MIN)	0.660 (MIN)
A2	0.100±0.005	2.540±0.127
B	0.018±0.003	0.457±0.076
B1	0.028 ±0.003	0.711±0.076
c	0.010±0.003	0.254±0.076
D	0.710±0.010	18.03±0.254
E	0.337±0.010	8.560±0.254
E1	0.300±0.005	7.620±0.127
e	0.050±0.003	1.270±0.076
L	0.087±0.010	2.210±0.254
S	0.030±0.004	0.762±0.102
Y	0.003 (MAX)	0.076 (MAX)

Note : 1.S/E/D dimension is not including mold flash.

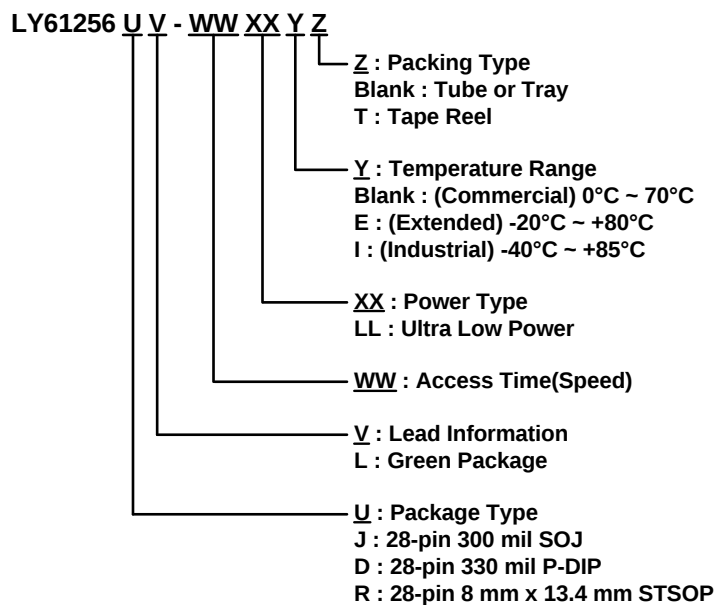
2.The end flash in package lengthwise is not more than 10 mils each side.

28 pin 8x13.4mm STSOP Package Outline Dimension


SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.00	1.10	1.20	0.040	0.043	0.047
A1	0.05	-	0.15	0.002	-	0.006
A2	0.91	1.00	1.05	0.036	0.039	0.041
b	0.17	0.22	0.27	0.007	0.009	0.011
c	0.10	0.15	0.20	0.004	0.006	0.008
HD	13.20	13.40	13.60	0.520	0.528	0.535
D	11.70	11.80	11.90	0.461	0.465	0.469
E	7.90	8.00	8.10	0.311	0.315	0.319
e	-	0.55	-	-	0.0216	-
L	0.30	0.50	0.70	0.012	0.020	0.028
L1	0.675	-	-	0.027	-	-
Y	0.00	-	0.076	0.000	-	0.003
θ	0°	3°	5°	0°	3°	5°



ORDERING INFORMATION





Lyontek Inc.

LY61256

Rev. 1.5

32K X 8 BIT HIGH SPEED CMOS SRAM

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