



VN02C

T-39-05



N-Channel Enhancement-Mode Vertical DMOS Power FETs

Ordering Information

BV_{DSS} / BV_{DGS}	$R_{DS(ON)}$ (max)	$I_{D(ON)}$ (min)	Order Number / Package		
			TO-39	TO-92	TO-220
160V	6Ω	1A	VN0216N2	VN0216N3	VN0216N5
200V	6Ω	1A	VN0220N2	VN0220N3	VN0220N5

Features

- ☐ Freedom from secondary breakdown
- ☐ Low power drive requirement
- ☐ Ease of paralleling
- ☐ Low C_{iss} and fast switching speeds
- ☐ Excellent thermal stability
- ☐ Integral Source-Drain diode
- ☐ High input impedance and high gain
- ☐ Complementary N- and P-Channel devices

Advanced DMOS Technology

These enhancement-mode (normally-off) power transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and negative temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex Vertical DMOS Power FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- ☐ Motor control
- ☐ Converters
- ☐ Amplifiers
- ☐ Switches
- ☐ Power supply circuits
- ☐ Drivers (Relays, Hammers, Solenoids, Lamps, Memories, Displays, Bipolar Transistors, etc.)

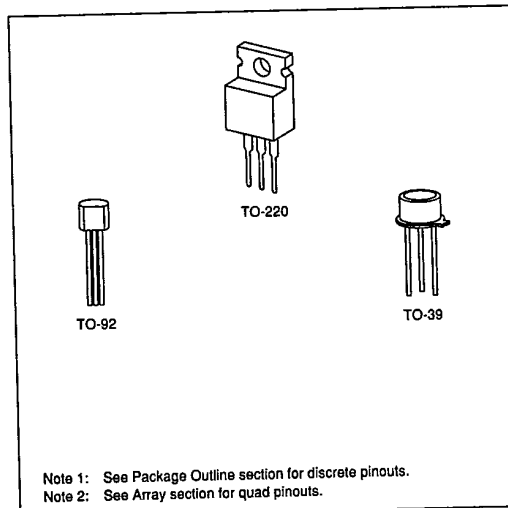
Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSS}
Drain-to-Gate Voltage	BV_{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

*Distance of 1.6 mm from case for 10 seconds.

Package Options

(Notes 1 and 2)



Note 1: See Package Outline section for discrete pinouts.
Note 2: See Array section for quad pinouts.

Thermal Characteristics

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Package	I_D (continuous)*	I_D (pulsed)*	Power Dissipation @ $T_C = 25^\circ\text{C}$	θ_{JA} $^\circ\text{C/W}$	θ_{JC} $^\circ\text{C/W}$	I_{DR}	I_{DRM}^*
TO-39	0.7A	2.5A	4W	125	32	0.7A	2.5A
TO-92	0.4A	2.5A	1W	170	125	0.5A	2.5A
TO-220	1.5A	2.5A	28W	70	4.6	1.7A	2.5A

* I_D (continuous) is limited by max rated T_J Electrical Characteristics (@ 25°C unless otherwise specified)

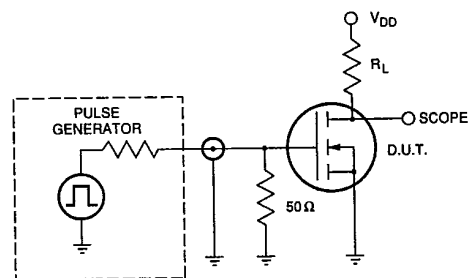
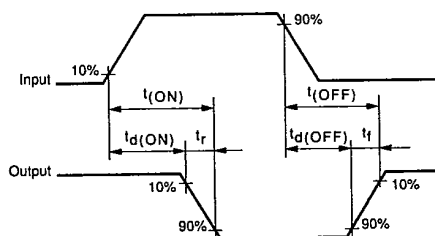
(Notes 1 and 2)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VN0216 160			V	$V_{GS} = 0, I_D = 2.0\text{mA}$
		VN0220 200				
$V_{GS(th)}$	Gate Threshold Voltage	0.75		3	V	$V_{GS} = V_{DS}, I_D = 2.0\text{mA}$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature		-4.6	-5.5	mV/ $^\circ\text{C}$	$V_{GS} = V_{DS}, I_D = 1.0\text{mA}$
I_{GSS}	Gate Body Leakage			100	nA	$V_{GS} = \pm 20\text{V}, V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current			25	μA	$V_{GS} = 0, V_{DS} = \text{Max Rating}$
				2.5	mA	$V_{GS} = 0, V_{DS} = 0.8 \text{ Max Rating}$ $T_A = 125^\circ\text{C}$
$I_{D(ON)}$	ON-State Drain Current	0.5	1.3		A	$V_{GS} = 5\text{V}, V_{DS} = 25\text{V}$
		1.0	2.2			$V_{GS} = 10\text{V}, V_{DS} = 25\text{V}$
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance		5.0	8	Ω	$V_{GS} = 5\text{V}, I_D = 0.5\text{A}$
			4.0	6		$V_{GS} = 10\text{V}, I_D = 0.5\text{A}$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature		0.8	1.4	%/ $^\circ\text{C}$	$V_{GS} = 10\text{V}, I_D = 500\text{mA}$
G_{FS}	Forward Transconductance	0.3	0.7		S	$V_{DS} = 25\text{V}, I_D = 1\text{A}$
C_{ISS}	Input Capacitance		75	150	pF	$V_{GS} = 0, V_{DS} = 25\text{V}$ $f = 1 \text{ MHz}$
C_{OSS}	Common Source Output Capacitance		34	85		
C_{RSS}	Reverse Transfer Capacitance		15	35		
$t_{d(ON)}$	Turn-ON Delay Time			10	ns	$V_{DD} = 25\text{V}$ $I_D = 0.5\text{A}$ $R_S = 50\Omega$
t_r	Rise Time			10		
$t_{d(OFF)}$	Turn-OFF Delay Time			20		
t_f	Fall Time			20		
V_{SD}	Diode Forward Voltage Drop		1.2	1.8	V	$V_{GS} = 0, I_{SD} = 1\text{A}$
t_{rr}	Reverse Recovery Time		430		ns	$V_{GS} = 0, I_{SD} = 1\text{A}$

Note 1: All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300 μs pulse, 2% duty cycle.)

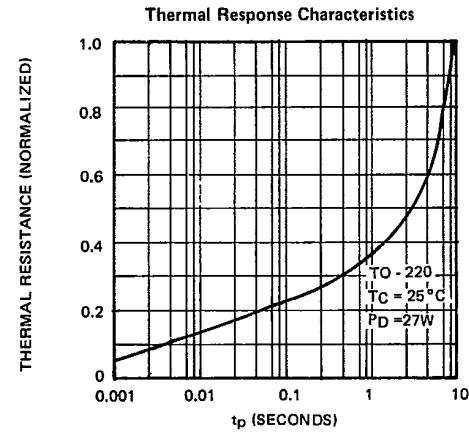
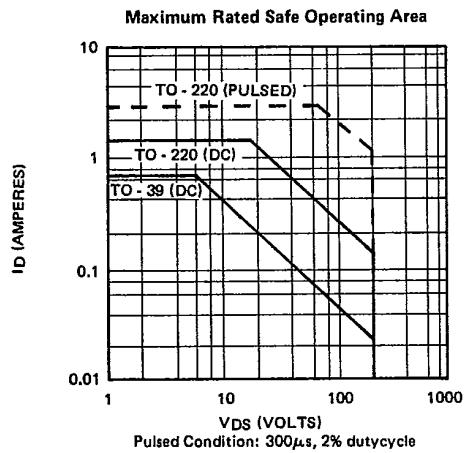
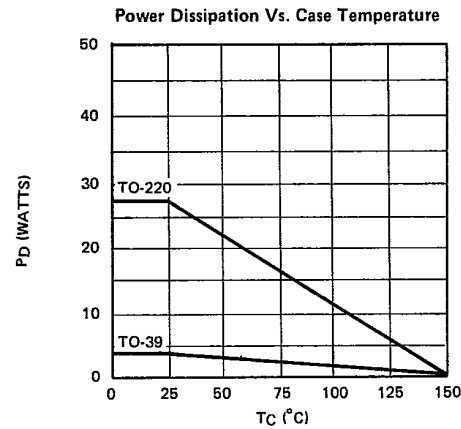
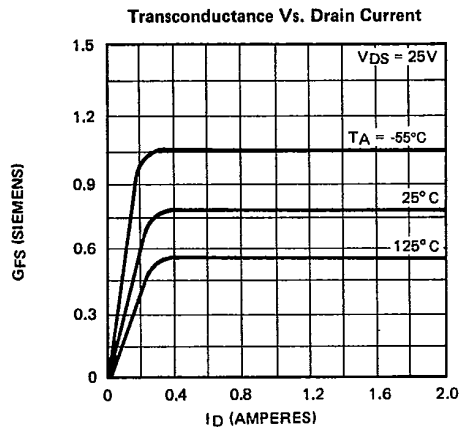
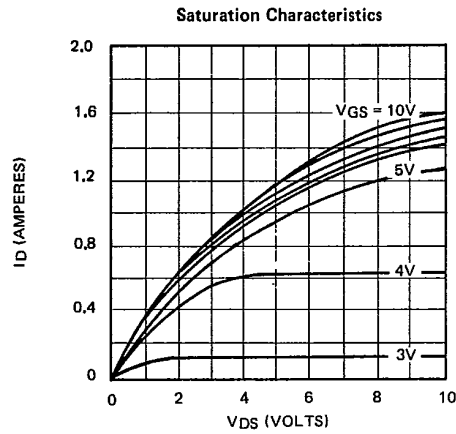
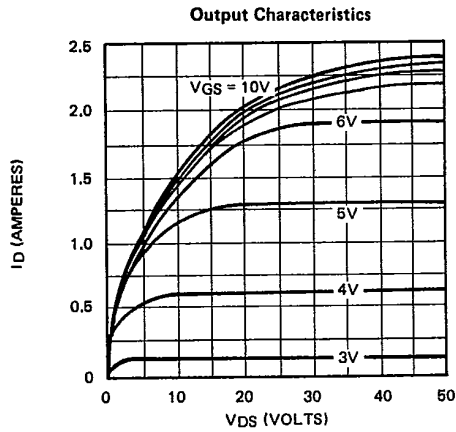
Note 2: All A.C. parameters sample tested.

Switching Waveforms and Test Circuit



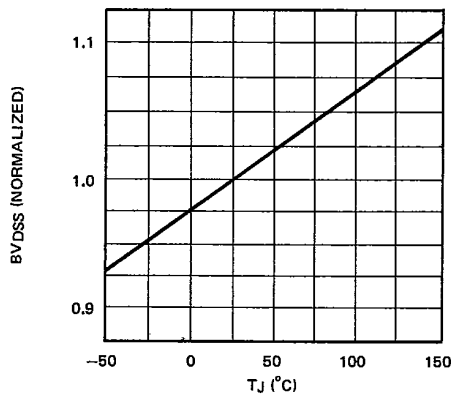
Typical Performance Curves

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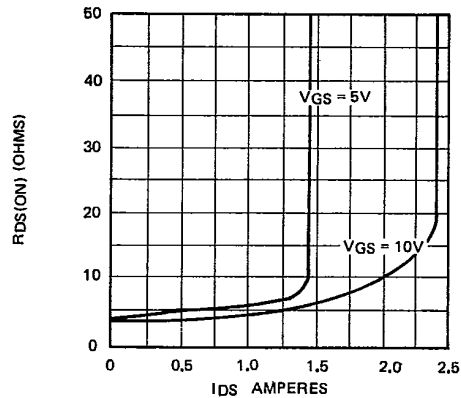


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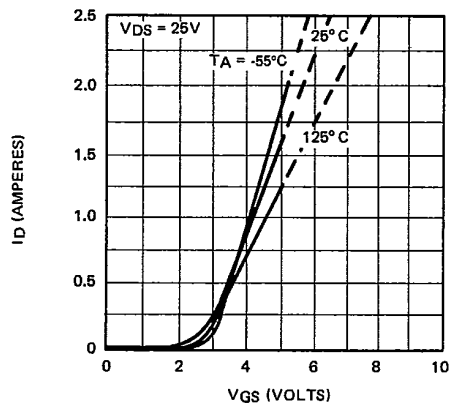
BVDSS Variation with Temperature



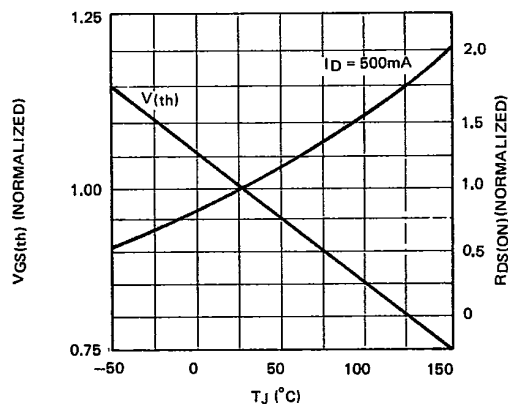
ON - Resistance Vs. Drain Current



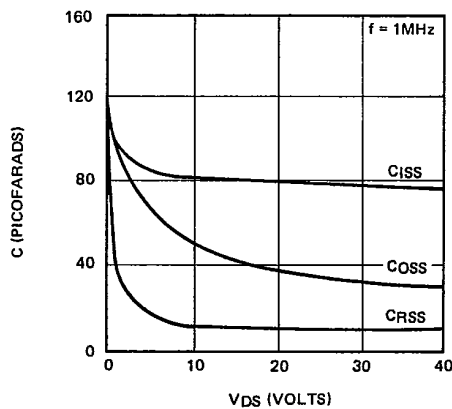
Transfer Characteristics



V(th) and RDS Variation with Temperature



Capacitance Vs. Drain-to-Source Voltage



Gate Drive Dynamic Characteristics

