# Dual Loop 8-Phase Step-Down DC/DC Controller with Digital Power System Management

## FEATURES

- **PMBus/I²C Compliant Serial Interface**
  - **Monitor Voltage, Current, Temperature and Faults**
  - **Digitally Program $V_{OUT}$, Margins, UV, OV, Current Limit, Soft-Start/Stop and Sequencing**
- **Expandable to >16 Phases**
- **External Resistor Divider Programs Output Voltage**
- **4.5V ≤ $V_{IN}$ ≤ 26.5V, 0.3V ≤ $V_{OUT}$ ≤ 3.45V**
- **±0.5% Output Voltage Accuracy**
- **Programmable PWM Loop Compensation**
- **Accurate PolyPhase® Current Sharing**
- **Internal EEPROM with ECC and Fault Logging**
- DrMOS Output Current Monitor Interface
- DrMOS Temperature/Fault Bus Interface
- DrMOS Gate Drive Supply Monitor
- Load Step Emulation
- Internal or External PWM Clock from 250kHz to 1MHz
- 52-Pin (5mm × 8mm) QFN Package
- AEC-Q100 Qualified for Automotive Applications

## APPLICATIONS

- High Current Distributed Power Systems
- Servers, Network and Storage Equipment

## DESCRIPTION

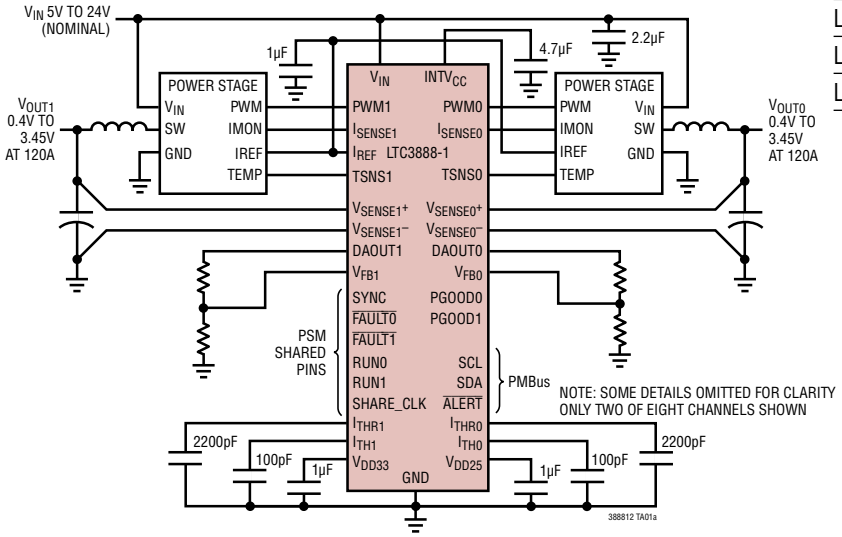
The LTC®3888-1 is a PMBus-compliant dual loop DC/DC synchronous step-down switching regulator controller with eight expandable phases supporting a wide range of master/slave configurations. The controller uses constant frequency current mode architecture to provide excellent transient response and output regulation. Each PWM master is capable of producing output voltages from 0.3V to 3.45V with multiple phase configurations using DrMOS devices that provide an output current monitor.

Output voltage is set with an external voltage divider. PMBus configuration and monitoring is supported by LTpowerPlay™ software. Programmable loop compensation and built-in load step emulation facilitate setting bandwidth based on input voltage and output load capacitance. PMBus commands allow read back of input voltage, output voltage and current, and operating status. Operating parameters can be set via PMBus command or stored in internal EEPROM for use at power up. Switching frequency, phase configuration, output current limit and device address can also be set using external programming resistors.



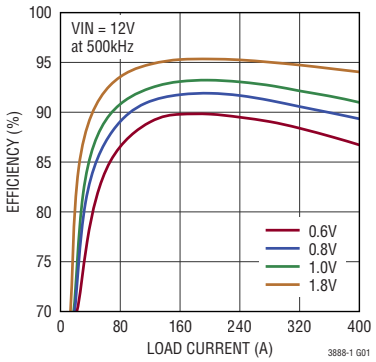
## TYPICAL APPLICATION

**Dual 4-phase PSM Rails**




| | SPI ADJUST OF $V_{OUT}$ | $V_{OUT}$ SET BY ANALOG $V_{FB}$ | PMBus CONTROL OF $V_{OUT}$ | OPTIONAL COMPENSATION ZERO |
|---|---|---|---|---|
| LTC3888 | • | | • | |
| LTC3888-1 | | • | • | • |
| LTC3888-2 | | | • | • |

**Efficiency vs Load Current (8-Phase Using LTC7051)**

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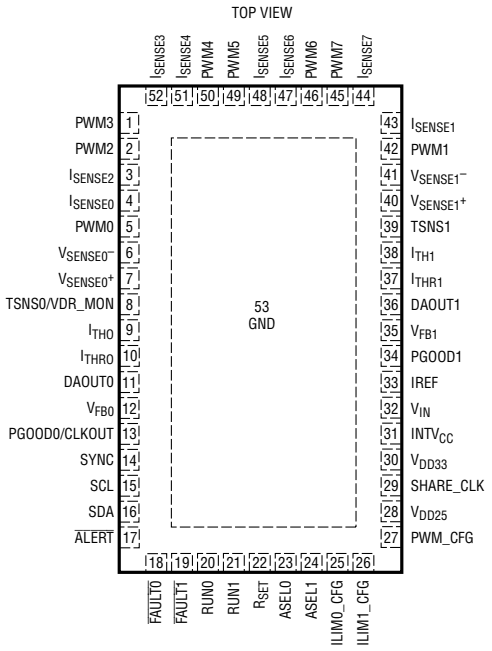
## ABSOLUTE MAXIMUM RATINGS

**(Note 1)**

$V_{IN}$ Supply Voltage ..... –0.3V to 40V
$V_{SENSEn}^+$, DAOUT*n* ..... –0.3V to 4.2V
$V_{SENSEn}^-$ ..... –0.3V to 0.3V
$I_{SENSEn}$, $V_{FBn}$ ..... –0.3V to 3.6V
TSNS*n*, VDR_MON ..... –0.3V to 6.0V
SYNC, $\overline{FAULTn}$, PGOODn, CLKOUT, SHARE_CLK ..... –0.3V to 3.6V
SCL, SDA, RUN*n*, $\overline{ALERT}$ ..... –0.3V to 5.5V
$INTV_{CC}$ ..... (Note 4)
$V_{DD33}$ ..... (Note 5)
IREF, PWM*n* ..... (Note 6)
$V_{DD25}$, $I_{THn}$, $I_{THRn}$, $R_{SET}$, ASEL*n*, ILIM*n*_CFG, PWM_CFG ..... (Note 7)
Operating Junction Temperature Range (Notes 2, 3) ..... –40°C to 125°C*
Storage Temperature Range ..... –65°C to 150°C*

*See Derating EEPROM Retention at Temperature in the Applications Information section for junction temperatures in excess of 125°C.

## PIN CONFIGURATION




UHG PACKAGE
52-LEAD (5mm × 8mm) PLASTIC QFN

$T_{JMAX}$ = 125°C, $\theta_{JA}$ = 36°C/W, $\theta_{JC}$ = 3.8°C/W
EXPOSED PAD (PIN 53) IS GND, MUST BE SOLDERED TO PCB

## ORDER INFORMATION

| LEAD FREE FINISH | TAPE AND REEL | PART MARKING* | PACKAGE DESCRIPTION | TEMPERATURE RANGE |
|---|---|---|---|---|
| LTC3888EUHG-1#PBF | LTC3888EUHG-1#TRPBF | 38881 | 52-Lead (5mm × 8mm) Plastic QFN | –40°C to 125°C |
| LTC3888IUHG-1#PBF | LTC3888IUHG-1#TRPBF | 38881 | 52-Lead (5mm × 8mm) Plastic QFN | –40°C to 125°C |
| **AUTOMOTIVE PRODUCTS**** | | | | |
| LTC3888IUHG-1#WPBF | LTC3888IUHG-1#WTRPBF | 38881 | 52-Lead (5mm × 8mm) Plastic QFN | –40°C to 125°C |

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at $T_A$ = 25°C (Notes 2, 8). $V_{IN}$ = 12V, $V_{SENSEn+}$ = 1V, $V_{SENSEn-}$ = GND = 0V, $f_{SYNC}$ = 500kHz (externally driven) unless otherwise specified.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **$V_{IN}$ Supply** | | | | | | | |
| $V_{IN}$ | $V_{IN}$ Operating Range | | ● | 4.5 | | 26.5 | V |
| $I_Q$ | IC Operating Current | RUN0,1 = 0V<br>RUN0,1 = 3.3V, $C_{PWMn}$ = 0pF | | | 24<br>28 | | mA<br>mA |
| **$INTV_{CC}$ Linear Regulator Supply** | | | | | | | |
| $INTV_{CC}$ | $INTV_{CC}$ Output Voltage | $V_{IN}$ ≥ 6V (Note 4) | | | 5.2 | | V |
| $EXTV_{CC}$ | $INTV_{CC}$ Input Voltage Range | $V_{IN}$ = $INTV_{CC}$ (Note 4) | ● | 4.5 | | 5.5 | V |
| $V5_{UVLO}$ | PWM Undervoltage Lockout Threshold<br>Hysteresis | $V_{DD33}$ Rising | ● | | | 4.45 | V<br>mV |
| | | | | | 300 | | |
| **$V_{DD33}$ Linear Regulator Supply** | | | | | | | |
| $V_{DD33}$ | $V_{DD33}$ Output Voltage | $INTV_{CC}$ ≥ 4.5V (Note 5) | ● | 3.15 | 3.3 | 3.45 | V |
| $V3_{UVLO}$ | PMBus Undervoltage Lockout Threshold<br>Hysteresis | $V_{DD33}$ Rising | ● | | | 3.10 | V<br>mV |
| | | | | | 275 | | |
| **$V_{DD25}$ Linear Regulator** | | | | | | | |
| $V_{DD25}$ | $V_{DD25}$ Output Voltage | (Note 7) | | | 2.5 | | V |
| **PWM Control Loops** | | | | | | | |
| $V_{FB}$ | Regulated Feedback Voltage | VOUT_SCALE_LOOP Not Programmed | | | 400 | | mV |
| $I_{FB}$ | $V_{FB}$ Input Current | $V_{FB}$ = 0.4V | ● | –100 | | 100 | nA |
| $V_{OUT}$ | Accuracy without Servo (Note 10)<br>Accuracy with Servo (Notes 9, 10, See Test Circuit)<br>Servo Resolution | 1V ≤ $V_{OUT}$ ≤ 3.45V<br>0.3V ≤ $V_{OUT}$ ≤ 3.45V<br>0.3V ≤ $V_{OUT}$ ≤ 3.45V | ●<br><br><br>● | –1.5<br><br>–0.5 | <br>±0.2<br><br>12 | 1.5<br><br>0.5 | %<br>%<br>%<br>Bits |
| $R_{VSENSE}$ | $V_{SENSE}$ Input Resistance | | ● | 30 | 43.3 | | kΩ |
| $V_{LINEREG}$ | Line Regulation | 6V ≤ $V_{IN}$ ≤ 24V (Note 10) | | –0.02 | | 0.02 | %/V |
| $V_{LOADREG}$ | Load Regulation | $\Delta_{ITHn}$ = ±600mV (Note 10) | | –0.1 | | 0.1 | % |
| $g_m$ | Resolution<br>Error Amplifier $g_{m(MAX)}$<br>Error Amplifier $g_{m(MIN)}$<br>LSB Step Size | $I_{TH}$ = 1.35V | | | 3<br>5.76<br>1<br>0.68 | | Bits<br>mmho<br>mmho<br>mmho |
| $R_{ITH}$ | Resolution (nonlinear) Compensation Resistance $R_{TH(MAX)}$ Compensation Resistance $R_{TH(MIN)}$ | | | | 5<br>62<br>1 | | Bits<br>kΩ<br>kΩ |
| $I_{SHARE\_TOL}$ | Phase-to-Phase Output Current Sharing Accuracy | $I_{SENSEn}$ – IREF ≥ 150mV | ● | –6.5 | <br>±3 | 6.5 | %<br>% |
| $I_{ISENSE}$ | $I_{SENSEn}$ Input Current | 1.5V ≤ $I_{SENSEn}$ ≤ 1.9V | ● | –1 | | 3 | µA |
| $V_{IREF}$ | Current Monitor Reference Output Voltage | $I_{IREF}$ = 3mA (Note 6) | | 1.52 | | 1.68 | V |
| $I_{IREF}$ | IREF Output Current | Source, IREF ≥ 1.52V<br>Sink, IREF ≤ 1.68V | | <br>10 | | –500 | µA<br>mA |
| $f_{SYNC}$ | SYNC Output Frequency Accuracy | | ● | –7.5 | | 7.5 | % |
| $t_{ON(MIN)}$ | Minimum On-Time | MFR_PWM_MODE_LTC3888-1[3] = 1<br>MFR_PWM_MODE_LTC3888-1[3] = 0 | ● | 30 | <br>21 | 60 | ns<br>ns |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at $T_A$ = 25°C (Notes 2, 8). $V_{IN}$ = 12V, $V_{SENSEn+}$ = 1V, $V_{SENSEn-}$ = GND = 0V, $f_{SYNC}$ = 500kHz (externally driven) unless otherwise specified.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **Difference Amplifiers** | | | | | | | |
| DA_$V_{OS}$ | Input Offset Voltage | Referred to $V_{SENSE^+}$ | ● | –16 | | 16 | mV |
| DA_GE | Gain Error | Nominal Gain at DAOUT: 1.00 (Note 10) | ● | –4 | | 4 | % |
| DA_BW | Unity-Gain Crossover Frequency | $R_L$ = 40kΩ (Note 16) | | | 25 | | MHz |
| DA_$I_{OUT}$ | Maximum Output Current | Sourced, DAOUT = 3.45V | ● | 325 | | | µA |
| DA_$V_{MAX}$ | Maximum Output Voltage | | | | 3.45 | | V |
| **Input Voltage Supervisor** | | | | | | | |
| $N_{VON}$ | Input ON/OFF Resolution LSB Step Size | | | | 9<br>54.7 | | Bits<br>mV |
| $V_{ON\_FS}$ | Full-Scale ON Threshold | | | | 28 | | V |
| $V_{ON\_TOL}$ | Input ON/OFF Threshold Accuracy | VIN_ON ≥ 6.5V | ● | –2 | | 2 | % |
| **Output Voltage Supervisors** | | | | | | | |
| $V_{UVOV\_TOL}$ | Accuracy (Note 10) | 0.5V ≤ $V_{OUT}$ < 1.0V (UV and OV)<br>1.0V ≤ $V_{OUT}$ ≤ 3.6V (UV and OV) | ●<br>● | –3<br>–2 | | 3<br>2 | %<br>% |
| **Output Current Supervisors** | | | | | | | |
| $N_{ILIMIT}$ | $I_{SENSE}$ Overcurrent Limit Resolution | | | | 7 | | Bits |
| $V_{OC\_FS}$ | Full-Scale Threshold | $I_{SENSEn}$ – IREF | | | 500 | | mV |
| $V_{OC\_TOL}$ | Accuracy | $I_{SENSEn}$ – IREF ≥ 100mV | ● | –6.5 | | 6.5 | % |
| **Gate Drive Voltage Supervisors** | | | | | | | |
| $I_{VDR\_MON}$ | VDR_MON Input Current | VDR_MON = 1.22V | ● | –1 | | 1 | µA |
| $V_{DR\_UV}$ | UV Threshold | | ● | 1.194 | | 1.243 | V |
| **ADC Readback Telemetry** (Note 11) | | | | | | | |
| $N_{VIN}$ | $V_{IN}$ Readback Resolution | (Note 12) | | | 10 | | Bits |
| $V_{IN\_TUE}$ | $V_{IN}$ Total Unadjusted Readback Error | $V_{IN}$ ≥ 4.5V | ● | | | 1 | % |
| $N_{VOUT}$ | $V_{OUT}$ Resolution<br>LSB Step Size | | | | 16<br>130 | | Bits<br>µV |
| $V_{OUT\_TUE}$ | $V_{OUT}$ Total Unadjusted Readback Error | Constant Load | <br>● | <br>–0.5 | ±0.2 | <br>0.5 | %<br>% |
| $V_{OUT\_OS}$ | $V_{OUT}$ Readback Offset Voltage | | | | ±300 | | µV |
| $N_{ISENSE}$ | $I_{OUT}$ Readback Resolution | (Note 12) | | | 10 | | Bits |
| $I_{SENSE\_TUE}$ | $I_{OUT}$ Total Unadjusted Readback Error | $I_{SENSEn}$ – IREF ≥ 40mV | ● | –1 | | 1 | % |
| $I_{SENSE\_OS}$ | $I_{OUT}$ Readback Offset Voltage | | | | ±125 | | µV |
| $N_{TEMP}$ | Temperature Resolution | (Note 12) | | | 10 | | Bits |
| $T_{TUE}$ | Temperature Total Unadjusted Readback Error | 0.24V ≤ TSNS*n* ≤ 1.8V (Note 13) | ● | –1.5 | | 1.5 | °C |
| $t_{CONVERT}$ | Update Rate (Note 14) | MFR_PWM_CONFIG_LTC3888-1[6] = 0<br>MFR_PWM_CONFIG_LTC3888-1[6] = 1 | | | 90<br>45 | | ms<br>ms |
| **Internal EEPROM** (Note 15) | | | | | | | |
| Endurance | Number of Write Operations | 0°C ≤ $T_J$ ≤ 85°C During All Write Operations | ● | 10,000 | | | Cycles |
| Retention | Stored Data Retention | $T_J$ ≤ 125°C | ● | 10 | | | Years |
| Mass Write Time | STORE_USER_ALL Execution Duration | 0°C ≤ $T_J$ ≤ 85°C During All Write Operations | ● | | 0.2 | 2 | s |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at $T_A$ = 25°C (Notes 2, 8). $V_{IN}$ = 12V, $V_{SENSEn+}$ = 1V, $V_{SENSEn-}$ = GND = 0V, $f_{SYNC}$ = 500kHz (externally driven) unless otherwise specified.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **Digital Inputs (SCL, SDA, RUN*n*, $\overline{\text{FAULT}}$*n*, SYNC, SHARE_CLOCK)** | | | | | | | |
| $V_{IH}$ | Input High Voltage | SCL, SDA, RUN*n*, $\overline{\text{FAULT}}$*n*<br>SYNC, SHARE_CLK | ●<br>● | 1.25<br>1.8 | | | V<br>V |
| $V_{IL}$ | Input Low Voltage | SCL, SDA, RUN*n*, $\overline{\text{FAULT}}$*n*<br>SYNC, SHARE_CLK | ●<br>● | | | 0.8<br>0.6 | V<br>V |
| $V_{HYST}$ | Input Hysteresis | SCL, SDA (Note 10) | | | 65 | | mV |
| $I_{IN}$ | Input Leakage Current | 0V ≤ SCL, SDA, RUN0, RUN1 ≤ 5.5V | ● | –5 | | 5 | µA |
| $C_{IN}$ | Input Capacitance | (Note 16) | | | | 10 | pF |
| $t_{FILT}$ | Input Digital Filter Delay | $\overline{\text{FAULT}}$*n*<br>RUN*n* | | | 3<br>10 | | µs<br>µs |
| **Digital Outputs (SCL, SDA, RUN*n*, $\overline{\text{FAULT}}$*n*, SYNC, SHARE_CLOCK, $\overline{\text{ALERT}}$, PWM*n*, PGOOD*n*, CLKOUT)** | | | | | | | |
| $V_{OL}$ | Output Low Voltage | $I_{SINK}$ = 3mA: SDA, SCL, $\overline{\text{FAULT}}$n, $\overline{\text{ALERT}}$, SYNC, RUN*n*, SHARE_CLK<br>$I_{SINK}$ = 2mA: PWM*n*, PGOOD*n*, CLKOUT | ●<br>● | | | 400<br>300 | mV<br>mV |
| $V_{OH}$ | Output High Voltage | PWM*n*, $I_{SOURCE}$ = 2mA | ● | 2.7 | | | V |
| $I_{LKG}$ | Output Leakage Current | 0V ≤ PWM*n*, PGOOD*n* ≤ $V_{DD33}$,<br>0V ≤ CLKOUT ≤ $V_{DD33}$<br>0V ≤ $\overline{\text{FAULT}}$*n*, SYNC ≤ 3.6V,<br>0V ≤ SHARE_CLOCK ≤ 3.6V<br>0V ≤ RUN*n*, SCL, SDA, $\overline{\text{ALERT}}$ ≤ 5.5V | ●<br>●<br>●<br>●<br>● | –2<br>–2<br>–2<br>–5<br>–5 | | 2<br>2<br>2<br>5<br>5 | µA<br>µA<br>µA<br>µA<br>µA |
| $t_{RO}$ | PWM*n* Output Rise Time | $C_{LOAD}$ = 30pF, 10% to 90% | | | 5 | | ns |
| $t_{FO}$ | PWM*n* Output Fall Time | $C_{LOAD}$ = 30pF, 90% to 10% | | | 4 | | ns |
| **Serial Bus Timing** | | | | | | | |
| $f_{SMB}$ | Serial Bus Operating Frequency | | ● | 10 | | 400 | kHz |
| $t_{BUF}$ | Bus Free Time Between Stop and Start | | ● | 1.3 | | | µs |
| $t_{HD,STA}$ | Hold Time After (Repeated) Start Condition. After this Period, the First Clock is Generated. | | ● | 0.6 | | | µs |
| $t_{SU,STA}$ | Repeated Start Condition Setup Time | | ● | 0.6 | | | µs |
| $t_{SU,STO}$ | Stop Condition Setup Time | | ● | 0.6 | | | µs |
| $t_{HD,DAT}$ | Data Hold Time:<br>Receiving Data<br>Transmitting Data | | <br>●<br>● | <br>0<br>0.3 | | <br><br>0.9 | <br>ns<br>µs |
| $t_{SU,DAT}$ | Input Data Setup Time | | ● | 100 | | | ns |
| $t_{TIMEOUT}$ | Clock Low Time-Out | | ● | 25 | | 35 | ms |
| $t_{LOW}$ | Serial Clock Low Period | | ● | 1.3 | | 10,000 | µs |
| $t_{HIGH}$ | Serial Clock High Period | | ● | 0.6 | | | µs |
| $t_F$ | Clock or Data Fall Time | 90% to 10% | ● | 20 | | 300 | ns |
| $t_R$ | Clock or Data Rise Time | 10% to 90% | ● | 20 | | 300 | ns |

# ELECTRICAL CHARACTERISTICS

**Note 1:** Absolute Maximum Ratings are given relative to GND, unless otherwise specified. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The LTC3888-1 is tested under pulsed load conditions such that $T_J \approx T_A$. Junction temperature $T_J$ is calculated in °C from the ambient temperature $T_A$ and power dissipation $P_D$ according to the formula: $T_J = T_A + (P_D \bullet \theta_{JA})$ where $\theta_{JA}$ is the package thermal impedance. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors. Refer to the Applications Information section.

**Note 3:** This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when this protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

**Note 4:** Do not apply a voltage source to $INTV_{CC}$ unless shorted to $V_{IN}$. Otherwise, connect only external passive components for LTC3888-1 configuration. See Electrical Characteristics for applicable limits beyond which permanent damage may occur.

**Note 5:** An external voltage source may be connected directly to $V_{DD33}$ only if the device is not powered from $V_{IN}$ or $INTV_{CC}$. Otherwise, connect only external passive components for LTC3888-1 configuration. See Electrical Characteristics for applicable limits beyond which permanent damage may occur.

**Note 6:** Do not apply a voltage source directly to these pins. See Electrical Characteristics for applicable limits beyond which permanent damage may occur.

**Note 7:** Do not apply a voltage or current source directly to these pins. Connect only external passive components for LTC3888-1 configuration and application, otherwise permanent damage may occur.

**Note 8:** All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to GND unless otherwise specified.

**Note 9:** Specified accuracy requires Servo Mode to be set with MFR_PWM_MODE_LTC3888-1 command bit 6. VOUT_COMMAND must be within ±5.5% of unadjusted $V_{OUT}$.

**Note 10:** LTC3888-1 output voltage control is trimmed and measured in a feedback loop that servos $I_{TH}$ to a specified value using a fixed external gain of 3.5. Output accuracy may be better than that of other loop-regulated voltages (DAOUT, VFB). Output accuracy without Servo Mode may degrade when external gain deviates from 3.5 in the application.

**Note 11:** ADC tested with PWMs disabled. Comparable capability demonstrated by in-circuit evaluations. Total unadjusted error includes all gain and linearity errors, as well as offsets.

**Note 12:** Internal 32-bit calculations using 16-bit ADC results are limited to 10-bit mantissa resolution by PMBus linear 11-bit data format.

**Note 13:** Limits guaranteed by TSNS voltage and current measurements during test, including ADC read backs.

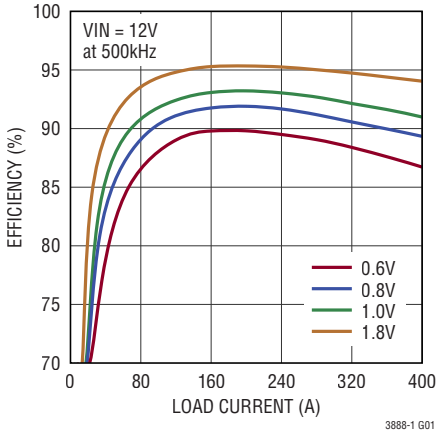
**Note 14:** Data conversion is done in round robin fashion. If all inputs signals are scanned, continuous in-sequence conversions result in a typical latency of 90ms.

**Note 15:** The EEPROM endurance, retention and mass write times are guaranteed by design, characterization and correlation with statistical process controls. Minimum retention applies only for devices cycled less than the minimum endurance specification. EEPROM read commands (e.g. RESTORE_USER_ALL) are valid over the entire specified operating junction temperature range.

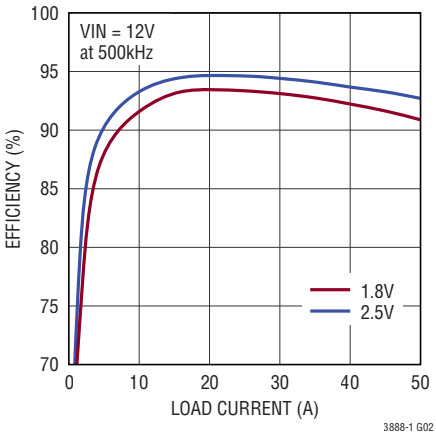
**Note 16:** Guaranteed by design.

# TYPICAL PERFORMANCE CHARACTERISTICS

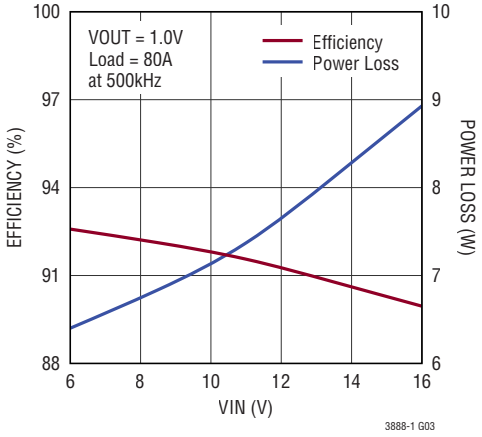
### Efficiency vs Load Current (8-Phase Using LTC7051)



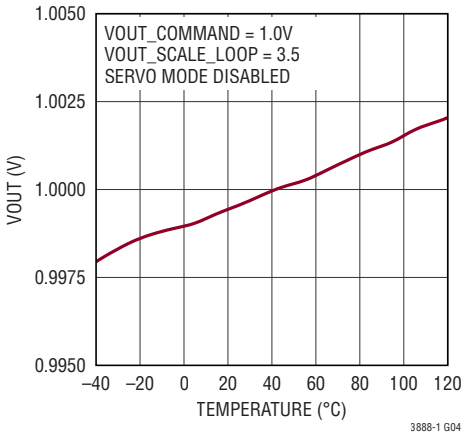

### Efficiency vs Load Current (1-Phase Using TDA21470)



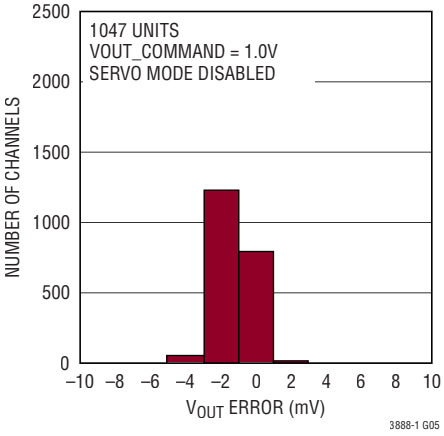

### Efficiency and Power Loss vs Input Voltage (4-Phase Using TDA21470)



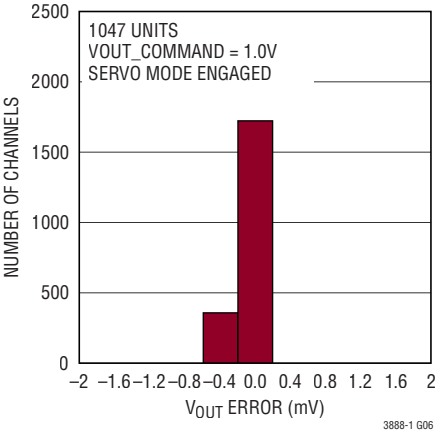

### Regulated Output vs Temperature



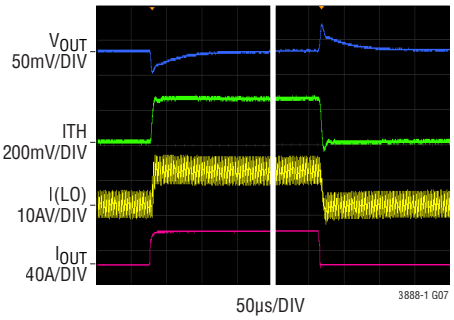

### Typical Output Voltage Distribution at 25°C Without Servo




### Typical Output Voltage Distrubtion at 25°C with Servo

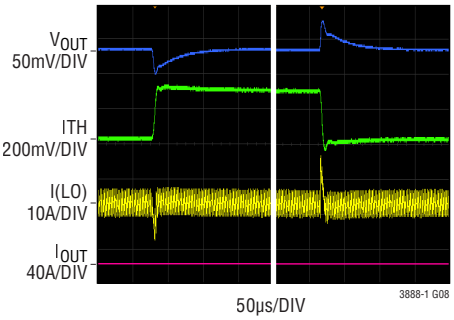



### 4-Phase Load Step Response (Using TDA21470)



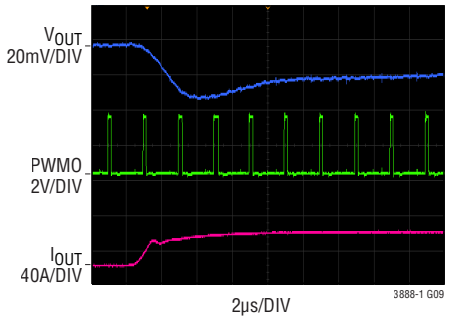

$V_{IN}$ = 12V
$V_{OUT}$ = 1.0V
10A TO 50A STEP

### Emulated 4-Phase Load Step Response (Using TDA21470)




$V_{IN}$ = 12V
$V_{OUT}$ = 1.0V
MFR_LOAD_EMULATION = 10A/PHASE

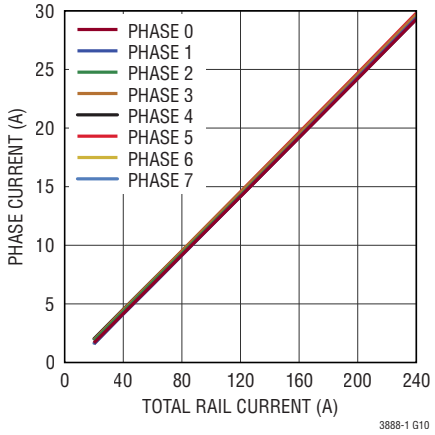
### 4-Phase Single Cycle Response (Using TDA21470 with $C_{OUT}$ = 4mF)



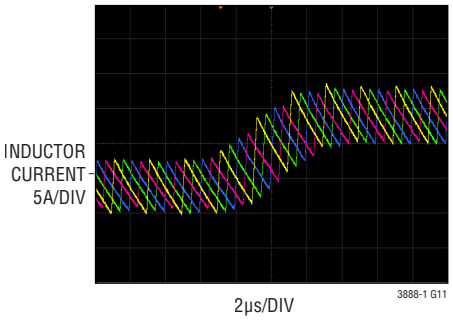

$V_{IN}$ = 12V
$V_{OUT}$ = 1.0V
SYNC = 500kHz
L = 215nH

# TYPICAL PERFORMANCE CHARACTERISTICS

### 8-Phase DC Output Current Sharing (Using TDA21470)

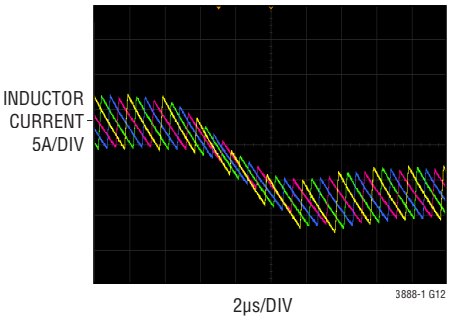



### 4-Phase Dynamic Load Sharing



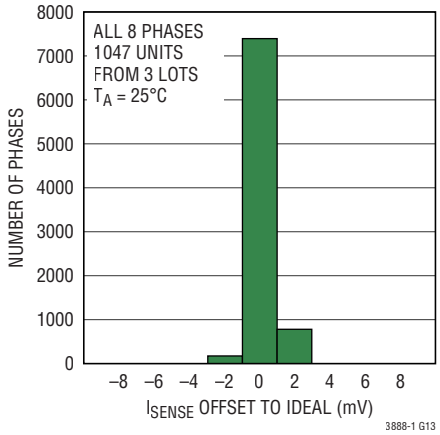

$V_{IN}$ = 12V
$V_{OUT}$ = 1.0V
SYNC = 500kHz
L = 215nH

### 4-Phase Dynamic Load Sharing

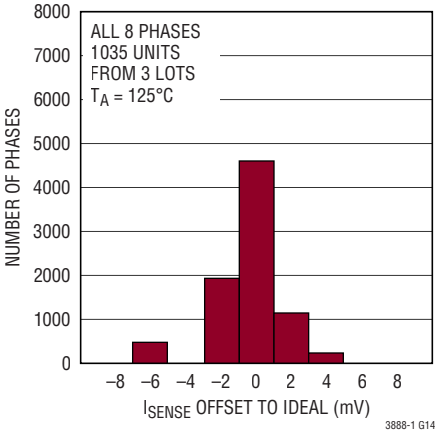



$V_{IN}$ = 12V
$V_{OUT}$ = 1.0V
SYNC = 500kHz
L = 215nH

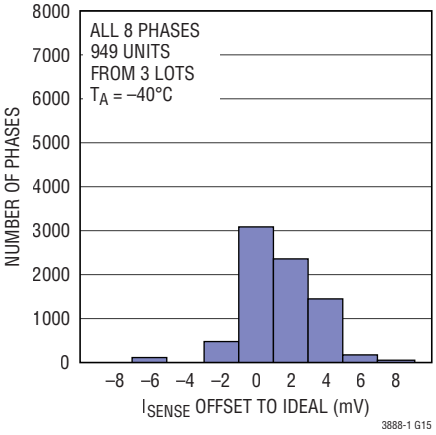
### Typical Distribution of Slave $I_{OUT}$ Offset (Not Including DrMOS Mismatch) Room



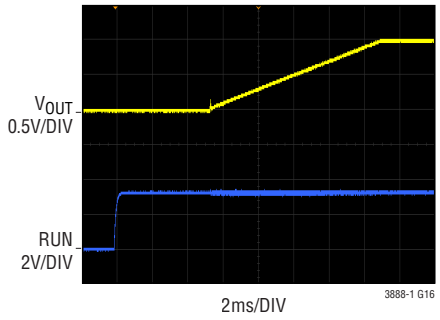

### Typical Distribution of Slave $I_{OUT}$ Offset (Not Including DrMOS Mismatch) Hot




### Typical Distribution of Slave $I_{OUT}$ Offset (Not Including DrMOS Mismatch) Cold

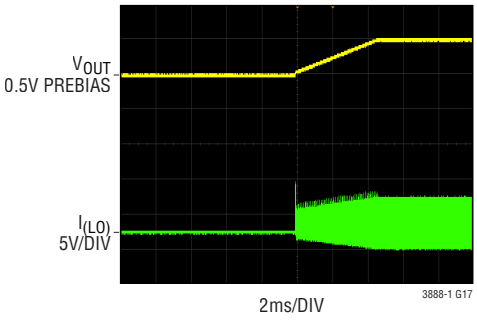



### Soft-Start Ramp



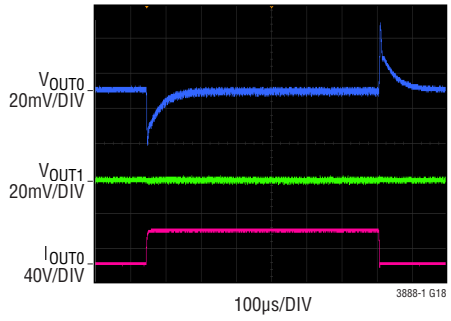

VOUT_COMMAND = 1.0V
VOUT_TRANSITION_RATE = 0.1V/ms
TON_DELAY = 5ms

### Start-Up Into a Prebiased Load



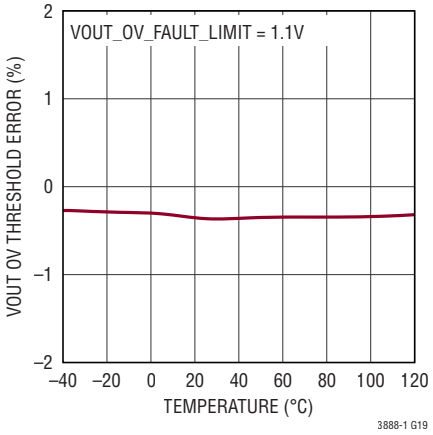

VOUT_COMMAND = 1.0V
VOUT_TRANSITION_RATE = 0.1V/ms

### 4+4 Channel Crosstalk (Using TDA21470)

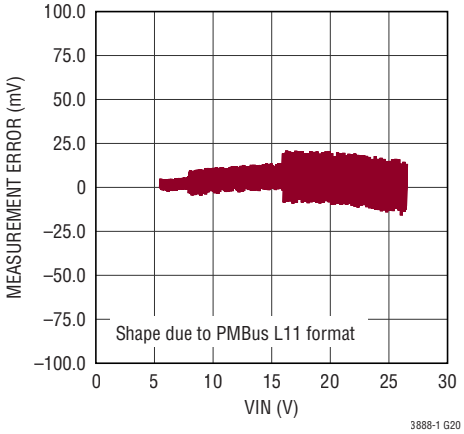


# TYPICAL PERFORMANCE CHARACTERISTICS

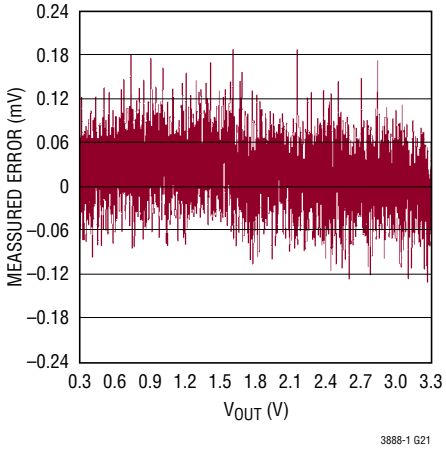
**Output Overvoltage Threshold Error vs Temperature**



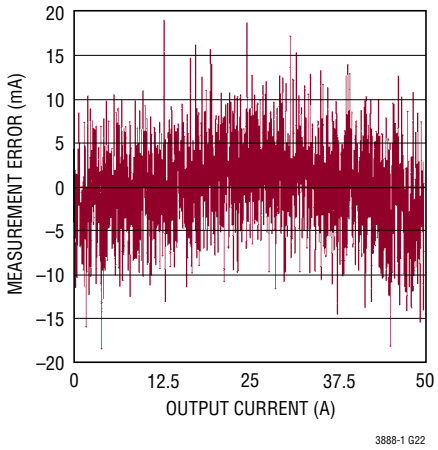

**$V_{IN}$ ADC TUE**



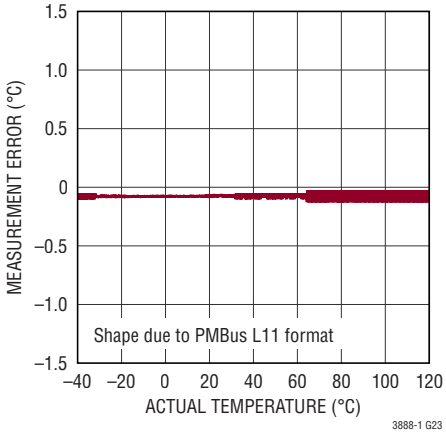

**$V_{OUT}$ ADC TUE**



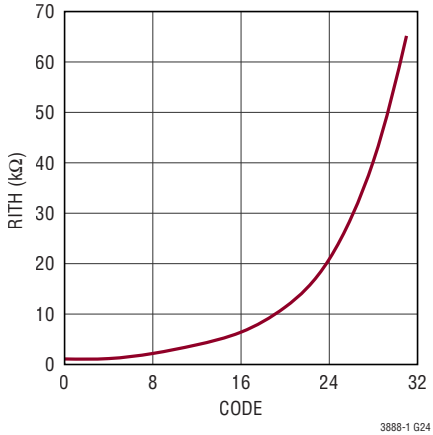

**$I_{OUT}$ ADC TUE**



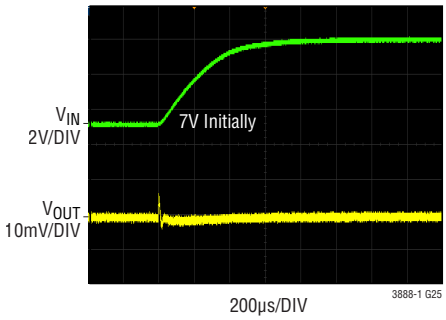

**Temperature ADC TUE (Not including DRMOS Error)**




**Programmable $R_{ITH}$**




**4-Phase Line Step Transient (Using TDA21470)**



## PIN FUNCTIONS

**PWM*n* (Pin 1, 2, 5, 42, 45, 46, 49, 50):** PWM Control Outputs. These eight pins provide 3.3V three-state PWM switching control for each phase. Leave these pins open if not used.

**$I_{SENSEn}$ (Pin 3, 4, 43, 44, 47, 48, 51, 52):** Current Sense Inputs. These eight inputs connect to the current monitor outputs of DrMOS devices. Short these pins to IREF if not used.

**$V_{SENSE0-}$/$V_{SENSE1-}$ (Pin 6/Pin 41):** Differential Amplifier and ADC Output Voltage Sense Negative Inputs. Short these pins to GND if not used.

**$V_{SENSE0+}$/$V_{SENSE1+}$ (Pin 7/Pin 40):** Differential Amplifier and ADC Output Voltage Sense Positive Inputs. Short these pins to $V_{SENSE-}$ if not used.

**TSNS0/TSNS1 (Pin 8/Pin 39):** External Temperature Sense Inputs. Connect these pins to the shared temperature/fault bus of DrMOS devices, otherwise refer to the Applications Information section for more detail.

**VDR_MON (Pin 8):** External Gate Drive Voltage Sense Input. This pin can be programmed to monitor the gate drive voltage the system is providing to external DrMOS power stages. Refer to MFR_CHAN_CONFIG command details.

**$I_{TH0}$/$I_{TH1}$ (Pin 9/Pin 38):** PWM Current Control Threshold and Loop Compensation Nodes. Peak current increases with $I_{TH}$ voltage. Attach a low ESR capacitor between these pins and GND for adequate loop compensation. Refer to the Applications Information section for more details.

**$I_{THR0}$/$I_{THR1}$ (Pin 10/Pin 37):** Loop Compensation Nodes. Attach a low ESR capacitor between these pins and GND for adequate loop compensation. Refer to the Applications Information section for more details.

**DAOUT0/DAOUT1 (Pin 11/Pin 36):** Differential Amplifier Outputs. DAOUT0/1 provide a voltage equal to the difference between $V_{SENSE+}$ and $V_{SENSE-}$ for that channel, referenced to GND (paddle). Leave these pins open if not used.

**$V_{FB0}$/$V_{FB1}$ (Pin 12/Pin 35):** Error Amplifier Inverting Input. The PWM control loop regulates this voltage when the output rail is on.

**PGOOD0/PGOOD1 (Pin 13/Pin 34):** Power Good Indicator Open-Drain Outputs. These outputs are driven low through an 80µs filter when the respective channel output is below its programmed UV fault limit or above its programmed OV fault limit. If used, a pull-up resistor is required in the application.

**CLKOUT (Pin 13):** Expansion Clock Output. This output provides a phase expansion clock to a second LTC3888-1 if bit 3 of MFR_PWM_ CONFIG_LTC3888-1 is set. If used, a pull-up resistor is required. Minimize the capacitance on this line to ensure its time constant is fast enough for the application.

**SYNC (Pin 14):** External Clock Synchronization Input and Open-Drain Output. If desired, an external clock can be applied to this pin to synchronize the internal PWM channels. Otherwise this pin can pull to ground at the selected PWM switching frequency with a 500ns pulse width. A pull-up resistor to 3.3V is required if SYNC is provided by the LTC3888-1. Minimize the capacitance on this line to ensure its time constant is fast enough for the application.

**SCL (Pin 15):** Serial Bus Clock Input and Open-Drain Output. SCL functions as an output only if clock stretching is enabled. A pull-up resistor to the bus supply is required in the application.

**SDA (Pin 16):** Serial Bus Data Input and Open-Drain Output. A pull-up resistor to the bus supply is required in the application.

**$\overline{\text{ALERT}}$ (Pin 17):** Open-Drain Status Output. This pin may be connected to the system SMBALERT# wire-AND interrupt signal. A pull-up resistor to the bus supply is required in the application. This pin should be left open if not used.

**$\overline{\text{FAULT0}}$/$\overline{\text{FAULT1}}$ (Pin 18/Pin 19):** Programmable Digital Inputs and Open-Drain Outputs for Fault Sharing. These pins are used for channel-to-channel fault communication and propagation. A pull-up resistor to 3.3V is required in the application.

## PIN FUNCTIONS

**RUN0/RUN1 (Pin 20/Pin 21):** Run Control Inputs and Open-Drain Outputs. A voltage above 2V is required on these pins to enable the respective PWM master channel. The LTC3888-1 may drive these pins low under certain reset/restart conditions regardless of any PMBus command settings. A pullup resistor is required in the application.

**$R_{SET}$ (Pin 22):** Resistor Configuration Set Input. Connect a 1% 18.7kΩ resistor between this pin and GND to set the selection values for the configuration resistors for programming bus address, output current limit and other PWM settings. Refer to the Applications Information section for more details.

**ASEL0/ASEL1 (Pin 23, Pin 24):** Serial Bus Address Select Inputs. Connect optional 1% resistors between these pins and GND to select the serial bus interface address. Refer to the Applications Information section for more detail.

**ILIM0_CFG/ILIM1_CFG (Pin 25/Pin 26):** Output Current Limit Configuration Inputs. Connect optional 1% resistors between these pins and GND to select the output current limit for each channel. Refer to the Applications Information section for more detail.

**PWM_CFG (Pin 27):** PWM Configuration Input. Connect an optional 1% resistor between this pin and GND to configure PWM switching frequency and master/slave configuration. Refer to the Applications Information section for more detail.

**$V_{DD25}$ (Pin 28):** Internal 2.5V Regulator Output. Bypass this pin to GND with a low ESR 1µF capacitor. Do not load this pin with external current.

**SHARE_CLK (Pin 29):** Share Clock Input and Open-Drain Output. Share clock, nominally 100kHz, is used to sequence multiple rails in a power system utilizing more than one ADI PMBus controller. A pull-up resistor to 3.3V is required in the application. Minimize the capacitance on this line to ensure the time constant is fast enough for the application.

**$V_{DD33}$ (Pin 30):** Internal 3.3V Regulator Output. Bypass this pin to GND with a low ESR capacitor (1µF to 2.2µF). The LTC3888-1 may also be powered from an external 3.3V source attached to this pin for programming purposes only, if the device is otherwise unpowered. Connect only external passive components for LTC3888-1 configuration and application.

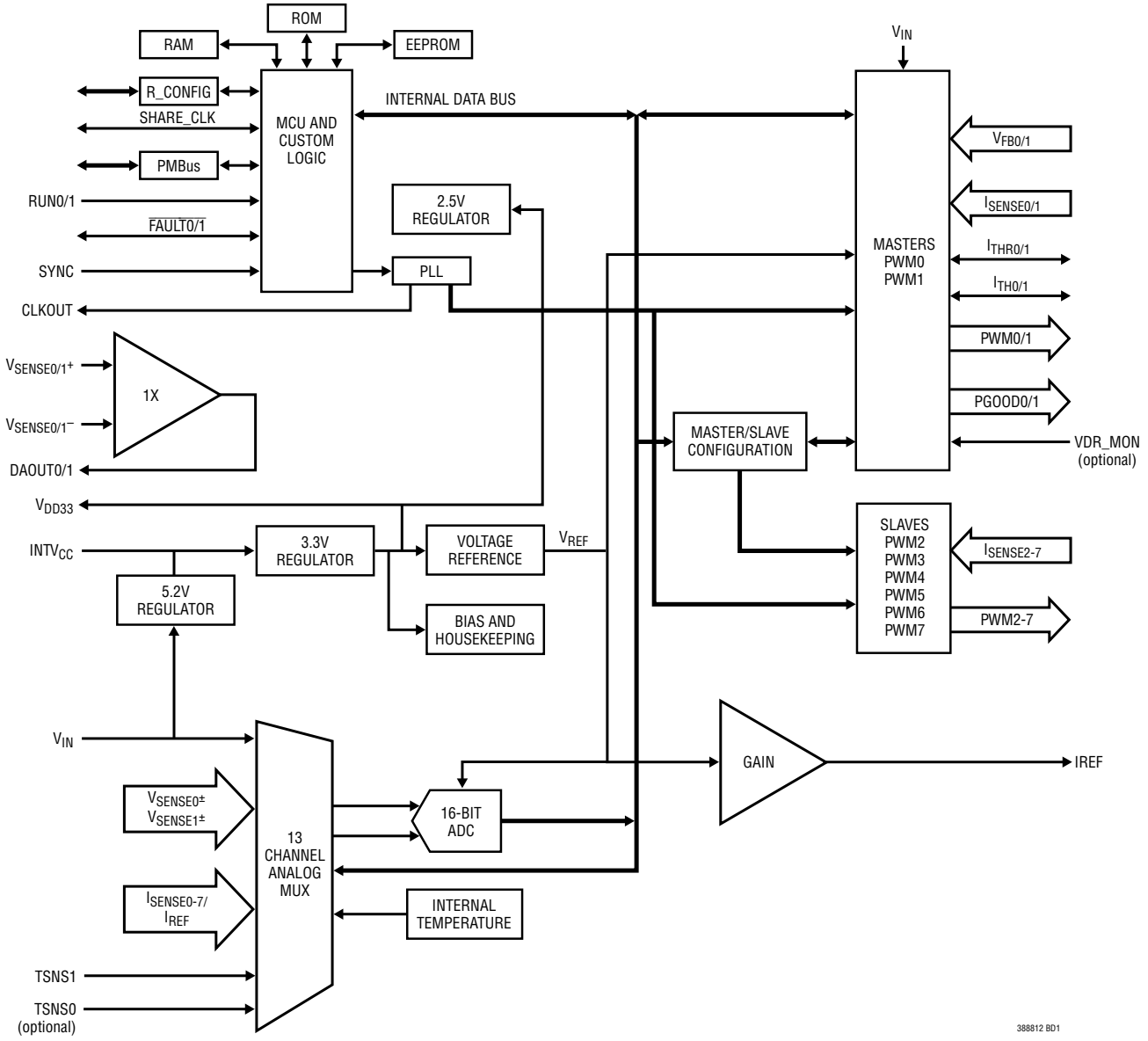
**$INTV_{CC}$ (Pin 31):** 5.2V Regulator Output. Bypass this pin to GND with a low ESR 4.7µF capacitor. Connect only external passive components for LTC3888-1 configuration and application.

**$V_{IN}$ (Pin 32):** Main Input Supply. Decouple this pin to GND with a low ESR capacitor (0.1µF to 2.2µF). In applications where $V_{IN}$ will always operate below 6V, short this pin and $INTV_{CC}$ together.

**IREF (Pin 33):** DrMOS Current Sense Reference. This voltage output provides reference bias for floating current monitors from DrMOS devices. Decouple this pin to GND (exposed pad) at the LTC3888-1 and each power stage with 100nF to 1µF using low ESR capacitors.

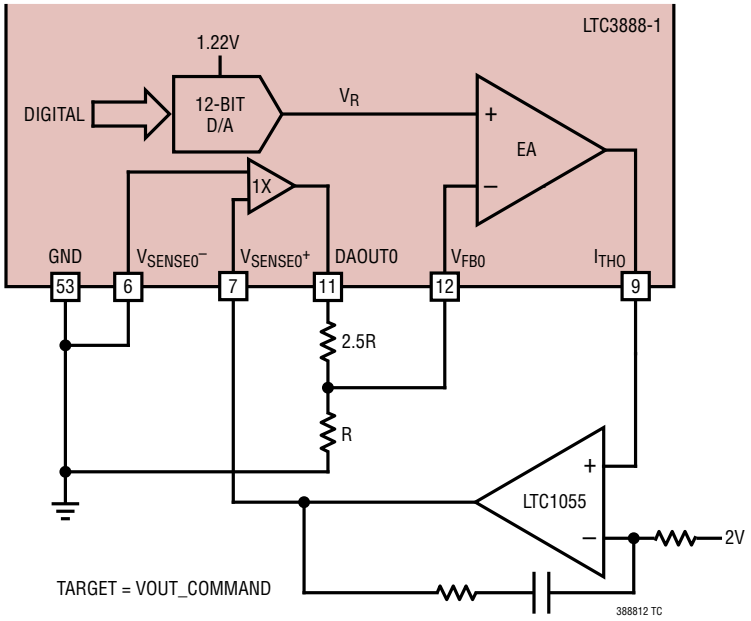
**GND (Exposed Pad Pin 53):** Ground. All small-signal and compensation components should connect to this pad. The exposed pad must be soldered to a suitable PCB copper ground plane for proper electrical operation and to obtain the specified package thermal resistance.

# BLOCK DIAGRAM

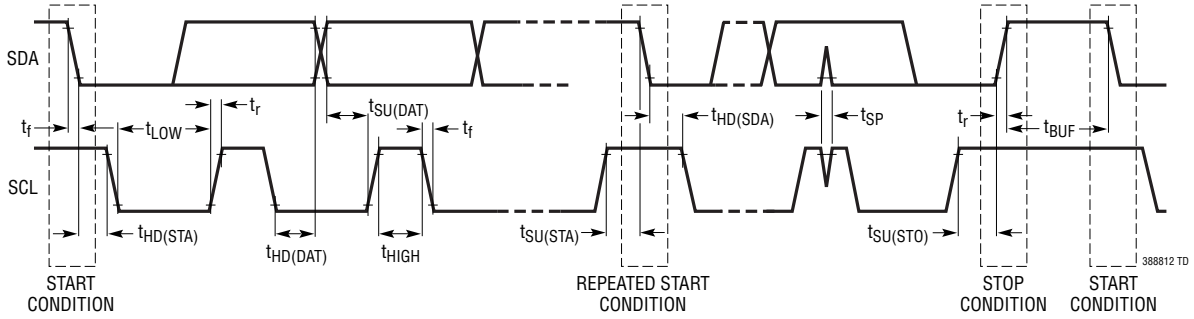



**LTC3888-1 Block Diagram**

## TEST CIRCUIT



## TIMING DIAGRAM



# OPERATION

## OVERVIEW

The LTC3888-1 is a constant frequency analog current mode controller for DC/DC step-down switch-mode applications. It provides up to two independent voltage loops (masters) and also contains six additional slave modulators, affording a wide range of predetermined PolyPhase configurations.

The device is designed to be used with external power stages that provide an output current monitor, either as a voltage or current. This includes higher level integrations such as non-isolated power blocks. The LTC3888-1 provides a direct interface to the shared temperature and fault indication bus commonly found on such power stages, as well as an optional DrMOS gate drive supply voltage supervisor.

The chip operates from a $V_{IN}$ power supply between 4.5V and 28.5V. Without any other programming, output voltage may be set to any value between 0.4V and 3.45V using an external resistor divider and the factory EEPROM settings.

The LTC3888-1 also features a PMBus compliant digital interface for monitoring and setting of important power system parameters, including direct output control using the external resistor divider, if desired.

### About This Document

PMBus command pages 0 and 1 control the two voltage regulation loops associated with PWM0 and PWM1, respectively. In this document, these may also be referred to as masters or master channels. There are often unique IC pins associated with each of these master channels, such as $I_{TH0}$ and $I_{TH1}$. In cases where discussion applies to both or either of the master channels, these pin names may appear without index.

PWM2 to PWM7 are not directly controlled by PMBus operation, but instead are managed by the master channel that is assigned to control them. In this document, the modulators associated with PWM2 to PWM7 will be referred to as slaves or slave channels. Occasionally the term PWM or channel may apply to any of the eight PWM modulators. Rail will designate a master channel and the group of slaves it controls to produce a single output voltage, including multiple master channels with wire-OR $I_{TH}$ control.

The phrase operating memory or simply RAM refers to volatile onboard RAM holding PMBus commands during operation.

PMBus commands in this document are given in all capital letters with no white space, although hyphens or underscores may be included. For brevity, the indentifying phrase PMBus command is most often omitted when this typeface appears. **All PMBus commands from 0x00 through 0xFF not listed in Table 7 are implicitly not supported by the LTC3888-1. Writing to any command not listed in this table may result in a CML fault and/or undesired operation of the part.**

## MAJOR PRODUCT FEATURES

- Analog and/or Digitally Programmable Output Voltage with UV/OV Supervisors
- Digitally Programmable Output Current Limit
- Digitally Programmable Input Voltage Supervisor
- Digitally Programmable Switching Frequency
- Digitally Programmable On and Off Delay Times
- Digitally Programmable Soft-Start/Stop
- Digitally Programmable Load Step Emulation
- Operating Condition Telemetry
- Phase-Locked Loop for Synchronous PolyPhase Operation
- Non-Volatile Configuration Memory
- Optional External Configuration Resistors for Key Operating Parameters
- Optional Time-Base Interconnect for Synchronization Between Multiple Controllers
- Fault Event Data Logging
- Capable of Standalone Operation via EEPROM Configuration
- PMBus Revision 1.2 Compliant Interface up to 400kHz

## OPERATION

The PMBus interface provides access to important power management data during system operation including:

- Average Input Voltage
- Average Output Voltages
- Average Output Currents
- PWM Operating Frequency
- Internal Device Temperature
- External Sensed Temperatures
- Warning and Fault Status, Including Input and Output Undervoltage and Overvoltage

The LTC3888-1 supports four PMBus bus addressing schemes to access the individual PWM voltage loops separately or jointly.

Fault reporting and system response behavior are fully configurable. The two status outputs ($\overline{FAULT0}$, $\overline{FAULT1}$) can be controlled independently. A separate $\overline{ALERT}$ pin also provides a maskable SMBALERT#. Fault responses for each channel may be individually programmed, depending on the fault type. PMBus status commands allow fault reporting over the serial bus to identify a specific fault event.

### MAIN CONTROL LOOP

The LTC3888-1 utilizes constant frequency current mode control with trailing-edge modulation. The main control loop used for each master channel is illustrated in Figure 1. During normal operation the top MOSFET in the external power stage (power switch) driving choke L1 is commanded on when the clock phase for that master sets the RS latch, unless the main PWM comparator ICMP indicates there is already too much current in L1. In that case no additional energy is delivered to the choke during that cycle (PWM output remains low, cycle skipped). Otherwise the latch is reset and power switch commanded off later in the cycle by the PWM comparator. Sensed output current is provided from the external power stage at the $I_{SENSE}$ pin. The point in the PWM cycle at which ICMP resets the RS latch is controlled by the $I_{TH}$ voltage provided by the output of error amplifier EA, including internal slope compensation for stable operation regardless of duty cycle. In steady state, $I_{TH}$ adjusts the PWM duty cycle to match the $V_{FB}$ voltage to the EA positive terminal voltage.

The positive terminal of EA is connected to the output of a 12-bit DAC with values ranging from 0V to approximately 1.22V. The DAC value is determined by command values retrieved from internal EEPROM or by a combination of PMBus commands to synthesize the desired output voltage. The factory default EEPROM sets the value of this DAC output to 400mV. The EA then regulates the output voltage based on the ratio of external resistors R1 and R2.

If load current increases, $V_{SENSE}^+$ and thus $V_{FB}$ will droop slightly, $V_{FB}$ with respect to the 12-bit DAC output. This causes the $I_{TH}$ voltage to increase until the average inductor current matches the new load current and the desired output voltage is restored. $I_{TH}$ is monitored to provide programmable over-current protection with comparator ILIM.

When the top MOSFET is commanded off by the PWM output, the bottom MOSFET is commanded on. The LTC3888-1 operates in continuous conduction mode (CCM), so the bottom MOSFET stays on until the PWM clock next turns on the top MOSFET or the rail is commanded off.

### POWER-UP AND INITIALIZATION

The LTC3888-1 is designed to provide standalone supply sequencing with controlled turn-on and turn-off functions. It operates from a $V_{IN}$ supply of 4.5V to 26.5V while three on-chip linear regulators generate internal 2.5V, 3.3V and 5.2V. If $V_{IN}$ is below 6V, the $V_{IN}$ and $INTV_{CC}$ pins must be shorted together and limited to a maximum operating voltage of 5.5V. Controller configuration is reset by the internal UVLO threshold, where $INTV_{CC}$ must be at or above 4.45V, $V_{DD33}$ must be at or above 3.1V and the internal 2.5V supply must be within about 20% of its regulated value. $V_{IN}$ must simply be high enough for the LDO outputs to reach these voltages. At that point the internal microcontroller begins initialization. A RESTORE_USER_ALL or MFR_RESET forces this same initialization.

The LTC3888-1 features an internal RAM built-in self-test (BIST) that runs during initialization. Should RAM BIST fail, the following steps are taken.

## OPERATION

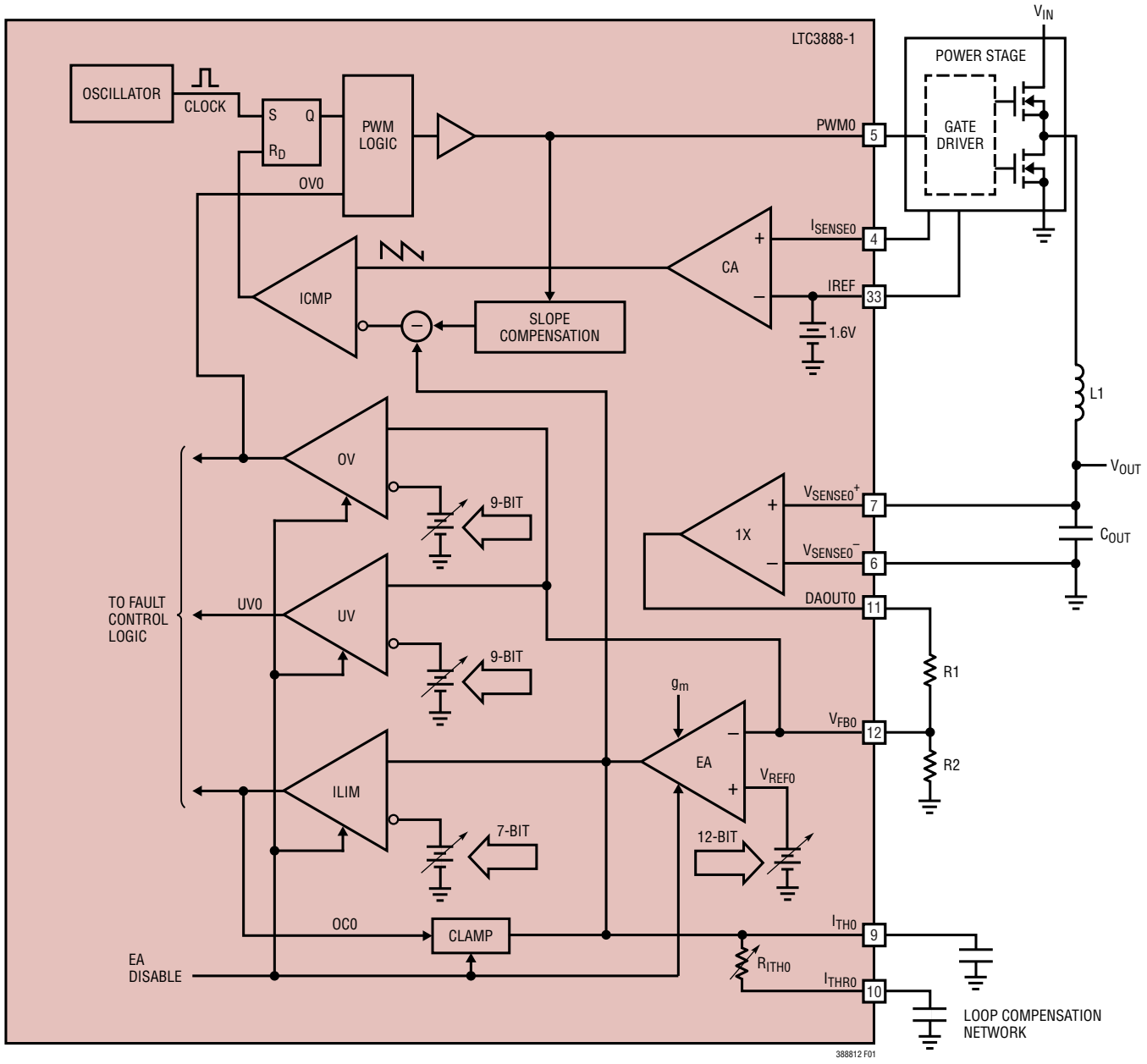



**Figure 1. LTC3888-1 Master Channel Control Loop Diagram**

## OPERATION

- Device responds only at device address 0x7C and global addresses 0x5A and 0x5B
- A persistent Memory Fault Detected is indicated by STATUS_CML
- Internal EEPROM is not accessed
- RUN pins and SHARE_CLK are driven low continuously

Normal operation can be restored if the RAM BIST subsequently passes, for instance as the result of another MFR_RESET issued to address 0x7C.

During initialization all PWM outputs are disabled. The RUN pins and SHARE_CLK are held low and $\overline{FAULT}$ pins are high impedance. External configuration resistors are identified and the contents of the onboard EEPROM are read into the controller command RAM. The LTC3888-1 can determine key operating parameters from external configuration resistors according to application Table 10 through Table 12. See the following Resistor Configuration Pins section for more detail. The resistor configuration pins only determine some of the preset values of the controller. The remaining values, retrieved from internal EEPROM, are programmed at the factory or with PMBus commands.

If the configuration resistor pins are all open, the LTC3888-1 will use only EEPROM contents to determine all operating parameters. If Ignore Resistor Configuration Pins is set (bit 6 of MFR_CONFIG_ALL), the LTC3888-1 will use only its EEPROM contents to determine all operating parameters except device address. Unless both ASEL pins are completely open, the LTC3888-1 will always determine some portion of its device address from the resistors on these pins. See Serial Bus Addressing later in this section.

### Testing Integrity of Output Voltage Sense

During initialization, the LTC3888-1 also runs a connectivity check on the output voltage sense line ($V_{SENSE}$+) of any enabled master channel (see bit 4 of MFR_PWM_MODE_LTC3888-1). If an open circuit is detected during this test, the failure is indicated in the PMBus status registers, and all PWMs on the IC are disabled until the test subsequently passes after MFR_RESET or device power cycle.

### ANALOG OUTPUT VOLTAGE CONTROL

The default factory EEPROM settings allow programming of output voltage using only the external resistors R1 and R2 shown in Figure 1. The control loop then produces the desired output in a classical fashion as $V_{FB}$ is regulated to 400mV. With other key parameters such as output current limit programmable using external configuration resistors, it is possible to create complex PolyPhase rail solutions without needing to connect the device to any digital bus. Refer to the Applications Information section for more details on using analog output voltage control with default factory EEPROM settings.

### PMBUS OUTPUT VOLTAGE CONTROL

Once external programming resistors R1 and R2 (Figure 1) are chosen, it is possible to also use the full range of digitally programmed output voltage control found on most ADI PSM controllers. This is accomplished by specifying the external divider gain with VOUT_SCALE_LOOP. Again, refer to Applications Information for complete details on controlling output voltage using built-in LTC3888-1 PMBus commands and features.

### SOFT-START

The internal microcontroller typically requires 35ms to complete initialization once all onboard supplies are above their UVLO threshold. After MCU initialization, an internal comparator monitors $V_{IN}$, which must exceed the VIN_ON threshold before output power sequencing can begin. SHARE_CLK is released to run and the RUN pins are released for external control after the part initializes and $V_{IN}$ is greater than the VIN_ON threshold. Accurate readback telemetry can then require an additional 90ms for initial round-robin A/D conversions.

## OPERATION

If multiple LTC3888-1 ICs are used in an application, shared RUN pins are held low until all units initialize and $V_{IN}$ exceeds the VIN_ON threshold for all devices. A common SHARE_CLK signal can also ensure all connected devices use the same time reference for initial start-up even if RUN pins cannot be shared due to other design requirements. SHARE_CLK is released by each IC once the conditions for power sequencing have been fully satisfied, regardless of RUN pin state.

After a channel RUN pin rises above 2V and any specified turn on delay (TON_DELAY) has expired, the LTC3888-1 performs an initial monotonic soft-start ramp on that channel, allowing inrush current control. This is carried out with a digitally controlled ramp of the internal EA reference voltage from 0mV to the commanded value (400mV factory default) at the VOUT_TRANSITION_RATE. The soft-start feature is disabled by setting the value of VOUT_TRANSITION_RATE to 4V/ms. The LTC3888-1 does not initiate PWM operation until the commanded output exceeds the actual rail voltage and $I_{TH}$ has risen to a level that will avoid negative average choke current. This allows the regulator to start up into a prebiased load.

### TIME-BASED OUTPUT SEQUENCING

The LTC3888-1 supports time-based output on and off sequencing using a shared time reference (SHARE_CLK). Following a qualified command to turn on, each output is enabled after waiting its programmed TON_DELAY. This can be used to sequence outputs in a prescribed order that can be reprogrammed as needed without hardware modification. Channel off-sequencing is accomplished in a similar way with the TOFF_DELAY command.

### OUTPUT RAMPING CONTROL

The LTC3888-1 supports synchronized output on and off ramping control using a shared time reference (SHARE_CLK). Power rail on and off relationships similar to those of conventional analog tracking functions can be achieved by using programmed delays and VOUT_TRANSITION_RATE. With LTC3888-1 digital control, ramping configurations can be reprogrammed as needed without hardware modification.

Programmable fault responses and fault sharing can ensure that any desired time-based output sequencing and ramping control is properly accomplished each time the system powers up or down. Refer to the Applications Information section for various LTC3888-1 hardware and PMBus command configurations needed to fully support synchronization for time-based sequencing and output ramping when using multiple ICs.

### VOLTAGE-BASED OUTPUT SEQUENCING

It is also possible to sequence outputs on using cascaded voltage events. To do this, the PGOOD status pin of one PWM channel can be used to control the RUN pin of a downstream channel. The controlling PGOOD pin holds RUN low if $V_{OUT}$ is below the VOUT_UV_FAULT_LIMIT or if power-good conditions are not being met. This keeps the downstream channel off until acceptable output conditions exist on the controlling channel. The LTC3888-1 does not readily support voltage-based off-sequencing. Refer to the Applications Information section for more details on voltage-based sequencing.

### OUTPUT DISABLE

All PWMs on the IC are disabled any time $V_{IN}$ is below the VIN_OFF threshold. The power stages are immediately shut off to stop the transfer of energy to the load(s) as quickly as possible.

PWM channels may also be disabled in response to certain internal fault conditions, an external fault propagated through a $\overline{\text{FAULT}}$ pin, or loss of SHARE_CLK. In these cases the power stages are immediately commanded off to stop the transfer of energy to the load as quickly as possible. Refer to the following Fault Detection and Handling section for additional details related to fault recovery.

Each rail can be disabled with an OPERATION command at any time if enabled by ON_OFF_CONFIG. This will force

## OPERATION

a controlled turn-off response with defined delay (TOFF_DELAY) and ramp down rate (VOUT_TRANSITION_RATE).

Finally, each rail can be commanded off by pulling the associated RUN pin low. Pulling the RUN pin low can force the master to perform a controlled turn off or immediately disable all rail power stages, depending on the programming of ON_OFF_CONFIG.

### Minimum Output Disable Times

When OPERATION is used to turn off an LTC3888-1 rail, a minimum output disable time of 120ms is imposed regardless of how quickly the rail is commanded back on. If bit 4 of MFR_CHAN_CONFIG is clear, a PMBus command to turn the channel off also pulses the RUN pin low. Once the RUN pin is pulled low internally or externally, a minimum output disable time (RUN forced low by the LTC3888-1) of TOFF_DELAY + $V_{OUT}$/VOUT_TRANSITION_RATE + 136ms is enforced. If MFR_RESTART_DELAY is greater than this mandatory minimum, the larger value of MFR_RESTART_DELAY is used. These minimum off times allow a consistent rail restart with coherent monitor ADC values and make the LTC3888-1 highly compatible with other ADI PMBus digital power system management products.

### OUTPUT SHORT CYCLE

An output short cycle condition is created when a master channel is commanded back on while waiting for controlled turn off to complete based on TOFF_DELAY and VOUT_TRANSITION_RATE. Any time this occurs, the LTC3888-1 asserts the short cycle bit in STATUS_MFR_SPECIFIC. Device response at that point is governed by bits in MFR_CHAN_CONFIG and SMBALERT_MASK. Refer to the detailed descriptions of those commands for additional details. Generally, the LTC3888-1 should be controlled so that short cycle conditions are not created during normal operation.

### SWITCHING FREQUENCY AND PHASE

There is a high degree of flexibility for setting the PWM operating frequency of the LTC3888-1. The switching frequency of the PWM can be established with an internal oscillator or an external time base. The internal phase-locked loop (PLL) synchronizes PWM control to this timing reference with proper phase relation. The device can also be configured to provide the master clock (SYNC) to other ICs through PMBus command or EEPROM setting. The LTC3888-1 is designated as a clock master by clearing bit 4 of MFR_CONFIG_ALL. As clock master, the LTC3888-1 will drive its open-drain SYNC pin at the selected rate with a pulse width of 500ns. An external pull-up resistor between SYNC and $V_{DD33}$ is required in this case. Only one device connected to SYNC should be designated to drive the pin. If more than one LTC3888-1 sharing SYNC is programmed as clock master, just one of the devices is automatically elected to provide the clock. The others disable their SYNC outputs and indicate this with bit 10 of MFR_PADS_LTC3888-1.

The LTC3888-1 will automatically accept an external SYNC input, disabling is own SYNC drive if necessary, as long as the external clock frequency is greater than one-half of the programmed internal oscillator. Whether configured to drive SYNC or not, the LTC3888-1 will continue PWM operation at the selected frequency (FREQUENCY_SWITCH) using its own internal oscillator if an external clock signal is subsequently lost.

The MFR_PWM_CONFIG_LTC3888-1 command can be used to create a specific master/slave configuration and assign the phase of each channel. Desired master/slave arrangement can also be set from EEPROM or external configuration resistors as outlined in Table 11. Phase designates the relationship between the falling edge of SYNC and the internal clock edge that sets the PWM latch for that channel. Additional small propagation delays to the PWM control pins will apply.

## OPERATION

PWM phase relationships and frequency are independent of each other, providing numerous application options. Multiple LTC3888-1 ICs can be synchronized to realize a PolyPhase array. Two LTC3888-1 devices can be combined to expand phase count while maintaining ideal phase separation of 360/n degrees, where n is the number of phases driving the output voltage rail. Refer to the Applications Information section for additional details.

### POLYPHASE LOAD SHARING

Multiple LTC3888-1 devices can be combined to provide a balanced load-share solution by configuring the necessary pins. The SHARE_CLK and SYNC pins of all load-sharing ICs should be bussed together. Connecting the SYNC pins synchronizes the PWM controllers with each other. Bussing the SHARE_CLK pins together allows the phases to start synchronously. Refer to the discussion in the previous Power-Up and Initialization section. The last device to see all start-up conditions satisfied controls the initiation of power sequencing for all phases.

The outputs of multiple LTC3888-1 error amplifiers ($I_{TH}$ pins) may be wired together in large PolyPhase applications if $V_{OUT}$ sensing for those channels is also shared. The error amplifier of only one master phase can also be designated for voltage control by redefining any remaining master phases as slaves using bit 4 of MFR_PWM_MODE_LTC3888-1. Additional details for properly constructing various PolyPhase designs are covered in the Applications Information section.

### VOLTAGE CONTROL LOOP COMPENSATION

Because the LTC3888-1 uses an operational transconductance amplifier (OTA) architecture for its error amplifier, Type II compensation is most commonly applied for stabilizing the voltage control loop. The LTC3888-1 offers several programmable features for flexability in designing and operating the PWM with optimum transient behavior over a wide range of output capacitance without additional hardware changes.

Bits[4:0] of MFR_PWM_COMP adjust an internal resistor which can be used to set the dominant zero against the primary compensation capacitance. This resistance appears between the $I_{TH}$ and $I_{THR}$ pins.

The transconductance of the error amplifier itself can also be adjusted using bits[7:5] of MFR_PWM_COMP.

Both of these parameters can be modified when the device is in operation, affording real-time evaluation of compensation settings. Refer to the Applications Information secton for additional details related to loop compensation.

### LOAD STEP EMULATION

Basic assembly integrity, PWM regulator loop response, and passive component aging or thermal degredation are best evaluated by analyzing load current transient response. The LTC3888-1 features a flexible load step emulation capability that allows in-situ transient response evaluation without the need to actually generate and apply large, regulated load current pulses at the regulator output. These features can find use in the design, debug, prototyping and preventative maintenence phases of a product life cycle.

Load step emulation is controlled by MFR_LOAD_EMULATION. All phases associated with each master channel can be programmed to emulate a load step of known amplitude (bits[1:0]). Bit 2 of the command determines whether the emulated load is applied as a continuous increase or as a 100µs pulse. Because internal application of data from a PMBus command is an asynchronous event, bit 3 of the command allows the PGOOD output to be repurposed to provide a trigger at the actual start of the emulated load step, if necessary.

### INPUT SUPPLY MONITORING

The input supply voltage is sensed by the LTC3888-1 at the $V_{IN}$ pin. Undervoltage, overvoltage, and valid on/off levels can be programmed for $V_{IN}$. Refer to the following PMBus Command Details section for more information on programming input supply thresholds. In addition, the telemetry ADC monitors $V_{IN}$ relative to GND. Conversion results are returned by READ_VIN.

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## OUTPUT VOLTAGE SENSING AND MONITORING

Both on-chip voltage control loops allow remote, differential sensing of the load voltage with $V_{SENSE}^{\pm}$ pins. The DAOUT0/1 outputs provide a 1X buffered version of this sensed differential referenced to package GND. These outputs are suitable for driving a resistor divider to GND supplying $V_{FB}$ to set the desired output voltage.

$V_{OUT}$ supervisor UV and OV fault limits are set from EEPROM or PMBus command. Factory EEPROM sets the supervisor limits and margin values as a percentage of $V_{FB}$ and hence $V_{OUT}$. If these are modified by PMBus command, they are specified in absolute volts.

The telemetry ADC is also fully differential and makes measurements of regulated output voltages at $V_{SENSE}^{\pm}$. Conversion results are returned by READ_VOUT.

## OUTPUT CURRENT SENSING AND MONITORING

Every PWM channel on the LTC3888-1 accepts an output current monitor signal from the power stage it controls. A proprietary input interface uses this information to control output pulse width on that phase. When the $I_{SENSE}$ pins for a channel are multiplexed to the differential inputs of the LTC3888-1 monitor ADC, they use IREF as the negative input. These ADC channels have a differential input range of approximately ±400mVdc. The internal ADC anti-aliasing filter and conversion rate produce an average reading of the $I_{SENSE}$ input voltage relative to IREF. The resulting value is returned by the READ_IOUT PMBus command. To allow reduction in round-robin latency, bit 6 of MFR_PWM_CONFIG_LTC3888-1 determines if the ADC converts $I_{SENSE}$ for all eight phases, or only the two master channels. If only $I_{SENSE0}$ and $I_{SENSE1}$ are monitored, the IOUT results for the remaining six channels are set to 0A. READ_IOUT returns readings for the two master channels, MFR_TOTAL_IOUT returns the sum of all output currents for on-chip phases assigned to each master channel, and MFR_READ_ALL_IOUT returns output current for each individual phase using block read format.

## TEMPERATURE SENSE

External temperature can be monitored by most modern power stages. This is normally presented on a highest-indicated wire-OR analog bus for each rail, where the device with highest internal temperature sets the bus voltage. The internal ADC converts these temperature inputs at one-third the rate of voltage or current channels, and those results are returned by READ_TEMPERATURE_1. READ_TEMPERATURE_2 returns the internal junction temperature of the LTC3888-1 using an on-chip diode with accurate $\Delta V_{BE}$ measurement and calculation.

## RESISTOR CONFIGURATION PINS

Six input pins can be used to configure key operating parameters with selected 1% resistors between each pin and GND. $R_{SET}$ establishes the proper bias levels for the remaining five pins and requires an 18.7kΩ resistor to GND. The remaining RCONFIG pins are ASEL0, ASEL1, ILIM0_CFG, ILIM1_CFG, and PWM_CFG. If any of these five pins are left open, the value stored in the corresponding EEPROM command(s) is used. The resistor configuration pins are only measured during power-up and execution of RESTORE_USER_ALL or MFR_RESET. If bit 6 of MFR_CONFIG_ALL is set in EEPROM, all resistor configuration pins except ASEL0 and ASEL1 are ignored. Per the PMBus specification, all pin-programmed parameters can be overridden at any time by commands from the digital interface.

The ASEL0/1 pin settings are described in application Table 12. These pins can be used to select the entire LTC3888-1 device address. ASEL0 always programs the bottom four bits of the device address for the LTC3888-1 unless left open. ASEL1 can be used to program the three most-significant bits. Either portion of the address can also be retrieved from the MFR_ADDRESS value in EEPROM. If both pins are left open, the full 7-bit MFR_ADDRESS value stored in EEPROM is used to determine the device address. The LTC3888-1 always responds to 7-bit global addresses 0x5A and 0x5B. MFR_ADDRESS should not be set to either of these values or 0x7C.

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The ILIM0_CFG and ILIM1_CFG pin settings are described in application Table 10. These pins select the per-phase output current limit for each related rail.

PWM_CFG pin settings are described in application Table 11. This pin selects the master/slave configurnation and switching frequency of the internal oscillator.

### INTERNAL EEPROM WITH CRC

The LTC3888-1 contains internal EEPROM with error correction code (ECC) to store user configuration settings and fault log information. EEPROM endurance and retention for user space and fault log pages are specified in the Absolute Maximum Ratings and Electrical Characteristics table.

The integrity of the entire onboard EEPROM is checked with a CRC calculation each time its data is to be read, such as after a power-on reset or execution of RESTORE_USER_ALL. If a CRC error occurs, the CML bit is set in STATUS_BYTE and STATUS_WORD, the EEPROM CRC Error bit in STATUS_MFR_SPECIFIC is set, and the $\overline{\text{ALERT}}$, SHARE_CLK and RUN pins are pulled low (PWM channels off). At that point the device will respond at special address 0x7C, which is activated after an invalid CRC has been detected. The chip no longer responds at its specifically assigned address, but will still respond at global addresses 0x5A and 0x5B. However, use of these global addresses when attempting to recover from a CRC issue is not recommended. All power supply rails associated with a device reporting an invalid CRC should remain disabled until the issue is resolved.

ADI recommends that the EEPROM not be written when die temperature is greater than 85°C. If internal die temperature exceeds 130°C, all EEPROM operations except RESTORE_USER_ALL and MFR_RESET are disabled. Full EEPROM operation is not re-enabled until die temperature falls below 125°C. Refer to the Applications Information section for equations to predict retention degradation due to elevated operating temperatures.

See the Applications Information section or contact the factory for details on efficient in-system EEPROM programming, including bulk EEPROM programming, which the LTC3888-1 also supports.

### FAULT DETECTION

A variety of fault and warning detection, reporting and handling mechanisms are provided by the LTC3888-1. Fault or warning detection capabilities include:

- Input Under/Overvoltage
- Power Stage UV or Fault
- Output Under/Overvoltage
- Output Overcurrent
- External Overtemperature
- Internal Overtemperature
- CML Fault (Communication, Memory, or Logic)
- External Fault Detection via Bidirectional $\overline{\text{FAULT}}$ Pins

Reporting is covered in following sections on status commands (registers) and $\overline{\text{ALERT}}$ pin function. Fault handling mechanisms include hardwired low level PWM safety responses that always occur and higher-level programmable event management. Both types are covered in the following sections.

#### Input Supply Faults

Input undervoltage and overvoltage limits are determined from multiplexed monitor ADC conversions. Therefore the input UV/OV response is naturally deglitched by the typical conversion cycle of the ADC (tens of milliseconds). There is no hardwired low level PWM response for any input supply fault.

#### Hardwired PWM Response to Power Stage Faults

Power stage faults are monitored on the shared TEMP/FAULT bus attached to an LTC3888-1 TSNS pin. A power stage fault condition is detected if this bus is pulled above any voltage expected for normal operating temperature range. The specific faults that are reported are determined by the power stage manufacturer. When a power stage fault is detected, the master and its associated slave channels are all commanded off. This state is indicated in the LTC3888-1 status registers and optionally on the $\overline{\text{ALERT}}$ pin. The off condition is latched until the rail is turned off

## OPERATION

and then back on by the RUN pin or OPERATION command, including IC reset or power supply cycling.

### Hardwired PWM Response to Power Stage UV

Some power stages can also report a undervoltage condition for their input supplies on the shared TEMP/FAULT bus. When supported, this condition is indicated by pulling the bus below any voltage expected for normal operating temperature range. The LTC3888-1 recognizes this UV indication if enabled by bit 0 of MFR_PWM_MODE_LTC3888-1.

If the power stage does not provide inherent UV indication on a shared TEMP/FAULT bus, the LTC3888-1 can be programmed to provide additional power stage undervoltage detection by setting bit 5 of MFR_CHAN_CONFIG on Page 0. Pin 8 is then converted to a VDR_MON input to monitor the FET gate drive supply voltage (VDR) of the external power stages for both master channels. Normally an external resistor divider to set the desired UV threshold is required. In this case TSNS1 serves as connection for the shared TEMP/FAULT bus for both master channels with UV detection disabled, regardless of the state of bit 0 of MFR_PWM_MODE_LTC3888-1 on either page.

When TSNS-based UV detection or VDR_MON are enabled, power stage UV condition is continuously indicated in bits[15:14] of MFR_PADS_LTC3888-1. If a power stage UV condition then occurs during PWM operation or is present when the PWM master is commanded to start, the master and its associated slave channels are all latched off. This state is indicated in the LTC3888-1 status registers and optionally on the $\overline{\text{ALERT}}$ pin. The off condition is latched until the rail is turned off and then back on by the RUN pin or OPERATION command, including IC reset or power supply cycling.

Note that if an enabled power stage UV indication exists on both master channels that are sequentially turned on by RUN pin or OPERATION command, the indicated fault on the first channel on will be cleared if bit 0 of MFR_CONFIG_ALL is set. However, both channels will be latched off as described above.

### Hardwired PWM Response to $V_{OUT}$ Faults

$V_{OUT}$ undervoltage (UV) and overvoltage (OV) faults are detected by supervisor comparators. The output overvoltage comparator guards against transient overshoots as well as long term overvoltages at the output. When an output OV fault is detected, the state is indicated in the LTC3888-1 status registers and optionally on the $\overline{\text{ALERT}}$ pin. The master and its associated slave channels are all commanded off, unless bit 4 of MFR_PWM_CONFIG_LTC3888-1 is set and bit 4 in the associated MFR_PWM_MODE_LTC3888-1 command is clear. In that special case the master phase of the OV rail commands its power stage to drive low as long as the OV condition is detected. Regardless, the off condition is latched until the rail is cycled off and then back on after the fault has cleared.

UV faults are masked if the channel has been commanded off or until all of the following criteria are achieved.

- TON_DELAY Has Expired
- The Soft-Start Ramp Has Completed
- TON_MAX_FAULT_LIMIT Has Been Reached
- IOUT_OC_FAULT_LIMIT Has Not Been Reached
- Soft-Off Is Not in Progress

The LTC3888-1 has no hardwired PWM response for output UV faults.

The LTC3888-1 supports optional output UV and OV warnings that are determined from multiplexed monitor ADC conversions. The LTC3888-1 has no hardwired PWM response for output UV or OV warnings.

### Power Good Indication

An LTC3888-1 master phase indicates Power Good on its PGOOD pin and in STATUS_WORD based on selected UV and OV fault limits. Power Good is indicated as long as the phase is enabled to run and $V_{OUT}$ is between the UV and OV fault limits.

### Hardwired PWM Response to $I_{OUT}$ Faults

The LTC3888-1 monitors output current as commanded by the $I_{TH}$ pins, taking into account power stage current monitor gain, which is provided by PMBus command or EEPROM values.

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An output overcurrent (OC) fault condition is detected by a supervisor comparator for each master channel when the $I_{TH}$ voltage for that channel reaches its maximum allowed value. Refer to IOUT_OC_FAULT_LIMIT for details. When an OC fault is detected the controller clamps $I_{TH}$ at the OC value.

Output OC warnings are determined from multiplexed monitor ADC conversions. The LTC3888-1 has no hardwired PWM response if an output OC warning occurs.

### Hardwired PWM Response to Internal Temperature Faults

An internal temperature sensor measured by the monitor ADC protects against EEPROM and other IC damage. When die temperature rises above 130°C, the LTC3888-1 will NACK any EEPROM-related command except RESTORE_USER_ALL and MFR_RESET and issue a CML fault for Invalid/Unsupported Command. Normal EEPROM access is re-enabled when die temperature drops below 125°C. Above 160°C, the part shuts down all PWM outputs until die temperature is below 150°C. Internal temperature fault limits cannot be adjusted. Writing to the EEPROM above a die temperature of 85°C is strongly discouraged. Refer to the Absolute Maximum Ratings for other important temperature limitations on internal EEPROM use.

### External Temperature Faults

The external shared (wire-OR) power stage temperature bus may also be monitored by the onboard ADC. There is no hardwired PWM response for sensed external temperature faults or warnings.

### Timing Faults

There is no hardwired PWM response to any timing faults.

TON_MAX_FAULT_LIMIT is the time allowed for $V_{OUT}$ to rise and settle at start-up. The TON_MAX_FAULT_LIMIT timer, which has a resolution of 10µs, is started after TON_DELAY has been reached and a soft-start sequence is started. If the VOUT_UV_FAULT_LIMIT is not reached or an OC fault remains after the specified time, fault response is determined by the value of TON_MAX_FAULT_RESPONSE.

An internal watchdog detects if SHARE_CLK remains low for more than 64µs. The part then actively holds SHARE_CLK low for 120ms, ensuring all devices connected to this shared control observe a minimum RETRY_DELAY event. The LTC3888-1 sets the SHARE_CLK_LOW bit in MFR_COMMON to indicate this fault condition.

### External Faults

There are no hardware-level responses to any external faults propagated into the IC through the $\overline{\text{FAULT}}$ pins.

### HIGHER-LEVEL FAULT HANDLING

Higher-level input and output fault event handling (response) can be programmed as described in the following PMBus Command Details section. Once a fault is detected, several tens of microseconds may be required for these higher level responses to occur, including related assertion of a $\overline{\text{FAULT}}$ output. Time filtering programmed in any specific fault response will be in addition to these normal processing delays. For many faults, the LTC3888-1 can manage response in one of three ways: ignore, autonomous recovery (hiccup), or latch off. The device takes no additional action beyond previously discussed hardware-level responses when programmed to ignore a fault.

For autonomous recovery a new soft-start is attempted if the fault condition is not present after the MFR_RETRY_DELAY interval has elapsed. MFR_RETRY_DELAY can be set from 120ms to 83 seconds in 1ms increments. If the fault persists, the controller will continue to retry with an interval specified by MFR_RETRY_DELAY. This avoids damage to external regulator components caused by repetitive, rapid power cycling.

No retry is attempted for a latch off fault response. In the latch off state the applicable external power stages are immediately disabled to stop the transfer of energy to the load as quickly as possible. The output remains disabled until the master channel is commanded off and then on, or IC supply power is cycled. Commanding a PWM channel off and on may require software and/or hardware intervention depending on its programmed configuration.

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The RUN pin must be released by any controlling external application circuits for that channel to restart from the latch off state. As the RUN pin for a given rail rises, associated internal fault indications are cleared automatically. The LTC3888-1 can also be programmed to clear faults for both master channels based solely on the run state of just one channel. See the MFR_CONFIG_ALL command. CLEAR_FAULTS can also be used to clear all fault bits at any time, independent of PWM channel state.

Higher-level handling of some internally generated faults can be digitally deglitched. External faults propagated into the chip using $\overline{\text{FAULT}}$ pins are not deglitched. Refer to the following section on $\overline{\text{FAULT}}$ Pin I/O.

### STATUS REGISTERS AND $\overline{\text{ALERT}}$ MASKING

Figure 2 summarizes the internal LTC3888-1 status registers accessible by PMBus command. These contain indication of various faults, warnings and other important operating conditions. As shown, STATUS_BYTE and STATUS_WORD also summarize contents of other status registers. Refer to PMBus Command Details for specific information.

NONE OF THE ABOVE in STATUS_BYTE indicates that one or more of the bits in the most-significant nibble of STATUS_WORD are also set.

Figure 2 also shows which of the status bits will assert $\overline{\text{ALERT}}$ if set and not masked. Once set, $\overline{\text{ALERT}}$ will remain low until one of the following occurs.

- A CLEAR_FAULTS, RESTORE_USER_ALL or MFR_RESET Command Is Issued
- The Related Status Bit Is Written to a One
- The Faulted Channel Is Properly Commanded Off and Back On
- The LTC3888-1 Successfully Transmits Its Address During a PMBus Alert Response Address (ARA)
- IC Supply Power Is Cycled

With some exceptions, the SMBALERT_MASK command can be used to prevent the LTC3888-1 from asserting $\overline{\text{ALERT}}$ on a bit-by-bit basis by register. These mask settings are promoted to STATUS_WORD and STATUS_BYTE in the same fashion as the status bits themselves. For example, if $\overline{\text{ALERT}}$ is masked for all bits in Channel 0 STATUS_VOUT, then $\overline{\text{ALERT}}$ is effectively masked for the VOUT bit in STATUS_WORD for PAGE 0.

The BUSY bit in STATUS_BYTE also asserts $\overline{\text{ALERT}}$ and cannot be masked. This bit can be set as a result of interaction between internal operations and PMBus communication. This fault occurs when a command is received that cannot be safely executed with one or both master channels enabled. As discussed in Application Information, BUSY faults can be avoided by polling MFR_COMMON before executing some commands.

Status information contained in MFR_COMMON and MFR_PADS_LTC3888-1 can be used to clarify the contents of STATUS_BYTE or STATUS_WORD as shown, but the contents of these registers do not affect the state of the $\overline{\text{ALERT}}$ pin and may not directly influence bits in STATUS_BYTE or STATUS_WORD.

### $\overline{\text{FAULT}}$ PIN I/O

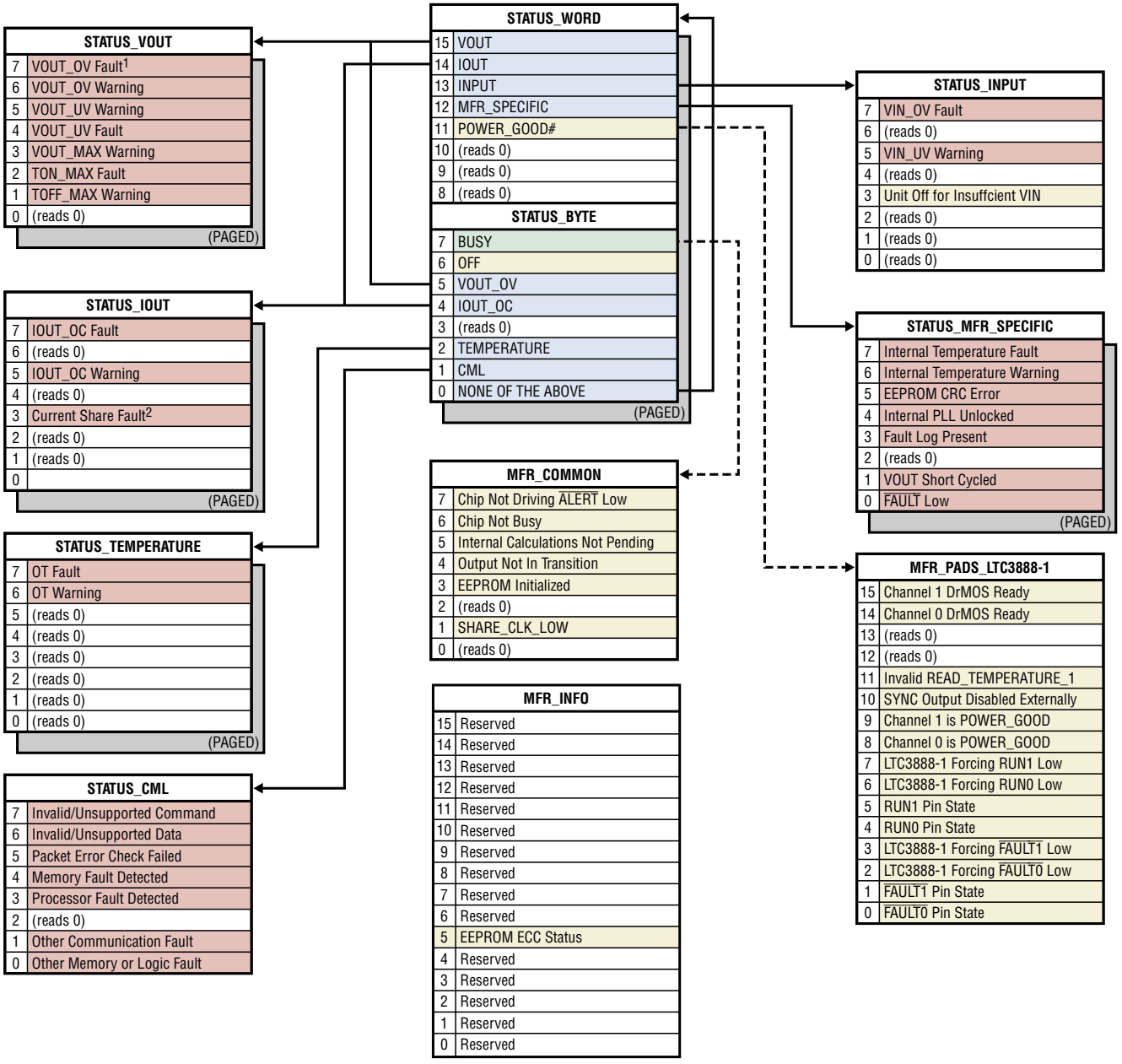
The LTC3888-1 can map various fault indicators to their respective $\overline{\text{FAULT}}$ pin using the MFR_FAULT_PROPAGATE command.

Channel-to-channel fault dependencies and communication can be created by connecting $\overline{\text{FAULT}}$ pins together. In the event of an internal fault, one or more of the channels is configured to pull the bussed $\overline{\text{FAULT}}$ pins low. All channels are then configured to shut down when the bussed $\overline{\text{FAULT}}$ pins are pulled low (MFR_FAULT_RESPONSE set to 0xC0). If latch off is the programmed response on the faulted channel, the $\overline{\text{FAULT}}$ pin remains low until one of the following occurs:

- A CLEAR_FAULTS, RESTORE_USER_ALL or MFR_RESET Command Is Issued
- The Related Status Bit Is Written to a One
- The Faulted Channel Is Properly Commanded Off and Back On
- IC Supply Power Is Cycled

For autonomous group retry, the faulted channel is configured to release the $\overline{\text{FAULT}}$ pin(s) after a retry interval,

## OPERATION




| DESCRIPTION | MASKABLE | GENERATES ALERT | BIT CLEARABLE |
|---|---|---|---|
| General Fault or Warning Event | Yes | Yes | Yes |
| General Non-Maskable Event | No | Yes | Yes |
| Dynamic | No | No | No |
| Status Derived from Other Bits | No | Not Directly | No |

[1]Set by VOUT_OV, DrMOS (power stage) fault or DrMOS UVLO during RUN
[2]Set only by detected power stage fault

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**Figure 2. LTC3888-1 Status Register Summary**

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assuming the original fault has cleared. All the channels in the group then begin a soft-start sequence.

As noted above, $\overline{\text{FAULT}}$ pins can also find use as inputs to detect faults external to the controller that require an immediate response. External faults propagated into the chip using $\overline{\text{FAULT}}$ pins are not deglitched.

Refer to MFR_FAULT_PROPAGATE for additional details.

### FAULT LOG OPERATION

The LTC3888-1 supports fault logging to provide telemetry recording capability. A conceptual diagram of the fault log is shown in Figure 3. During normal operation the contents of primary status registers and all ADC readings, including peak voltage and current results, are stored in a continuously updated RAM buffer if enabled by bit 7 of MFR_CONFIG_ALL. The operation is similar to a strip recorder. When a fault occurs that disables either master channel, recording to internal memory is halted (locked) and the fault log information is made available from RAM via the MFR_FAULT_LOG command. Some contents of the locked RAM fault log are also copied into EEPROM for nonvolatile storage. See Fault Log Details below.

A fault log write to EEPROM is allowed above a die temperature of 85°C, but 10 years of retention is not guaranteed. When die temperature exceeds 130°C, any EEPROM fault log storage is delayed until the temperature drops below 125°C.

Once created, a fault log cannot be overwritten by subsequent fault events, even if the log is only partial. An MFR_FAULT_LOG_CLEAR command must be executed to erase an existing log, leaving the IC free to generate a new one.

Faults propagated into the IC through $\overline{\text{FAULT}}$ pins do not trigger a fault logging event, regardless of their impact on PWM operation. Faults that generate a fault log should be fully cleared before the log is erased to prevent creation of spurious fault logs.

When the LTC3888-1 powers up it checks the EEPROM for a valid fault log. If one is found the Fault Log Present bit in STATUS_MFR_SPECIFIC is set. If the Memory Fault Detected bit is also set in STATUS_CML, then the stored fault log is partial. Data in one or more event records may be incomplete or incorrect.

### Fault Log Details

The MFR_FAULT_LOG command uses a block read protocol with a fixed length of 147 bytes. The LTC3888-1 returns a block byte count of zero if a fault log is not present.

Contents of a fault log are shown in Table 1 through Table 4. Refer to Table 6 for an explanation of data formats. Each event record represents one complete conversion cycle through all multiplexed monitor ADC inputs and related status. When a fault log is created the present ADC input cycle is completed and the ADC input being converted at the time of the fault is noted in the log header. Referring to Figure 3, the six most recent event records are maintained in internal RAM in reverse chronological order. If input power is cycled or the part is reset after a fault log is creatred, the RAM record is restored from EEPROM where only the four most recent events are retained due to available storage.

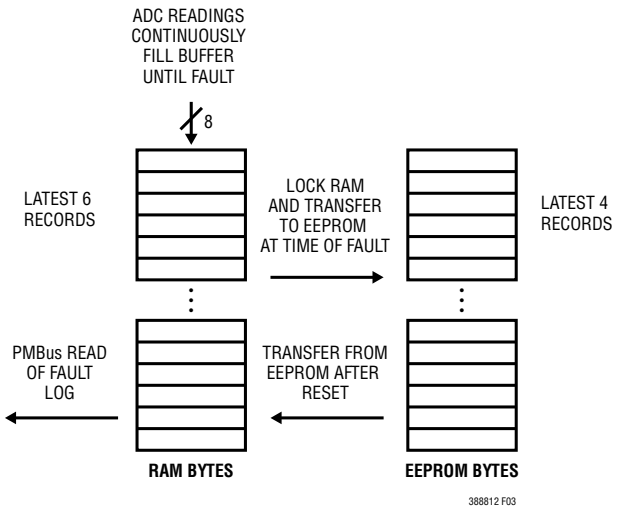


**Figure 3. Fault Log Conceptual Diagram**

# OPERATION

**Table 1. LTC3888-1 Fault Log Contents**

| RECORD TYPE | STARTING BYTE | ENDING BYTE | COMMENTS |
|---|---|---|---|
| Header Information | 0 | 26 | See Table 2. |
| Fault Event Record | 27 | 46 | Fault may have occurred anywhere during this event record. See byte 4 of Table 2 and all of Table 3 and Table 4. |
| Event Record N-1 | 47 | 66 | Last complete cyclical data read before the fault was detected. |
| Event Record N-2 | 67 | 86 | Older data records… |
| Event Record N-3 | 87 | 106 | |
| Event Record N-4 | 107 | 126 | |
| Event Record N-5 | 127 | 146 | Oldest recorded data. |

**Table 2. Fault Log Header Information**

| RECORD | BITS | FORMAT | BLOCK BYTE COUNT | DETAILS |
|---|---|---|---|---|
| Fault Log Preface | [7:0] | ASC | 0 | Returns LTxx beginning at byte 0 if a partial or complete fault log exists. Word xx is a factory identifier that may vary part to part. |
| | [7:0] | | 1 | |
| | [15:8] | Reg | 2 | |
| | [7:0] | | 3 | |
| Fault Source | [7:0] | Reg | 4 | Refer to Table 3. |
| MFR_REAL_TIME | [7:0] | Reg | 5 | 48 bit share-clock counter value when fault occurred (200µs resolution). |
| | [15:8] | | 6 | |
| | [23:16] | | 7 | |
| | [31:24] | | 8 | |
| | [39:32] | | 9 | |
| | [47:40] | | 10 | |
| MFR_VOUT_PEAK (PAGE 0) | [15:8] | L16 | 11 | Peak READ_VOUT on Channel 0 since last power-on or CLEAR_PEAKS command. |
| | [7:0] | | 12 | |
| MFR_VOUT_PEAK (PAGE 1) | [15:8] | L16 | 13 | Peak READ_VOUT on Channel 1 since last power-on or CLEAR_PEAKS command. |
| | [7:0] | | 14 | |
| MFR_IOUT_PEAK (PAGE 0) | [15:8] | L11 | 15 | Peak READ_IOUT on Channel 0 since last power-on or CLEAR_PEAKS command. |
| | [7:0] | | 16 | |
| MFR_IOUT_PEAK (PAGE 1) | [15:8] | L11 | 17 | Peak READ_IOUT on Channel 1 since last power-on or CLEAR_PEAKS command. |
| | [7:0] | | 18 | |
| MFR_VIN_PEAK | [15:8] | L11 | 19 | Peak READ_VIN since last power-on or CLEAR_PEAKS command. |
| | [7:0] | | 20 | |
| READ_TEMPERATURE1 (PAGE 0) | [15:8] | L11 | 21 | External temperature sensor 0 during last event. |
| | [7:0] | | 22 | |
| READ_TEMPERATURE1 (PAGE 1) | [15:8] | L11 | 23 | External temperature sensor 1 during last event. |
| | [7:0] | | 24 | |
| READ_TEMPERATURE2 | [15:8] | L11 | 25 | Internal temperature sensor during last event. |
| | [7:0] | | 26 | |

# OPERATION

**Table 3. Fault Source Values**

| FAULT SOURCE VALUE | CAUSE OF FAULT LOG | CHANNEL |
|---|---|---|
| 0x00 | TON_MAX | 0 |
| 0x01 | VOUT_OV | |
| 0x02 | VOUT_UV | |
| 0x03 | IOUT_OC | |
| 0x05 | Over Temperature | |
| 0x07 | VIN_OV | |
| 0x0A | Internal Temperature | |
| 0x10 | TON_MAX | 1 |
| 0x11 | VOUT_OV | |
| 0x12 | VOUT_UV | |
| 0x13 | IOUT_OC | |
| 0x15 | Over Temperature | |
| 0x17 | VIN_OV | |
| 0x1A | Internal Temperature | |
| 0xFF | MFR_FAULT_LOG_STORE | |

**Table 4. Fault Log Event Record**

| DATA | BITS | FORMAT | RECORD BYTE INDEX |
|---|---|---|---|
| READ_VOUT (PAGE 0) | [15:8] | L16 | 0 |
| | [7:0] | | 1 |
| READ_VOUT (PAGE 1) | [15:8] | L16 | 2 |
| | [7:0] | | 3 |
| MFR_TOTAL_IOUT (PAGE 0) | [15:8] | L11 | 4 |
| | [7:0] | | 5 |
| MFR_TOTAL_IOUT (PAGE 1) | [15:8] | L11 | 6 |
| | [7:0] | | 7 |
| READ_VIN | [15:8] | L11 | 8 |
| | [7:0] | | 9 |
| (Not used) | [15:8] | L11 | 10 |
| | [7:0] | | 11 |
| STATUS_VOUT (PAGE 0) | [7:0] | Reg | 12 |
| STATUS_VOUT (PAGE 1) | [7:0] | Reg | 13 |
| STATUS_WORD (PAGE 0) | [15:8] | Reg | 14 |
| | [7:0] | | 15 |
| STATUS_WORD (PAGE 1) | [15:8] | Reg | 16 |
| | [7:0] | | 17 |
| STATUS_MFR_SPECIFIC (PAGE 0) | [7:0] | Reg | 18 |
| STATUS_MFR_SPECIFIC (PAGE 1) | [7:0] | Reg | 19 |

# OPERATION

## FACTORY DEFAULT OPERATION

The LTC3888-1 ships from the factory with a default configuration stored in its non-volatile memory unless custom programming has been requested. These command values are loaded into volatile RAM when the chip is initialized. Prior to receiving any PMBus commands, a stock LTC3888-1 will operate in the factory default mode. If a STORE_USER_ALL command is executed, the contents of the non-volatile memory are replaced with active command values from internal RAM, and that will permanently overwrite the factory defaults. Table 5 summarizes the default factory operation settings of the LTC3888-1 if all resistor configuration pins are left open. These defaults allow parameters listed in bold text in the table to be overridden with configuration resistor programming. Warning limits are given in Table 5 because exceeding them will cause the $\overline{\text{ALERT}}$ pin to be asserted even if the PMBus interface is not being utilized.

**Table 5. Factory Default Operation Summary**

| PARAMETER* | DEFAULT SETTING | UNITS |
|---|---|---|
| **PMBus Address** | All writes enabled to Channel 0 at address 0x4F (no PEC). | – |
| Operation | OPERATION enabled with RUN pin control and soft-off. | – |
| Input Voltage OFF Threshold | 6.0 | V |
| Input Voltage UV Warning Limit | 6.3 | V |
| Input Voltage ON Threshold | 6.5 | V |
| Input Voltage OV Fault Limit | 15.5 | V |
| Input Voltage OV Fault Response | Latch off | – |
| Soft-Start Time | 1.6 (with no delay) | ms |
| Maximum Start-Up Time (TMAX) | 10 | ms |
| TMAX Fault Response | Retry every 350ms | – |
| Output Voltage UV Fault Limit | –10% of nominal $V_{OUT}$ | – |
| Output Voltage UV Fault Response | Retry every 350ms | – |
| Output Voltage | Set by external R-divider ($V_{FB}$ = 400mV, $V_{OUT}$ servo disabled) | – |
| Output Voltage OV Fault Limit | 10% of nominal $V_{OUT}$ | – |
| Output Voltage OV Fault Response | Latch off | – |
| Shut Down | 1.6ms soft-off | – |
| Output Current Monitor Gain | 5.0 | mΩ |
| **Output Current OC Warning/Fault Limits** | 20/29.75 | A |
| Output Current OC Fault Response | Ignore | – |
| **PWM Switching Frequency** | 500 | kHz |
| **Master/Slave Configuration** | 4+4 (or 8-phase) | – |
| Internal Overtemperature Warning/Fault Limits | 130/160 | °C |
| Internal Overtemperature Responses | Warning: EEPROM disabled; Fault: PWM disabled | – |
| External Overtemperature Warning/Fault Limits | 85/100 | °C |
| External Overtemperature Fault Response | Retry every 350ms | – |
| $\overline{\text{FAULT}}$ | Asserts low for the following faults: $V_{OUT}$ UV or OV, $V_{IN}$ OV, external or internal OT, TON_MAX, or output short cycle | – |
| $\overline{\text{ALERT}}$ Masking | Masked for loss of PLL lock and external fault inputs | – |

*Bold entries can be changed with external configuration resistors

# OPERATION

## SERIAL INTERFACE

The LTC3888-1 has a PMBus compliant serial interface that can operate at any frequency between 10kHz and 400kHz. The LTC3888-1 is a bus slave device that communicates bidirectionally with a host (master) using standard PMBus protocols. The Timing Diagram found earlier in this document, along with related Electrical Characteristics table entries, define the timing relationships of the SDA and SCL bus signals. SDA and SCL must be high when the bus is not in use. External pull-up resistors or current sources are required on these lines.

PMBus, an incremental extension of the SMBus standard, offers more robust operation than a 2-wire $I^2C$ interface. In addition to adding a protocol layer to improve interoperability and facilitate reuse, PMBus supports bus timeout recovery for system reliability, optional packet error checking (PEC) to ensure data integrity, and peripheral hardware alerts for system fault management. In general, a programmable device capable of functioning as an $I^2C$ bus master can be configured for PMBus management with little or no change to hardware. However, not all $I^2C$ controllers support repeat start (restart) required for PMBus reads.

For a description of the minor extensions and exceptions PMBus makes to the SMBus standard, refer to PMBus Specification Part I Revision 1.2 Paragraph 5 on Transport.

For a description of the differences between SMBus and $I^2C$, refer to System Management Bus (SMBus) Specification Version 2.0 Appendix B on Differences Between SMBus and $I^2C$.

The user is encouraged to reference Part I of the latest PMBus Power System Management Protocol Specification to understand how to interface the LTC3888-1 to a PMBus system. This specification can be found at http://www.pmbus.org/specs.html.

The LTC3888-1 uses the following standard serial interface protocols defined in the SMBus and PMBus specifications:

- Quick Command
- Send Byte
- Write Byte
- Write Word
- Read Byte
- Read Word
- Block Read
- Block Write – Block Read Process Call
- Alert Response Address

The LTC3888-1 does not require PEC for Quick Command under any circumstances. The LTC3888-1 also supports group command protocol (GCP) as required by PMBus specification Part I, section 5.2.3. GCP is used to send commands to more than one PMBus device in one continuous transmission. It should not be used with commands that require the receiving device to respond with data, such as a STATUS_BYTE command. Refer to Part I of the PMBus specification for additional details on using GCP.

All LTC3888-1 message transmission types allow for packet error checking. The later section on Serial Communication Errors provides more detail on packet error checking.

Figure 5 to Figure 21 illustrate these protocols. Figure 4 provides a key to the protocol diagrams. Not all protocol elements will be present in every data packet. For instance, not all packets are required to include the packet error code. A number shown above a field in these diagrams indicates the number of bits in that field. All data transfers are initiated by the present bus master regardless of how many times data direction flow may change during the subsequent transmission. The LTC3888-1 never functions as a bus master.

This device includes handshaking features to ensure robust system communication. Please refer to the PMBus Communication and Command Processing section in Applications Information for more details.

## OPERATION

| | |
|---|---|
| S | START CONDITION |
| Sr | REPEATED START CONDITION |
| Rd | READ (BIT VALUE OF 1) |
| Wr | WRITE (BIT VALUE OF 0) |
| A | ACKNOWLEDGE (BIT SHOULD BE 0), OR |
| NA | NOT ACKNOWLEDGE (BIT SHOULD BE 1) |
| P | STOP CONDITION |
| PEC | PACKET ERROR CODE |
| | MASTER TO SLAVE |
| | SLAVE TO MASTER |
| ··· | CONTINUATION OF PROTOCOL |

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**Figure 4. PMBus Packet Protocol Diagram Element Key**

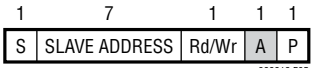


**Figure 5. Quick Command Protocol**

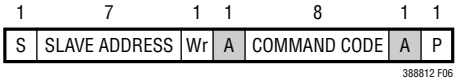


**Figure 6. Send Byte Protocol**

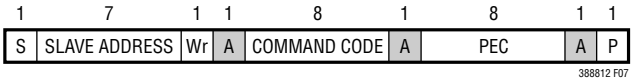


**Figure 7. Send Byte Protocol with PEC**

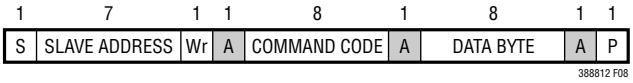


**Figure 8. Write Byte Protocol**

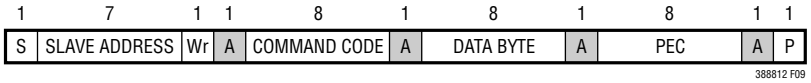


**Figure 9. Write Byte Protocol with PEC**

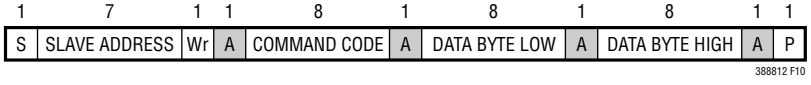


**Figure 10. Write Word Protocol**

## OPERATION

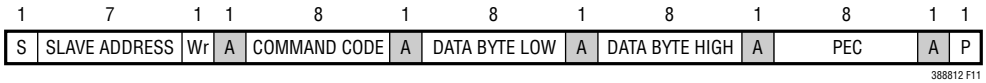


**Figure 11. Write Word Protocol with PEC**

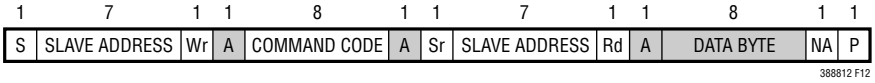


**Figure 12. Read Byte Protocol**

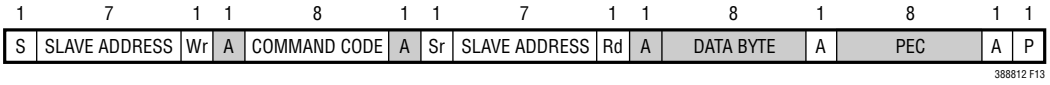


**Figure 13. Read Byte Protocol with PEC**

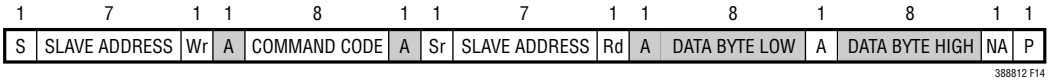


**Figure 14. Read Word Protocol**

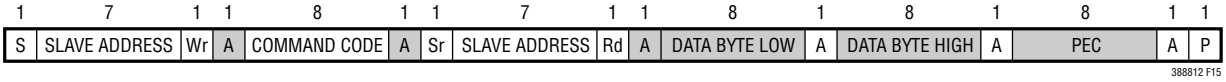


**Figure 15. Read Word Protocol with PEC**

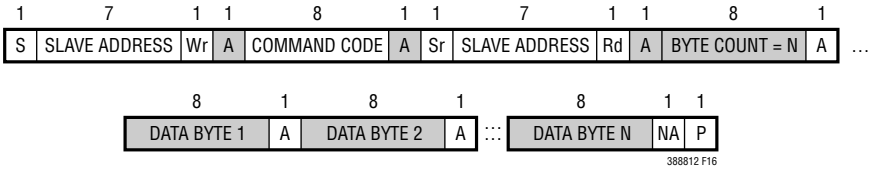


**Figure 16. Block Read Protocol**

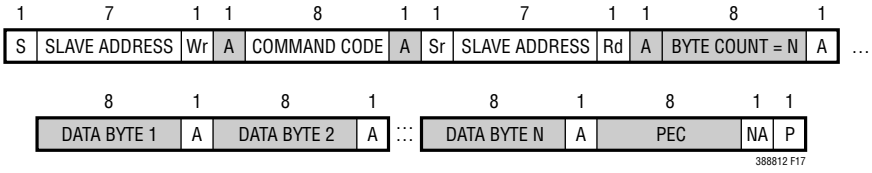


**Figure 17. Block Read Protocol with PEC**

## OPERATION

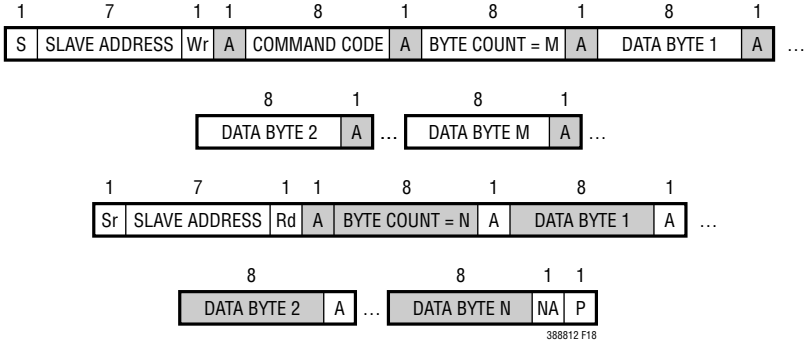


**Figure 18. Block Write – Block Read Process Call**

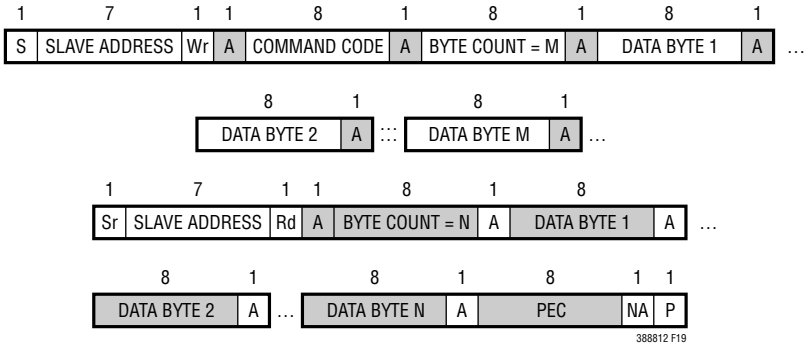


**Figure 19. Block Write – Block Read Process Call with PEC**

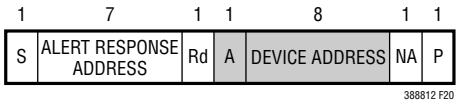


**Figure 20. Alert Response Address Protocol**

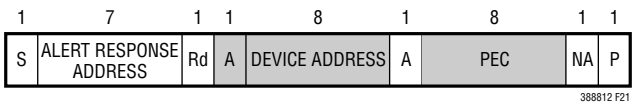


**Figure 21. Alert Response Address Protocol with PEC**

# OPERATION

### Serial Bus Addressing

The LTC3888-1 supports four types of serial bus addressing:

- Global Bus Addressing
- Power Rail Addressing
- Individual Device Addressing
- Page+ Master Channel Addressing

Global addressing provides a means for the bus master to communicate with all LTC3888-1 devices on the bus simultaneously. The LTC3888-1 global addresses of 0x5A and 0x5B cannot be changed or disabled. Commands sent to address 0x5A are applied to both master channels as if the PAGE command were set to 0xFF. Global address 0x5B is paged, allowing channel-specific control of all LTC3888-1 devices on the bus. Other ADI device types may respond at one or both of these global addresses. Reading from global addresses is strongly discouraged.

Rail addressing provides a means for the bus master to simultaneously communicate with all master channels connected together to produce a single output voltage (PolyPhase). While similar to global addressing, the rail address can be dynamically assigned with the paged MFR_RAIL_ADDRESS command, allowing for any logical grouping of channels that might be required for reliable system control. Reading from rail addresses is also strongly discouraged.

Device addressing is the most common means used by a bus master to communicate with an LTC3888-1. The value of the device address is set by the combination of ASEL0/ASEL1 pin programming and the MFR_ADDRESS command. Refer to the previous section on Resistor Configuration Pins for details.

Direct, individual channel addressing (Page+) allows the bus master to communicate directly with a specific LTC3888-1 PWM master channel without first using a PAGE command. Refer to the PAGE_PLUS commands for additional details.

Use of any of the four types of addressing requires careful planning to avoid address-related bus conflicts. Communication to LTC3888-1 devices at global and rail addresses should be limited to command write operations.

### Serial Bus Timeout

The LTC3888-1 implements a timeout feature to avoid hanging the serial interface. The data packet timer begins running at the first START event before the SLAVE ADDRESS write byte and ends with the STOP bit. Packet transmission must be completed before the timer expires, or the LTC3888-1 will tri-state the bus and ignore all message data. The data packet includes the SLAVE ADDRESS byte, COMMAND CODE byte, repeated START and SLAVE ADDRESS byte (if a read operation), all ACKNOWLEDGE and flow control bits (R/$\overline{W}$) and all data bytes.

The packet timer is typically set to 30ms. If bit 3 of MFR_CONFIG_ALL is set, this period is extended to 255ms. The LTC3888-1 automatically allows a packet transmission time of 255ms for MFR_FAULT_LOG block reads regardless of the setting of this bit. In no circumstances will the timeout period be less than the $t_{TIMEOUT}$ specification (25ms minimum).

The LTC3888-1 supports a PMBus frequency range of 10kHz to 400kHz.

### Serial Communication Errors

The LTC3888-1 supports the optional PMBus packet error checking protocol. This protocol appends a packet error code (PEC) to the end of applicable message transfers to improve communication reliability. The PEC is a CRC-8 error-checking byte calculated by the bus device sending the last data byte. Refer to SMBus specification 1.2 or higher for additional implementation details. All LTC3888-1 read operations will return a valid PEC if the bus master requests it. If bit 2 in the MFR_CONFIG_ALL command is set, the IC will not act in response to a bus write operation unless a valid PEC is also received from the host.

PEC errors on command writes, attempts to access unsupported commands, or writing invalid data to supported commands all cause the LTC3888-1 to generate a CML fault. The CML bit is then set in the STATUS_BYTE and STATUS_WORD commands, and the appropriate bit is set in the STATUS_CML command.

# PMBUS COMMAND SUMMARY

## PMBus Commands

Table 7 lists supported PMBus commands and manufacturer specific commands. Additional information about these commands can be found in Revision 1.2 of Part II of the PMBus Power System Management Protocol Specification. Users are encouraged to reference that manual. Exceptions or manufacturer-specific implementations are detailed in the tables below. All standard PMBus commands from 0x00 through 0xCF not listed in this table are implicitly not supported by the LTC3888-1. All commands from 0xD0 through 0xFF not listed in Table 7 are implicitly reserved by the manufacturer. The LTC3888-1 may execute additional commands not listed in this table, and these can change without notice. Reading these unlisted commands is harmless to the operation of the IC. Writes to any unsupported or reserved command should be avoided, as that may result in a CML fault and/or undesired operation of the part.

If PMBus commands are received faster than they are being processed, the part may become too busy to handle new commands. In these cases the LTC3888-1 follows the protocols defined in the PMBus Specification V1.2, Part II, Section 10.8.7, to communicate that it is busy. This device includes handshaking features to eliminate busy responses, simplify error handling software and ensure robust communication and system behavior. Please refer to PMBus Communication and Command Processing in the Applications Information section for further details.

ADI has made an effort to establish PMBus command compatibility and functional uniformity among its family of parts. However, differences may occur due to specific product requirements. Compatibility of PMBus commands among any ICs should not be assumed based simply on command name. Always refer to the manufacturer's data sheet of each device for a complete definition of a command function.

## Data Formats

PMBus supports specific floating point number formats and allows for a wide range of other data formats.

Table 6 describes the data formats used by the LTC3888-1. Abbreviations of these formats appear throughout this document.

**Table 6. Abbreviations of Supported Data Formats**

| | PMBus | | ADI | | |
|---|---|---|---|---|---|
| | TERMINOLOGY | SPECIFICATION REFERENCE | TERMINOLOGY | DEFINITION | EXAMPLE |
| L11 | Linear | Part II ¶7.1 | Linear_5s_11s | Floating point 16-bit data: value = Y • $2^N$, where N = b[15:11] and Y = b[10:0], both two's compliment binary integers. | b[15:0] = 0x9807 = 10011_000_0000_0111 value = 7 • $2^{-13}$ = 854E-6 |
| L16 | Linear VOUT_MODE | Part II ¶8.2 | Linear_16u | Floating point 16-bit data: value = Y • $2^{-12}$, where Y = b[15:0], an unsigned integer. | b[15:0] = 0x4C00 = 0100_1100_0000_0000 value = 19456 • $2^{-12}$ = 4.75 |
| CF | DIRECT | Part II ¶7.2 | Varies | Data with a custom format defined in the detailed PMBus command description. | Often an unsigned or two's compliment integer. |
| Reg | Register Bits | Part II ¶10.3 | Reg | Per-bit meaning defined in detailed PMBus command description. | PMBus STATUS_BYTE command. |
| ASC | Text Characters | Part II ¶22.2.1 | ASCII | ISO/IEC 8859-1 [A05] | LTC (0x4C5443) |

# PMBUS COMMAND SUMMARY

**Table 7. PMBus Command Summary**

| COMMAND NAME | CMD CODE | DESCRIPTION | TYPE | PAGED | DATA FORMAT | UNITS | NVM | DEFAULT VALUE | SEE PAGE |
|---|---|---|---|---|---|---|---|---|---|
| PAGE | 0x00 | Channel (page) presently selected for any paged command. | R/W Byte | N | Reg | | | 0x00 | 67 |
| OPERATION | 0x01 | On, off and margin control. | R/W Byte | Y | Reg | | ● | 0x80 | 71 |
| ON_OFF_CONFIG | 0x02 | RUN pin and PMBus on/off command configuration. | R/W Byte | Y | Reg | | ● | 0x1E | 70 |
| CLEAR_FAULTS | 0x03 | Clear all set fault bits. | Send Byte | N | | | | | 91 |
| PAGE_PLUS_WRITE | 0x05 | Write a command directly to a specified page. | W Block | N | | | | | 67 |
| PAGE_PLUS_READ | 0x06 | Read a command directly from a specified page. | Block R/W Process | N | | | | | 68 |
| WRITE_PROTECT | 0x10 | Protect the device against unintended PMBus modifications. | R/W Byte | N | Reg | | ● | 0x00 | 68 |
| STORE_USER_ALL | 0x15 | Store entire operating memory in EEPROM. | Send Byte | N | | | | | 102 |
| RESTORE_USER_ALL | 0x16 | Restore entire operating memory from EEPROM. | Send Byte | N | | | | | 102 |
| CAPABILITY | 0x19 | Summary of supported optional PMBus features. | R Byte | N | Reg | | | 0xB0 | 69 |
| SMBALERT_MASK | 0x1B | Mask $\overline{\text{ALERT}}$ activity. | Block R/W | Y | Reg | | ● | see CMD details | 99 |
| VOUT_TRANSITION_RATE | 0x27 | Slew rate for $V_{FB}$ (default) or $V_{OUT}$ soft-on/off and margining, including changes to VOUT_COMMAND. | R/W Word | Y | L11 | V/ms | ● | 0.25 AA00 | 88 |
| FREQUENCY_SWITCH | 0x33 | PWM frequency control. | R/W Word | N | L11 | kHz | ● | 500kHz 0xFBE8 | 72 |
| VIN_ON | 0x35 | Minimum input voltage to begin power conversion. | R/W Word | N | L11 | V | ● | 6.5V 0xCB40 | 78 |
| VIN_OFF | 0x36 | Decreasing input voltage at which power conversion stops. | R/W Word | N | L11 | V | ● | 6.0V 0xCB00 | 78 |
| IOUT_CAL_GAIN | 0x38 | Ratio of $I_{SENSE}$ voltage to sensed current. | R/W Word | Y | L11 | mΩ | ● | 5mΩ 0xCA80 | 81 |
| VOUT_OV_FAULT_RESPONSE | 0x41 | Fault response for $V_{OUT}$ overvoltage and power stage fault. | R Byte | Y | Reg | | | 0x80 | 95 |
| VOUT_UV_FAULT_RESPONSE | 0x45 | $V_{OUT}$ undervoltage fault response. | R/W Byte | Y | Reg | | ● | 0xB8 | 96 |
| IOUT_OC_FAULT_LIMIT | 0x46 | Output overcurrent fault limit. | R/W Word | Y | L11 | A | ● | 29.75A 0xDBB8 | 82 |
| IOUT_OC_FAULT_RESPONSE | 0x47 | Output overcurrent fault response. | R/W Byte | Y | Reg | | ● | 0x00 | 97 |
| IOUT_OC_WARN_LIMIT | 0x4A | Output overcurrent warning limit. | R/W Word | Y | L11 | A | ● | 20.0A 0xDA80 | 82 |
| OT_FAULT_LIMIT | 0x4F | External overtemperature fault limit. | R/W Word | Y | L11 | °C | ● | 100.0°C 0xEB20 | 85 |
| OT_FAULT_RESPONSE | 0x50 | External overtemperature fault response. | R/W Byte | Y | Reg | | ● | 0xB8 | 98 |
| OT_WARN_LIMIT | 0x51 | External overtemperature warning limit. | R/W Word | Y | L11 | °C | ● | 85.0°C 0xEAA8 | 85 |

# PMBUS COMMAND SUMMARY

**Table 7. PMBus Command Summary**

| COMMAND NAME | CMD CODE | DESCRIPTION | TYPE | PAGED | DATA FORMAT | UNITS | NVM | DEFAULT VALUE | SEE PAGE |
|---|---|---|---|---|---|---|---|---|---|
| VIN_OV_FAULT_LIMIT | 0x55 | $V_{IN}$ overvoltage fault limit. | R/W Word | N | L11 | V | ● | 15.5V 0xD3E0 | 78 |
| VIN_OV_FAULT_RESPONSE | 0x56 | $V_{IN}$ overvoltage fault response. | R/W Byte | Y | Reg | | ● | 0x80 | 96 |
| VIN_UV_WARN_LIMIT | 0x58 | $V_{IN}$ undervoltage warning limit. | R/W Word | N | L11 | V | ● | 6.3V 0xCB26 | 78 |
| TON_DELAY | 0x60 | Delay from RUN pin or OPERATION on command to $V_{OUT}$ ramp start. | R/W Word | Y | L11 | ms | ● | 0.0ms 0x8000 | 83 |
| TON_MAX_FAULT_LIMIT | 0x62 | Maximum time allowed for $V_{OUT}$ to rise above VOUT_UV_FAULT_LIMIT after TON_DELAY. | R/W Word | Y | L11 | ms | ● | 10.0ms 0xD280 | 84 |
| TON_MAX_FAULT_RESPONSE | 0x63 | Fault response when TON_MAX_FAULT_ LIMIT is exceeded. | R/W Byte | Y | Reg | | ● | 0xB8 | 98 |
| TOFF_DELAY | 0x64 | Delay from RUN pin or OPERATION off command to TOFF_FALL ramp start. | R/W Word | Y | L11 | ms | ● | 0.0ms 0x8000 | 84 |
| STATUS_BYTE | 0x78 | One-byte channel status summary. | R/W Byte | Y | Reg | | | | 86 |
| STATUS_WORD | 0x79 | Two-byte channel status summary. | R/W Word | Y | Reg | | | | 87 |
| STATUS_VOUT | 0x7A | $V_{OUT}$ fault and warning status. | R/W Byte | Y | Reg | | | | 87 |
| STATUS_IOUT | 0x7B | $I_{OUT}$ fault and warning status. | R/W Byte | Y | Reg | | | | 88 |
| STATUS_INPUT | 0x7C | Input supply fault and warning status. | R/W Byte | N | Reg | | | | 88 |
| STATUS_ TEMPERATURE | 0x7D | External temperature fault and warning status. | R/W Byte | Y | Reg | | | | 88 |
| STATUS_CML | 0x7E | Communication, memory and logic fault and warning status. | R/W Byte | N | Reg | | | | 89 |
| STATUS_MFR_ SPECIFIC | 0x80 | IC-specific status. | R/W Byte | Y | Reg | | | | 89 |
| READ_VIN | 0x88 | Measured $V_{IN}$. | R Word | N | L11 | V | | | 92 |
| READ_VOUT | 0x8B | Measured $V_{OUT}$. | R Word | Y | L16 | V | | | 93 |
| READ_IOUT | 0x8C | Measured $I_{OUT}$. | R Word | Y | L11 | A | | | 93 |
| READ_TEMPERATURE_1 | 0x8D | Measured external temperature. | R Word | Y | L11 | °C | | | 94 |
| READ_TEMPERATURE_2 | 0x8E | Measured internal temperature. | R Word | N | L11 | °C | | | 94 |
| READ_FREQUENCY | 0x95 | Measured PWM input clock frequency. | R Word | Y | L11 | kHz | | | 94 |
| PMBUS_REVISION | 0x98 | Supported PMBus version. | R Byte | N | Reg | | | 0x22 V1.2 | 69 |
| MFR_ID | 0x99 | Manufacturer identification. | R String | N | ASC | | | LTC | 104 |
| IC_DEVICE_ID | 0xAD | LTC3888-1 model number. | R String | N | ASC | | | LTC3888-1 | 104 |
| **Commands for Digital Output Voltage Control** (See Applications Information or PMBus Command for Details) | | | | | | | | | |
| VOUT_MODE | 0x20 | Voltage-related format (Linear) and exponent. | R Byte | Y | Reg | | | 0x14 $2^{-12}$ | 82 |
| VOUT_COMMAND | 0x21 | Default Nominal $V_{FB}$ regulation. Nominal $V_{OUT}$ value when VOUT_SCALE_LOOP is defined. | R/W Word | Y | L16 | V | ● | 400mV 0x0666 | 82 |
| VOUT_MAX | 0x24 | Maximum $V_{OUT}$ capability. | R Word | Y | L16 | V | | 1.1V 0x119A | 82 |

# PMBUS COMMAND SUMMARY

**Table 7. PMBus Command Summary**

| COMMAND NAME | CMD CODE | DESCRIPTION | TYPE | PAGED | DATA FORMAT | UNITS | NVM | DEFAULT VALUE | SEE PAGE |
|---|---|---|---|---|---|---|---|---|---|
| **Commands for Digital Output Voltage Control** (Continued) | | | | | | | | | |
| VOUT_MARGIN_HIGH | 0x25 | $V_{FB}$ (default) or $V_{OUT}$ at high margin, **must be greater than VOUT_COMMAND**. | R/W Word | Y | L16 | V | ● | 420mV 0x06B8 | 83 |
| VOUT_MARGIN_LOW | 0x26 | $V_{FB}$ (default) or $V_{OUT}$ at low margin, **must be less than VOUT_COMMAND**. | R/W Word | Y | L16 | V | ● | 380mV 0x0614 | 83 |
| VOUT_SCALE_LOOP | 0x29 | Nominal $V_{OUT}$/ $V_{FB}$ gain provided by external feedback network. | R/W Word | Y | L11 | V/V | ● | N/A | 83 |
| VOUT_OV_FAULT_LIMIT | 0x40 | Default $V_{FB}$ overvoltage fault limit. $V_{OUT}$ OV limit if VOUT_SCALE_LOOP is defined. | R/W Word | Y | L16 | V | ● | 440mV 0x070A | 83 |
| VOUT_OV_WARN_LIMIT | 0x42 | $V_{OUT}$ overvoltage warning limit, sensed at $V_{SENSE}$±. | R/W Word | Y | L16 | V | ● | 3.6V 0x3981 | 83 |
| VOUT_UV_WARN_LIMIT | 0x43 | $V_{OUT}$ undervoltage warning limit, sensed at $V_{SENSE}$±. | R/W Word | Y | L16 | V | ● | 0.0V 0x0000 | 84 |
| VOUT_UV_FAULT_LIMIT | 0x44 | Default $V_{FB}$ undervoltage fault limit. $V_{OUT}$ UV limit if VOUT_SCALE_LOOP is defined. | R/W Word | Y | L16 | V | ● | 360mV 0x05C3 | 84 |
| TOFF_MAX_WARN_LIMIT | 0x66 | Maximum time for $V_{OUT}$ to reach 0.125xVOUT_COMMAND after being commanded to 0.0V. | R/W Word | Y | L11 | ms | ● | 0ms 0x8000 | 88 |
| **LTC3888-1 Custom Commands** | | | | | | | | | |
| MFR_VOUT_MAX | 0xA5 | Maximum VOUT_MAX. | R Word | Y | L16 | V | | 3.75V 0x3C00 | 79 |
| USER_DATA_00 | 0xB0 | EEPROM word reserved for LTpowerPlay. | R/W Word | N | Reg | | ● | | 103 |
| USER_DATA_01 | 0xB1 | EEPROM word reserved for LTpowerPlay. | R/W Word | Y | Reg | | ● | | 103 |
| USER_DATA_02 | 0xB2 | EEPROM word reserved for OEM use. | R/W Word | N | Reg | | ● | | 103 |
| USER_DATA_03 | 0xB3 | EEPROM word available for general data storage. | R/W Word | Y | Reg | | ● | 0x0000 | 103 |
| USER_DATA_04 | 0xB4 | EEPROM word available for general data storage. | R/W Word | N | Reg | | ● | 0x0000 | 103 |
| MFR_INFO | 0xB6 | Manufacturer-specific information | R Word | N | Reg | | | | 91 |
| MFR_EE_UNLOCK | 0xBD | (contact the factory) | | | | | | | 103 |
| MFR_EE_ERASE | 0xBE | (contact the factory) | | | | | | | 103 |
| MFR_EE_DATA | 0xBF | (contact the factory) | | | | | | | 103 |
| MFR_CHAN_CONFIG | 0xD0 | General channel-specific configuration. | R/W Byte | Y | Reg | | ● | 0x1D | 73 |
| MFR_CONFIG_ALL | 0xD1 | General device-level configuration. | R/W Byte | N | Reg | | ● | 0x21 | 70 |
| MFR_FAULT_PROPAGATE | 0xD2 | Configure fault propagation via $\overline{\text{FAULT}}$ pins. | R/W Word | Y | Reg | | ● | 0x6993 | 100 |
| MFR_PWM_COMP | 0xD3 | Channel-specific PWM loop compensation. | R/W Byte | Y | Reg | | ● | 0xAE | 77 |
| MFR_PWM_MODE_LTC3888-1 | 0xD4 | LTC3888-1 channel-specific PWM mode control. | R/W Byte | Y | Reg | | ● | 0x02 | 76 |
| MFR_FAULT_RESPONSE | 0xD5 | PWM response when $\overline{\text{FAULT}}$ pin is low due to external fault. | R/W Byte | Y | Reg | | ● | 0xC0 | 101 |
| MFR_OT_FAULT_RESPONSE | 0xD6 | Internal overtemperature fault response. | R Byte | N | Reg | | | 0xC0 | 98 |

# PMBUS COMMAND SUMMARY

**Table 7. PMBus Command Summary**

| COMMAND NAME | CMD CODE | DESCRIPTION | TYPE | PAGED | DATA FORMAT | UNITS | NVM | DEFAULT VALUE | SEE PAGE |
|---|---|---|---|---|---|---|---|---|---|
| MFR_IOUT_PEAK | 0xD7 | Maximum master channel $I_{OUT}$ measurement since last MFR_CLEAR_PEAKS. | R Word | Y | L11 | A | | | 93 |
| MFR_RETRY_DELAY | 0xDB | Minimum time before retry after a fault. | R/W Word | Y | L11 | ms | ● | 350ms 0xFABC | 99 |
| MFR_RESTART_DELAY | 0xDC | Minimum time RUN pin is held low by the LTC3888-1. | R/W Word | Y | L11 | ms | ● | 500ms 0xFBE8 | 83 |
| MFR_VOUT_PEAK | 0xDD | Maximum $V_{OUT}$ measurement since last MFR_CLEAR_PEAKS. | R Word | Y | L16 | V | | | 93 |
| MFR_VIN_PEAK | 0xDE | Maximum $V_{IN}$ measurement since last MFR_CLEAR_PEAKS. | R Word | N | L11 | V | | | 93 |
| MFR_TEMPERATURE_1_PEAK | 0xDF | Maximum external temperature measurement since last MFR_CLEAR_ PEAKS (LTC3888-1 only). | R Word | Y | L11 | °C | | | 94 |
| MFR_TOTAL_IOUT | 0xE1 | Read total IOUT for each page/rail defined by MFR_PWM_CONFIG_LTC3888-1[2:0] | R Word | Y | L11 | A | | | 93 |
| MFR_CLEAR_PEAKS | 0xE3 | Clear all peak values. | Send Byte | N | | | | | 94 |
| MFR_PADS_LTC3888-1 | 0xE5 | State of selected LTC3888-1 pads. | R Word | N | Reg | | | | 90 |
| MFR_ADDRESS | 0xE6 | Specify right-justified 7-bit device address. | R/W Byte | N | Reg | | ● | 0x4F | 69 |
| MFR_SPECIAL_ID | 0xE7 | Unique manufacturer product ID | R Word | N | Reg | | | 0x488X | 103 |
| MFR_FAULT_LOG_STORE | 0xEA | Force capture of fault log in RAM and transfer to EEPROM. | Send Byte | N | | | | | 103 |
| MFR_FAULT_LOG_CLEAR | 0xEC | Clear existing EEPROM fault log. | Send Byte | N | | | | | 101 |
| MFR_FAULT_LOG | 0xEE | Read fault log data. | R Block | N | Reg | | | | 101 |
| MFR_COMMON | 0xEF | ADI-generic device status reporting. | R Byte | N | Reg | | | | 90 |
| MFR_COMPARE_USER_ALL | 0xF0 | Compare contents of command RAM with EEPROM. | Send Byte | N | | | | | 93 |
| MFR_TEMPERATURE_2_PEAK | 0xF4 | Maximum internal temperature measurement since last MFR_CLEAR_PEAKS. | R Word | N | L11 | °C | | | 94 |
| MFR_PWM_CONFIG_ LTC3888-1 | 0xF5 | LTC3888-1 PWM configuration common to both master channels. | R/W Byte | N | Reg | | ● | 0x03 | 73 |
| MFR_LOAD_EMULATION | 0xF7 | Load step emulation control. | R/W Byte | Y | Reg | | | 0x00 | 81 |
| MFR_TEMP_1_GAIN | 0xF8 | Slope for external temperature calculations (LTC3888-1 only). | R/W Word | Y | L11 | mV/ °C | ● | 8 mV/ °C 0xD200 | 85 |
| MFR_TEMP_1_OFFSET | 0xF9 | 0 °C offset for external temperature calculations (LTC3888-1 only). | R/W Word | Y | L11 | mV | ● | 600mV 0x0258 | 85 |
| MFR_RAIL_ADDRESS | 0xFA | Specify unique right-justified 7-bit address for channels comprising a PolyPhase output. | R/W Byte | Y | Reg | | ● | 0x80 | 69 |
| MFR_RESET | 0xFD | Force full reset without removing power. | Send Byte | N | | | | | 71 |

NVM ● Indicates a command value stored to and restored from internal EEPROM using the STORE_USER_ALL and RESTORE_USER_ALL commands, respectively.

# APPLICATIONS INFORMATION

## EFFICIENCY CONSIDERATIONS

Normally, one of the primary goals of any LTC3888-1 application will be to obtain the highest practical conversion efficiency. The efficiency of a switching regulator is equal to the output power divided by the input power. It is often useful to analyze individual losses to determine what is limiting the efficiency and to ascertain which change would produce the most improvement. Balancing or limiting these individual losses plays a dominant role in the component selection process outlined over the next few sections.

Percent efficiency can be expressed as:

$$\%\text{Efficiency} = 100\% - (L1 + L2 + L3 + \ldots)$$

where L1, L2, et al, are the individual losses as a percentage of input power: $100 \bullet P_{Ln}/P_{IN}$.

Although all dissipative elements in the system produce losses, four main sources usually account for most of the losses in LTC3888-1 applications: IC supply current, $I^2R$ losses, topside power MOSFET transition losses and total gate drive current.

1. The LTC3888-1 IC supply current is a DC value given in the Electrical Characteristics table. The absolute loss created by the IC itself is approximately this current times the $V_{IN}$ supply voltage. IC supply current typically results in a small loss (<0.1%).
2. $I^2R$ losses occur mainly in the DC resistances of the selected power stage, inductor, PCB routing, and input and output capacitor ESR. It is crucial that careful attention is paid to the layout of the power path on the PCB to minimize that resistance. In a 2-phase 1.2V system, 1mΩ of PCB resistance at the output costs 5% in efficiency with the output running at 60A.
3. Transition losses apply only to the selected power stage and normally do not become significant until operating above 12V.
4. Gate drive current is equal to the sum of the top and bottom MOSFET gate charges multiplied by the frequency of operation. These charges are based on internal power stage design and are normally included in overall efficiency (or power loss) numbers provded by the manufacturer at a given operating condtion.

Other sources of loss include internal body or external Schottky diode conduction during the power stage FET driver non-overlap time, as well as inductor core losses. These latter categories generally account for less than 2% total additional loss.

## POWER STAGE SELECTION AND INTERFACE

The LTC3888-1 operates with power stages that provide a voltage or current monitor of the output current they sense. As a minimum, these stages must also accept 3.3V-compatible three-state PWM input control. Other features such as PWM input off-state biasing, power stage temperature monitoring, fault detection and indication, and UVLO protection are optional. Examples of these kinds of devices include the TDA21470, IR35411 and FDM3170.

The LTC3888-1 $I_{SENSE}$ pins are high impedance inputs to internal interface circuits and the monitor ADC, both using a common mode of IREF (1.6V). Maximum instantaneous differential current sense input relative to IREF is 525mV, and maximum DC input differential is 400mV. These inputs must be properly connected in the application at all times. While not strictly required, it is recommended to short $I_{SENSE}$ to IREF on PWM channels disabled by MFR_PWM_CONFIG_LTC3888-1 master/slave setting.

As shown in Figure 22 and Figure 23, the LTC3888-1 is designed to interface to power stages that provide either a current or voltage analog of sensed output current. The LTC3888-1 IREF output should be used to provide the common mode voltage for this output current monitor, with some bypass located adjacent to each power stage and returned to GND (IC paddle). The LTC3888-1 is designed to work best when the power stage output current monitor is scaled to provide between 3mV/A and 10mV/A to its $I_{SENSE}$ input. This scaling must be identical for all phases on a rail. For most power stages providing a voltage-mode monitor, no additional external scaling components are required.

Some of these power stages require the controller to provide a PWM pulse with a minimum width. The LTC3888-1 can be configured to accommodate this requirement by setting bit 1 of MFR_PWM_MODE_LTC3888-1.

## APPLICATIONS INFORMATION

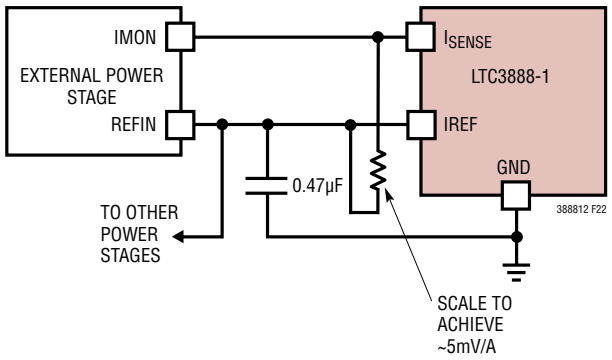


**Figure 22. Interface to Current-Mode Output Current Sense**

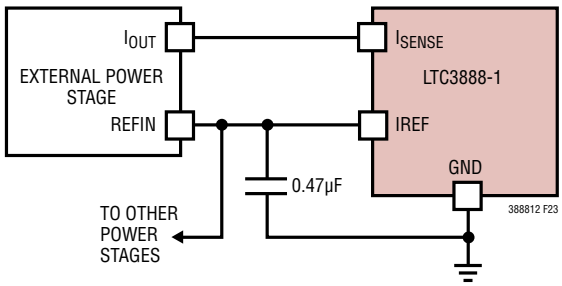


**Figure 23. Interface to Voltage-Mode Output Current Sense**

The LTC3888-1 TSNS pins interface directly to the wire-OR shared TEMP/FAULT bus found on most power stages offering output current monitor. When all phases are fault-free, the voltage on this bus indicates the highest power stage temperature on the rail. The internal monitor ADC converts this voltage, and the computed temperature value is returned by the paged READ_TEMPERATURE_1 telemetry command. The slope of the external temperature sensor can be modified to fit the selected power stage using the coefficient stored in MFR_TEMP_1_GAIN. The offset of the external temperature sense can be adjusted by MFR_TEMP_1_OFFSET, which designates the bus voltage indicating 0°C.

The LTC3888-1 also recognizes indicated power stage fault conditions on the shared TEMP/FAULT bus. This includes support for optional power stage UV indication when enabled with bit 0 of MFR_PWM_MODE_LTC3888-1. These events are reported through standard PMBus status registers for improved system state observation by the bus host as shown in Table 8. Refer to previous Operation section discussions on Hardwired PWM Response to Power Stage Faults and Status Registers and $\overline{\text{ALERT}}$ Masking for additional details.

**Table 8. Special LTC3888-1 Status Indications[1]**

| | PAGED | | | MFR_PADS_LTC3888-1[5] |
|---|---|---|---|---|
| **CONDITION INDICATED** | **STATUS_VOUT BIT 7 (VOUT_OV FAULT)** | **STATUS_VOUT BIT 4 (VOUT_UV FAULT)** | **STATUS_IOUT BIT 3** | **CH0/1 DrMOS READY BIT 14/15** |
| $V_{OUT}$ OV | • | | | • |
| $V_{OUT}$ UV | | • | | • |
| $V_{SENSE}$+ OPEN[2,3] | • | • | | • |
| Power Stage UV (TSNS)[4] or VDR Monitor UV | • (IFF CH Set to Run) | | | |
| Power Stage Fault[6] | • | | • | • |

[1]With the exception of $V_{SENSE}$+ Open, all VOUT_OV Fault conditions are handled by VOUT_OV_FAULT_RESPONSE, which is immediate off with no retry, and a VOUT_UV fault condition is handled by VOUT_UV_FAULT_RESPONSE.

[2]Both $V_{SENSE}$+ lines are tested each time the LTC3888-1 powers up or resets. The response of the LTC3888-1 for any open $V_{SENSE}$+ line is to disable all outputs. A detected open line condition can only be cleared with successful retesting by power cycle or MFR_RESET.

[3]Both bit 7 and bit 4 of STATUS_VOUT may also be set if a power stage UV or fault occurs during a true $V_{OUT}$ UV with the PWM still running. In this case STATUS_IOUT and MFR_PADS will continue to accurately indicate power stage state, which does not require a full reset to clear.

[4]Detection of this condition must be enabled by setting bit 0 of MFR_PWM_MODE_LTC3888-1 (paged). No UV indication is given or response taken if bit 0 of MFR_PWM_MODE_LTC3888-1 is clear.

[5]MFR_PADS_LTC3888-1[15:14] respond to enabled power stage UV detection by indicating NOT READY (1'b0) for their respective channels, regardless of PWM run state. Otherwise these bits indicate READY (1'b1).

[6]The exact nature of fault indicated in this case varies by manufacturer and can include such issues as gross output overcurrent or power stage overtemperature.

## APPLICATIONS INFORMATION

If power stage UV detection is enabled, a check of the MFR_PADS_LTC3888-1 status bits shown in Table 8 is strongly recommended before turning on a rail. Otherwise, if the power stage UV is in the process of clearing during system power-up, the resulting LTC3888-1 fault condition cannot be distinquished from overvoltage on the output.

### USING THE VDR MONITOR

When a shared TEMP/FAULT bus is not provided from the power stages in an application, or if a necessary UV indication is not provided by the particular power stage selected, pin 8 of the LTC3888-1 can be programmed to function as a VDR_MON input by bit 5 of MFR_CHAN_CONFIG on Page 0 to observe UV conditions on the power stage gate drive supply. As shown in Figure 24 this simply requires sensing the supply to be monitored with a resistor divider that produces 1.22V at the desired UV threshold.

$V_{UV} = 1.22V \bullet (R1+R2)/R2$

A single VDR_MON input is provided for both master channels. The state of bit 0 of MFR_PWM_CONFIG_LTC3888-1 is ignored and UV detection on TSNS1 fully disabled when VDR_MON is active.

### UNUSED TSNS INPUTS

In cases where a shared TEMP/FAULT bus is not available or monitoring of external temperature is simply not required, unused TSNS inputs may be left open or wired to GND as long as bit 0 of MFR_PWM_MODE_LTC3888-1 (paged) is left clear. The LTC3888-1 will then continue to respond to READ_TEMPERATURE_1 requests, but the data returned will be meaningless.

### PWM FREQUENCY AND INDUCTOR SELECTION

The selection of the PWM switching frequency is a trade-off between efficiency, transient response and component size. High frequency operation reduces the size of the inductor and output capacitor as well as increasing the maximum practical control loop bandwidth. However, efficiency is generally lower due to increased transition and switching losses. The inductor value is related to the switching frequency $f_{PWM}$ and step-down ratio. It should be selected to meet choke ripple current requirements. The inductor value can be calculated using the following equation:

$$L = \left(\frac{V_{OUT}}{f_{PWM} \bullet \Delta I_L}\right) \bullet \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Allowing a larger value of choke ripple current ($\Delta I_L$) leads to smaller L, but results in greater core loss and higher output voltage ripple for a given output capacitance and/or ESR. A reasonable starting point for setting the ripple current is 30% of the maximum output current.

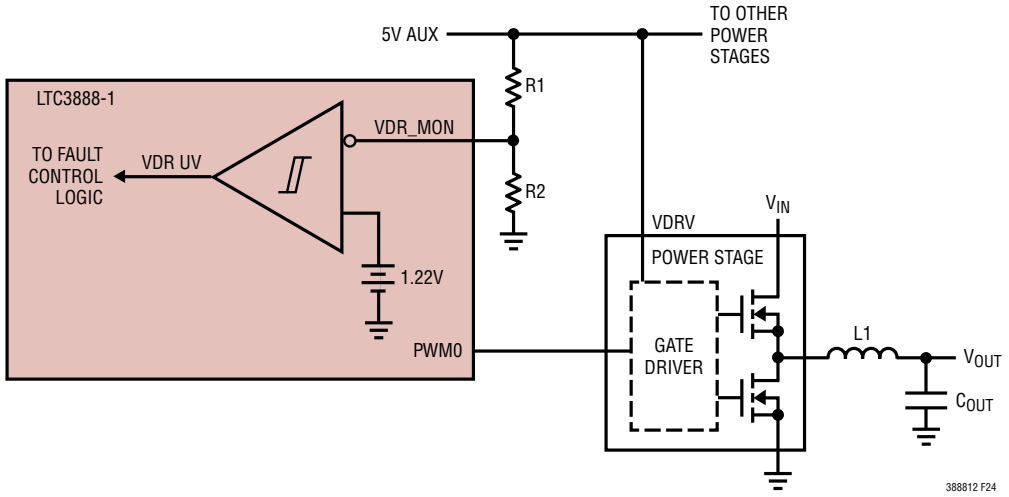


**Figure 24. LTC3888-1 Power Stage VDR Monitor**

## APPLICATIONS INFORMATION

The inductor saturation current rating needs to be higher than the peak inductor current during transient conditions. If $I_{OUT}$ is the maximum rated load current, then the maximum transient current $I_{MAX}$ would normally be chosen to be some factor greater than $I_{OUT}$ (e.g., 1.6 • $I_{OUT}$).

The minimum saturation current rating should be chosen to allow margin due to manufacturing and temperature variation in the power stage output current monitor. A reasonable $I_{SAT}$ value would be 2.2 • $I_{OUT}$.

The programmed current limit IOUT_OC_FAULT_LIMIT must be low enough to ensure that the inductor never saturates and high enough to allow increased current during transient conditions. For example, if:

$I_{SAT}$ = 2.2 • $I_{OUT}$, and

$I_{MAX}$ = 1.6 • $I_{OUT}$

a reasonable output current limit would be

IOUT_OC_FAULT_LIMIT = 1.8 • $I_{OUT}$

Once the value of L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core losses found in low-cost powdered iron cores, forcing the use of more expensive ferrite or molypermalloy cores. Also, core losses decrease as inductance increases. Unfortunately, increased inductance requires more turns of wire, larger inductance and larger copper losses.

Ferrite designs have very low core loss and are preferred at high switching frequencies. However, these core materials exhibit hard saturation, causing an abrupt reduction in the inductance when the peak current capability is exceeded. Do not allow the core to saturate.

### $C_{IN}$ SELECTION

The input bypass capacitance for an LTC3888-1 power circuit needs to have ESR low enough to keep the supply drop low as the top MOSFETs turn on, RMS current capability adequate to withstand the ripple current at the input, and a capacitance value large enough to maintain the input voltage until the input supply can make up the difference. Generally, a capacitor that meets the first two requirements (particularly a non-ceramic type) will have far more capacitance than is required to keep capacitance-based droop under control.

The input capacitance voltage rating should be at least 1.4 times the maximum input voltage. Power loss due to ESR occurs as $I^2R$ dissipation in the capacitor itself. The input capacitor RMS current and its impact on any preceding input network is reduced by PolyPhase architecture. It can be shown that the worst case RMS current occurs when only one phase is operating. The phase with the highest ($V_{OUT}$)($I_{OUT}$) product should be used to determine the maximum RMS current requirement. Increasing the number of phases will decrease the input RMS ripple current from this maximum value. 2-phase operation typically reduces the input capacitor RMS ripple current by a factor of 30% to 70%.

In continuous inductor conduction mode, the source current of the top power MOSFET is approximately a square wave of duty cycle $V_{OUT}/V_{IN}$. The maximum RMS capacitor current in this case is given by:

$$I_{RMS} \approx I_{OUT(MAX)} \frac{\sqrt{V_{OUT}\left(V_{IN} - V_{OUT}\right)}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where

$I_{RMS} = I_{OUT}/2$

This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief.

Note that manufacturer ripple current ratings for capacitors are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor or to choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. Always consult the manufacturer if there is any question.

Ceramic, tantalum, semiconductor electrolyte (OS-CON), hybrid conductive polymer (SUNCON) and switcher-rated electrolytic capacitors can be used as input capacitors, but each has drawbacks. Ceramics have high voltage coefficients of capacitance and may have audible piezoelectric effects; tantalums need to be surge-rated; OS-CONs suffer from higher inductance, larger case size and limited

## APPLICATIONS INFORMATION

surface mount applicability; and electrolytic capacitors have higher ESR and can dry out. Sanyo OS-CON SVP(D) series, Sanyo POSCAP TQC series, or Panasonic EE-FT series aluminum electrolytic capacitors can be used in parallel with high performance ceramic capacitors as an effective means of achieving low ESR and high bulk capacitance.

In addition to PWM bulk input capacitance, a small (0.01µF to 1µF) bypass capacitor between the chip $V_{IN}$ pin and ground, placed close to the LTC3888-1, is also suggested. A small resistor placed between the bulk $C_{IN}$ and the $V_{IN}$ pin/bypass provides further isolation between rails. However, if the time constant of any such R-C network on the $V_{IN}$ pin exceeds 30ns, dynamic line transient response can be adversely affected.

### $C_{OUT}$ SELECTION

The selection of $C_{OUT}$ is primarily determined by the ESR required to minimize voltage ripple and load step transients. The output ripple $\Delta V_{OUT}$ is approximately bounded by:

$$\Delta V_{OUT} \le \Delta I_L \left( ESR + \frac{1}{8 \bullet f_{PWM} \bullet C_{OUT}} \right)$$

where $\Delta I_L$ is the inductor ripple current.

$$\Delta I_L = \frac{V_{OUT}}{L \bullet f_{PWM}} \left( 1 - \frac{V_{OUT}}{V_{IN}} \right)$$

Since $\Delta I_L$ increases with input voltage, the output ripple voltage is highest at maximum input voltage. Typically once the ESR requirement is satisfied, the capacitance is adequate for filtering and has the necessary RMS current rating.

Manufacturers such as Sanyo, Panasonic and Cornell Dubilier should be considered for high performance through-hole capacitors. The OS-CON semiconductor electrolyte capacitor available from Sanyo has a good (ESR)(size) product. Additional ceramic capacitors in parallel with polarized capacitors is recommended to offset the effect of lead inductance.

In surface mount applications, multiple capacitors may have to be paralleled to meet the ESR or transient current handling requirements of the application. Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. New polymer surface mount capacitors also offer very low ESR but have much lower capacitive density. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. Several excellent output capacitor choices include the Sanyo POSCAP TPD/E/F series, the Kemet T520, T530 and A700 series, NEC/Tokin NeoCapacitors and Panasonic SP series. Other suitable capacitor types include Nichicon PL series and Sprague 595D series. Consult the manufacturer for other specific recommendations.

### PROGRAMMABLE LOOP COMPENSATION

Because the LTC3888-1 uses an OTA error amplifier architecture, Type II compensation is most commonly applied for stabilizing the voltage control loop as shown in Figure 25. The LTC3888-1 offers programmable loop compensation to optimize the transient response without requiring a hardware change. Internal error amplifier $g_m$ can be varied from 1mmho to 5.73 mmho, and internal compensation resistor $R_{ITH}$ can be varied from 1kΩ to 62kΩ with the MFR_PWM_COMP command. A maximum of two external capacitors are then required to stabilize each voltage control loop.

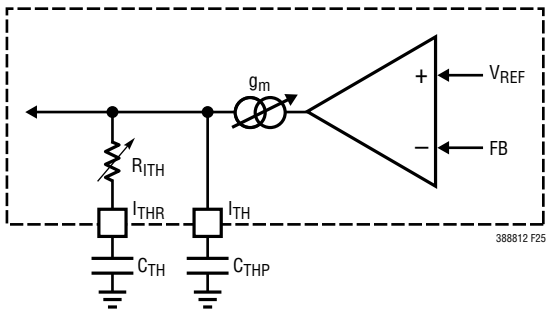


**Figure 25. Programmable Loop Compensation**

By adjusting EA $g_m$ and $R_{ITH}$ the LTC3888-1 can provide flexible Type II compensation for loop optimization over a wide range of output capacitance. Adjusting $g_m$ will change compensation gain over the entire frequency range without adjusting any pole-zero locations as shown in Figure 26.

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Adjusting $R_{ITH}$ will change the pole-zero locations as shown in Figure 27. LTpowerCAD is a freeware tool available from ADI suitable for determining optimum values for $g_m$ and $R_{ITH}$ for the LTC3888-1.

Internal $R_{ITH}$ and external $C_{TH}$ combine to set the dominant pole-zero loop compensation. Adjust the value of $R_{ITH}$ to optimize transient response after final PCB layout is complete and a particular $C_{TH}$ and output filter capacitor have been selected. The types and values used for these capacitors will strongly influence loop gain and phase.

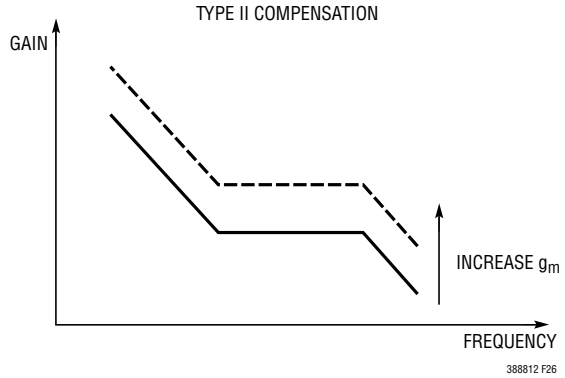


**Figure 26. Error AMP $g_m$ Adjust**

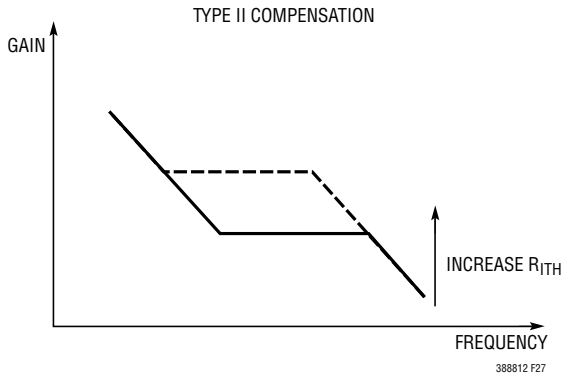


**Figure 27. $R_{ITH}$ Adjust**

Occassionally, fine tuning of AC compensation to optimize transient response may benefit from additional mid-band phase recovery. In this case, another pole-zero pair can be added to the feedback loop with a small capacitor or R-C across the top resistor of the $V_{OUT}$ feedback network, as shown in Figure 28. Often R3 is replaced with a short when the error amplifer is an OTA, as is the case with the LTC3888-1. Adding R3 provides additional AC gain control, if needed. This allows total loop compensation approaches similar to a Type III network.

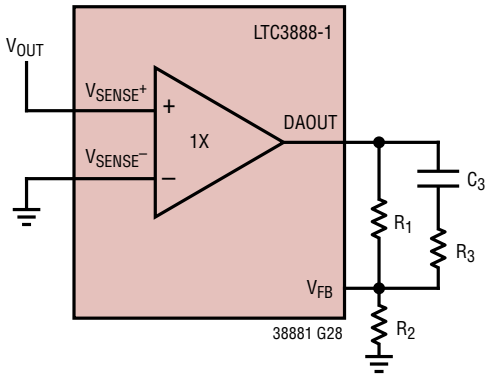


**Figure 28. Remote Sense and Setting Output Voltage**

Regulator loop stability can be checked by observing a load transient response. Post-transient output voltage settling is related to closed-loop stability and will demonstrate actual overall supply performance. Switching regulators can require several clock cyles to respond to a direct step in DC load current due to the time required for a voltage feedback error signal to develop. As the loop responds and adjusts to remove the developing error signal, $V_{OUT}$ can be monitored for an over-damped, sluggish response or excessive overshoot or ringing, which would then indicate a stability problem.

The LTC3888-1 features flexible load step emulation (PMBus MFR_LOAD_EMULATION command) to simulate calibrated output loads placed simultaneously on all phases of the rail. It is not necessary to generate an actual, high powered and regulated load step on the rail output. This creates a $V_{OUT}$ response that is identical to that of a physical output load step with $C_{OUT}$ ESR effects removed from the initial step edge. This makes observation of $V_{OUT}$ useful for loop evalution. In a predominantly second-order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at the output. Bandwidth can also be estimated by the rise time of the $V_{OUT}$ waveform in this case.

A more severe load step case is created if unpowered loads with large supply bypass capacitors (>1µF) are cold-switched to the rail output for power. The discharged bypass capacitors are effectively put in parallel wth $C_{OUT}$, causing a rapid drop in $V_{OUT}$. No regulator can alter power delvery quickly enough to prevent this sudden step change in output voltage if the load switch resistance is low and

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driven on quickly. If the ratio of such a switched $C_{LOAD}$ to $C_{OUT}$ is greater than 1:50, the switch rise time should be limited to approximately 25 • $C_{LOAD}$. As an example, a 10µF switched load would require a 250µs rise time with charging current limited to about 200mA.

### PCB LAYOUT CONSIDERATIONS

To prevent magnetic and electrical field radiation, or high frequency resonant problems, and to ensure correct IC operation, proper layout of the components connected to the LTC3888-1 is essential. Refer to Figure 29, which also illustrates current waveforms typically present in the circuit branches. In this drawing SW0/1 and D0/1 respresent salient features of the selected power stage. For maximum efficiency, the switch node (input to L0/1) rise and fall times should be minimized. The following PCB design priority list will help ensure proper topology.

1. Place a ground or DC voltage layer between a power layer and a small-signal layer. Generally, power planes should be placed on the top layer (4-layer PCB), or top and bottom layer if more than 4 layers are used. Use wide/short copper traces for power components and avoid improper use of thermal relief around power plane vias to minimize resistance and inductance.
2. Low ESR input capacitors should be placed as close as possible to the power stage FET supply and ground connections with the shortest copper traces possible. The power stage must be on the same layer of copper as the input capacitors with a common topside power connection at $C_{IN}$. Do not attempt to split the input decoupling for multiple phases, as a large resonant loop can result. Vias should not be used to make these connections. Avoid blocking forced air flow to the power stages with large size passive components.
3. Place the inductor input as close as possible to the power stage. Minimize the surface area of the switch node. Make the trace width the minimum needed to support the maximum output current. Avoid copper fills or pours. Avoid running the connection on multiple copper layers in parallel. Minimize capacitance from the switch node to any other trace or plane.
4. PCB traces for remote voltage sense should be run together back to the LTC3888-1 in pairs with the smallest spacing possible on any given layer on which they are routed. Avoid high frequency switching signals and ideally shield with ground planes. Locate any filter component on these traces next to the LTC3888-1, and not at the Kelvin sense location.
5. PCB traces for output current sense ($I_{SENSE}$, IREF) should avoid high frequency switching signals and ideally be shielded with ground planes. Filter components on these traces should return to GND (IC paddle) and not to a local PGND.
6. Place low ESR output capacitors adjacent to the inductor output and ground. Output capacitor ground connections must feed into the same copper that connects to the input capacitor ground before connecting back to system ground.
7. Connection of switching ground to system ground, small-signal analog ground or any internal ground plane should be single-point. If the system has an internal system ground plane, a good way to do this is to cluster vias into a single star point to make the connection. This cluster should be located directly beneath the IC GND paddle, which serves as analog signal ground. A useful CAD technique is to make separate ground nets and use a 0Ω resistor to connect them to system ground.
8. Place all small-signal components away from high frequency switching nodes. Place decoupling capacitors for the LTC3888-1 immediately adjacent to the IC.
9. A good rule of thumb for via count in a given high current path is to use 0.5A per via. Be consistent when applying this rule.
10. Copper fills or pours are good for all power connections except as noted above in rule 3. Copper planes on multiple layers can also be used in parallel. This helps with thermal management and lowers trace inductance, which further improves EMI performance.

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## OUTPUT VOLTAGE SENSING

Accurate Kelvin sensing techniques should be used to connect the output voltage differentially back to the LTC3888-1 $V_{SENSE±}$ pins of the master channel for best output voltage regulation at the point of load. These pins also provide the ADC inputs for output voltage telemetry. These connections are not strictly required for disabled master channels (i.e. forced to be slave phases using bit 4 of MFR_PWM_MODE_LTC3888-1, with an external $I_{TH}$ connection). However, because the LTC3888-1 error amplifier is an OTA, it is sometimes advantageous to wire-OR $I_{TH}$ pins and use multiple $V_{OUT}$ sense points to provide improved power plane voltage averaging. Post-manufacture selection of the most ideal load sense point via final EEPROM programming is also possible. So in general, sound Kelvin $V_{OUT}$ sensing techniques for all LTC3888-1 master channels is recommended. Refer to Figure 28.

## CLASSICAL ANALOG OUTPUT VOLTAGE CONTROL

The LTC3888-1 employs a classical analog approach for setting output voltage when using default factory EEPROM values. This control uses the circuit of Figure 28, where external resistors R1 and R2 are used to set $V_{OUT}$ according to the following equation.

$V_{OUT}$=(R1+R2)/R2x400mV

In this mode, output margining is still possible using the OPERATION command. The margining levels, along with undervoltage and overvoltage supervisor fault thresholds, are preset according to the following table. These values are relative to the nominal output voltage created by R1 and R2.

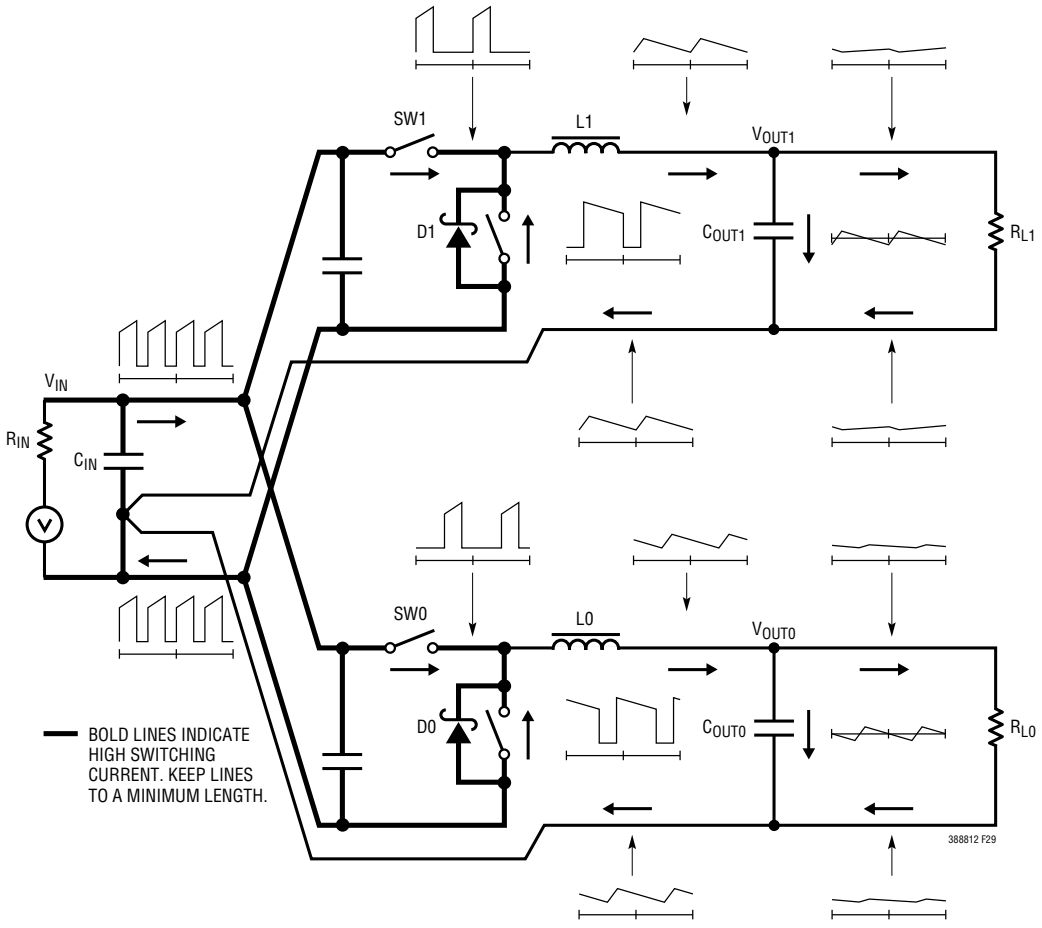


**Figure 29. High Frequency Paths and Branch Current Waveforms**

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**Table 9. Factory EEPROM Output-Related Settings**

| Quantity | PMBus Command | Value |
|---|---|---|
| UV Threshold | VOUT_UV_FAULT_LIMIT | –10% |
| Margin Low | VOUT_MARGIN_LOW | –5% |
| Margin High | VOUT_MARGIN_HIGH | +5% |
| OV Threshold | VOUT_OV_FAULT_LIMIT | +10% |

Under and overvoltage warning limits are effectively disabled by the default factory EEPROM settings. Several other points should also be carefully noted when using the LTC3888-1 default factory configuration.

1. In this mode VOUT_TRANSITION_RATE (in V/ms) applies to the $V_{FB}$ point, not $V_{OUT}$. Absolute slew rates at $V_{OUT}$ will then be scaled by a factor of (R1+R2)/R2.
2. In this mode, bit 6 of MFR_PWM_MODE_LTC3888-1 must be left clear, which is the factory default. $V_{OUT}$ servo should not be used with these EEPROM settings. Refer to PWM Control Loops in Electrical Characteristics for device tolerances that apply to $V_{OUT}$ accuracy in this case. Also refer to command details for MFR_PWM_MODE_LTC3888-1. Proper use of $V_{OUT}$ servo in full PMBus control context is covered in the next few paragraphs.

### PMBUS OUTPUT VOLTAGE CONTROL

It is also possible to utilize the full range of digitally programmable output voltage controls afforded by the PMBUs interface once external components R1 and R2 have been chosen. The following steps should be taken to properly enable this control mode on the LTC3888-1.

1. Disable the master (page) that will utilize full PMBus control by using the RUN pin or OPERATION command.
2. Program VOUT_SCALE_LOOP to a value equal to (R1+R2)/R2.
3. While internal calculations are performed to implement this change in output control mode, wait for bits[6:5] of MFR_COMMON to both be clear. This may take as much as 500ms.
4. Program VOUT_COMMAND to the value desired (range of 300mV to 3.45V). See VOUT_MAX details below for limitations on this value.
5. Program related values for $V_{OUT}$ margins, warning levels and hard supervisor thresholds (UV/OV) using good practices for the bracketing of nominal $V_{OUT}$ with these quantities.
6. Re-enable the output using RUN pin and/or OPERATION command. $V_{OUT}$ servo can also be enabled before the rail is turned on, or at any time afterward. See Using Output Voltage Servo below for details.

Once direct PMBus control of VOUT is established in this way, VOUT_TRANSITION_RATE then applies to the output voltage proper, not $V_{FB}$. Also, when using VOUT_SCALE_LOOP on the LTC3888-1, some restrictions apply.

1. VOUT_SCALE_LOOP cannot be changed on the fly. The rail must be commanded off by RUN pin or OPERATION command. Bits[6:5] of MFR_COMMON should be polled whenever this command value is written. A rail-off update time of up to 500ms may be required. During this period, processing of any other $V_{OUT}$-related commands sent to the LTC3888-1 will be delayed until new VOUT_SCALE_LOOP calcuations have completed. It is strongly recommended to set this value just once after the desired value of (R1+R2)/R2 is determined.
2. Sending $V_{OUT}$-related commands to the LTC3888-1 or re-enabling the output before the device indicates it has completed processing of VOUT_SCALE_LOOP for that channel may result in erroroneous faults or undesirable controller operation.
3. VOUT_MAX is a read-only command that returns a value based on VOUT_SCALE_LOOP, with a maximum given by the read-only value of MFR_VOUT_MAX. This calculated value sets the maximum output that can be programmed with a particular R1/R2 combination for nominal $V_{OUT}$, margin or fault. See command details for VOUT_MAX.

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### USING OUTPUT VOLTAGE SERVO

For best output voltage accuracy, enable $V_{OUT}$ servo mode on the master phase by setting bit 6 of MFR_PWM_MODE_LTC3888-1 once PMBus output control is fully programmed. In $V_{OUT}$ servo mode, the LTC3888-1 will adjust the regulated output voltage based on its related monitor ADC reading. Every time that output voltage ADC channel is converted, the $V_{OUT}$ servo will step the internal EA reference by 297.5µV until the output produces the correct ADC reading.

In order for the LTC3888-1 to servo $V_{OUT}$, VOUT_SCALE_LOOP must be used. This will allow the final $V_{OUT}$ created by the servo at any condition to have ±0.2% typical accuracy (±0.5% absolute maximum). The raw output created by the application must be within ±5.5% of VOUT_COMMAND for the $V_{OUT}$ servo to function to full effectiveness, so external feedback resistors with ±0.5% tolerance are recommended.

When the master channel is turned on, $V_{OUT}$ servo is enabled after all of the following conditions are satisfied.

- Bit 6 of MFR_PWM_MODE_LTC3888-1 Is Set
- The Soft-Start Sequence Is Complete
- A VOUT_UV_FAULT Is Not Present
- An IOUT_OC_FAULT Is Not Present

$V_{OUT}$ servo mode then engages after TON_MAX_ FAULT_LIMIT has expired as shown in Figure 30, unless that limit is set to 0s (infinite). In that case, the mode is engaged as soon as the above conditions are satisfied.

### SOFT-START AND STOP

The LTC3888-1 uses digital ramp control to create both soft-start and soft-stop.

The LTC3888-1 must enter the run state prior to soft-start. The RUN pins are released after the part initializes and $V_{IN}$ is determined to be greater than the VIN_ON threshold.

Once in the run state, soft-start is performed after any additional prescribed delay (see next section) by actively regulating the load voltage while digitally ramping the target voltage from 0V to the final expected value. Rise time of the voltage ramp can be programmed using VOUT_TRANSITION_RATE to minimize inrush currents associated with the start-up voltage ramp. The maximum rate at which the LTC3888-1 can move the output in this fashion is 100µs/step. Soft-start is disabled by setting VOUT_TRANSITION_RATE to 4V/ms. The LTC3888-1 will internally perform the math necessary to assure the voltage ramp is controlled to the desired slope. However, the voltage slope cannot be any faster than fundamental limits imposed by the power stage. The larger VOUT_TRANSITION_RATE becomes, the more noticeable an output voltage stair-step may become.

The LTC3888-1 also supports soft turn off in the same manner it controls turn on. Soft-off is performed when the RUN pin goes low or if the part is commanded off. The LTC3888-1 can produce a controlled ramp off as long as VOUT_TRANSITION_RATE is sufficiently slow to allow the control loop and power stage to achieve the desired slope. If VOUT_TRANSITION_RATE is too high to discharge the load capacitance, the output will not reach 0V. In this case, the power stage will still be commanded off at the end of soft-off and $V_{OUT}$ will decay at a rate determined by the load. The larger VOUT_TRANSITION_RATE becomes, the more noticeable an output voltage stair-step may become. If a rail faults off for any reason, all related PWM phases are instantly commanded off. The output will then decay as a function of load current.

### TIME-BASED OUTPUT SEQUENCING AND RAMPING

The LTC3888-1 TON_DELAY and TOFF_DELAY commands can be used in combination with VOUT_TRANSITION_RATE to implement a wide range of versatile sequencing and ramping schemes. The key to time-based sequencing and ramping is the ability of LTC3888-1 master phases to move their outputs up and down according to PMBus command values as shown in Figure 30 and Figure 31.

There is a fixed delay and other timing uncertainty associated with all changes in output voltage controlled by the LTC3888-1. A nominal fixed timing delay of 270µs exists to process any change in output voltage including soft-start/stop and margining. The start of all time-based output operations occur with an uncertainty of ±50µs and have a nominal step resolution of 100µs. This means the minimum controlled time delay the LTC3888-1 can produce

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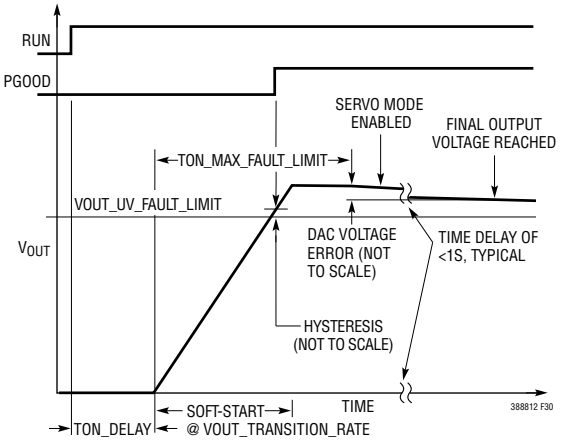


**Figure 30. Time-Based $V_{OUT}$ Turn-On with Servo**

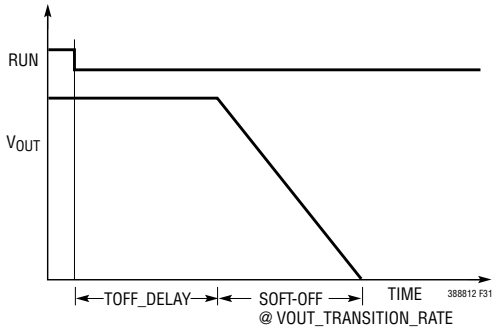


**Figure 31. Time-Based $V_{OUT}$ Turn-Off**

will range from 220µs to 320µs, not including basic oscillator tolerances. For software-based output changes (e.g., margining), this algorithmic delay begins when the STOP bit is received on the serial bus. An example of this minimum turn on/off delay and step-wise output control can be seen in Figure 33, where TON_DELAY = 0s.

To effectively implement tracking and sequencing between rails controlled by ADI digital power products, two signals should be shared between all controlling ICs: SHARE_CLK and RUN (CONTROL pin on LTC297x products). This facilitates synchronized rail sequencing on or off based on shared input supply state (VIN_ON threshold), external hardware control (RUN pin), or PMBus commands (possibly using global addressing).

Figure 33 shows an example of output supply sequencing using TON_DELAY.

Conventional coincident and ratiometric tracking can also be emulated by setting equivalent turn-on/off delays and appropriate rates as shown in Figure 34 and Figure 35.

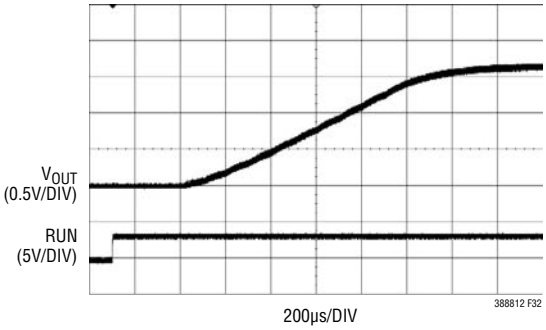


**Figure 32. Example of Fixed LTC3888-1 Processing Delay and Soft-Start**

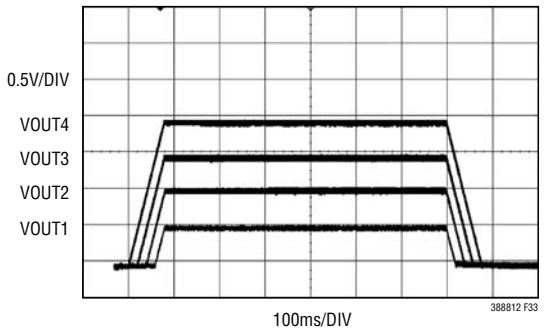


**Figure 33. LTC3888-1 Time-Based Supply Sequencing**

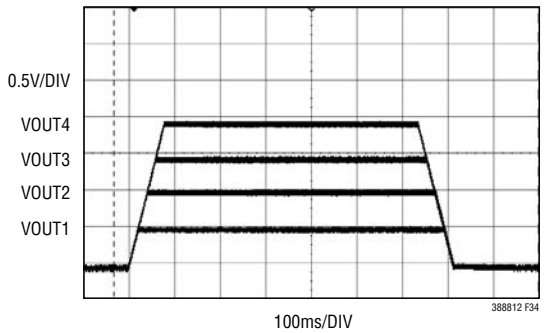


**Figure 34. LTC3888-1 Time-Based Coincident Supply Ramping**

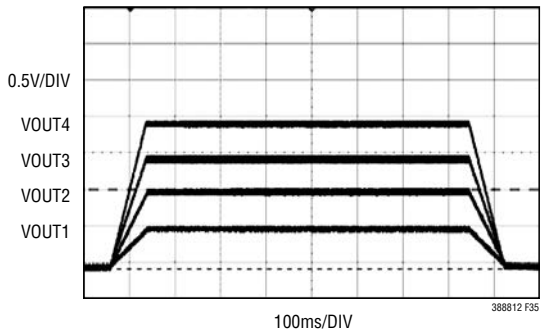


**Figure 35. LTC3888-1 Time-Based Ratiometric Supply Ramping**

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In addition, these schemes can easily be mixed and matched to create any necessary ramping controls, some of which might prove difficult to implement with conventional analog-only controllers. These programmable features greatly simplify system development because rails can be resequenced without a hardware change as final product requirements evolve. The LTpowerPlay GUI and LTC3888-1 onboard EEPROM can be used for this task, avoiding the need for firmware development to modify turn on/off relationships between rails. Entire power systems can easily be scaled up or down, facilitating reuse of proven hardware macro designs.

### VOLTAGE-BASED OUTPUT SEQUENCING

The LTC3888-1 is capable of voltage-based output sequencing. For concatenated events between members of the ADI PSM family, it is possible to control one RUN pin from a $\overline{\text{GPIO}}$, $\overline{\text{FAULT}}$ or PGOOD pin of a different controller. A hardware configuration of the type shown in Figure 36 disables the next downstream controller anytime the upstream output is below the specific UV threshold. If $\overline{\text{GPIO}}$ or $\overline{\text{FAULT}}$ is used, the controlling output must be configured to only propagate VOUT_UV_UF, and that IC must have its MFR_GPIO/FAULT_RESPONSE set to ignore (0x00). Use of the unfiltered $V_{OUT}$ UV fault limit is recommended because there is less delay between crossing the UV threshold and the $\overline{\text{GPIO}}$/$\overline{\text{FAULT}}$ pin releasing. When $\overline{\text{GPIO}}$/$\overline{\text{FAULT}}$ UV propagation is utilized, an output deglitching filter can ensure the control does not toggle repeatedly at lower values of output transition due to noise on $V_{OUT}$. If unwanted transitions still occur with only the internal filter found on most ADI PSM deviced (typically 250µs), place a capacitor to ground on the output pin. The RC time-constant of the filter should be low enough to assure no appreciable delay is incurred. A value of 300µs to 500µs will provide some additional filtering without significant delay of the trigger event.

When the system is turned off, rails will shut down in the same order as they turn on, as shown in Figure 37. If a different sequence is required, the circuit must be rewired or delays must be added by programming TON_DELAY or TOFF_DELAY. A fundamental limitation of this application When the system is turned off, rails will shut down in the same order as they turn on, as shown in Figure 37. If a different sequence is required, the circuit must be rewired or delays must be added by programming TON_DELAY or TOFF_DELAY. A fundamental limitation of this application is the inability of upstream rails to detect a start-up failure of downstream rails. Due to this, cascade sequencing should not be implemented without an external fast supervisor to monitor downstream rails and assert a system fault if problems occur.

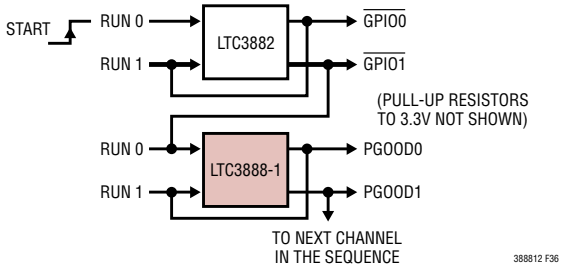


**Figure 36. Cascade Sequencing Configuration Example**

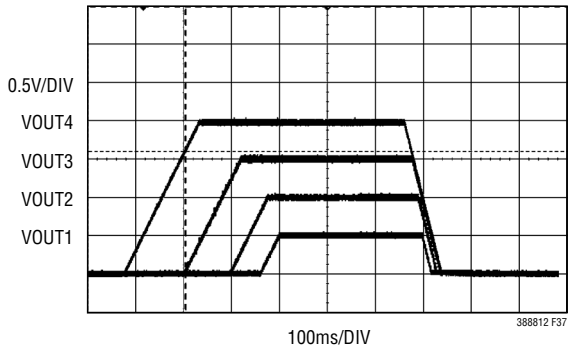


**Figure 37. Cascade Sequencing Waveforms**

### PWM FREQUENCY SYNCHRONIZATION

The LTC3888-1 incorporates an internal phase-locked loop (PLL) which enables synchronization of all PWM channels to an external CMOS clock from 250kHz to 1MHz. The PLL is locked to the falling edge of the SYNC pin clock signal. For synchronization required by the application, SYNC may be driven from a separate source, including another LTC3888-1 or other ADI PSM device. If SYNC is not externally clocked, the PWMs will operate at the frequency specified by the FREQUENCY_SWITCH command.

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All ICs of a PolyPhase rail may be required to share SYNC pins. If phase expansion for a single rail is all that is required, the IC providing the master clock simply drives the clock slave IC SYNC input with its CLKOUT. If SYNC is shared between ADI PSM devices, only one device should be programmed to control the SYNC output. Refer to the following section for additional PolyPhase details.

The PLL generates very accurate channel phase relationships which can be selected with MFR_PWM_CONFIG_LTC3888-1. For PolyPhase applications, all phases should be spaced evenly around the unit circle for best results. For instance, a 4-phase system should use a separation of 90° between channels.

The PLL has a lock detection circuit. If the PLL should lose lock during operation, bit 4 of the STATUS_MFR_SPECIFIC command is asserted and the $\overline{\text{ALERT}}$ pin is pulled low, if not masked. The fault can be cleared by writing a 1 to STATUS_MFR_SPECIFIC bit 4.

### POLYPHASE OPERATION AND LOAD SHARING

Single IC PolyPhase LTC3888-1 configuration are controlled by bits [2:0] of MFR_PWM_CONFIG_LTC3888-1. All necessary slave phase control is managed internal to the device in this case. When operating a high power rail requires between ten and sixteen phases, the LTC3888-1 affords dual-IC phase expansion to keep those phases ideally spaced around the unit circle as shown in Figure 38. To do this, bit 3 of MFR_PWM_CONFIG_LTC3888-1 is set, making that device the clock master. The PGOOD0 pin is redefined to provide CLKOUT to drive the SYNC input of the second LTC3888-1. A pull-up resistor to 3.3V is still required on CLKOUT. Bits[2:0] of MFR_PWM_CONFIG_LTC3888-1 are then set to the same value on both ICs, yielding the following additional dual-IC rail configurations:

- 10+(1 or 3)+(1 or 3)
- 12+(1 or 2)+(1 or 2)
- 14+1+1
- 16-phase

As shown in Figure 38 master channel 0 and its assigned slaves from the two ICs combine to form a single high phase count rail with ideal phase separation, in this case 360/12 = 30 degrees. While a great deal of flexibility exists in utilizing the remaining voltage control loops and slaves, some phasing limitations do exist. For example, in a 10-phase case, the remaining three phases on each IC are separated by 120 degrees, so a 2-phase rail built from one of those loops would not be capable of 180° phasing. The two remaining loops would also not produce uniform 60° separation if combined into a single 6-phase rail. While none of the phases on these remaining two 3-phase loops overlap each other, one or more may overlap those of the primary high count rail.

Whether using the phase expansion feature of the LTC3888-1 or not, the following pins should be shared between two or more devices devices on a large PolyPhase rail:

- $V_{IN}$ (if separatre ICs)
- $V_{SENSE}\pm$ (see previous Output Voltage Sensing discussion)
- $I_{TH}$ / $I_{THR}$
- TSNS/VDR_MON
- SYNC (if not using phase expansion)
- $I^2C$ bus pins (SCL, SDA)
- $\overline{\text{ALERT}}$
- $\overline{\text{FAULT}}$ pins
- RUN
- SHARE_CLK (if separate ICs)

When $I_{TH}$ pins are shorted, one $I_{THR}$ pin can be selected to apply primary loop compensation, with all other $I_{THR}$ pins shorted to the common $I_{TH}$. Alternatively, all $I_{THR}$ pins can be shorted, making the effective resistance the parallel combination of all these $R_{ITH}$. This will reduce dynamic range of $R_{ITH}$ but will increase programming resolution.

Linear regulator outputs such as $V_{DD33}$ and resistor configuration pins, including $R_{SET}$, should not be shared between devices. PGOOD may be shared between all master channels on a single rail, or a single PGOOD output can be selected to indicate the rail output voltage is in regulation.

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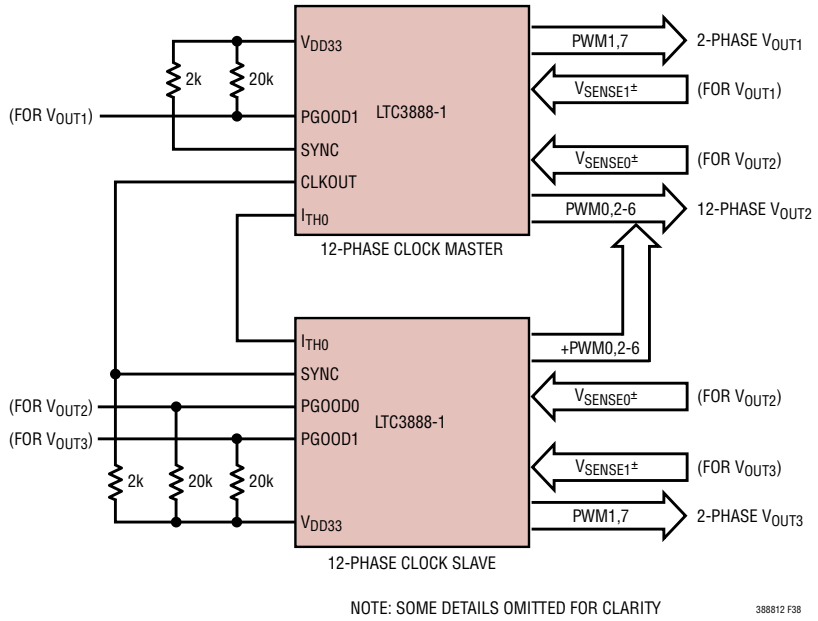


**Figure 38. Simplified Schematic Showing 12 + 2 + 2 Phase Expansion**

At any point that additional output current is required without the need for additional phase separation, it is always possible to simply add overlapping phases on an LTC3888-1 rail. For example, two LTC3888-1s can be combined to provide two 5-phase rails with a third 6-phase rail with two PWMs driving each phase. In this case, SYNC would be shared between the ICs (one configured as clock master) and all rails would have phases with the desired uniform spacing around the unit circle. Refer to Figure 39.

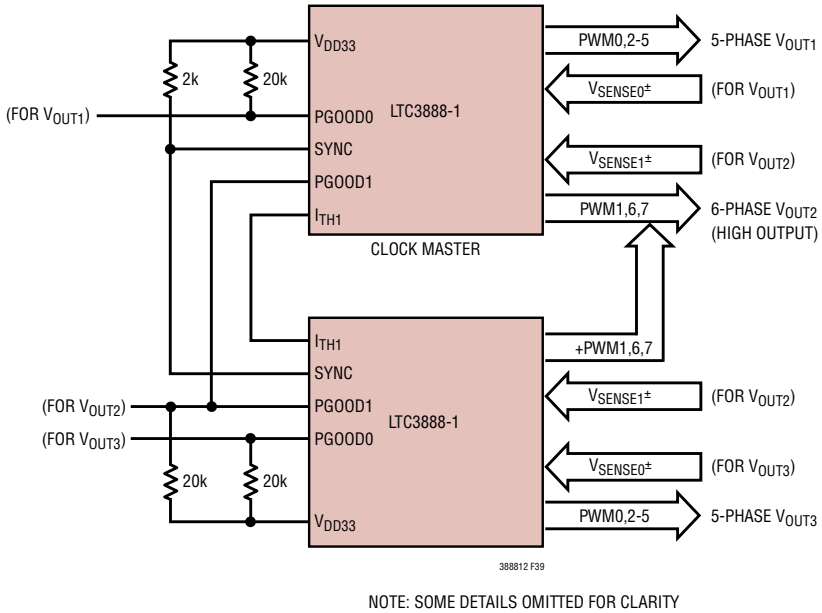


**Figure 39. Simplified Schematic Showing 5+5+6 Application**

## APPLICATIONS INFORMATION

Load sharing accuracy is based on the power stage output current monitor interface of each slave phase. The gain matching errors of these channels tend to be small and negligible. The input-referred offset of the LTC3888-1 current interface is trimmed at the factory but will still dominate the sharing error budget, especially at lower phase current levels. Specifications for on-chip and off-chip output current matching are given in the Electrical Characteristics table. These specifications do not include the current error created by mismatch of the output current monitors of the individual power stages.

Every master channel on a rail should use identical values for all PMBus commands related to output voltage control (including margin and start/stop timing), input and output warning limits (both voltage and current), all fault limits and associated responses, and all PWM configuration controls. The correct current sense gain should also be set for each master (IOUT_CAL_GAIN) to achieve accurate $I_{OUT}$ telemetry and consistent fault handling across phases.

A PolyPhase power supply significantly reduces the amount of ripple current in both the input and output capacitors. The RMS input ripple current is divided by, and the effective ripple frequency is multiplied by, the number of phases used as long as the input voltage is greater than the number of phases times the output voltage. Output voltage ripple amplitude is also reduced by the number of phases used. Figure 40 graphically illustrates the principle.

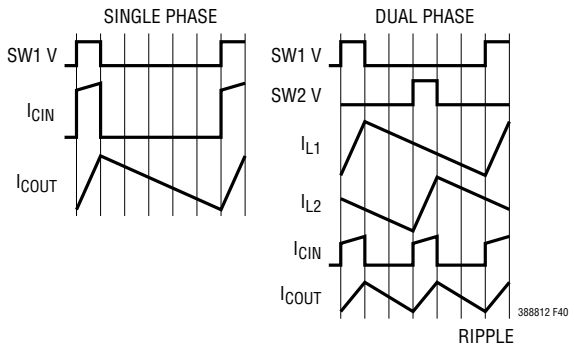


**Figure 40. Single and 2-Phase Current Waveforms**

The worst-case RMS ripple current for a single stage design peaks at an input voltage of twice the output voltage. The worst case RMS ripple current for a 2-phase design peaks at output voltages of one-quarter and three-quarters of the input voltage. When the RMS current is calculated, higher effective duty factor results and the peak current levels are divided as long as the current in each stage is balanced. Refer to Application Note 19 for a detailed description of how to calculate RMS current for a single stage switching regulator. Figure 41 and Figure 42 illustrate how the input and output currents are reduced by using an additional phase. For a 2-phase converter, the input current peaks drop in half and the frequency is doubled. The input capacitor requirement is then theoretically reduced by a factor of four.

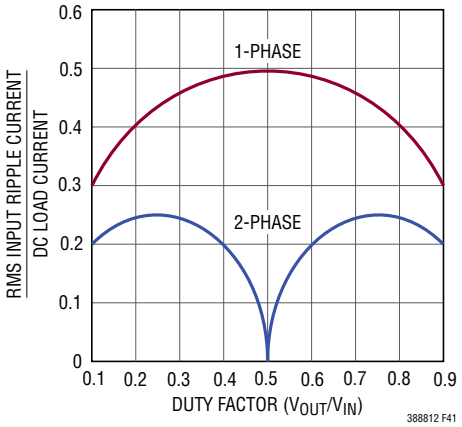


**Figure 41. Normalized RMS Input Ripple Current**

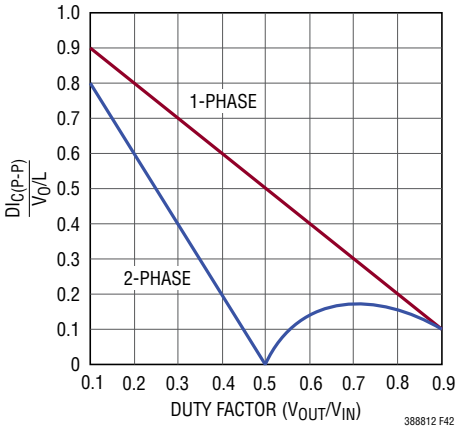


**Figure 42. Normalized Output Ripple Current**

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## RESISTOR CONFIGURATION PINS

As a factory default, the LTC3888-1 is programmed to use external resistor configuration, allowing output current limit, PWM frequency and phasing, and the PMBus address to be set without programming the part through its serial interface or purchasing devices with custom EEPROM contents. An 18.7kΩ resistor with a tolerance of 1% or better must be wired between the $R_{SET}$ pin and GND. This component establishes the correct bias level for the remaining RCONFIG pins, which are programmed with a resistor to GND. The RCONFIG pins are only interrogated at initial power up and during a reset, so modifying their values on the fly is not recommended. RCONFIG pins on the same IC can share a single resistor if they require identical programming. Resistors with a tolerance of 1% or better must be used to assure proper operation. Noisy clock signals should not be routed near these pins.

Output current limit can be set as shown in Table 10. For example, setting this resistor to 4.42kΩ is equivalent to programming a IOUT_OC_WARN_LIMIT value of 32A with IOUT_OC_FAULT_LIMIT set to 40A.

**Table 10. Resistor Programming of OC Warning and Fault Limits**

| $R_{CONFIG}$ (kΩ) | IOUT_OC_WARN_LIMIT (A) | IOUT_OC_FAULT_LIMIT (A) |
|---|---|---|
| OPEN | from EEPROM | from EEPROM |
| 11.8 | 68 | 85 |
| 10.2 | 64 | 80 |
| 9.31 | 60 | 75 |
| 8.66 | 56 | 70 |
| 7.87 | 52 | 65 |
| 7.15 | 48 | 60 |
| 6.49 | 44 | 55 |
| 5.9 | 40 | 50 |
| 5.11 | 36 | 45 |
| 4.42 | 32 | 40 |
| 3.74 | 28 | 35 |
| 3.09 | 24 | 30 |
| 2.43 | 20 | 25 |
| 1.74 | 16 | 20 |
| 1.02 | 12 | 15 |
| GND | 8 | 10 |

Any of the single-IC master/slave configurations that the LTC3888-1 supports can be programmed with PWM_CFG using one of two frequencies as shown in Table 11. Phase expansion is not supported when using an external resistor to set master/slave configuration.

**Table 11. PWM_CFG Resistor Programming**

| $R_{CONFIG}$ (kΩ) | MFR_PWM_CONFIG_LTC3888-1[3:0] | | SWITCHING FREQUENCY (kHz) |
|---|---|---|---|
| | BINARY | MASTER/SLAVE | |
| OPEN | from EEPROM | | |
| 11.8 | 0111 | 7 + 1 | 550 |
| 10.2 | 0110 | 6 + 2 | |
| 9.31 | 0101 | 6 + 1 | |
| 8.66 | 0100 | 5 + 3 | |
| 7.87 | 0011 | 4 + 4 (or 8-phase) | |
| 7.15 | 0010 | 4 + 3 | |
| 6.49 | 0001 | 4 + 2 | |
| 5.9 | 0000 | 3 + 3 | |
| 5.11 | 0111 | 7 + 1 | 450 |
| 4.42 | 0110 | 6 + 2 | |
| 3.74 | 0101 | 6 + 1 | |
| 3.09 | 0100 | 5 + 3 | |
| 2.43 | 0011 | 4 + 4 (or 8-phase) | |
| 1.74 | 0010 | 4 + 3 | |
| 1.02 | 0001 | 4 + 2 | |
| GND | 0000 | 3 + 3 | |

The LTC3888-1 address is selected based on the programming of the two configuration pins ASEL0 and ASEL1 according to Table 12. ASEL0 programs the bottom four bits of the device address for the LTC3888-1, and ASEL1 programs the three most-significant bits. Either portion of the address can also be retrieved from the MFR_ADDRESS value in EEPROM. If both pins are left open, the full 7-bit MFR_ADDRESS value stored in EEPROM is used to determine the device address. It is recommended that each LTC3888-1 in a system have a unique address, and the ASEL pins provide an efficient way to accomplish this without a plethora of custom EEPPOM programming. The LTC3888-1 also responds to 7-bit global addresses 0x5A and 0x5B. MFR_ADDRESS and MFR_RAIL_ADDRESS should not be set to either of these values.

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**Table 12. Resistor Programming of MFR_ADDRESS**

| $R_{CONFIG}$ (kΩ) | ASEL1 | | ASEL0 | |
|---|---|---|---|---|
| | DEVICE ADDRESS BITS[6:4] | | DEVICE ADDRESS BITS[3:0] | |
| | BINARY | HEX | BINARY | HEX |
| OPEN | from EEPROM | | from EEPROM | |
| 11.8 | | | 1111 | F |
| 10.2 | | | 1110 | E |
| 9.31 | | | 1101 | D |
| 8.66 | | | 1100 | C |
| 7.87 | | | 1011 | B |
| 7.15 | | | 1010 | A |
| 6.49 | | | 1001 | 9 |
| 5.9 | | | 1000 | 8 |
| 5.11 | 0111 | 7 | 0111 | 7 |
| 4.42 | 0110 | 6 | 0110 | 6 |
| 3.74 | 0101 | 5 | 0101 | 5 |
| 3.09 | 0100 | 4 | 0100 | 4 |
| 2.43 | 0011 | 3 | 0011 | 3 |
| 1.74 | 0010 | 2 | 0010 | 2 |
| 1.02 | 0001 | 1 | 0001 | 1 |
| GND | 0000 | 0 | 0000 | 0 |

## INTERNAL REGULATOR OUTPUTS

The $INTV_{CC}$ pin provides supply current for much of the internal LTC3888-1 analog circuitry at a nominal value of 5.2V. The LTC3888-1 features an internal linear regulator that can be used to supply 5.2V to $INTV_{CC}$ from the primary $V_{IN}$ supply. At lower supply voltages, the LTC3888-1 will also accept an external 5V supply attached to this pin if $V_{IN}$ and $INTV_{CC}$ are shorted. If the internal 5.2V LDO is used, $INTV_{CC}$ must be bypassed to GND with a low ESR X5R or X7R ceramic capacitor with a value between 1µF and 4.7µF. If an external 5V source supplies $V_{IN}$ and $INTV_{CC}$, a local low ESR bypass capacitor with a value between 0.01µF and 0.1µF should be placed directly between the shorted power pins and GND.

$INTV_{CC}$ powers secondary internal 3.3V and 2.5V LDOs whose outputs are present on $V_{DD33}$ and $V_{DD25}$, respectively. The 3.3V supply provides power for internal auxillary circuits, and the 2.5V supply provides power for much of the internal processor logic on the LTC3888-1. Both of these LDO outputs should be bypassed directly to GND with a low ESR X5R or X7R ceramic capacitor with a value of 1µF or greater.

Do not draw any external system current from these LDO supplies beyond that required for specific LTC3888-1 configuration or load/pull-up resistors.

## IC JUNCTION TEMPERATURE

The user must ensure that the maximum rated junction temperature is not exceeded under all operating conditions. The thermal resistance of the LTC3888-1 package ($\theta_{JA}$) is 36°C/W, provided the exposed pad is in good thermal contact with the PCB. The actual thermal resistance in the application will depend on forced air cooling and other heat sinking means, especially the amount of copper on the PCB to which the LTC3888-1 is attached. The following formula may be used to estimate the maximum average power dissipation $P_D$ (in watts) of the LTC3888-1.

$$P_D = V_{IN}(.03 + I_{EXT} + I_{RC25})$$

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where:

$I_{EXT}$ = total external load drawn from $V_{DD33}$, including local pull-up resistors, in amps

$I_{RC25}$ = total current drawn from $V_{DD25}$ by LTC3888-1 configuration resistors, in amps

and $f_{PWM}$ is the PWM switching frequency in kHz

The maximum junction temperature of the LTC3888-1 in °C may then be found from the following equation

$$T_J = T_A + 36 \bullet P_D$$

with ambient temperature $T_A$ expressed in °C

### DERATING EEPROM RETENTION AT TEMPERATURE

EEPROM read operations between 85°C and 125°C will not affect data storage. But retention will be degraded if the EEPROM is written above 85°C or stored or operated above 125°C. If an occasional fault log is generated above 85°C, the slight reduction in data retention in the EEPROM fault log area will not affect the use of the function or other EEPROM storage. See the Operation section for other high temperature EEPROM functional details. Degradation in data retention can be approximated by calculating the dimensionless acceleration factor using the following equation.

$$AF = e^{\left[\left(\frac{Ea}{k}\right)\bullet\left(\frac{1}{T_{USE}+273}-\frac{1}{T_{STRESS}+273}\right)\right]}$$

Where:

AF = acceleration factor

Ea = activation energy = 1.4eV

$k = 8.617 \bullet 10^{-5}$ eV/°K

$T_{USE}$ = is the specified junction temperature

$T_{STRESS}$ = actual junction temperature in °C

As an example, if the device is stored at 130°C for 10 hours,

$T_{STRESS}$ = 130°C, and

$$AF = e^{\left[\left(\frac{1.4}{8.617\bullet10^{-5}}\right)\bullet\left(\frac{1}{398}-\frac{1}{403}\right)\right]} = 1.66$$

indicating the effect is the same as operating the device at 125°C for 10 • 1.66 = 16.6 hours, resulting in a retention derating of 6.6 hours.

### CONFIGURING OPEN-DRAIN PINS

The LTC3888-1 has the following open-drain pins:

- 3.3V Pins
  1. PGOOD0/CLKOUT
  2. PGOOD1
  3. $\overline{\text{FAULT0}}$, $\overline{\text{FAULT1}}$
  4. SYNC
  5. SHARE_CLK
- 5V Capable Pins

(These pins operate correctly when pulled to 3.3V.)

1. RUN0, RUN1
2. $\overline{\text{ALERT}}$
3. SCL
4. SDA

Most of the above pins have on-chip pull-down transistors that can sink 3mA at 0.4V. The low state threshold on these pins provides ample noise margin with 3mA of current. For 3.3V pins, 3mA of current is produced by a 1.1k pull-up resistor. Unless there are transient speed issues associated with the RC time constant of the net, a 10k resistor or larger is generally recommended.

The pull-up resistor for PGOOD should be terminated to the LTC3888-1 $V_{DD33}$ pin or a separate bias supply under 3.6V that is up before the LTC3888-1 is enabled. Otherwise, power-not-good may be falsely indicated after the PWM outputs are running.

For high speed signals such as SDA and SCL, a lower value resistor may be required. The RC time constant should be set to one-third to one-fifth the required rise time to avoid timing issues. For a 100pF load and a 400kHz

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PMBus communication rate, the resistor pull-up on the SDA and SCL pins with the time constant set to one-third the required rise time equals

$$R_{PULLUP} = \frac{t_{RISE}}{3 \bullet 100pF} = 1k\Omega$$

The closest 1% resistor value is 1kΩ. Limit to 1.1kΩ for best noise margin.

Be careful to minimize parasitic capacitance on the SDA and SCL lines to avoid communication problems. To estimate the loading capacitance, monitor the signal in question and measure how long it takes for the desired signal to reach approximately 63% of the output value. This is one time constant.

The SYNC pin has an on-chip pull-down transistor with the output held low for nominally 500ns when driven by the LTC3888-1. If the internal oscillator is set for 500kHz and the load is 100pF with a one-third rise time required, the resistor calculation is as follows:

$$R_{PULLUP} = \frac{2\mu s - 500ns}{3 \bullet 100pF} = 5.0k\Omega$$

The closest 1% resistor is 4.99kΩ .

If timing errors are occurring or if the SYNC amplitude is not as large as required, monitor the waveform and determine if the RC time constant is too long for the application. If possible reduce the parasitic capacitance. Otherwise reduce the pull-up resistor sufficiently to assure proper operation.

Similar results (R < 5kΩ) should be applied to the PGOOD0 output when configured as CLKOUT to ensure proper clocking of the slave IC.

The SHARE_CLK output has a nominal period of 10µs and is pulled low for about 1µs. If the system load on this shared line is 100pF, the resistor calculation for this line with a one-third rise time is:

$$R_{PULLUP} = \frac{9\mu s}{3 \bullet 100pF} = 30k\Omega$$

The closest 1% resistor is 30.1kΩ .

### PMBUS COMMUNICATION AND COMMAND PROCESSING

The LTC3888-1 has a one deep buffer to hold the last data written for each supported command prior to processing, as shown in Figure 43. Two distinct parallel sections of the LTC3888-1 manage command buffering and command processing to ensure the last data written to any command is never lost. When the part receives a new command from the bus, command data buffering copies the data into the write command data buffer and indicates to the internal processor that data for that command should be handled. The internal processor runs in parallel and performs the sometimes slower task of fetching, converting (to internal format) and executing commands marked for processing.

Some computationally intensive commands (e.g., timing parameters, temperatures, voltages and currents) have internal processor execution times that may be long relative to PMBus timing. If the part is busy processing a command, and a new command(s) arrives, execution may be delayed or processed in a different order than received. The part indicates when internal calculations are in process with bit 5 of MFR_COMMON (Internal Calculations Not Pending). When the internal processor is busy calculating, bit 5 is cleared. When this bit is set, the part is ready for another command. An example polling loop is provided in Figure 44, which ensures that commands are processed in order while simplifying error handling routines. MFR_COMMON always returns valid data at PMBus speeds between 10kHz and 400kHz.

When the part receives a new command while it is busy, it will communicate this condition using standard PMBus protocol. Depending on device configuration and state it may either NACK the command or return all ones (0xFF) for reads. It may also generate a BUSY fault and $\overline{\text{ALERT}}$ notification, or stretch the SCL clock low. For more information refer to PMBus Specification V1.2, Part II, Section 10.8.7 and SMBus V2.0 section 4.3.3. Clock stretching can be enabled by asserting bit 1 of MFR_CONFIG_ALL. Clock stretching will only occur if enabled and the bus communication speed exceeds 100kHz.

PMBus protocols for busy devices are well accepted standards but can make writing system level software

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somewhat complex. The part provides three handshaking status bits which reduce this complexity while enabling robust system level communication. The three hand shaking status bits are in the MFR_COMMON register. When the part is busy executing an internal operation, it will clear bit 6 of MFR_COMMON (Chip Not BUSY). When internal calculations are in process, the part will clear bit 5 of MFR_COMMON (Internal Calculations Not Pending). When the part is busy specifically because it is transitioning $V_{OUT}$ (margining or on/off) it will clear bit 4 of MFR_COMMON (Output Not In Transition). These three status bits can be polled with a PMBus read byte of the MFR_COMMON register until all three bits are set. A command immediately following all these status bits being set will be accepted without a NACK, BUSY fault or $\overline{\text{ALERT}}$ notification. The part can NACK commands for

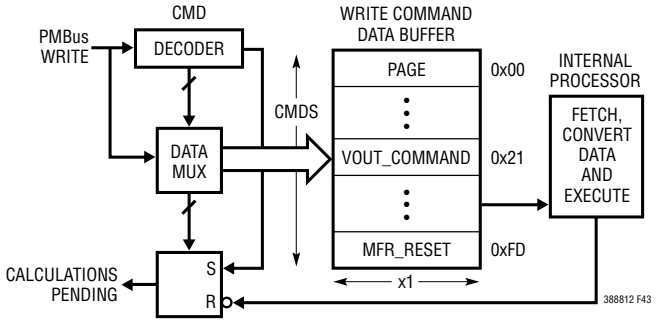


**Figure 43. Write Command Data Processing**

other reasons, however, as required by the PMBus specification (e.g., an invalid command or data).

An example of a robust command write algorithm for the VOUT_COMMAND register is provided in Figure 44. It is recommended that all command writes be preceded with such a polling loop to avoid the extra complexity of dealing with busy behavior or unwanted $\overline{\text{ALERT}}$ notifications. A simple way to achieve this is to embed the polling in subroutines to write command bytes and words. This polling mechanism will allow system software to remain clean and simple while robustly communicating with the part.

When communicating using bus speeds at or below 100kHz, the polling mechanism previously shown provides a simple solution that ensures robust communication without clock stretching. At bus speeds in excess of 100kHz, it is strongly recommended that the part be enabled to use clock stretching, requiring a PMBus master that supports that function. Clock stretching does not allow the LTC3888-1 to communicate reliably on busses operating above 400kHz. Operating the LTC3888-1 with PMBus SCL rates above 400kHz is not recommended. System software that detects and properly recovers from the standard PMBus NACK responses or BUSY faults described in PMBus Specification V1.2, Part II, Section 10.8.7 is required to communicate above 100kHz without clock stretching.

Refer to Application Note 135 for techniques that may also apply to implement a robust PMBus interface to the LTC3888-1.

### STATUS AND FAULT LOG MANAGEMENT

Due to internal operation, very infrequently the LS byte of STATUS_WORD may be inconsistent with the state of bits in the MS byte. This condition is quite transient and can normally be resolved by simply re-reading STATUS_WORD.

If power is lost during an internal store of a fault log to EEPROM, a partial write of the log can result. In this situation, the LTC3888-1 will indicate that a partial fault log is present the next time adequate supply voltage is applied by setting bit 3 of STATUS_MFR_SPECIFIC and bit 4 of STATUS_CML. Additional logging remains disabled. The only way to then determine how much of the log is actually valid is by subjective evaluation of the contents of each log event record. MFR_FAULT_LOG_CLEAR will permanently erase a partial fault log, allowing a subsequent log to be written. It is a good practice to always check for a partial fault log at power-up if fault logging is enabled (bit 7 of MFR_CONFIG_ALL).

**Refer to Fault Log Details in the Operation section for more details.**

### LTPOWERPLAY – AN INTERACTIVE DIGITAL POWER GUI

LTpowerPlay is a powerful Windows-based development environment that supports Analog Devices Power System Management ICs, including the LTC3888-1. LTpowerPlay can be used to evaluate ADI products by connecting to

## APPLICATIONS INFORMATION

an Analog Devices demo circuit or user application. LTpowerPlay can also be used offline (no hardware present) to build multiple IC configuration files that can be saved and later reloaded. LTpowerPlay uses the DC1613 USB-to-I$^2$C/SMBus/PMBus controller to communicate with a system for evaluation, development or debug. The software also features automatic update to remain up-to-date with the latest application code and documentation available from Analog Devices. A great deal of context sensitive help is available within LTpowerPlay, along with several tutorials.

```
// wait until bits 6, 5, and 4 of MFR_COMMON are all set
do
{
        mfrCommonValue = PMBUS_READ_BYTE(0xEF);
        partReady = (mfrCommonValue & 0x68) == 0x68;
}while(!partReady)

// now the part is ready to receive the next command
PMBUS_WRITE_WORD(0x21, 0x2000); //write VOUT_COMMAND to 2V
```

**Figure 44. Example of a Polling Loop to Write VOUT_COMMAND**

### INTERFACING TO THE DC1613

The ADI DC1613 USB-to-I$^2$C/SMBus/PMBus controller can be interfaced to the LTC3888-1 on any board for programming, telemetry and system debug. This includes the DC2652 from Analog Devices, or any customer target system. The controller, when used in conjunction with LTpowerPlay, provides a powerful way to debug an entire power system. Faults are quickly diagnosed using telemetry, status registers and the fault log. A final design configuration can be quickly developed and stored to the LTC3888-1 EEPROM and/or LTpowerPlay configuration file.

The DC1613 can communicate with, program and even power one or more LTC3888-1devices, regardless of whether system power is present. The DC2086 Powered Programming Adapter can be used to extend the power sourcing capability of the DC1613. Figure 45 illustrates an application schematic for in-system programming of multiple LTC3888-1 devices normally powered from $V_{IN}$. If the DC2086 is used, PFETs with lower $R_{DS(ON)}$, such as the SiA907EDJT, should be used in place of the Si2305CDS devices. If system power is not present, the

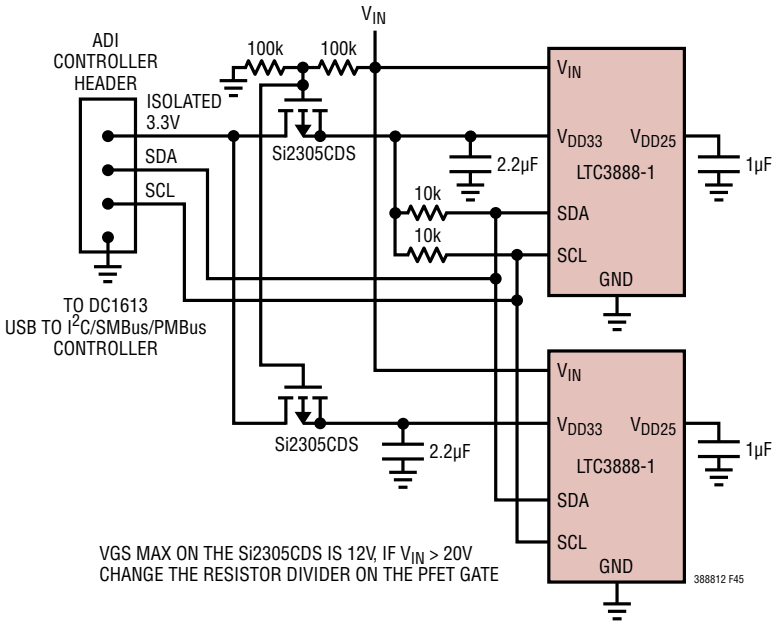


**Figure 45. DC1613 Connections**

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DC1613 or DC2086 will power the LTC3888-1 $V_{DD33}$ supply, allowing in-circuit configuration or manufacturing customization. With $V_{DD33}$ applied in this fashion, the device(s) can be initialized when the system is not powered by using PMBus address 0x5B to send a value of 0x2B to command 0xBD. If this is followed with a value of 0xC4 to 0xBD at address 0x5B, the LTC3888-1 will begin to communicate and allow PMBus command values to be updated at its normal PMBus device address. Any changes will become permanent (stored to EEPROM) by a subsequent STORE_USER_ALL command. When $V_{IN}$ is reapplied, MFR_RESET must be excuted to establish normal operation if command 0xBD has been used for communication in the absence of system power.

The DC1613 $I^2C$ connections are opto-isolated from the host PC USB. The DC1613 3.3V current limit is only 100mA, so it should be used to power only one or two LTC3888-1 devices in-system. Because of this limited current sourcing capability, only the LTC3888-1 devices, their associated pull-up resistors and the $I^2C$ pull-up resistors should be powered from the isolated 3.3V supply provided by the DC1613. Using the DC2086 will enable in-system programming of several tens of LTC3888-1 devices without normal system power applied. Some small current, normally less than 1mA, may be driven back into the internal $INTV_{CC}$ LDO output or $V_{IN}$ supply by each LTC3888-1 when power is applied only to $V_{DD33}$.

Any other device sharing the $I^2C$ bus with the LTC3888-1 should not have internal body diodes between SDA/SCL pins and their respective logic supply, because this will interfere with bus communication in the absence of system power. Configure both masters to be off, for example by driving both RUN pins low, to avoid providing power to the load until the part is fully configured.

### DESIGN EXAMPLE

As a design example, consider a 280W dual output application such as the one shown in Figure 46, where $V_{IN}$ = 12V, $V_{OUT0}$ = 1V, and $V_{OUT1}$ = 1.8V. Both rails support a rated load of 100A. The TDA21470 is chosen as the power stage for both rails based on its output current capability, feature set, and small package size. Assume that an auxillary 5V supply VDR will be available in the system for TDA21470 power requirements. Details are shown in Figure 46 for biasing and bypassing one of the power stages. This detail is not shown for the remaining seven TDA21470 devices but should be repeated for each (including $V_{IN}$ bypass and output filter capacitance), with components located close to each device using the PCB layout guidelines given in previous discussion.

The necessary local bypassing is then provided for the LTC3888-1 $INTV_{CC}$ (4.7µF), $V_{DD33}$ (2.2µF) and $V_{DD25}$ (1µF) LDO outputs. These LDO outputs should not be shared with outputs of other ICs that might have the same name, because they have independent internal control loops.

Next, the regulated output for each rail is established by selecting suitable values for R284, R285 ($V_{OUT1}$), R277 and R278 ($V_{OUT0}$). Maintaining a total load on DAOUT of 50kΩ to 100kΩ is recommended.

The PWM_CONFIG pin is left open to select the factory default master/slave configuration (4+4) and a PWM operating frequency (FREQUENCY_SWITCH) of 500kHz, both of which are desired targets for this appliation. In this configuration the four phases of each rail are separateed by 90°, and none of the eight phases overlap, producing the lowest input and output ripple possible.

The design will plan on a nominal output ripple of about 55% of $I_{OUT}$ to minimize the magnetics volume, and the inductance value is chosen based on this assumption. Each phase supplies an average of 25A to the output at full load, resulting in a ripple of $14A_{P-P}$ in each choke. A 215nH inductor would create this peak-to-peak ripple at 500kHz on the 1.8V rail. (Ripple on the 1V rail will be less.) A Cooper FP1007R3-R22-R 220nH inductor is selected with a 50A saturation current limit at room temperature.

For input filtering, a bank of six 270µF Panasonic OS_CON capacitors are selected to provide acceptable AC impedance against the designed converter ripple current. High frequency bypassing (1Ω into 2.2µF) is provided for the LTC3888-1 itself, and additional ceramic bulk bypass local to each power stage will also lower ESR on this input at higher frequencies.

# APPLICATIONS INFORMATION

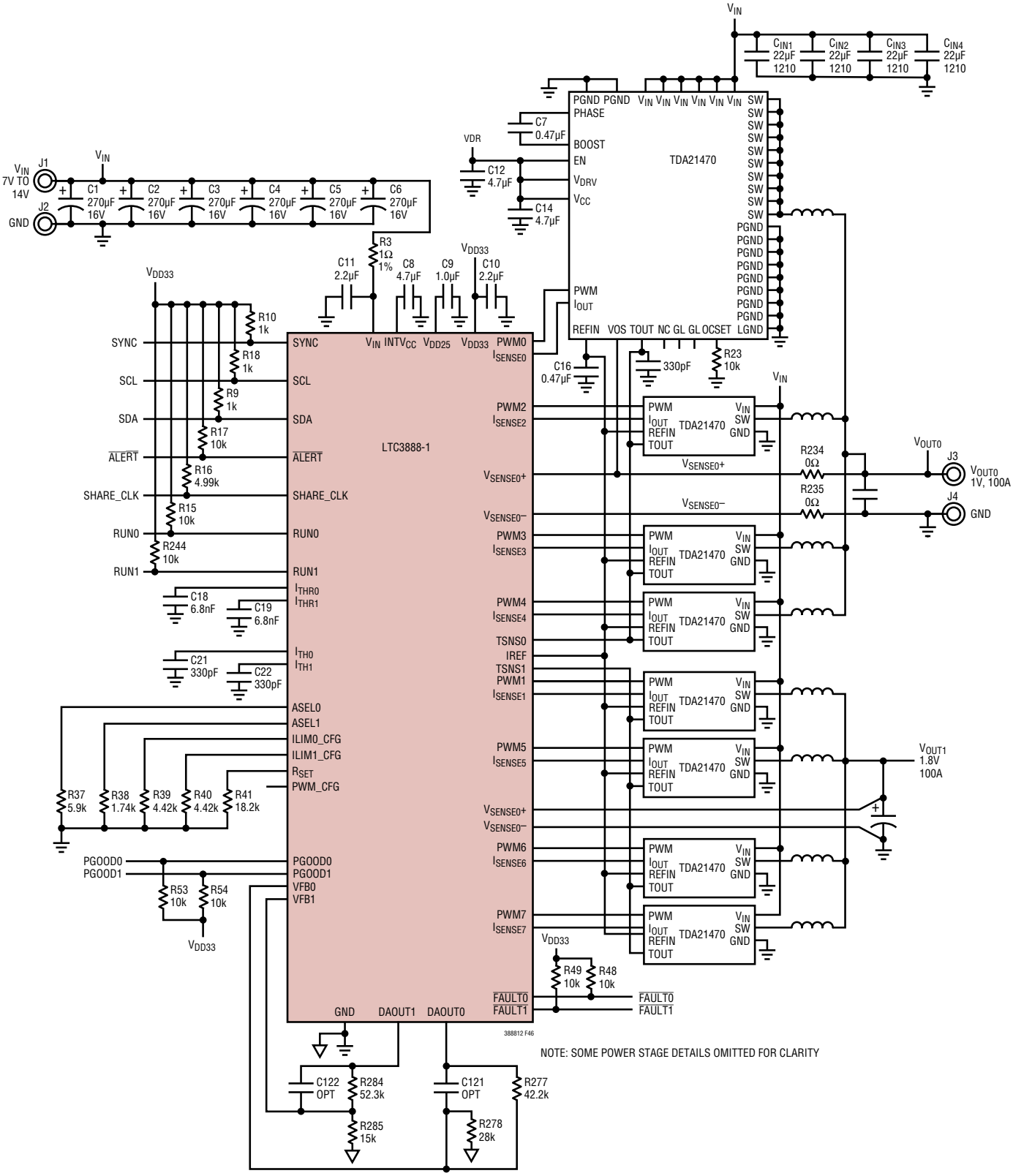



**Figure 46. 1V/100A and 1.8V/100A 500kHz Converter using the TDA21470 DrMOS**

## APPLICATIONS INFORMATION

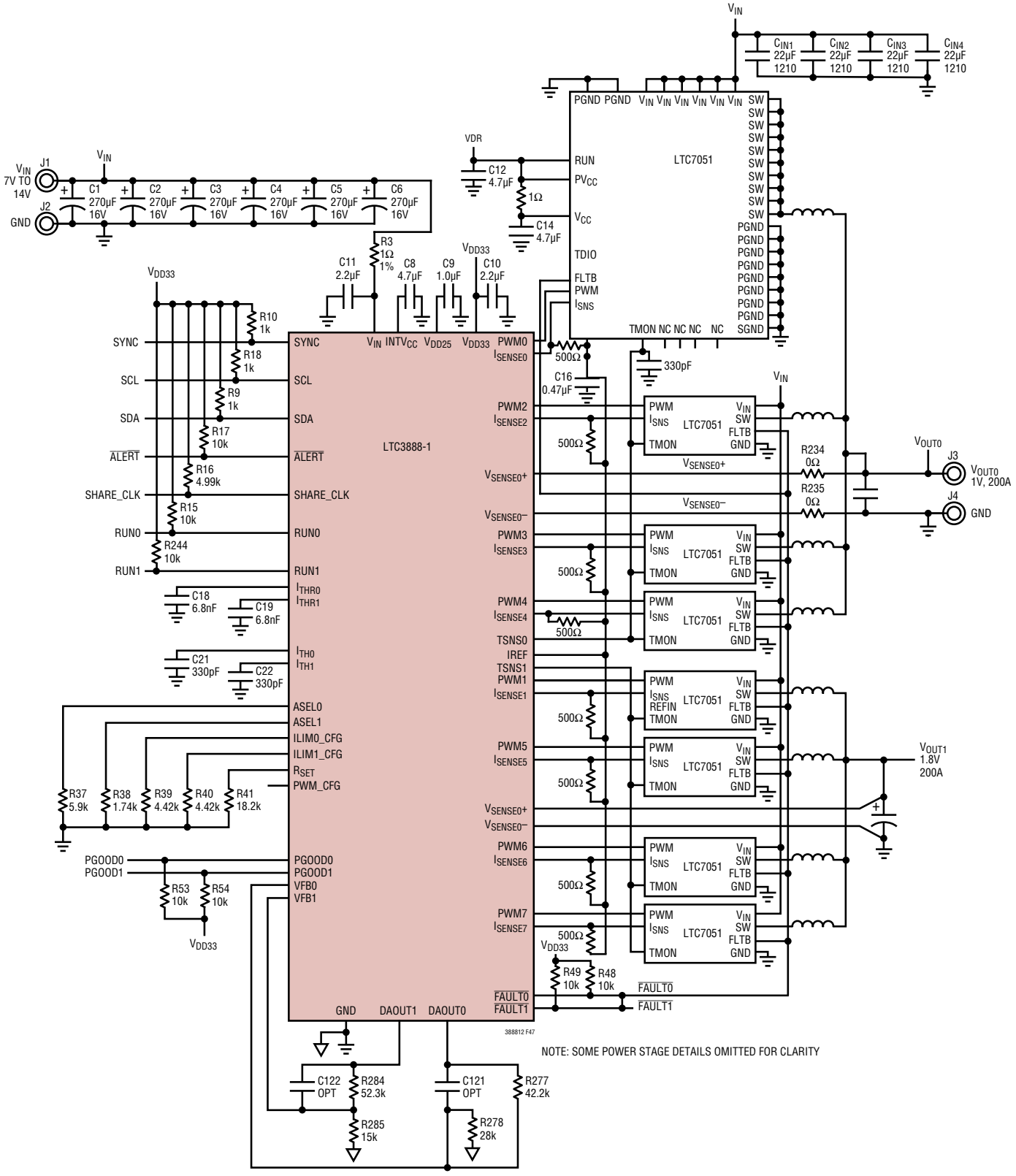



**Figure 47. 1V/200A and 1.8V/200A 500kHz Converter using the LTC7051 DrMOS**

## APPLICATIONS INFORMATION

Two 470µF Panasonic 5mΩ POSCAPs and three 100µF ceramic capacitors are chosen for each phase output to maintain supply regulation during severe transient conditions and to minimize output voltage ripple.

The loop compensation components C18, C21 ($V_{OUT0}$) and C19,C22 ($V_{OUT1}$) provide a good starting point to tune the crossover frequency by programming error amplifer transconductance and internal $R_{ITH}$ with the help of LTpowerCAD, LTpowerPlay and built-in LTC3888-1 load step emulation. With a 500kHz switching frequency, an initial crossover target of 100kHz should provide good transient performance. System phase margin of around 65° is recommended at that bandwidth.

For output current sensing, the TDA21470 provides a voltage-mode monitor scaled to 5mV/A, ideal for the LTC3888-1and allowing direct connection from $I_{OUT}$ to the LTC3888-1 $I_{SENSE}$ pin. The IREF output of the LTC3888-1 is used to provide the necessary common mode reference to all power stages. Each DrMOS device then has 470nF of local bypassing on this DC reference (REFIN) to limit introduction of switching noise and crosstalk. These capacitors should be returned to GND (the LTC3888-1 package paddle) for best noise performance.

External temperatures of interest are also sensed by the individual power stages. The highest temperature for each rail is indicated on the shared TOUT/FLT bus, which is connected directly to the respective LTC3888-1 TSNS input.

The required $R_{SET}$ resistor (18.7kΩ) is connected to GND. Resistor configuration is then used on the ASEL0 and ASEL1 pins to program PMBus address (MFR_ADDRESS) to 0x28. Each LTC3888-1 must be configured for a unique address. Using both ASEL pins to accomplish this is recommended for simpliest in-system programming. Check the selected address to avoid collision with global addresses or other any other specific devices. The LTC3888-1 also responds to 7-bit global addresses 0x5A and 0x5B. MFR_ADDRESS and MFR_RAIL_ADDRESS should not be set to either of these values. Resistors are used to program ILIM0_CFG and ILIM1_CFG to set IOUT_OC_WARN_LIMIT to 32A and IOUT_OC_FAULT_LIMIT to 40A, based on the design value of 25A rated load per phase (100A total) with a room temperature choke saturation of 50A.

PMBus connection (three signals), as well as shared RUN control and fault propagation ($\overline{FAULT}$) for each rail are provided. SYNC can be used to synchronize other PWMs to this device if required.

Pull-ups are provided on all open-drain signals assuming a maximum 100pF line load and PMBus rate of 100kHz. These pins should not be left floating. Termination to 3.3V ensures the absolute maximum ratings for the pins are not exceeded. All other operating parameters such as soft-start/stop and desired fault responses are programmed via PMBus command values stored in internal LTC3888-1 EEPROM.

# PMBus COMMAND DETAILS (by Functional Groups)

## ADDRESSING AND WRITE PROTECT

| COMMAND NAME | CMD CODE | DESCRIPTION | TYPE | PAGED | DATA FORMAT | UNITS | NVM | DEFAULT VALUE |
|---|---|---|---|---|---|---|---|---|
| PAGE | 0x00 | Channel (page) presently selected for any paged command. | R/W Byte | N | Reg | | | 0x00 |
| PAGE_PLUS_WRITE | 0x05 | Write a command directly to a specified page. | W Block | N | | | | |
| PAGE_PLUS_READ | 0x06 | Read a command directly from a specified page. | Block R/W Process | N | | | | |
| WRITE_PROTECT | 0x10 | Protect the device against unintended PMBus modifications. | R/W Byte | N | Reg | | ● | 0x00 |
| MFR_ADDRESS | 0xE6 | Specify right-justified 7-bit device address. | R/W Byte | N | Reg | | ● | 0x4F |
| MFR_RAIL_ADDRESS | 0xFA | Specify unique right-justified 7-bit address for channels comprising a PolyPhase output. | R/W Byte | Y | Reg | | ● | 0x80 |

### *PAGE*

The PAGE command provides the ability to configure, control and monitor both master channels through only one physical address, either the MFR_ADDRESS or global device address. Each PAGE contains the operating memory for one master channel.

Pages 0x00 and 0x01 correspond to Channel 0 (or PWM0) and Channel 1 (or PWM1), respectively.

Setting PAGE to 0xFF applies any following paged commands to both master channels. With PAGE set to 0xFF the LTC3888-1 will respond to read commands as if PAGE were set to 0x00 (Channel 0 results only).

This command has one data byte.

### *PAGE_PLUS_WRITE*

The PAGE_PLUS_WRITE command provides a way to set the page within a device, send a command and then send the data for the command, all in one communication packet. Commands allowed by the present write protection level may be sent with PAGE_PLUS_WRITE.

The value stored in the PAGE command is not affected by PAGE_PLUS_WRITE. If PAGE_PLUS_WRITE is used to send a non-paged command, the Page Number byte is ignored.

This command uses Write Block protocol. An example of the PAGE_PLUS_WRITE command with PEC sending a command that has two data bytes is shown in Figure 48.

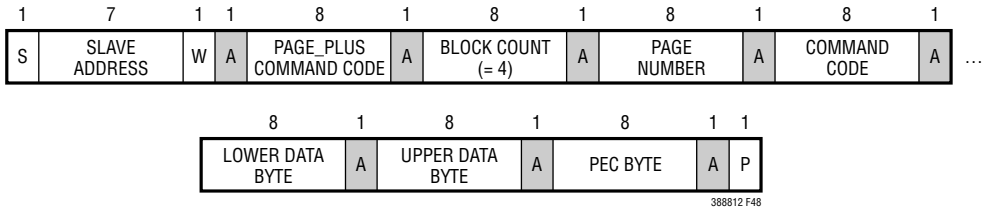



**Figure 48. Example of PAGE_PLUS_WRITE**

## PMBus COMMAND DETAILS (Addressing and Write Protect)

### *PAGE_PLUS_READ*

The PAGE_PLUS_READ command provides the ability to set the page within a device, send a command and then read the data returned by the command, all in one communication packet .

The value stored in the PAGE command is not affected by PAGE_PLUS_READ. If PAGE_PLUS_READ is used to access data from a non-paged command, the Page Number byte is ignored.

This command uses Block Write – Block Read Process Call protocol. An example of the PAGE_PLUS_READ command with PEC is shown in Figure 49.

NOTE: PAGE_PLUS commands cannot be nested. A PAGE_PLUS command cannot be used to read or write another PAGE_PLUS command. If this is attempted, the LTC3888-1 will NACK the entire PAGE_PLUS packet and issue a CML fault for Invalid/Unsupported Data.

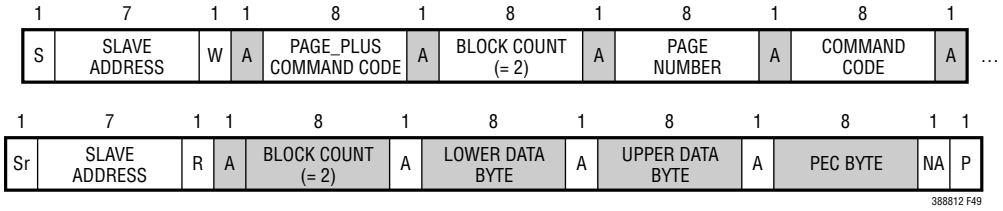



**Figure 49. Example of PAGE_PLUS_READ**

### *WRITE_PROTECT*

The WRITE_PROTECT command is used to control PMBus write access to the LTC3888-1.

**Supported Values:**

| VALUE | MEANING |
|---|---|
| 0x80 | Disable all writes except WRITE_PROTECT, PAGE, STORE_USER_ALL and MFR_EE_UNLOCK commands. |
| 0x40 | Disable all writes except WRITE_PROTECT, PAGE, STORE_USER_ALL, MFR_EE_UNLOCK, OPERATION, CLEAR_PEAKS and CLEAR_ FAULTS commands. Individual faults can also be cleared by writing a 1 to the respective status bit. |
| 0x20 | Disable all writes except WRITE_PROTECT, PAGE, STORE_USER_ ALL, MFR_EE_UNLOCK, OPERATION, CLEAR_PEAKS, CLEAR_FAULTS, ON_OFF_CONFIG and VOUT_COMMAND commands. Individual faults can be cleared by writing a 1 to the respective status bit. |
| 0x00 | Enables writes to all commands. |

This command has one data byte.

## PMBus COMMAND DETAILS (Addressing and Write Protect/General Device Configuration)

### *MFR_ADDRESS*

The MFR_ADDRESS command sets the seven bits of the PMBus device address for this unit.

Setting this command to a value of 0x80 disables device-level addressing. The global device addresses 0x5A and 0x5B cannot be disabled. The LTC3888-1 always responds at these addresses. The device address, or any portion of an address, specified with external resistors on ASEL0 or ASEL1 is applied. If both of these pins are open, the device address is determined strictly by the MFR_ADDRESS value stored in EEPROM. Refer to the Operation section on Resistor Configuration Pins for additional details.

This command has one data byte.

### *MFR_RAIL_ADDRESS*

The MFR_RAIL_ADDRESS command sets a direct PMBus address for the active channel(s) as determined by the PAGE command. This address should be common to all master channels attached to a single power supply rail. Setting this command to a value of 0x80 disables rail addressing for the selected channel. Only command writes should be made to the rail address. If a read is performed from this address, a CML fault may result.

This command has one data byte.

### GENERAL DEVICE CONFIGURATION

| COMMAND NAME | CMD CODE | DESCRIPTION | TYPE | PAGED | DATA FORMAT | UNITS | NVM | DEFAULT VALUE |
|---|---|---|---|---|---|---|---|---|
| PMBUS_REVISION | 0x98 | Supported PMBus version. | R Byte | Y | Reg | | | 0x22<br>V1.2 |
| CAPABILITY | 0x19 | Summary of supported optional PMBus features. | R Byte | N | Reg | | | 0xB0 |
| MFR_CONFIG_ALL | 0xD1 | General device-level configuration. | R/W Byte | N | Reg | | ● | 0x21 |

### *PMBUS_REVISION*

The PMBUS_REVISION command returns the revision of the PMBus Specification that the device supports. The LTC3888-1 is compliant with PMBus Version 1.2, both Part I and Part II.

This read-only command has one data byte.

### *CAPABILITY*

The CAPABILITY command reports some key LTC3888-1 features to the PMBus host device.

The LTC3888-1 supports packet error checking, 400kHz bus speeds and has an $\overline{\text{ALERT}}$ output.

This read-only command has one data byte.

# PMBus COMMAND DETAILS (General Device Configuration/On, Off and Margin Control)

## *MFR_CONFIG_ALL*

The MFR_CONFIG_ALL command provides device-level configuration common to multiple ADI PMBus products.

**Bit Definitions:**

| BIT | MEANING |
|---|---|
| 7 | Enable fault logging. |
| 6 | Ignore ILIM and PWM resistor configuration pins. |
| 5 | Disable CML fault for quick command message. |
| 4 | Disable SYNC output. |
| 3 | Enable 255ms PMBus timeout. |
| 2 | Require valid PEC for PMBus write. |
| 1 | Enable PMBus clock stretching. |
| 0 | Execute CLEAR_FAULTS when either channel is turned on by RUN pin or OPERATION command. |

If a legal command is received with an invalid PEC, the LTC3888-1 will not execute the command, regardless of the state of bit 2. If clock stretching is enabled, the LTC3888-1 only uses it as required, generally above SCL rates of 100kHz.

This command has one data byte.

## ON, OFF AND MARGIN CONTROL

| COMMAND NAME | CMD CODE | DESCRIPTION | TYPE | PAGED | DATA FORMAT | UNITS | NVM | DEFAULT VALUE |
|---|---|---|---|---|---|---|---|---|
| ON_OFF_CONFIG | 0x02 | RUN pin and PMBus on/off command configuration. | R/W Byte | Y | Reg | | ● | 0x1E |
| OPERATION | 0x01 | On, off and margin control. | R/W Byte | Y | Reg | | ● | 0x80 |
| MFR_RESET | 0xFD | Force full reset without removing power. | Send Byte | N | | | | |

## *ON_OFF_CONFIG*

The ON_OFF_CONFIG command specifies the combination of RUN pin input state and PMBus commands needed to turn the addressed output rail on and off.

**Supported Values:**

| VALUE | MEANING |
|---|---|
| 0x1F | OPERATION value and RUN pin must both command the device to start/run. Device executes immediate off when commanded off. |
| 0x1E | OPERATION value and RUN pin must both command the device to start/run. Device uses TOFF_ command values when commanded off. |
| 0x17 | RUN pin control with immediate off when commanded off. OPERATION on/off control ignored. |
| 0x16 | RUN pin control using TOFF_ command values when commanded off. OPERATION on/off control ignored. |

Programming an unsupported ON_OFF_CONFIG value will generate a CML fault and the command will be ignored.

This command has one data byte.

## PMBus COMMAND DETAILS (On, Off and Margin Control)

### *OPERATION*

The OPERATION command is used to turn the related output rail on and off in conjunction with RUN pin hardware control. This command may also be used to move the output voltage to margin levels. $V_{OUT}$ changes commanded by OPERATION margin commands occur at the programmed VOUT_TRANSITION_RATE. The unit stays in the commanded operating state until an OPERATION command or RUN pin voltage instructs the device to change to another state.

Execution of margin commands is delayed until any on-going output transition sequencing is completed. Margin operations that ignore faults are not supported by the LTC3888-1.

**Supported Values:**

| VALUE | MEANING |
|---|---|
| 0xA8 | Margin high. |
| 0x98 | Margin low. |
| 0x80 | On (i.e. nominal $V_{OUT}$, even if bit 3 of ON_OFF_CONFIG is not set). |
| 0x40* | Soft off (with sequencing). |
| 0x00* | Immediate off (no sequencing). |

*Device does not respond to these commands if bit 3 of ON_OFF_CONFIG is not set.

Programming an unsupported OPERATION value will generate a CML fault and the command will be ignored.

This command has one data byte.

### *MFR_RESET*

This command provides a means to fully reset the LTC3888-1 from the serial bus. This forces the LTC3888-1 to turn off all PWM channels, load the operating memory from internal EEPROM, clear all faults and then perform a soft-start of all PWM channels that are enabled.

This write-only command has no data bytes.

# PMBus COMMAND DETAILS (PWM Configuration)

## PWM CONFIGURATION

| COMMAND NAME | CMD CODE | DESCRIPTION | TYPE | PAGED | DATA FORMAT | UNITS | NVM | DEFAULT VALUE |
|---|---|---|---|---|---|---|---|---|
| FREQUENCY_SWITCH | 0x33 | PWM frequency control. | R/W Word | N | L11 | kHz | ● | 500kHz 0xFBE8 |
| MFR_CHAN_CONFIG | 0xD0 | General channel-specific configuration. | R/W Byte | Y | Reg | | ● | 0x1D |
| MFR_PWM_CONFIG_LTC3888-1 | 0xF5 | LTC3888-1 PWM configuration common to both master channels. | R/W Byte | N | Reg | | ● | 0x03 |
| MFR_PWM_MODE_LTC3888-1 | 0xD4 | Channel-specific LTC3888-1 PWM mode control. | R/W Byte | Y | Reg | | ● | 0x02 |
| MFR_PWM_COMP | 0xD3 | Channel-specific PWM loop compensation | R/W Byte | Y | Reg | | ● | 0xAE |

### *FREQUENCY_SWITCH*

The FREQUENCY_SWITCH command sets the switching frequency of all LTC3888-1 PWM channels in kilohertz. The valid range for this command value is 250 to 1000, inclusive. At most only one IC sharing SYNC should be programmed as clock master. See bit 4 in MFR_CONFIG_ALL. FREQUENCY_SWITCH value will determine the free-running frequency of PWM operation if an expected external clock source is not present or the bussed SYNC line becomes stuck due an external fault or conflict. Both master channels must be turned off by the RUN pins, OPERATION command, or their combination to process this command. If this command is sent while either master channel is operating, the LTC3888-1 will NACK the command byte, ignore the command and its data, and assert a BUSY fault. A PLL Unlocked status may be reported after changing the value of this command until the new frequency is established.

This command has two data bytes in Linear_5s_11s format.

# PMBus COMMAND DETAILS (PWM Configuration)

## *MFR_CHAN_CONFIG*

The MFR_CHAN_CONFIG command provides per-channel configuration common to multiple ADI PMBus products.

**Bit Definitions:**

| BIT | MEANING |
|---|---|
| 7:6 | (Reserved, must write as 0). |
| 5 | Pin 8 function control: (Page 0 only)<br>0: Pin 8 functions as TSNS0.<br>1: Pin 8 functions as VDR_MON. |
| 4 | RUN pin control:<br>0: When the channel is commanded off, the associated RUN pin is pulsed low for TOFF_DELAY + $V_{OUT}$/VOUT_TRANSITION_RATE + 136ms (or MFR_RESTART_DELAY, if longer) regardless of the state of bit 3.<br>1: RUN pin is not pulsed low if channel is commanded off. |
| 3 | Short cycle control:<br>0: No special control. Device attempts to follow on/off commands exactly as issued.<br>1: Output is immediately disabled if commanded back on while waiting for TOFF_DELAY or $V_{OUT}$/VOUT_TRANSITION_RATE to expire. A minimum off time of 120ms is then enforced before the channel is turned back on. Additional delay will apply if bit 4 is clear. |
| 2 | SHARE_CLK output control:<br>0: No special control.<br>1: Output disabled if SHARE_CLK is held low. |
| 1 | (Reserved, must write as 0). |
| 0 | MFR_RETRY_DELAY control:<br>0: No retry allowed after output off for any reason until $V_{OUT} \leq 0.125$xVOUT_COMMAND.<br>1: No special control (TOFF_MAX_WARN_LIMIT also disabled). |

This command has one data byte.

## *MFR_PWM_CONFIG_LTC3888-1*

The MFR_PWM_CONFIG_LTC3888-1 command controls primary master/slave configuration and monitor ADC sampling control for the LTC3888-1. Both master channels must be turned off by the RUN pins, OPERATION command, or their combination to process this command. If this command is sent while either master channel is operating, the LTC3888-1 will NACK the command byte, ignore the command and its data, and assert a BUSY fault.

# PMBus COMMAND DETAILS (PWM Configuration)

### Bit Definitions

| BIT | MEANING |
|---|---|
| 7 | (Reserved, must write as 0) |
| 6 | Slave $I_{OUT}$ Telemetry:<br>0: The LTC3888-1 provides continuous IOUT telemetry for all enabled phases.<br>1: The LTC3888-1 only provides IOUT telemetry for master channels PWM0 and PWM1. |
| 5 | (Reserved) |
| 4 | VOUT_OV_FAULT HW Response:<br>0: No special low level response, master phase obeys VOUT_OV_FAULT_RESPONSE of immediate off (PWM Hi-Z).<br>1: PWM of master phase driven low during VOUT_OV_FAULT, synchronous bottom power FET attempts to discharge $V_{OUT}$ with rail off. |
| 3 | Phase Expansion:<br>0: The power-good state for Channel 0 is output on PGOOD0.<br>1: A phase expansion clock (CLKOUT) is output on PGOOD0 to drive SYNC on a second LTC3888-1. |

| [2:0] Value | Master/Slave Configuration | | |
|---|---|---|---|
| | Master | Configuration / Slave | Phase (*) |
| 111 | **PWM0** | 7-Phase | 0 |
| | PWM0 | PWM2 | 51.4 |
| | PWM0 | PWM3 | 154.3 |
| | PWM0 | PWM4 | 205.7 |
| | PWM0 | PWM5 | 102.9 |
| | PWM0 | PWM6 | 257.1 |
| | PWM0 | PWM7 | 308.6 |
| | **PWM1** | 1-Phase | 25.7 |
| 110 | **PWM0** | (6-Phase) | 0 |
| | PWM0 | PWM2 | 60 |
| | PWM0 | PWM3 | 180 |
| | PWM0 | PWM4 | 240 |
| | PWM0 | PWM5 | 120 |
| | PWM0 | PWM6 | 300 |
| | **PWM1** | (2-Phase) | 30 |
| | PWM1 | PWM7 | 210 |
| 101 | **PWM0** | (6-Phase) | 0 |
| | PWM0 | PWM2 | 60 |
| | PWM0 | PWM3 | 180 |
| | PWM0 | PWM4 | 240 |
| | PWM0 | PWM5 | 120 |
| | PWM0 | PWM6 | 300 |
| | **PWM1** | (1-Phase) | 30 |
| | | PWM7 | Off |

# PMBus COMMAND DETAILS (PWM Configuration)

**MFR_PWM_CONFIG_LTC3888-1 Bit Definitions (continued)**

| | Value | Master/Slave Configuration | | |
|---|---|---|---|---|
| | | Master | Configuration / Slave | Phase (*) |
| [2:0] | 100 | **PWM0** | (5-Phase) | 0 |
| | | PWM0 | PWM2 | 72 |
| | | PWM0 | PWM3 | 144 |
| | | PWM0 | PWM4 | 216 |
| | | PWM0 | PWM5 | 288 |
| | | **PWM1** | (3-Phase) | 34.3 |
| | | PWM1 | PWM6 | 274.4 |
| | | PWM1 | PWM7 | 154.3 |
| | 011 | **PWM0** | (4-Phase, optional 8-phase with PWM1) | 0 |
| | | PWM0 | PWM2 | 90 |
| | | PWM0 | PWM3 | 180 |
| | | PWM0 | PWM4 | 270 |
| | | **PWM1** | (4-Phase, Optional 8-Phase with PWM0) | 45 |
| | | PWM1 | PWM5 | 135 |
| | | PWM1 | PWM6 | 225 |
| | | PWM1 | PWM7 | 315 |
| | 010 | **PWM0** | (4-Phase) | 0 |
| | | PWM0 | PWM2 | 90 |
| | | PWM0 | PWM3 | 180 |
| | | PWM0 | PWM4 | 270 |
| | | **PWM1** | (3-Phase) | 42.9 |
| | | PWM1 | PWM5 | 162.9 |
| | | PWM1 | PWM6 | 282.9 |
| | | | PWM7 | Off |
| | 001 | **PWM0** | (4-Phase) | 0 |
| | | PWM0 | PWM2 | 90 |
| | | PWM0 | PWM3 | 180 |
| | | PWM0 | PWM4 | 270 |
| | | **PWM1** | (2-Phase) | 45 |
| | | | PWM5 | Off |
| | | PWM1 | PWM6 | 225 |
| | | | PWM7 | Off |
| | 000 | **PWM0** | (3-Phase) | 0 |
| | | PWM0 | PWM2 | 120 |
| | | | PWM3 | Off |
| | | PWM0 | PWM4 | 240 |
| | | **PWM1** | (3-Phase, Optional 6-Phase with PWM0) | 60 |
| | | PWM1 | PWM5 | 180 |
| | | PWM1 | PWM6 | 300 |
| | | | PWM7 | Off |

Phase is expressed from the falling edge of SYNC to the rising edge of PWM.

This command has one data byte.

# PMBus COMMAND DETAILS (PWM Configuration)

## *MFR_PWM_MODE_LTC3888-1*

The MFR_PWM_MODE_LTC3888-1 command sets important PWM controls for each master channel. The addressed channel(s) must be turned off by its RUN pin, OPERATION command, or their combination when this command is issued. Otherwise the LTC3888-1 will NACK the command byte, ignore the command and its data, and assert a BUSY fault.

**Bit Definitions**

| BIT | MEANING |
|---|---|
| 7 | (Reserved) |
| 6 | Enable $V_{OUT}$ servo. (VOUT_LOOP_SCALE should be programmed first.) |
| 5 | (Reserved, must write as 0) |
| 4 | Error Amplifier Disable:<br>0: Error Amplifier output ($I_{TH}$) enabled. Channel operates as voltage loop master.<br>1: Error Amplifier output disabled ($I_{TH}$ high-Z input). Channel operates as slave phase to another master. |
| 3 | (Reserved) |
| 2 | (Reserved) |
| 1 | $t_{ON\_MIN}$ Control:<br>0: Minimum PWM On Time Set by Controller (can be < 30ns).<br>1: Minimum PWM On Time Limited to ≥ 30ns. |
| 0 | Power Stage UV HW Response: (see Applications Information for exceptions)<br>0: Rail ignores any UV indication on shared TEMP/FAULT bus.<br>1: Rail is latched off if UV is indicated on the shared TEMP/FAULT bus while operating.<br>(WARNING: Not all power stages support this feature.) |

This command has one data byte.

# PMBus COMMAND DETAILS (PWM Configuration)

## *MFR_PWM_COMP*

The MFR_PWM_COMP command sets the transconductance of the voltage loop error amplifier and the value of the internal compensation resistor $R_{ITH}$ for each master channel.

**Bit Definitions**

| BIT | MEANING | |
|---|---|---|
| | **Value** | **Error Amplifier gm (mS)** |
| | 000b | 1.00 |
| | 001b | 1.68 |
| | 010b | 2.35 |
| [7.5] | 011b | 3.02 |
| | 100b | 3.69 |
| | 101b | 4.36 |
| | 110b | 5.04 |
| | 111b | 5.73 |
| | **Value** | **$R_{ITH}$ (kΩ)** |
| | 00000b | 1 |
| | 00001b | 1 |
| | 00010b | 1 |
| | 00011b | 1 |
| | 00100b | 1 |
| | 00101b | 1.25 |
| | 00110b | 1.5 |
| | 00111b | 1.75 |
| | 01000b | 2 |
| | 01001b | 2.5 |
| | 01010b | 3 |
| | 01011b | 3.5 |
| | 01100b | 4 |
| | 01101b | 4.5 |
| | 01110b | 5 |
| [4:0] | 01111b | 5.5 |
| | 10000b | 6 |
| | 10001b | 7 |
| | 10010b | 8 |
| | 10011b | 9 |
| | 10100b | 11 |
| | 10101b | 13 |
| | 10110b | 15 |
| | 10111b | 17 |
| | 11000b | 20 |
| | 11001b | 24 |
| | 11010b | 28 |
| | 11011b | 32 |
| | 11100b | 38 |
| | 11101b | 46 |
| | 11110b | 54 |
| | 11111b | 62 |

This command has one data byte.

# PMBus COMMAND DETAILS (Input Voltage and Limits)

## INPUT VOLTAGE AND LIMITS

| COMMAND NAME | CMD CODE | DESCRIPTION | TYPE | PAGED | DATA FORMAT | UNITS | NVM | DEFAULT VALUE |
|---|---|---|---|---|---|---|---|---|
| VIN_ON | 0x35 | Minimum input voltage to begin power conversion. | R/W Word | N | L11 | V | ● | 6.5V 0xCB40 |
| VIN_OFF | 0x36 | Decreasing input voltage at which power conversion stops. | R/W Word | N | L11 | V | ● | 6.0V 0xCB00 |
| VIN_OV_FAULT_LIMIT | 0x55 | $V_{IN}$ overvoltage fault limit. | R/W Word | N | L11 | V | ● | 15.5V 0xD3E0 |
| VIN_UV_WARN_LIMIT | 0x58 | $V_{IN}$ undervoltage warning limit. | R/W Word | N | L11 | V | ● | 6.3V 0xCB26 |

Related commands: STATUS_INPUT, SMBALERT_MASK, READ_VIN, VIN_OV_FAULT_RESPONSE

### *VIN_ON*

The VIN_ON command sets the input voltage, in volts, required to start power conversion.

This command has two data bytes in Linear_5s_11s format.

### *VIN_OFF*

The VIN_OFF command sets the minimum input voltage, in volts, at which power conversion stops.

This command has two data bytes in Linear_5s_11s format.

### *VIN_OV_FAULT_LIMIT*

The VIN_OV_FAULT_LIMIT command sets the value of the input voltage measured by the ADC, in volts, that causes an input overvoltage fault.

This command has two data bytes in Linear_5s_11s format.

### *VIN_UV_WARN_LIMIT*

The VIN_UV_WARN_LIMIT command sets the value of input voltage measured by the ADC, in volts, that causes an input undervoltage warning. This warning is disabled until the input exceeds the VIN_ON command value and the unit has been enabled. If the VIN_UV_WARN_LIMIT is then exceeded, the device:

- Sets the INPUT Bit in the STATUS_WORD
- Sets the $V_{IN}$ Undervoltage Warning Bit in the STATUS_INPUT Command
- Notifies the Host by Asserting $\overline{\text{ALERT}}$, Unless Masked

# PMBus COMMAND DETAILS (Output Voltage and Limits)

## OUTPUT VOLTAGE AND LIMITS (for PMBus Control, DEFAULT VALUE Applies to Analog Control)

| COMMAND NAME | CMD CODE | DESCRIPTION | TYPE | PAGED | DATA FORMAT | UNITS | NVM | DEFAULT VALUE |
|---|---|---|---|---|---|---|---|---|
| VOUT_COMMAND | 0x21 | Default $V_{FB}$ regulation. Nominal $V_{OUT}$ value when VOUT_SCALE_LOOP is defined. | R/W Word | Y | L16 | V | ● | 400mV 0x0666 |
| VOUT_MAX | 0x24 | Maximum $V_{OUT}$ capability. | R Word | Y | L16 | V | | 1.1V 0x119A |
| MFR_VOUT_MAX | 0xA5 | Maximum value allowed for VOUT_MAX. | R Word | Y | L16 | V | | 3.75V 0x3C00 |
| VOUT_MARGIN_HIGH | 0x25 | $V_{FB}$ (default) or $V_{OUT}$ at high margin, *must be greater than VOUT_COMMAND*. | R/W Word | Y | L16 | V | ● | 420mV 0x06B8 |
| VOUT_MARGIN_LOW | 0x26 | $V_{FB}$ (default) or $V_{OUT}$ at low margin, *must be greater than VOUT_COMMAND*. | R/W Word | Y | L16 | V | ● | 380mV 0x0614 |
| VOUT_SCALE_LOOP | 0x29 | Nominal $V_{OUT}/V_{FB}$ gain provided by external feedback network. | R/W Word | Y | L11 | V | ● | N/A |
| VOUT_OV_FAULT_LIMIT | 0x40 | Default $V_{FB}$ overvoltage fault limit. $V_{OUT}$ OV limit if VOUT_SCALE_LOOP is defined. | R/W Word | Y | L16 | V | ● | 440mV 0x070A |
| VOUT_OV_WARN_LIMIT | 0x42 | $V_{OUT}$ overvoltage warning limit sensed at $V_{SENSE}^{\pm}$. | R/W Word | Y | L16 | V | ● | 3.6V 0x3981 |
| VOUT_UV_WARN_LIMIT | 0x43 | $V_{OUT}$ undervoltage warning limit sensed at $V_{SENSE}^{\pm}$. | R/W Word | Y | L16 | V | ● | 0.0V 0x0000 |
| VOUT_UV_FAULT_LIIMIT | 0x44 | Default $V_{FB}$ undervoltage fault limit. $V_{OUT}$ UV limit if VOUT_SCALE_LOOP is defined. | R/W Word | Y | L16 | V | ● | 360mV 0x05C3 |

Related commands: STATUS_VOUT, SMBALERT_MASK, READ_VOUT, MFR_VOUT_PEAK, VOUT_OV_FAULT_RESPONSE, VOUT_UV_FAULT_RESPONSE

### *VOUT_MODE*

The VOUT_MODE command gives the format used by the device for output voltage related commands. Only Linear Mode is supported, with a resolution of 244µV. Sending the VOUT_MODE command to the LTC3888-1 using a write protocol will result in a CML fault.

This read-only command has one data byte.

### *VOUT_COMMAND*

VOUT_COMMAND is used to set the output voltage in volts if VOUT_SCALE_LOOP has been defined. Execution of this command is delayed if VOUT_SCALE_LOOP is being processed or until any ongoing soft-on/off output sequence is ccomplete. Otherwise, the output voltage moves to a new value at VOUT_TRANSITION_RATE.

This command has two data bytes in Linear_16u format.

### *VOUT_MAX*

The VOUT_MAX command returns the maximum value, in volts, allowed for any $V_{OUT}$-related command, including VOUT_OV_FAULT_LIMIT. This value represents the maximum regulated voltage the selected rail is capable of producing based on internal design and the value of VOUT_SCALE_LOOP.

This read-only command has two data bytes in Linear_16u format.

## PMBus COMMAND DETAILS (Output Voltage and Limits)

### *MFR_VOUT_MAX*

The MFR_VOUT_MAX command returns the maximum value, in volts, allowed for VOUT_MAX based on internal device capability.

This read-only command has two data bytes in Linear_16u format.

### *VOUT_MARGIN_HIGH*

The VOUT_MARGIN_HIGH command programs the value of $V_{FB}$ (or $V_{OUT}$ if VOUT_SCALE_LOOP has been defined), in volts, to be produced when Margin High is set with the OPERATION command. The value must be greater than VOUT_COMMAND. Execution of this command is delayed if VOUT_SCALE_LOOP is being processed.

This command has two data bytes in Linear_16u format.

### *VOUT_MARGIN_LOW*

The VOUT_MARGIN_LOW command programs the value of $V_{FB}$ (or $V_{OUT}$ if VOUT_SCALE_LOOP has been defined), in volts, to be produced when Margin Low is set with the OPERATION command. The value must be less than VOUT_COMMAND. Execution of this command is delayed if VOUT_SCALE_LOOP is being processed.

This command has two data bytes in Linear_16u format.

### *VOUT_SCALE_LOOP*

The VOUT_SCALE_LOOP command programs the gain, in volts per volt, produced from $V_{FB}$ to $V_{OUT}$ by the external voltage feedback network. Values from 1 to 9 are considered valid. The LTC3888-1 will assert a CML fault and ignore the value if an attempt is made to write VOUT_SCALE_LOOP to a value outside of this range.

This command has two data bytes in Linear_5s_11s format.

### *VOUT_OV_FAULT_LIMIT*

The VOUT_OV_FAULT_LIMIT command sets the value value of $V_{FB}$ (or $V_{OUT}$ if VOUT_SCALE_LOOP has been defined), in volts, that causes an output overvoltage fault. If VOUT_OV_FAULT_LIMIT is modified while the channel is on, 2ms should be allowed for the new value to take effect. Modifying $V_{OUT}$ during that time can result in an erroneous OV fault. The LTC3888-1 sets MFR_COMMON bits[6:5] low while a new VOUT_OV_FAULT_LIMIT is established. Execution of this command is delayed if VOUT_SCALE_LOOP is being processed.

This command has two data bytes in Linear_16u format.

### *VOUT_OV_WARN_LIMIT*

The VOUT_OV_WARN_LIMIT command sets the value, in volts, of the $V_{SENSE}^{\pm}$ differential voltage measured by the ADC that causes an output overvoltage warning. If the VOUT_OV_WARN_LIMIT is exceeded, the device:

- Sets the VOUT Bit in the STATUS_WORD
- Sets the $V_{OUT}$ Overvoltage Warning Bit in the STATUS_VOUT Command
- Notifies the Host by Asserting $\overline{\text{ALERT}}$, Unless Masked

This command has two data bytes in Linear_16u format.

## PMBus COMMAND DETAILS (Output Voltage and Limits)

### *VOUT_UV_WARN_LIMIT*

The VOUT_UV_WARN_LIMIT command sets the value, in volts, of the $V_{SENSE}^{\pm}$ differnetial voltage measured by the ADC that causes an output undervoltage warning. If the VOUT_UV_WARN_LIMIT is exceeded, the device:

- Sets the VOUT Bit in the STATUS_WORD
- Sets the $V_{OUT}$ Undervoltage Warning Bit in the STATUS_VOUT Command
- Notifies the Host by Asserting $\overline{ALERT}$, Unless Masked

This command has two data bytes in Linear_16u format.

### *VOUT_UV_FAULT_LIMIT*

The VOUT_UV_FAULT_LIMIT command sets the value of $V_{FB}$ (or $V_{OUT}$ if VOUT_SCALE_LOOP has been defined), in volts, that causes an output undervoltage fault. If VOUT_UV_FAULT_LIMIT is modified while the channel is on, 2ms should be allowed for the new value to take effect. Modifying $V_{OUT}$ during that time can result in an erroneous UV fault. The LTC3888-1 sets MFR_COMMON bits[6:5] low while a new VOUT_UV_FAULT_LIMIT is established. Execution of this command is delayed if VOUT_SCALE_LOOP is being processed.

This command has two data bytes in Linear_16u format.

# PMBus COMMAND DETAILS (Output Current and Limits)

## OUTPUT CURRENT AND LIMITS

| COMMAND NAME | CMD CODE | DESCRIPTION | TYPE | PAGED | DATA FORMAT | UNITS | NVM | DEFAULT VALUE |
|---|---|---|---|---|---|---|---|---|
| IOUT_CAL_GAIN | 0x38 | Ratio of $I_{SENSE}$ voltage to sensed current. | R/W Word | Y | L11 | mΩ | ● | 5mΩ 0xCA80 |
| MFR_LOAD_EMULATION | 0xF7 | Load step emulation control. | R/W Byte | Y | Reg | | | 0x00 |
| IOUT_OC_FAULT_LIMIT | 0x46 | Per phase output overcurrent fault limit. | R/W Word | Y | L11 | A | ● | 29.75A 0xDBB8 |
| IOUT_OC_WARN_LIMIT | 0x4A | Per phase output overcurrent warning limit. | R/W Word | Y | L11 | A | ● | 20.0A 0xDA80 |

Related commands: STATUS_IOUT, SMBALERT_MASK, READ_IOUT, MFR_IOUT_PEAK, MFR_TOTAL_IOUT, MFR_READ_ALL_IOUT,IOUT_OC_FAULT_RESPONSE

### *IOUT_CAL_GAIN*

The IOUT_CAL_GAIN command is used to set the power stage output current monitor gain at $I_{SENSE}$ in milliohms. If both master channels are not commanded off by their RUN pin or OPERATION command when IOUT_CAL_GAIN is sent to either page, the LTC3888-1 will assert a CML fault.

This command has two data bytes in Linear_5s_11s format.

### *MFR_LOAD_EMULATION*

The MFR_LOAD_EMULATION command is used to control load step emulation for all phases on each master channel.

**MFR_LOAD_EMULATION**

| BIT | MEANING | |
|---|---|---|
| 7 | (Reserved) | |
| 6 | (Reserved) | |
| 5 | (Reserved) | |
| 4 | (Reserved) | |
| 3 | Enable Load Step Emulation (LSE) Event Scope Trigger on PGOOD (negative edge) | |
| 2 | LSE Mode Control:<br>0: Non-pulsed: LSE state statically follows data written to bits[1:0}.<br>1: Pulsed: Writing any non-zero state to bits [1:0] produces an LSE pulse of the specified magnitude with a width of ~ 100µs. | |
| [1:0] | **Value** | **Load Step Emulated at IOUT_CAL_GAIN = 5mΩ** |
| | 11b | 30A/Phase |
| | 10b | 20A/Phase |
| | 01b | 10A/Phase |
| | 00b | Off |

This command has one data byte.

## PMBus COMMAND DETAILS (Output Current and Limits)

### *IOUT_OC_FAULT_LIMIT*

The IOUT_OC_FAULT_LIMIT command sets the value of the per phase output current, in amperes, which will cause the OC supervisor to detect an output overcurrent fault. The LTC3888-1 uses IOUT_CAL_GAIN and the voltage between the $I_{SENSE}$ inputs and IREF to determine output current. Output overcurrent faults are ignored during turn-on and turn-off output transitions.

This command has two data bytes in Linear_5s_11s format.

### *IOUT_OC_WARN_LIMIT*

The IOUT_OC_WARN_LIMIT command sets the value of the average per phase output current measured by the ADC, in amperes, that causes an output overcurrent warning. To provide meaningful responses, this value should be set below IOUT_OC_FAULT_LIMIT. If the IOUT_OC_WARN_LIMIT is exceeded, the device:

- Sets the IOUT Bit in the STATUS_WORD
- Sets the $I_{OUT}$ Overcurrent Warning Bit in the STATUS_IOUT Command
- Notifies the Host by Asserting $\overline{ALERT}$, Unless Masked

Output overcurrent warnings are ignored during turn-on and turn-off output transitions.

This command has tw°o data bytes in Linear_5s_11s format.

# PMBus COMMAND DETAILS (Output Timing, Delays, and Ramping)

## OUTPUT TIMING, DELAYS, AND RAMPING

| COMMAND NAME | CMD CODE | DESCRIPTION | TYPE | PAGED | DATA FORMAT | UNITS | NVM | DEFAULT VALUE |
|---|---|---|---|---|---|---|---|---|
| MFR_RESTART_DELAY | 0xDC | Minimum time RUN pin is held low by the LTC3888-1. | R/W Word | Y | L11 | ms | ● | 500ms 0xFBE8 |
| TON_DELAY | 0x60 | Delay from RUN pin or OPERATION on command to beginning of soft-start ramp. | R/W Word | Y | L11 | ms | ● | 0.0ms 0x8000 |
| TON_MAX_FAULT_LIMIT | 0x62 | Maximum time for $V_{FB}$ (default) or $V_{OUT}$ to rise above VOUT_UV_FAULT_LIMIT after TON_DELAY. | R/W Word | Y | L11 | ms | ● | 10.0ms 0xD280 |
| VOUT_TRANSITION_RATE | 0x27 | Slew rate for $V_{FB}$ (default) or $V_{OUT}$ soft-on/off and margining, including changes to VOUT_COMMAND. | R/W Word | Y | L11 | $ms^{-1}$ | ● | 0.01 0x82BF |
| TOFF_DELAY | 0x64 | Delay from RUN pin or OPERATION off command to beginning of soft-off ramp. | R/W Word | Y | L11 | ms | ● | 0.0ms 0x8000 |
| TOFF_MAX_WARN_LIMIT | 0x66 | Maximum time for $V_{OUT}$ to reach 0.125xVOUT_COMMAND after being commanded to 0.0V. | R/W Word | Y | L11 | ms | ● | 0.0ms 0x8000 |

Related commands: MFR_RETRY_DELAY, STATUS_VOUT, SMBALERT_MASK, TON_MAX_FAULT_RESPONSE

These commands can be used to establish required sequencing and tracking for any number of system power supply rails.

### *MFR_RESTART_DELAY*

The MFR_RESTART_DELAY command specifies the minimum rail off time (RUN low) in milliseconds. The LTC3888-1 will actively hold its RUN pin low for this length of time if a falling RUN edge is detected. After this delay, a standard start-up sequence can be initiated. A minimum of TOFF_DELAY + TOFF_FALL + 136ms is recommended for this command value. Valid value range is 136ms to 65.52 seconds. The LTC3888-1 will not produce delays outside of this range and uses a resolution of 16ms for this command.

This command has two data bytes in Linear_5s_11s format.

### *TON_DELAY*

The TON_DELAY command sets the delay, in milliseconds, between a PWM start condition and the beginning of the output voltage rise. Values from 0ms to 83 seconds are considered valid, and the LTC3888-1 will not produce delays outside of this range.

This command has two data bytes in Linear_5s_11s format.

### *TON_MAX_FAULT_LIMIT*

The TON_MAX_FAULT_LIMIT command sets the maximum time, in milliseconds, the unit is allowed from the beginning of the soft-start ramp to power up the output without passing VOUT_UV_FAULT_LIMIT. A value of 0ms means there is no limit and the unit can attempt to bring up the output voltage indefinitely. The maximum allowed TON_MAX is 8 seconds. To avoid generation of spurious faults, the value of this command should be set to meet the following guideline.

TON_MAX_FAULT_LIMIT ≥ 1.25xVOUT_COMMAND/VOUT_TRANSITION_RATE

This command has two data bytes in Linear_5s_11s format.

## PMBus COMMAND DETAILS (Output Timing, Delays, and Ramping)

### *VOUT_TRANSITION_RATE*

When using factory defaults, the VOUT_TRANSITION_RATE command sets the rate at which $V_{FB}$ changes during soft-on/off and when margin commands are executed. If VOUT_SCALE_LOOP is definded this command specifies the rate at which the output voltage changes whenever commanded to moved. In either case this rate of change does not apply to operations that immediately turn the PWM channel on or off.

This command has two data bytes in Linear_5s_11s format.

### *TOFF_DELAY*

The TOFF_DELAY command sets the delay, in milliseconds, between a stop condition and the beginning of the output voltage fall. Values from 0s to 16s are considered valid.

This command has two data bytes in Linear_5s_11s format.

### *TOFF_MAX_WARN_LIMIT*

The TOFF_MAX_WARN_LIMIT command sets the time, in milliseconds, $V_{OUT}$ is allowed to drop to 0.125xVOUT_COMMAND after being commanded to 0V. This time begins after TOFF_DELAY+VOUT_COMMAND/VOUT_TRANSITION expires if the output is not commanded to immediate off. If this limit is exceeded a warning is issued in VOUT_STATUS and $\overline{\text{ALERT}}$ asserted if not masked. No warning limit is enforced if bit 0 of MFR_CHAN_CONFIG is set or the value of this command is programmed to zero. Otherwise, values from 120ms to 524s are considered valid. In order to avoid erroneous $\overline{\text{ALERT}}$ indication, VOUT_SCALE_LOOP and all other related $V_{OUT}$ commands must be defined before this command is set to a non-zero value.

This command has two data bytes in Linear_5s_11s format.

# PMBus COMMAND DETAILS (External Temperature and Limits)

## EXTERNAL TEMPERATURE AND LIMITS

| COMMAND NAME | CMD CODE | DESCRIPTION | TYPE | PAGED | DATA FORMAT | UNITS | NVM | DEFAULT VALUE |
|---|---|---|---|---|---|---|---|---|
| MFR_TEMP_1_GAIN | 0xF8 | Slope for external temperature calculations. | R/W Word | Y | L11 | mV/°C | ● | 8mV/°C 0xD200 |
| MFR_TEMP_1_OFFSET | 0xF9 | 0°C offset for external temperature calculations. | R/W Word | Y | L11 | mV | ● | 600mV 0x0258 |
| OT_FAULT_LIMIT | 0x4F | External overtemperature fault limit. | R/W Word | Y | L11 | °C | ● | 100.0°C 0xEB20 |
| OT_WARN_LIMIT | 0x51 | External overtemperature warning limit. | R/W Word | Y | L11 | °C | ● | 85.0°C 0xEAA8 |

Related commands: STATUS_TEMPERATURE, SMBALERT_MASK, READ_TEMPERATURE_1,MFR_TEMPERATURE1_PEAK, OT_FAULT_RESPONSE

### *MFR_TEMP_1_GAIN*

The MFR_TEMP_1_GAIN command sets the slope, in mV/°C, used in the calculation of external temperature based on monitor ADC conversions of the shared TEMP/FAULT bus (TSNS pins).

This command has two data bytes in Linear_5s_11s format.

### *MFR_TEMP_1_OFFSET*

The MFR_TEMP_1_OFFSET command sets the 0°C offset, in mV, used in the calculation of external temperature based on monitor ADC conversions of the shared TEMP/FAULT bus (TSNS pins).

This command has two data bytes in Linear_5s_11s format.

### *OT_FAULT_LIMIT*

The OT_FAULT_LIMIT command sets the value of sensed external temperature, in degrees Celsius, which causes an overtemperature fault.

This command has two data bytes in Linear_5s_11s format.

### *OT_WARN_LIMIT*

The OT_WARN_LIMIT command sets the value of sensed external temperature, in degrees Celsius, which causes an overtemperature warning. If the OT_WARN_LIMIT is exceeded, the device:

- Sets the TEMPERATURE Bit in the STATUS_BYTE
- Sets the Overtemperature Warning Bit in the STATUS_TEMPERATURE Command
- Notifies the Host by Asserting $\overline{\text{ALERT}}$, Unless Masked

This command has two data bytes in Linear_5s_11s format.

# PMBus COMMAND DETAILS (Status Reporting)

## STATUS REPORTING

| COMMAND NAME | CMD CODE | DESCRIPTION | TYPE | PAGED | DATA FORMAT | UNITS | NVM | DEFAULT VALUE |
|---|---|---|---|---|---|---|---|---|
| STATUS_BYTE | 0x78 | One-byte channel status summary. | R/W Byte | Y | Reg | | | |
| STATUS_WORD | 0x79 | Two-byte channel status summary. | R/W Word | Y | Reg | | | |
| STATUS_VOUT | 0x7A | $V_{OUT}$ fault and warning status. | R/W Byte | Y | Reg | | | |
| STATUS_IOUT | 0x7B | $I_{OUT}$ fault and warning status. | R/W Byte | Y | Reg | | | |
| STATUS_INPUT | 0x7C | Input supply fault and warning status. | R/W Byte | N | Reg | | | |
| STATUS_TEMPERATURE | 0x7D | External temperature fault and warning status. | R/W Byte | Y | Reg | | | |
| STATUS_CML | 0x7E | Communication, memory and logic fault and warning status. | R/W Byte | N | Reg | | | |
| STATUS_MFR_SPECIFIC | 0x80 | IC-specific status. | R/W Byte | Y | Reg | | | |
| MFR_PADS_LTC3888-1 | 0xE5 | State of selected LTC3888-1 pads. | R Word | N | Reg | | | |
| MFR_COMMON | 0xEF | ADI-generic device status reporting. | R Byte | N | Reg | | | |
| MFR_INFO | 0xB6 | Manufacturer-specific information | R Word | N | Reg | | | |
| CLEAR_FAULTS | 0x03 | Clear all set fault bits. | Send Byte | N | | | | |

Refer to Figure 2 for a graphical depiction of these register contents and their relationships. Refer to Power Stage Selection and Interface in the Applications Information section for details of special status reporting related to external power stages that is supported by the LTC3888-1.

### *STATUS_BYTE*

The STATUS_BYTE command returns a one-byte summary of the most critical faults.

**STATUS_BYTE Message Contents:**

| BIT | STATUS BIT NAME | MEANING |
|---|---|---|
| 7* | BUSY | A fault was declared because the device was unable to respond. |
| 6 | OFF | This bit is set if the channel is not providing power to its output, regardless of the reason, including simply not being enabled. |
| 5 | VOUT_OV | An output overvoltage or power stage fault has occurred. Also set if open $V_{SENSE}$+ is detected. |
| 4 | IOUT_OC | An output overcurrent fault has occurred. |
| 3 | VIN_UV | Not supported (device returns 0). |
| 2 | TEMPERATURE | A temperature fault or warning has occurred. (LTC3888-1 only) |
| 1 | CML | A communications, memory or logic fault has occurred. |
| 0 | NONE OF THE ABOVE | A fault Not listed in bits[7:1] has occurred. |

*$\overline{\text{ALERT}}$ can be asserted if this bit is set. It may be cleared by writing a 1 to that bit position in the STATUS_BYTE, in lieu of a CLEAR_FAULTS command.

This command has one data byte.

# PMBus COMMAND DETAILS (Status Reporting)

## *STATUS_WORD*

The STATUS_WORD command returns a two-byte summary of the channel's fault condition. The low byte of the STATUS_WORD is the same as the STATUS_BYTE command.

**STATUS_WORD High Byte Message Contents:**

| BIT | STATUS BIT NAME | MEANING |
|---|---|---|
| 15 | VOUT | An output voltage fault or warning has occurred. Also set if a power stage fault or open $V_{SENSE}$+ is detected. |
| 14 | IOUT | An output current fault or warning has occurred. Also set if a power stage fault is detected. |
| 13 | INPUT | An input voltage fault or warning has occurred. |
| 12 | MFR_SPECIFIC | A fault or warning specific to the LTC3888-1 has occurred. |
| 11 | POWER_GOOD# | The POWER_GOOD state is false if this bit is set. |
| 10 | FANS | Not supported (LTC3888-1 returns 0). |
| 9 | OTHER | Not supported (LTC3888-1 returns 0). |
| 8 | UNKNOWN | Not supported (LTC3888-1 returns 0). |

This command has two data bytes.

## *STATUS_VOUT*

The STATUS_VOUT command returns one byte of $V_{OUT}$ status information. Refer to Table 8 for additional details.

**STATUS_VOUT Message Contents:**

| BIT | MEANING |
|---|---|
| 7 | $V_{OUT}$ overvoltage fault, power stage fault, or open $V_{SENSE}$+ input. |
| 6 | $V_{OUT}$ overvoltage warning. |
| 5 | $V_{OUT}$ undervoltage warning. |
| 4 | $V_{OUT}$ undervoltage fault or open $V_{SENSE}$+ input. |
| 3 | VOUT_MAX warning. |
| 2 | TON_MAX fault. |
| 1 | Not supported by the LTC3888-1 (returns 0). |
| 0 | Not supported by the LTC3888-1 (returns 0). |

$\overline{\text{ALERT}}$ can be asserted if any of bits[7:2] are set. These may be cleared by writing a 1 to their bit position in STATUS_VOUT, in lieu of a CLEAR_FAULTS command.

This command has one data byte.

## PMBus COMMAND DETAILS (Status Reporting)

### *STATUS_IOUT*

The STATUS_IOUT command returns one byte of $I_{OUT}$ status information. Refer to Table 8 for additional details.

**STATUS_IOUT Message Contents:**

| BIT | MEANING |
|---|---|
| 7 | $I_{OUT}$ overcurrent fault. |
| 6 | Not supported (LTC3888-1 returns 0). |
| 5 | $I_{OUT}$ overcurrent warning. |
| 4 | Not supported (LTC3888-1 returns 0). |
| 3 | Power stage fault detected (differs from standard PMBus meaning). |
| 2:0 | Not supported (LTC3888-1 returns 0). |

$\overline{ALERT}$ can be asserted if any supported bits are set. Any supported bit may be cleared by writing a 1 to that bit position in STATUS_IOUT, in lieu of a CLEAR_FAULTS command.

This command has one data byte.

### *STATUS_INPUT*

The STATUS_INPUT command returns one byte of $V_{IN}$ status information.

**STATUS_INPUT Message Contents:**

| BIT | MEANING |
|---|---|
| 7 | $V_{IN}$ overvoltage fault. |
| 6 | Not supported (LTC3888-1returns 0). |
| 5 | $V_{IN}$ undervoltage warning. |
| 4 | Not supported (LTC3888-1 returns 0). |
| 3 | Unit off for insufficient $V_{IN}$. |
| 2:0 | Not supported (LTC3888-1 returns 0). |

$\overline{ALERT}$ can be asserted if bit 7 is set. Bit 7 may be cleared by writing it to a 1, in lieu of a CLEAR_FAULTS command.

This command has one data byte.

### *STATUS_TEMPERATURE*

The STATUS_TEMPERATURE command returns one byte of sensed external temperature status information.

**STATUS_TEMPERATURE Message Contents:**

| BIT | MEANING |
|---|---|
| 7 | External overtemperature fault. |
| 6 | External overtemperature warning. |
| 5 | Not supported (LTC3888-1 returns 0). |
| 4 | Not supported (LTC3888-1 returns 0). |
| 3:0 | Not supported (LTC3888-1 returns 0). |

$\overline{ALERT}$ can be asserted if any supported bits are set. Any supported bit may be cleared by writing a 1 to that bit position in STATUS_TEMPERATURE, in lieu of a CLEAR_FAULTS command.

This command has one data byte.

# PMBus COMMAND DETAILS (Status Reporting)

## *STATUS_CML*

The STATUS_CML command returns one byte of status information on received commands, internal memory and logic.

**STATUS_CML Message Contents:**

| BIT | MEANING |
|---|---|
| 7 | Invalid or unsupported command received. |
| 6 | Invalid or unsupported data received. |
| 5 | Packet error check failed. |
| 4 | Memory fault detected. |
| 3 | Processor fault detected. |
| 2 | Reserved (LTC3888-1 returns 0). |
| 1 | Other communication fault. |
| 0 | Other memory or logic fault. |

$\overline{\text{ALERT}}$ can be asserted if any supported bits are set. Any supported bit may be cleared by writing a 1 to that bit position in STATUS_CML, in lieu of a CLEAR_FAULTS command.

This command has one data byte.

## *STATUS_MFR_SPECIFIC*

The STATUS_MFR_SPECIFIC command returns one byte with device-specific status information.

**STATUS_MFR_SPECIFIC Message Contents:**

| BIT | MEANING |
|---|---|
| 7 | Internal temperature fault (>160°C). |
| 6 | Internal temperature warning (>130°C). |
| 5 | EEPROM CRC error. |
| 4 | Internal PLL unlocked. |
| 3 | Fault log present. |
| 2 | Not supported (LTC3888-1 returns 0). |
| 1 | Output short cycled. |
| 0 | $\overline{\text{FAULT}}$ low. |

If any supported bits are set, the MFR bit in the STATUS_WORD will be set and $\overline{\text{ALERT}}$ may be asserted. Any supported bit may be cleared by writing a 1 to that bit position in STATUS_MFR_SPECIFIC, in lieu of a CLEAR_FAULTS command.

This command has one data byte.

# PMBus COMMAND DETAILS (Status Reporting)

### *MFR_PADS_LTC3888-1*

The MFR_PADS_LTC3888-1 command provides status of the LTC3888-1 digital I/O and control pins, in addition to general output voltage conditions.

**MFR_PADS_LTC3882 Message Contents:**

| BIT | MEANING |
|---|---|
| 15 | Channel 1 power stages all report ready. |
| 14 | Channel 0 power stages all report ready. |
| 13:12 | Not supported (LTC3888-1 returns 0). |
| 11 | ADC results for READ_TEMPERATURE_1 may be invalid. |
| 10 | SYNC output disabled externally. |
| 9 | Channel 1 POWER_GOOD. |
| 8 | Channel 0 POWER_GOOD. |
| 7 | LTC3888-1 forcing RUN1 low. |
| 6 | LTC3888-1 forcing RUN0 low. |
| 5 | RUN1 pin state. |
| 4 | RUN0 pin state. |
| 3 | LTC3888-1 forcing $\overline{\text{FAULT1}}$ low. |
| 2 | LTC3888-1 forcing $\overline{\text{FAULT0}}$ low. |
| 1 | $\overline{\text{FAULT1}}$ pin state. |
| 0 | $\overline{\text{FAULT0}}$ pin state. |

This read-only command has two data bytes.

### *MFR_COMMON*

The MFR_COMMON command contains status bits that are common to multiple ADI PMBus products.

**MFR_COMMON Message Contents:**

| BIT | MEANING |
|---|---|
| 7 | LTC3888-1 not forcing $\overline{\text{ALERT}}$ low. |
| 6 | LTC3888-1 not BUSY. |
| 5 | LTC3888-1 calculations not pending. |
| 4 | LTC3888-1 output not in transition. |
| 3 | LTC3888-1 EEPROM initialized. |
| 2 | Not supported (LTC3888-1 returns 0). |
| 1 | SHARE_CLK timeout. |
| 0 | Not supported (LTC3888-1 returns 0). |

This read-only command has one data byte.

# PMBus COMMAND DETAILS (Status Reporting)

### *MFR_INFO*

The MFR_INFO command contains status bits providing manufacturer-specific information.

**MFR_INFO Message Contents:**

| BIT | MEANING |
|---|---|
| 15:6 | Reserved. |
| 5 | EEPROM ECC Status:<br>0: Corrections have been made in the EEPROM user space.<br>1: No corrections have been made in the EEPROM user space. |
| 4:0 | Reserved. |

This read-only command has two data bytes.

### *CLEAR_FAULTS*

The CLEAR_FAULTS command clears any fault bits that have been set and deasserts (releases) the $\overline{\text{ALERT}}$ pin. This command clears all fault bits in all status commands simultaneously.

CLEAR_FAULTS does not cause a channel that has latched off for a fault condition to restart. Channels that are latched off for a fault condition are restarted when the output is commanded to turn off and then on through the OPERATION command or RUN pins, or IC supply power is cycled.

If a fault is still present when CLEAR_FAULTS is commanded, that fault bit will immediately be set again and $\overline{\text{ALERT}}$ asserted low if not masked.

This write-only command has no data bytes.

# PMBus COMMAND DETAILS (Telemetry)

## TELEMETRY

| COMMAND NAME | CMD CODE | DESCRIPTION | TYPE | PAGED | DATA FORMAT | UNITS | NVM | DEFAULT VALUE |
|---|---|---|---|---|---|---|---|---|
| READ_VIN | 0x88 | Measured $V_{IN}$. | R Word | N | L11 | V | | |
| MFR_VIN_PEAK | 0xDE | Maximum $V_{IN}$ measurement since last MFR_CLEAR_PEAKS. | R Word | N | L11 | V | | |
| READ_VOUT | 0x8B | Measured $V_{OUT}$. | R Word | Y | L16 | V | | |
| MFR_VOUT_PEAK | 0xDD | Maximum $V_{OUT}$ measurement since last MFR_CLEAR_PEAKS. | R Word | Y | L16 | V | | |
| READ_IOUT | 0x8C | Measured master channel $I_{OUT}$. | R Word | Y | L11 | A | | |
| MFR_IOUT_PEAK | 0xD7 | Maximum master channel $I_{OUT}$ measurement since last MFR_CLEAR_PEAKS. | R Word | Y | L11 | A | | |
| MFR_TOTAL_IOUT | 0xE1 | Measured total $I_{OUT}$ for each rail defined by MFR_PWM_CONFIG_LTC3888-1. | R Word | Y | L11 | A | | |
| MFR_READ_ALL_IOUT | 0xE4 | Measured $I_{OUT}$ for each individual PWM phase. | R Block | N | L11 | A | | |
| READ_TEMPERATURE_1 | 0x8D | Measured external temperature. | R Word | Y | L11 | °C | | |
| MFR_TEMPERATURE_1_PEAK | 0xDF | Maximum external temperature measurement since last MFR_CLEAR_PEAKS. | R Word | Y | L11 | °C | | |
| READ_TEMPERATURE_2 | 0x8E | Measured internal temperature. | R Word | N | L11 | °C | | |
| MFR_TEMPERATURE_2_PEAK | 0xF4 | Maximum internal temperature measurement since last MFR_CLEAR_PEAKS. | R Word | N | L11 | °C | | |
| READ_FREQUENCY | 0x95 | Measured PWM input clock frequency. | R Word | Y | L11 | kHz | | |
| MFR_CLEAR_PEAKS | 0xE3 | Clear all peak values. | Send Byte | N | | | | |

Related commands: IOUT_CAL_GAIN

### *READ_VIN*

The READ_VIN command returns the input voltage measured between $V_{IN}$ and GND in volts.

This read-only command has two data bytes in Linear_5s_11s format.

## PMBus COMMAND DETAILS (Telemetry)

### *MFR_VIN_PEAK*

The MFR_VIN_PEAK command reports the highest voltage, in volts, measured for READ_VIN. This peak value can be reset by a MFR_CLEAR_PEAKS command.

This read-only command has two data bytes in Linear_5s_11s format.

### *READ_VOUT*

The READ_VOUT command returns the output voltage measured at the $V_{SENSE}^{\pm}$ pins in volts.

This read-only command has two data bytes in Linear_16u format.

### *MFR_VOUT_PEAK*

The MFR_VOUT_PEAK command reports the highest voltage, in volts, measured for READ_VOUT. This peak value can be reset by a MFR_CLEAR_PEAKS command.

This read-only command has two data bytes in Linear_16u format.

### *READ_IOUT*

The READ_IOUT command returns the master channel output current in amperes. This value is computed by applying IOUT_CAL_GAIN to the voltage measured between $I_{SENSE}$ and IREF.

This read-only command has two data bytes in Linear_5s_11s format.

### *MFR_IOUT_PEAK*

The MFR_IOUT_PEAK command reports the highest current, in amperes, calculated for READ_IOUT. This peak value can be reset by a MFR_CLEAR_PEAKS command.

This read-only command has two data bytes in Linear_5s_11s format.

### *MFR_TOTAL_IOUT*

The MFR_TOTAL_IOUT command reports the total output current for all on-chip phases of the entire rail as defined by MFR_PWM_CONFIG_LTC3888-1. The value is calculated from the sum of the individual phase $I_{OUT}$ ADC conversions. If bit 6 of MFR_PWM_CONFIG_LTC3888-1 is set, PWM2-PWM7 report 0A regardless of the actual output load. Sums are always reported by page, even if the master channel has been defined as a slave (see bit 4 of MFR_PWM_MODE_LTC3888-1). Sums across IC boundaries are not supported.

This read-only command has two data bytes in Linear_5s_11s format.

### *MFR_READ_ALL_IOUT*

The MFR_READ_ALL_IOUT command reports the output current for each of the eight phases on the LTC3888-1 using block read protocol. Monitor ADC results are presented in order from PWM0 to PWM7. If bit 6 of MFR_PWM_CONFIG_LTC3888-1 is set, PWM2-PWM7 report 0A.

This read-only command uses block protocol with 17 bytes of data delivering $I_{OUT}$ results in Linear_5s_11s format.

## PMBus COMMAND DETAILS (Telemetry)

### *READ_TEMPERATURE_1*

The READ_TEMPERATURE_1 command returns the temperature, in degrees Celsius, of external power stages connected to the device TSNS pin(s).

This read-only command has two data bytes in Linear_5s_11s format.

### *MFR_TEMPERATURE_1_PEAK*

The MFR_TEMPERATURE_1_PEAK command reports the highest temperature, in degrees Celsius, calculated for READ_TEMPERATURE_1. This peak value can be reset by a MFR_CLEAR_PEAKS command.

This read-only command has two data bytes in Linear_5s_11s format.

### *READ_TEMPERATURE_2*

The READ_TEMPERATURE_2 command returns the LTC3888-1 internal temperature in degrees Celsius.

This read-only command has two data bytes in Linear_5s_11s format.

### *MFR_TEMPERATURE_2_PEAK*

The MFR_TEMPERATURE_2_PEAK command reports the highest temperature, in degrees Celsius, calculated for READ_TEMPERATURE_2. This peak value can be reset by a MFR_CLEAR_PEAKS command.

This read-only command has two data bytes in Linear_5s_11s format.

### *READ_FREQUENCY*

The READ_FREQUENCY command returns the switching frequency supplied to the internal PLL in kilohertz, whether generated internally or provided by external clock on the SYNC pin.

This read-only command has two data bytes in Linear_5s_11s format.

### *MFR_CLEAR_PEAKS*

The MFR_CLEAR_PEAKS command resets all stored _PEAK values. The LTC3888-1 determines new peak values after this command is received.

This write-only command has no data bytes.

# PMBus COMMAND DETAILS (Fault Response and Communication)

## FAULT RESPONSE AND COMMUNICATION

| COMMAND NAME | CMD CODE | DESCRIPTION | TYPE | PAGED | DATA FORMAT | UNITS | NVM | DEFAULT VALUE |
|---|---|---|---|---|---|---|---|---|
| VIN_OV_FAULT_RESPONSE | 0x56 | $V_{IN}$ overvoltage fault response. | R/W Byte | Y | Reg | | ● | 0x80 |
| VOUT_OV_FAULT_RESPONSE | 0x41 | $V_{OUT}$ overvoltage fault response. | R Byte | Y | Reg | | ● | 0x80 |
| VOUT_UV_FAULT_RESPONSE | 0x45 | $V_{OUT}$ undervoltage fault response. | R/W Byte | Y | Reg | | ● | 0xB8 |
| IOUT_OC_FAULT_RESPONSE | 0x47 | Output overcurrent fault response. | R/W Byte | Y | Reg | | ● | 0x00 |
| OT_FAULT_RESPONSE | 0x50 | External overtemperature fault response. | R/W Byte | Y | Reg | | ● | 0xB8 |
| MFR_OT_FAULT_RESPONSE | 0xD6 | Internal overtemperature fault response. | R/W Byte | N | Reg | | ● | 0xC0 |
| TON_MAX_FAULT_RESPONSE | 0x63 | Fault response when TON_MAX_FAULT_LIMIT is exceeded. | R/W Byte | Y | Reg | | ● | 0xB8 |
| MFR_RETRY_DELAY | 0xDB | Minimum time before retry after a fault. | R/W Word | N | L11 | ms | ● | 350ms 0xFABC |
| SMBALERT_MASK | 0x1B | Mask $\overline{\text{ALERT}}$ Activity. | Block R/W | Y | Reg | | ● | See Following Details |
| MFR_FAULT_PROPAGATE | 0xD2 | Configure fault propagation via $\overline{\text{FAULT}}$ pins. | R/W Word | Y | Reg | | ● | 0x6993 |
| MFR_FAULT_RESPONSE | 0xD5 | PWM response when $\overline{\text{FAULT}}$ pin is low due to external fault. | R/W Byte | Y | Reg | | ● | 0xC0 |
| MFR_FAULT_LOG | 0xEE | Read fault log data. | R Block | N | Reg | | | |
| MFR_FAULT_LOG_CLEAR | 0xEC | Clear existing EEPROM fault log. | Send Byte | N | | | | |

Related commands: STATUS_BYTE, STATUS_WORD, MFR_PADS_LTC3888-1, MFR_RESTART_DELAY, MFR_FAULT_LOG_STORE, CLEAR_FAULTS

These commands detail programmable device responses for detected faults beyond the hardware-level actions described in the Operation section. LTC3888-1 hardware-level fault responses cannot be modified. PMBus warning event responses are listed under _WARN_LIMIT command details.

### *VIN_OV_FAULT_RESPONSE*

The VIN_OV_FAULT_RESPONSE command instructs the device on what action to take in response to an input overvoltage fault. The format for this command is given in Table 14. The device also:

- Sets the INPUT Bit in the STATUS_WORD
- Sets the $V_{IN}$ Overvoltage Fault Bit in the STATUS_INPUT Command
- Notifies the Host by Asserting $\overline{\text{ALERT}}$, Unless Masked

This command has one data byte.

## PMBus COMMAND DETAILS (Fault Response and Communication)

### *VOUT_OV_FAULT_RESPONSE*

The VOUT_OV_FAULT_RESPONSE command reports the actions the device will take in response to an output overvoltage fault, power stage fault or qualified UVLO (LTC3888-1 only) or qualified VDR supply UV during operation. The format for this command is given in Table 13. The device also:

- Sets the VOUT_OV Bit in the STATUS_BYTE
- Sets the VOUT Bit in the STATUS_WORD
- Sets the $V_{OUT}$ Overvoltage Fault Bit in the STATUS_VOUT Command
- Notifies the Host by Asserting $\overline{\text{ALERT}}$, Unless Masked

This read-only command has one data byte.

### *VOUT_UV_FAULT_RESPONSE*

The VOUT_UV_FAULT_RESPONSE command instructs the device on what action to take in response to an output undervoltage fault. The format for this command is given in Table 13. The device also:

- Sets the VOUT Bit in the STATUS_WORD
- Sets the $V_{OUT}$ Undervoltage Fault Bit in the STATUS_VOUT Command,
- Notifies the Host by Asserting $\overline{\text{ALERT}}$, Unless Masked

This command has one data byte.

**Table 13. Data Byte Contents for VOUT_OV_FAULT_RESPONSE and VOUT_UV_FAULT_RESPONSE**

| BITS | DESCRIPTION | VALUE | MEANING |
|---|---|---|---|
| [7:6] | For all values of bits [7:6], the LTC3888-1:<br>• Sets the corresponding fault bits in the status commands.<br>• Notifies the host by asserting $\overline{\text{ALERT}}$, unless masked.<br>The fault, once set, is cleared only when one or more of the following events occurs:<br>• The device receives a CLEAR_FAULTS command.<br>• The corresponding STATUS_VOUT bit is written to a one.<br>• The output is commanded off, then on, by the RUN pin or OPERATION command.<br>• The device receives a RESTORE_USER_ALL command.<br>• The device receives an MFR_RESET command.<br>• IC supply power is cycled. | 00 | The LTC3888-1 continues to operate indefinitely with the normal hardware response described in the Operation section. |
| | | 01 | The LTC3888-1 continues operating with the normal hardware response for the delay time specified by bits [2:0]. If the fault is continuously present for the entire delay, the unit then disables the output and responds according to the retry setting in bits [5:3]. |
| | | 10 | The LTC3888-1 immediately disables the output and responds according to the retry setting in bits [5:3]. |
| | | 11 | Not supported. Writing this value will generate a CML fault. |
| [5:3] | Retry setting. | 000-110 | The LTC3888-1 does not attempt to restart. The output remains disabled until the fault is cleared, the device is commanded off and then on, or IC supply power is cycled. |
| | | 111 | The LTC3888-1 attempts to restart continuously without limitation with an interval set by MFR_RETRY_DELAY. This response persists until the unit is commanded off, or IC supply power is removed, or another fault response forces shutdown without retry. |
| [2:0] | Delay time. | xxx | Response delay time in 10µs increments. This delay time determines how long the fault may have to persist before the controller is disabled, depending on bits [7:6]. Hardware-level response, if any, will occur during this delay. |

# PMBus COMMAND DETAILS (Fault Response and Communication)

## *IOUT_OC_FAULT_RESPONSE*

The IOUT_OC_FAULT_RESPONSE command instructs the device on what action to take in response to an output overcurrent fault. The device also:

- Sets the IOUT_OC Bit in the STATUS_BYTE
- Sets the IOUT Bit in the STATUS_WORD
- Sets the $I_{OUT}$ Overcurrent Fault Bit in the STATUS_IOUT Command
- Notifies the Host by Asserting $\overline{\text{ALERT}}$, Unless Masked

Output overcurrent faults are ignored during turn-on and turn-off output transitions.

**Data Byte Contents for IOUT_OC_FAULT_RESPONSE:**

| BITS | DESCRIPTION | VALUE | MEANING |
|---|---|---|---|
| [7:6] | For all values of bits [7:6], the LTC3888-1:<br>• Sets the corresponding fault bits in the status commands.<br>• Notifies the host by asserting $\overline{\text{ALERT}}$, unless masked.<br>The fault, once set, is cleared only when one or more of the following events occurs:<br>• The device receives a CLEAR_FAULTS command.<br>• The corresponding STATUS_IOUT bit is written to a one.<br>• The output is commanded off, then on, by the RUN pin or OPERATION command.<br>• The device receives a RESTORE_USER_ALL command.<br>• The device receives an MFR_RESET command.<br>• IC supply power is cycled. | 00 | The LTC3888-1 continues to operate indefinitely with the normal hardware response described in the Operation section. |
| | | 01 | Not supported. Writing this value will generate a CML fault. |
| | | 10 | The LTC3888-1 continues operating with the normal hardware response for the delay time specified by bits [2:0]. If the fault is continuously present for the entire delay, the unit then disables the output and responds according to the retry setting in bits [5:3]. |
| | | 11 | The LTC3888-1 immediately disables the output and responds according to the retry setting in bits [5:3]. |
| [5:3] | Retry setting. | 000-110 | The LTC3888-1 does not attempt to restart. The output remains disabled until the fault is cleared, the device is commanded off and then on, or IC supply power is cycled. |
| | | 111 | The LTC3888-1 attempts to restart continuously without limitation with an interval set by MFR_RETRY_DELAY. This response persists until the unit is commanded off, IC supply power is removed, or another fault response forces shutdown without retry. |
| [2:0] | Delay time. | xxx | Response delay time in 16ms increments. This delay time determines how long the fault may have to persist before the controller is disabled, depending on bits [7:6]. These bits always return zero if bits [7:6]. |

This command has one data byte.

## PMBus COMMAND DETAILS (Fault Response and Communication)

### *OT_FAULT_RESPONSE*

The OT_FAULT_RESPONSE command instructs the device on what action to take in response to an external overtemperature fault. The format for this command is given in Table 14. The device also:

- Sets the TEMPERATURE Bit in the STATUS_BYTE
- Sets the Overtemperature Fault Bit in the STATUS_TEMPERATURE Command
- Notifies the Host by Asserting $\overline{\text{ALERT}}$, Unless Masked

This command has one data byte.

### *MFR_OT_FAULT_RESPONSE*

The MFR_OT_FAULT_RESPONSE command instructs the device on what action to take in response to an internal overtemperature fault (150°C to 160°C). The device also:

- Sets the MFR Bit in the STATUS_WORD
- Sets the Overtemperature Fault Bit in the STATUS_MFR_SPECIFIC Command
- Notifies the Host by Asserting $\overline{\text{ALERT}}$, Unless Masked

**Supported Values:**

| VALUE | MEANING |
|---|---|
| 0xC0 | The LTC3888-1 continues to operate indefinitely with the normal hardware response described in the Operation section. |
| 0x80 | The LTC3888-1 shuts down immediately and does not attempt to restart. The output remains disabled until the fault is cleared and the unit is commanded off and then on, or IC supply power is cycled. |

Programming an unsupported MFR_OT_FAULT_RESPONSE value will generate a CML fault and the command will be ignored.

This command has one data byte.

### *TON_MAX_FAULT_RESPONSE*

The TON_MAX_FAULT_RESPONSE command instructs the device on what action to take in response to a TON_MAX fault. The format for this command is given in Table 14. The device also:

- Sets the VOUT Bit in the STATUS_WORD
- Sets the TON_MAX Fault Bit in the STATUS_VOUT Command
- Notifies the Host by Asserting $\overline{\text{ALERT}}$, Unless Masked

This command has one data byte.

## PMBus COMMAND DETAILS (Fault Response and Communication)

**Table 14. Data Byte Contents for the Following _FAULT_RESPONSE Commands: VIN_OV, OT and TON_MAX**

| BITS | DESCRIPTION | VALUE | MEANING |
|---|---|---|---|
| [7:6] | For all values of bits [7:6], the LTC3888-1:<br>• Sets the corresponding fault bits in the status commands.<br>• Notifies the host by asserting $\overline{\text{ALERT}}$, unless masked.<br>The fault, once set, is cleared only when one or more of the following events occurs:<br>• The device receives a CLEAR_FAULTS command.<br>• The corresponding fault bit is written to a one.<br>• The output is commanded off, then on, by the RUN pin or OPERATION command.<br>• The device receives a RESTORE_USER_ALL command.<br>• The device receives an MFR_RESET command.<br>• IC supply power is cycled. | 00 | The LTC3888-1 continues operating without interruption. |
| | | 01 | Not supported. Writing this value will generate a CML fault. |
| | | 10 | The LTC3888-1 shuts down immediately (disables the output) and responds according to the retry setting in bits [5:3]. |
| | | 11 | Not supported. Writing this value will generate a CML fault. |
| [5:3] | Retry setting. | 000-110 | The LTC3888-1 does not attempt to restart. The output remains disabled until the fault is cleared, the device is commanded off and then on, or IC supply power is cycled. |
| | | 111 | The LTC3888-1 attempts to restart continuously without limitation with an interval set by MFR_RETRY_DELAY. This response persists until the unit is commanded off, IC supply power is removed, or another fault response forces shutdown without retry. |
| [2:0] | Delay time. | xxx | Not supported. Values ignored. |

### *MFR_RETRY_DELAY*

The MFR_RETRY_DELAY command sets the time, in milliseconds, between restart attempts for all retry fault responses. Retry delay starts once the fault is no longer detected by the LTC3888-1 or its $\overline{\text{FAULT}}$ pin is externally released. Legal values run from 120ms to 32.7 seconds.

This command has two data bytes in Linear_5s_11s format.

### *SMBALERT_MASK*

The SMBALERT_MASK command can be used to prevent a particular status bit or bits from pulling $\overline{\text{ALERT}}$ low as they are asserted.

Figure 50 shows an example of the Write Word format used to set an $\overline{\text{ALERT}}$ mask, in this case without PEC. The bits in the mask byte align with bits in the specified status register. For example, if the STATUS_TEMPERATURE command code is sent in the first data byte, and the mask byte contains 0x40, then a subsequent External Overtemperature Warning would still set bit 6 of STATUS_TEMPERATURE but not assert $\overline{\text{ALERT}}$. All other supported STATUS_TEMPERATURE bits would continue to assert $\overline{\text{ALERT}}$ if set.

Figure 51 shows an example of the Block Write – Block Read Process Call protocol used to read back the present state of the $\overline{\text{ALERT}}$ mask for any supported status register, again without PEC.

SMBALERT_MASK cannot be applied to STATUS_BYTE, STATUS_WORD, MFR_COMMON or MFR_PADS_LTC3888-1. Factory default masking for applicable status registers is shown below. Providing an unsupported command code to SMBALERT_MASK will generate a CML for Invalid/Unsupported Data.

# PMBus COMMAND DETAILS (Fault Response and Communication)

**SMBALERT_MASK Default Setting: (Refer Also to Figure 2)**

| STATUS RESISTER | ALERT Mask Value | MASKED BITS |
|---|---|---|
| STATUS_VOUT | 0x00 | None |
| STATUS_IOUT | 0x00 | None |
| STATUS_TEMPERATURE | 0x00 | None |
| STATUS_CML | 0x00 | None |
| STATUS_INPUT | 0x00 | None |
| STATUS_MFR_SPECIFIC | 0x11 | Bit 4 (internal PLL unlocked), bit 0 ($\overline{FAULT}$ low) |

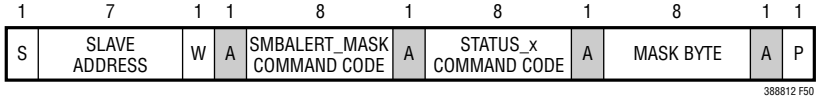



**Figure 50. Example of Setting SMBALERT_MASK**

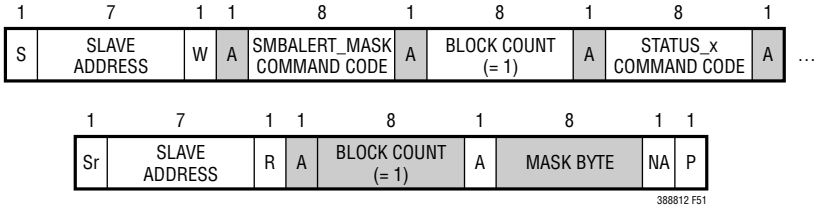



**Figure 51. Example of Reading SMBALERT_MASK**

## *MFR_FAULT_PROPAGATE*

The MFR_FAULT_PROPAGATE command determines internal events that cause $\overline{FAULT}$ to be asserted. Setting a bit in this register allows the specified condition to also assert the $\overline{FAULT}$ output for that channel. $\overline{FAULT}$ is not asserted by a fault, even if set to propagate, if that FAULT_RESPONSE is set to Ignore. The state of SMBLALERT_MASK does not affect fault propagation.

**Supported Values:**

| BIT | PROPAGATED CONDITION |
|---|---|
| 15 | (Reserved). |
| 14 | $V_{OUT}$ short cycled (automatically deasserted 120ms after $V_{OUT}$ is fully OFF). |
| 13 | TON_MAX_FAULT_LIMIT exceeded. |
| 12 | VOUT_UV_FAULT_LIMIT exceeded (unfiltered, aka VOUT_UV_UF). |
| 11 | MFR_OT_FAULT_LIMIT exceeded. |
| 10* | Channel 1 POWER_GOOD false. |
| 9* | Channel 0 POWER_GOOD false. |
| 8 | (Reserved). |

## PMBus COMMAND DETAILS (Fault Response and Communication)

| BIT | PROPAGATED CONDITION |
|---|---|
| 7 | OT_FAULT_LIMIT exceeded. |
| 6 | (Reserved). |
| 5 | (Reserved). |
| 4 | VIN_OV_FAULT_LIMIT exceeded. |
| 3 | (Reserved). |
| 2 | IOUT_OC_FAULT_LIMIT exceeded. |
| 1 | VOUT_UV_FAULT_LIMIT exceeded |
| 0 | VOUT_OV_FAULT_LIMIT exceeded, power stage fault or UV, or VDR monitor UV |

*If this bit is set, MFR_FAULT_RESPONSE should be set to ignore (0x00), otherwise the rail might not start.

This command has two data bytes.

### *MFR_FAULT_RESPONSE*

The MFR_FAULT_RESPONSE command instructs the device on what action to take in response to a $\overline{\text{FAULT}}$ pin being pulled low externally.

**Supported Values:**

| VALUE | MEANING |
|---|---|
| 0xC0 | Related rail is immediately disabled. |
| 0x00 | Input ignored, PWM operation continues without interruption. |

When a $\overline{\text{FAULT}}$ pin is pulled low externally, the device also:

- Sets the MFR_SPECIFIC Bit in the STATUS_WORD
- Sets Bit 0 in the STATUS_MFR_SPECIFIC Command to Indicate $\overline{\text{FAULT}}$ Is or Has Been Pulled Low
- Notifies the Host by Asserting $\overline{\text{ALERT}}$, Unless Masked

This command has one data byte.

### *MFR_FAULT_LOG*

The MFR_FAULT_LOG command allows the contents of the fault log to be read. This log is created with MFR_FAULT_LOG_STORE or at the first fault occurrence after an MFR_FAULT_LOG_CLEAR. If a fault occurs within the first second after applying power, some earlier pages in the log may not contain valid data.

This read-only command uses block protocol with 147 bytes of data requiring an estimated data transfer time of 3.4ms at 400kHz. The $t_{TIMEOUT}$ parameter is extended when this command is executed and a fault log is present.

**Refer to Fault Log Details in the Operation section for complete information on using the LTC3888-1 fault log.**

### *MFR_FAULT_LOG_CLEAR*

The MFR_FAULT_LOG_CLEAR command erases all stored fault log values. After a clear is issued, up to 8ms may be required to clear related bit 3 in STATUS_MFR_SPECIFIC.

This write-only command has no data bytes.

# PMBus COMMAND DETAILS (EEPROM User Access)

## EEPROM USER ACCESS

| COMMAND NAME | CMD CODE | DESCRIPTION | TYPE | PAGED | DATA FORMAT | UNITS | NVM | DEFAULT VALUE |
|---|---|---|---|---|---|---|---|---|
| STORE_USER_ALL | 0x15 | Store entire operating memory in EEPROM. | Send Byte | N | | | | |
| RESTORE_USER_ALL | 0x16 | Restore entire operating memory from EEPROM. | Send Byte | N | | | | |
| MFR_COMPARE_USER_ALL | 0xF0 | Compare operating memory with EEPROM contents. | Send Byte | N | | | | |
| MFR_FAULT_LOG_STORE | 0xEA | Force capture of fault log in RAM and transfer to EEPROM. | Send Byte | N | | | | |
| MFR_EE_UNLOCK | 0xBD | (contact the factory) | | | | | | |
| MFR_EE_ERASE | 0xBE | (contact the factory) | | | | | | |
| MFR_EE_DATA | 0xBF | (contact the factory) | | | | | | |
| USER_DATA_00 | 0xB0 | EEPROM word reserved for LTpowerPlay. | R/W Word | N | Reg | | ● | |
| USER_DATA_01 | 0xB1 | EEPROM word reserved for LTpowerPlay. | R/W Word | Y | Reg | | ● | |
| USER_DATA_02 | 0xB2 | EEPROM word reserved for OEM use. | R/W Word | N | Reg | | ● | |
| USER_DATA_03 | 0xB3 | EEPROM word available for general data storage. | R/W Word | Y | Reg | | ● | 0x0000 |
| USER_DATA_04 | 0xB4 | EEPROM word available for general data storage. | R/W Word | N | Reg | | ● | 0x0000 |

Related commands: MFR_CONFIG_ALL

Note that if the LTC3888-1 die temperature exceeds 130°C, execution of any command in the above table except RESTORE_USER_ALL and MFR_FAULT_LOG_STORE will be disabled until the IC temperature drops below 125°C. RESTORE_USER_ALL is executed immediately, and MFR_FAULT_LOG_STORE to *EEPROM* is executed after the IC temperature drops below 125°C. *Using any command that writes data to the EEPROM is strongly discouraged if bit 6 of STATUS_MFR_ SPECIFIC is set, indicating the internal die temperature is above 85°C. Data retention of 10 years is not guaranteed if the EEPROM is written above a junction temperature of 85°C.*

### *STORE_USER_ALL*

The STORE_USER_ALL command instructs the PMBus device to copy the entire contents of the operating memory to internal EEPROM PMBus configuration space.

This write-only command has no data bytes.

### *RESTORE_USER_ALL*

The RESTORE_USER_ALL command instructs the PMBus device to copy the entire contents of the internal EEPROM to matching locations in operating memory. The values in operating memory are overwritten by the values retrieved from EEPROM. Both master channels should be turned off prior to issuing this command. The LTC3888-1 ensures all PWM channels are off, loads the operating memory from internal EEPROM, clears all faults, reads the resistor configuration pins, and then performs a soft-start of any enabled master channels.

This write-only command has no data bytes.

# PMBus COMMAND DETAILS (EEPROM User Access/Unit Identification)

### *MFR_COMPARE_USER_ALL*

The MFR_COMPARE_USER_ALL command instructs the LTC3888-1 to compare current operating memory with the contents of the internal EEPROM. If the compared memories differ, a CML fault is generated.

This write-only command has no data bytes.

### *MFR_FAULT_LOG_STORE*

The MFR_FAULT_LOG_STORE command forces a data log to be written to RAM (at any temperature) and transferred to internal EEPROM as if a fault event had occurrred. Execution of this command will lock the fault log until a subsequent MFR_FAULT_LOG_CLEAR is received. Die temperature limitations apply to the EEPROM write, as noted above. This command will generate a CML fault if the Enable Fault Logging bit is clear in MFR_CONFIG_ALL.

This write-only command has no data bytes.

### *MFR_EE_xxxx*

The MFR_EE_xxxx commands facilitate bulk programming of the LTC3888-1 internal EEPROM. Contact the factory for details.

### *USER_DATA_0x*

The USER_DATA_0x commands provide uncommitted EEPROM locations that may be applied as system scratchpad space. USER_DATA_00 and USER_DATA_01 should not be modified when using the LTpowerPlay GUI. Some contract manufacturers also reserve use of USER_DATA_02 for their own inventory control.

## UNIT IDENTIFICATION

| COMMAND NAME | CMD CODE | DESCRIPTION | TYPE | PAGED | DATA FORMAT | UNITS | NVM | DEFAULT VALUE |
|---|---|---|---|---|---|---|---|---|
| MFR_ID | 0x99 | Manufacturer identification. | R String | N | ASC | | | LTC |
| IC_DEVICE_ID | 0xAD | LTC3888-1 model number. | R String | N | ASC | | | LTC3888-1 |
| MFR_SPECIAL_ID | 0xE7 | Unique manufacturer product ID | R Word | N | REG | | | 0x488x |

The following three read-only commands use block format.

### *MFR_ID*

The MFR_ID command returns the manufacturer ID of the LTC3888-1 using 8-bit ASCII characters.

### *IC_DEVICE_ID*

The IC_DEVICE_ID command returns the ADI IC part number using 8-bit ASCII characters.

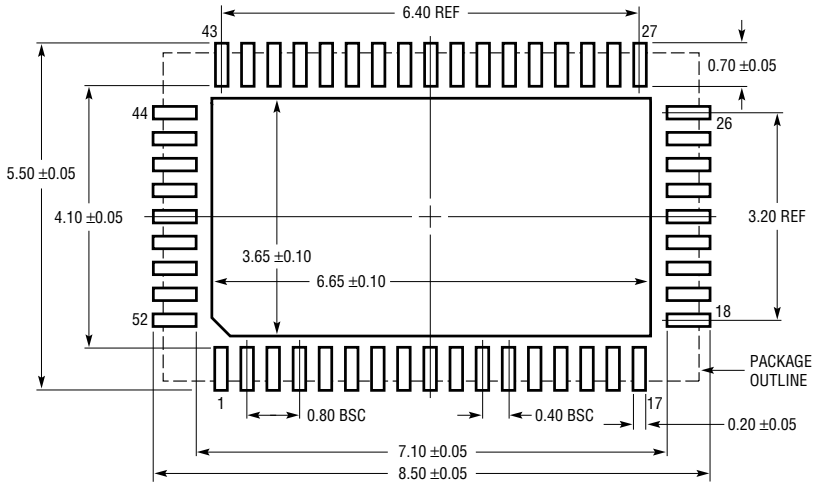
### *MFR_SPECIAL_ID*

The MFR_SPECIAL_ID command returns a unique binary product code for the device. X is adjustable by the maufacturer.

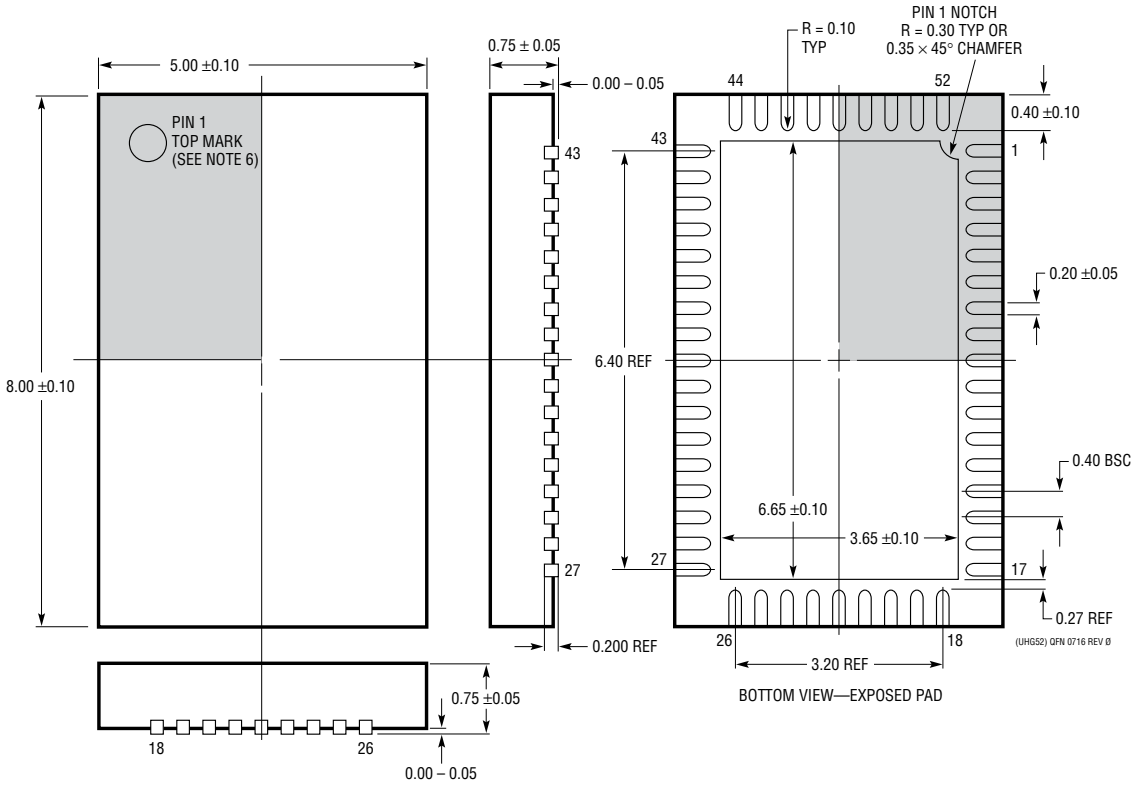
This read-only command has two data bytes.

# PACKAGE DESCRIPTION

**UHG Package**
**52-Lead Plastic QFN (5mm × 8mm)**
(Reference LTC DWG # 05-08-1550 Rev Ø)




RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED




NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

Rev. 0

# TYPICAL APPLICATIONS

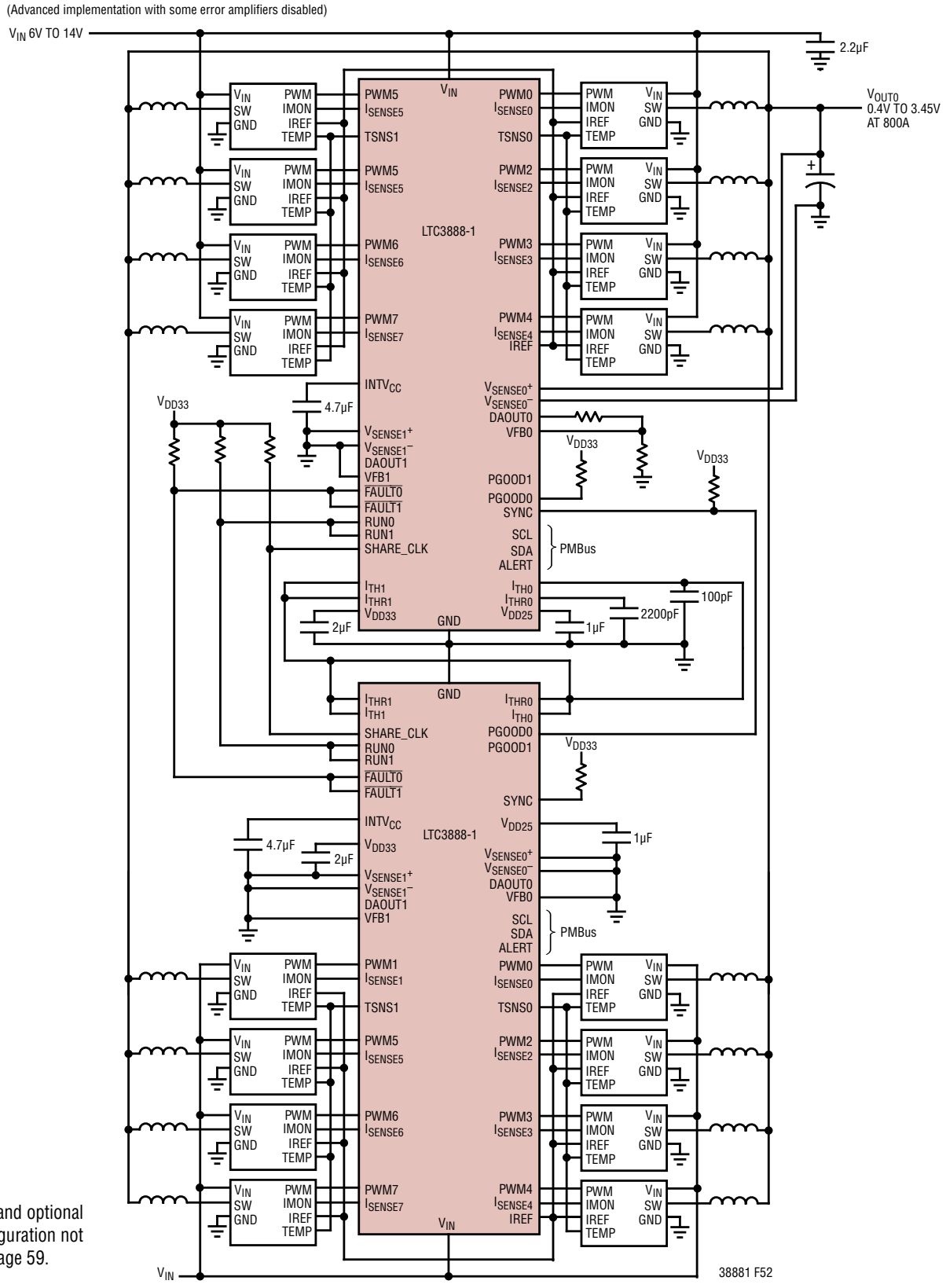
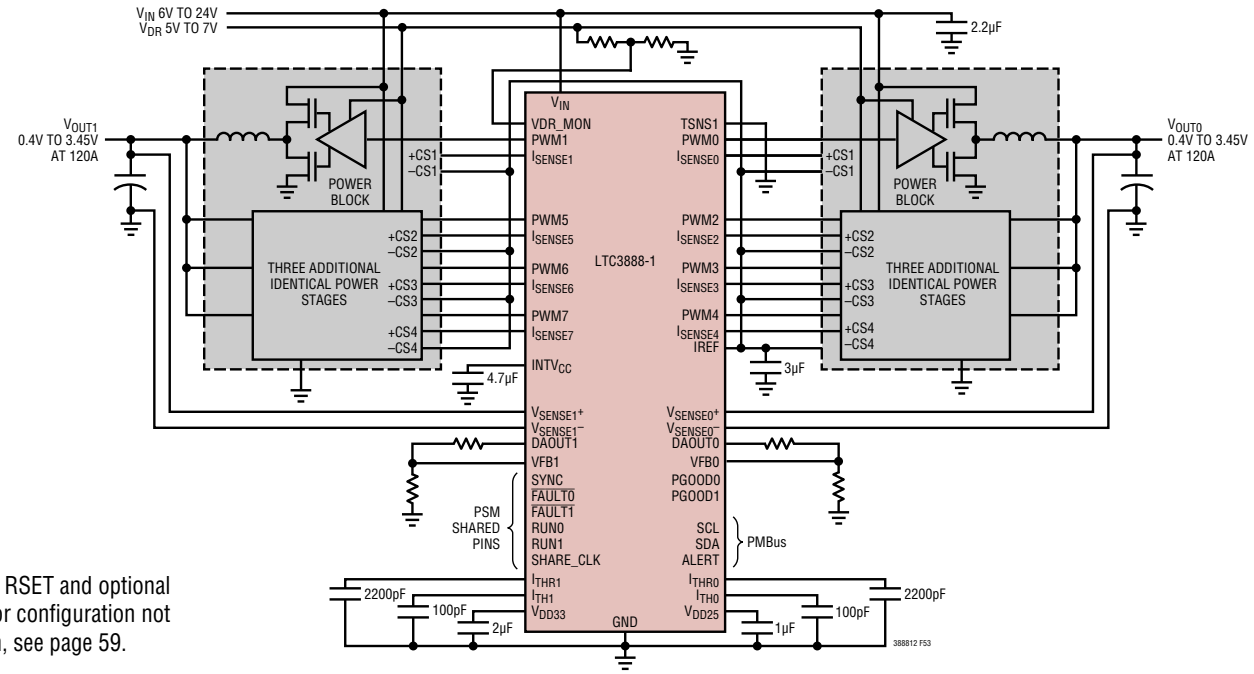



**Figure 52. 16-Phase 800A Output**

## TYPICAL APPLICATIONS




NOTE: RSET and optional resistor configuration not shown, see page 59.

**Figure 53. Dual 4-Phase 120A Power Block Rails**

## RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|---|---|---|
| LTM4676A | Dual 13A or Single 26A Step-Down DC/DC µModule Regulator with Digital Power Management | $V_{IN}$ Up to 26.5V, 0.5V ≤ $V_{OUT}$ (±0.5%) ≤ 5.4V, ±2% $I_{OUT}$ ADC Accuracy, Fault Logging, $I^2C$/PMBus Interface, 16mm × 16mm × 5mm BGA Package |
| LTM4677 | Dual 18A or Single 36A Step-Down DC/DC µModule Regulator with Digital Power System Management | 4.5V ≤ $V_{IN}$ ≤ 16V, 0.5V ≤ $V_{OUT}$ (±0.5%) ≤ 1.8V, $I^2C$/PMBus Interface, 16mm × 16mm × 5mm BGA Package |
| LTM4700 | Dual 50A or Single 100A Step-Down DC/DC µModule Regulator with Digital Power System Management | 4.5V ≤ $V_{IN}$ ≤ 16V, 0.5V ≤ $V_{OUT}$ ≤ 1.8V, ±0.5% $V_{OUT}$ Accuracy, Fault Logging, $I^2C$/PMBus Interface, 15mm × 22mm × 7.87mm BGA Package |
| LTC2977 | 8-Channel PMBus Power System Manager | Fault Logging of 8 Output Voltages, $V_{IN}$ and Die Temperature |
| LTC3882/ LTC3882-1 | Dual Output Multiphase Step-Down DC/DC Voltage Mode Controller Digital Power System Management | $V_{IN}$ Up to 38V, 0.5V ≤ $V_{OUT}$ ≤ 5.25V, ±0.5% $V_{OUT}$ Accuracy, Fault Logging, $I^2C$/PMBus Interface with EEPROM and 16-Bit ADC |
| LTC3884/ LTC3884-1 | Dual Output Multiphase Step-Down DC/DC Current Mode Controller with Sub-mΩ DCR Sensing and Digital Power System Management | 4.5V ≤ $V_{IN}$ ≤ 38V, 0.5V ≤ $V_{OUT}$ (±0.5%) ≤ 5.5V, Fault Logging, $I^2C$/PMBus Interface with EEPROM and 16-Bit ADC, Programmable Analog Loop Compensation, Input Current Sense |
| LTC3874 | Multiphase Step-Down DC/DC Current Mode Slave Controller with Sub-mΩ DCR Sensing | 4.5V ≤ $V_{IN}$ ≤ 38V, 0.5V ≤ $V_{OUT}$ Up to 5.5V, Accurate Current Sharing |
| LTC3887/ LTC3887-1 | Dual Output Multiphase Step-Down DC/DC Current Mode Controller Digital Power System Management | $V_{IN}$ Up to 24V, 0.5V ≤ $V_{OUT}$ ≤ 5.5V, ±0.5% $V_{OUT}$ Accuracy, Fault Logging, $I^2C$/PMBus Interface with EEPROM and 16-Bit ADC |
| LTC3886 | 60V Dual Output Multiphase Step-Down DC/DC Current Mode Controller Digital Power System Management | 4.5V ≤ $V_{IN}$ ≤ 60V, 0.5V ≤ $V_{OUT}$ (±0.5%) ≤ 13.8V, Fault Logging, $I^2C$/PMBus Interface with EEPROM and 16-Bit ADC, Programmable Analog Loop Compensation, Input Current Sense |
| LTC3889 | 60V Dual Output Multiphase Step-Down DC/DC Current Mode Controller Digital Power System Management | 5V ≤ $V_{IN}$ ≤ 60V, 1V ≤ $V_{OUT}$ ≤ 40V, ±0.5% $V_{OUT}$ Accuracy, Fault Logging, $I^2C$/PMBus Interface with EEPROM and 16-Bit ADC, Programmable Analog Loop Compensation, Input Current Sense |
| LTC3870/ LTC3870-1 | 60V Multiphase Step-Down DC/DC Current Mode Slave Controller | $V_{IN}$ Up to 60V, 0.5V ≤ $V_{OUT}$ Up to 14V, Accurate Current Sharing |
| LTC3888/ LTC3888-2 | Dual Output 8-Phase Expandable Step-Down DC/DC Current Mode Controller with Digital Power System Management and SPI Interface | 4.5V ≤ $V_{IN}$ ≤ 28.5V, 0.3V ≤ $V_{OUT}$ (±0.5%) ≤ 3.45V, Fault Logging, $I^2C$/PMBus Interface with EEPROM and 16-Bit ADC, Programmable Analog Loop Compensation with Load Step Emulation |