19-6164; Rev 0; 12/11

DS2483

Single-Channel 1-Wire Master with Adjustable Timing and Sleep Mode

General Description

The DS2483 is an I²C-to-1-Wire® bridge device that interfaces directly to standard (100kHz max) or fast (400kHz max) I²C masters to perform protocol conversion between the I²C master and any downstream 1-Wire slave devices. Relative to any attached 1-Wire slave device, the DS2483 is a 1-Wire master. Internal, user-adjustable timers relieve the system host processor from generating time-critical 1-Wire waveforms, supporting both standard and overdrive 1-Wire communication speeds. In addition, the 1-Wire bus can be powered down under software control. The dual-voltage operation allows different operating voltages on the I²C and 1-Wire side. Strong pullup features support 1-Wire power delivery to 1-Wire devices such as EEPROMs and sensors. When not in use, the DS2483 can be put in sleep mode where power consumption is minimal.

Applications

Printers

Medical Instruments

Industrial Sensors

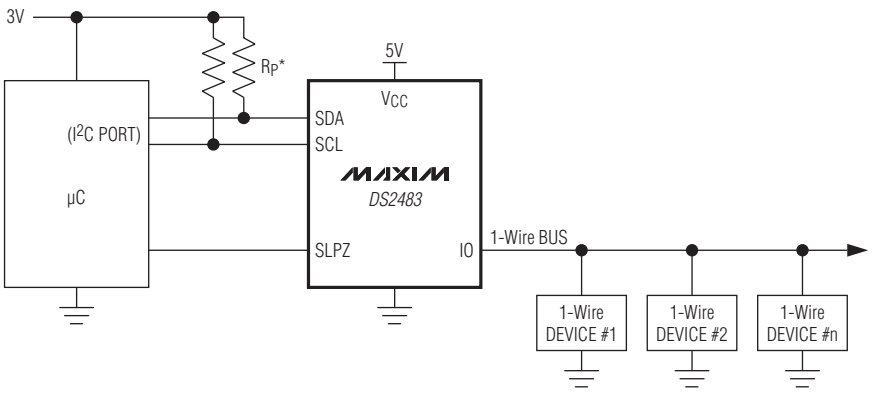
Cell Phones

Benefits and Features

- **I²C Host Interface Supports 100kHz and 400kHz I²C Communication Speeds**
- **Standard and Overdrive 1-Wire Communication Speeds**
- **Adjustable 1-Wire Timing for t_{RSTL}, t_{MSP}, t_{W0L}, and t_{REC0}**
- **1-Wire Port Can Be Powered Down Under Software Control**
- **Supports Power-Saving Sleep Mode (SLPZ Pin), Where the 1-Wire Port is in High Impedance**
- **I²C Operating Voltages: 1.8V ±5%, 3.3V ±10%, and 5.0V +5/-10%**
- **Built-In Level Translator: 1-Wire Operating Voltage from 1.8V -5% to 5.0V +5%, Independent of I²C Voltage**
- **Built-In ESD Protection Level of ±8kV Human Body Model (HBM) Contact Discharge on IO Pin**
- **-40°C to +85°C Operating Temperature Range**
- **8-Pin TDFN and 6-Pin SOT23 Packages**

***Ordering Information* appears at end of data sheet.**

Typical Application Circuit



*RP = I²C PULLUP RESISTOR (SEE THE *Pullup Resistor RP Sizing* SECTION FOR RP SIZING)

1-Wire is a registered trademark of Maxim Integrated Products, Inc.

*For related parts and recommended products to use with this part, refer to: **www.maxim-ic.com/DS2483.related***

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Pin Relative to Ground.....-0.5V to +6V
Maximum Current into Any Pin.....20mA
Operating Temperature Range..... -40°C to +85°C
Junction Temperature .....+150°C
Storage Temperature Range..... -55°C to +125°C
Lead temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(T_A = -40°C to +85°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		1.71		5.25	V
I^2C Voltage (Note 2)	V_{CI2C}	1.8V	1.71	1.8	1.89	V
		3.3V	2.97	3.3	3.63	
		5V	4.5	5.0	5.25	
Supply Current	I_{CC}	No communication, V_{CC} = full range			300	µA
		Sleep mode, V_{CC} = 5.25V			4	
		Sleep mode, V_{CC} = 3.6V			3.0	
Power-On-Reset Trip Point	V_{POR}	V_{CC} = full range		1.0	1.5	V
IO PIN: GENERAL DATA						
1-Wire Input High Voltage	V_{IH1}	V_{CC} = full range	0.6 x V_{CC}			V
1-Wire Input Low Voltage	V_{IL1}	V_{CC} = full range			0.2 x V_{CC}	V
1-Wire Weak Pullup Resistor	R_{WPU}	Low range	375	500	815	Ω
		High range	700	1000	1375	
1-Wire Output Low Voltage	V_{OL1}	I_{OL} = 8mA sink current			0.2	V
Active Pullup On-Threshold	V_{IAPO}	V_{CC} = full range	0.6	0.95	1.2	V
Active Pullup On-Time (Note 3)	t_{APU}	1-Wire time slot	Equal to t_{REC0}			µs
		1-Wire reset standard speed	2.375	2.5	2.625	
		1-Wire reset overdrive speed	0.475	0.5	0.525	
Active Pullup Impedance	R_{APU}	V_{CC} = 1.71V, 4mA load			100	Ω
		V_{CC} = 3.0V, 4mA load			60	
		V_{CC} = 4.5V, 4mA load			40	
1-Wire Output Fall Time (Note 4)	t_{F1}	Standard, 10pF < C_{LOAD} < 400pF	0.25		1	µs
		Overdrive, 10pF < C_{LOAD} < 400pF	0.05		0.2	
IO PIN: 1-Wire TIMING (Note 5)						
Reset Low Time	t_{RSTL}	Standard	-5%	See Table 7	+5%	µs
		Overdrive				
Reset High Time	t_{RSTH}	Standard and overdrive	Equal to t_{RSTL}			µs

ELECTRICAL CHARACTERISTICS (continued)

(T_A = -40°C to +85°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Presence-Detect Sample Time	t_{MSP}	Standard	-5%	See Table 7	+5%	µs
		Overdrive				
Sampling for Short and Interrupt	t_{SI}	Standard	7.6	8	8.4	µs
		Overdrive	0.71	0.75	0.79	
Write-One/Read Low Time	t_{W1L}	Standard	7.6	8	8.4	µs
		Overdrive (Note 6)	0.71	0.75	0.79	
Read Sample Time	t_{MSR}	Standard	11.4	12	12.6	µs
		Overdrive	1.66	1.75	1.84	
Write-Zero Low Time	t_{W0L}	Standard	-5%	See Table 7	+5%	µs
		Overdrive				
Write-Zero Recovery Time	t_{REC0}	Standard and overdrive	-5%	See Table 7	+5%	µs
1-Wire Time Slot	t_{SLOT}	Standard and overdrive	Equal to t_{W0L} + t_{REC0}			µs
SLPZ PIN						
Low-Level Input Voltage	V_{IL}	V_{CC} = full range	-0.5		+0.5	V
High-Level Input Voltage	V_{IH}	(Note 7)	1.3		V_{CCACT}	V
Input Leakage Current (Note 2)	I_I	$V_{CI2C} \le 1.89V$			6	µA
		$V_{CI2C} \le 3.63V$			15	
		$V_{CI2C} \le 5.25V$			32	
Wake-Up Time from Sleep Mode	t_{SWUP}	(Notes 4, 8)			2	ms
I²C SCL AND SDA PINS (Note 9)						
Low-Level Input Voltage	V_{IL}	V_{CI2C} = full range	-0.5		0.3 x V_{CI2C}	V
High-Level Input Voltage	V_{IH}		0.7 x V_{CI2C}		V_{CI2C} + 0.5V	V
Hysteresis of Schmitt Trigger Inputs (Note 4)	V_{HYS}	V_{CI2C} > 2.0V	0.05 x V_{CI2C}			V
		V_{CI2C} < 2.0V	0.1 x V_{CI2C}			
Low-Level Output Voltage at 3mA Sink Current	V_{OL}	V_{CI2C} > 2.0V			0.4	V
		V_{CI2C} < 2.0V			0.2 x V_{CI2C}	
Output Fall Time from $V_{IH(MIN)}$ to $V_{IL(MAX)}$ with a Bus Capacitance from 10pF to 400pF	t_{OF}	(Note 4)	60		250	ns
Pulse Width of Spikes Suppressed by Input Filter	t_{SP}				50	ns

ELECTRICAL CHARACTERISTICS (continued)

(T_A = -40°C to +85°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Current with Input Voltage Between 0.1 x $V_{CC(MAX)}$ and 0.9 x $V_{CC(MAX)}$	I_I	(Note 10)	-10		+10	µA
Input Capacitance	C_I	(Note 4)			10	pF
SCL Clock Frequency	f_{SCL}		0		400	kHz
Hold Time (Repeated) START Condition (After this period, the first clock pulse is generated.)	$t_{HD:STA}$		0.6			µs
Low Period of the SCL Clock	t_{LOW}		1.3			µs
High Period of the SCL Clock	t_{HIGH}		0.6			µs
Setup Time for a Repeated START Condition	$t_{SU:STA}$		0.6			µs
Data Hold Time	$t_{HD:DAT}$	(Notes 11, 12)			0.9	µs
Data Setup Time	$t_{SU:DAT}$	(Note 13)	250			ns
Setup Time for STOP Condition	$t_{SU:STO}$		0.6			µs
Bus Free Time Between a STOP and START Condition	t_{BUF}		1.3			µs
Capacitive Load for Each Bus Line	C_B	(Notes 4, 14)			400	pF
Oscillator Warmup Time	t_{OSCWUP}	(Notes 4, 8)			2	ms

Note 1: Limits are 100% production tested at T_A = +25°C and/or T_A = +85°C. Limits over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization. Typical values are not guaranteed.

Note 2: The V_{CI2C} voltage is applied at the SLPZ pin. V_{CI2C} must always be ≤ V_{CC}. The DS2483 measures V_{CI2C} after t_{SWUP} (wakeup from sleep mode) or after t_{OSCWUP} (power-on reset). The Device Reset command does not cause the DS2483 to measure V_{CI2C}.

Note 3: The active pullup does not apply to the rising edge of a presence pulse outside of a 1-Wire Reset command or during the recovery after a short on the 1-Wire line.

Note 4: Guaranteed design and not production tested.

Note 5: Except for t_{F1}, all 1-Wire timing specifications are derived from the same timing circuit.

Note 6: Although 1-Wire slave data sheets specify a t_{W1L} and t_{RL} minimum of 1µs, 1-Wire slaves will accept the shorter 0.71µs t_{W1L} and t_{RL} of the DS2483.

Note 7: V_{CCACT} refers to the V_{CC} level being applied in the application.

Note 8: I^2C communication should not take place for the max t_{OSCWUP} or t_{SWUP} time following a power-on reset or a wake-up from sleep mode.

Note 9: All I^2C timing values are referenced to $V_{IH(MIN)}$ and $V_{IL(MAX)}$ levels.

Note 10: The DS2483 does not obstruct the SDA and SCL lines if SLPZ is at 0V or if V_{CC} is switched off.

Note 11: The DS2483 provides a hold time of at least 300ns for the SDA signal (referenced to the $V_{IH(MIN)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.

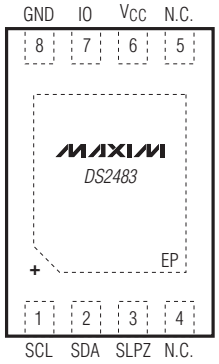
Note 12: The maximum $t_{HD:DAT}$ must only be met if the device does not stretch the low period (t_{LOW}) of the SCL signal.

Note 13: A fast mode I^2C bus device can be used in a standard mode I^2C bus system, but the requirement $t_{SU:DAT} \geq 250ns$ must then be met. This requirement is met since the DS2483 does not stretch the low period of the SCL signal. Also the acknowledge timing must meet this setup time (I^2C bus specification Rev. 03, 19 June 2007).

Note 14: C_B = Total capacitance of one bus line in pF. The maximum bus capacitance allowable can vary from this value depending on the actual operating voltage and frequency of the application (I^2C bus specification Rev. 03, 19 June 2007).

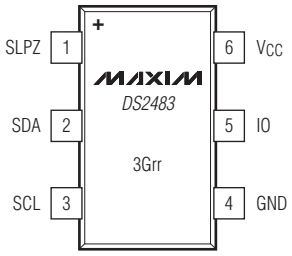
Pin Configurations

TOP VIEW



TDFN (2mm x 3mm)

TOP VIEW



SOT23

"rr" = REVISION CODE

Pin Description

PIN		NAME	FUNCTION
TDFN-EP	SOT23		
1	3	SCL	I^2C Serial-Clock Input. Must be connected to the I^2C bus supply voltage through a pullup resistor.
2	2	SDA	I^2C Serial-Data Input/Output. Must be connected to the I^2C bus supply voltage through a pullup resistor.
3	1	SLPZ	Power Supply for I^2C Port and Active-Low Control Input to Activate the Low-Power Sleep Mode. This pin can be driven directly by a push-pull port or by an open-drain port with a 2.2kΩ pullup resistor to the I^2C voltage (V_{CI2C}) over the entire operating voltage range.
4, 5	—	N.C.	No Connection. Not internally connected.
6	6	V_{CC}	Power-Supply Input
7	5	IO	Input/Output Driver for 1-Wire Line
8	4	GND	Ground Reference
—	—	EP	Exposed Pad (TDFN Only). Solder evenly to the board's ground plane for proper operation. Refer to Application Note 3273: *Exposed Pads: A Brief Introduction* for additional information.

Single-Channel 1-Wire Master with Adjustable Timing and Sleep Mode

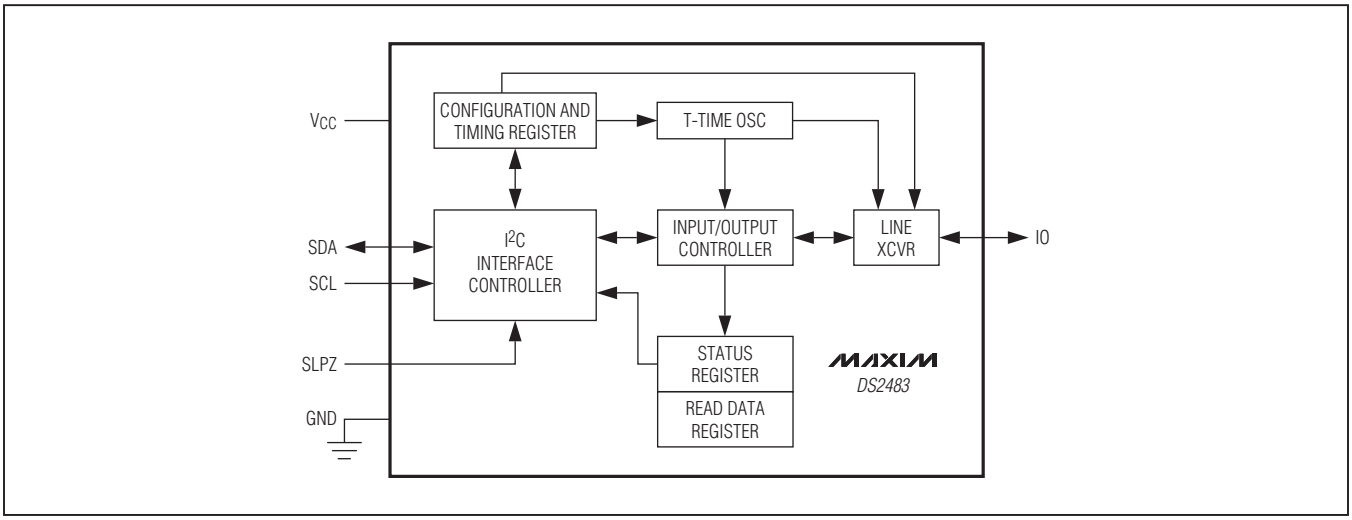


Figure 1. Block Diagram

Table 1. Device Configuration Register Bit Assignment

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
$\overline{1WS}$	$\overline{SPU}$	$\overline{PDN}$	$\overline{APU}$	1WS	SPU	PDN	APU

Detailed Description

The DS2483 is a self-timed 1-Wire master that supports advanced 1-Wire waveform features including standard and overdrive speeds, active pullup, and strong pullup for power delivery. The active pullup affects rising edges on the 1-Wire side. The strong pullup function uses the same pullup transistor as the active pullup, but with a different control algorithm. Once supplied with command and data, the input/output controller of the DS2483 performs time-critical 1-Wire communication functions such as reset/presence-detect cycle, read-byte, write-byte, single bit R/W, and triplet for ROM Search, without requiring interaction with the host processor. The host obtains feedback (completion of a 1-Wire function, presence pulse, 1-Wire short, search direction taken) through the Status register and data through the Read Data register. The DS2483 communicates with a host processor through its I²C bus interface in standard mode or in fast mode. See Figure 1 for a block diagram.

Device Registers

The DS2483 has four registers that the I²C host can read: Device Configuration, Status, Read Data, and Port Configuration. These registers are addressed by a read pointer. The position of the read pointer, i.e., the register that the host reads in a subsequent read access, is defined by the instruction the DS2483 executed last. To enable certain 1-Wire features, the host has read- and write-access to the Device Configuration and Port Configuration registers.

Device Configuration Register

The DS2483 supports four 1-Wire features that are enabled or selected through the Device Configuration register (Table 1). These features are as follows:

- Active Pullup (APU)
- 1-Wire Power-Down (PDN)
- Strong Pullup (SPU)
- 1-Wire Speed (1WS)

APU, SPU, and 1WS can be selected in any combination. While APU and 1WS maintain their states, SPU returns to its inactive state as soon as the strong pullup has ended.

After a device reset (power-up cycle or initiated by the Device Reset command), the Device Configuration register reads 00h. When writing to the Device Configuration register, the new data is accepted only if the upper nibble (bits 7 to 4) is the one's complement of the lower nibble (bits 3 to 0). When read, the upper nibble is always 0h.

Active Pullup (APU)

The APU bit controls whether an active pullup (low impedance transistor) or a passive pullup (R_{WPU} resistor) is used to drive a 1-Wire line from low to high. When APU = 0, active pullup is disabled (resistor mode). Enabling active pullup is generally recommended for best 1-Wire bus performance. **The active pullup does not apply to the rising edge of a recovery after a short on the 1-Wire line.** If enabled, a fixed-duration active pullup (typically 2.5µs standard speed, 0.5µs overdrive speed) also applies in a reset/presence detect cycle on the rising edges after t_{RSTL} and after t_{PDL}.

The circuit that controls rising edges operates as follows (Figure 2): At t_1, the pulldown (from DS2483 or 1-Wire slave) ends. From this point on the 1-Wire bus is pulled high through R_{WPU} internal to the DS2483. V_{CC} and the capacitive load of the 1-Wire line determine the slope. In case that active pullup is disabled (APU = 0), the resistive pullup continues, as represented by the solid line. With active pullup enabled (APU = 1), and when at t_2 the voltage has reached the V_{IAPO} threshold, the DS2483 activates a low-impedance pullup transistor, as represented by the dashed line. The active pullup remains active until the end of the time slot (t_3), after which the resistive pullup continues. The shortest duration of the active pullup is $t_{RECO} - (t_2 - t_1)$ in a write-zero time slot and the longest duration is $t_{W0L} + t_{RECO} - t_{W1L} - (t_2 - t_1)$ in a write-one time slot. In a read-data time slot, the active pullup duration is slave dependent. See the *Strong Pullup (SPU)* section for a way to keep the pullup transistor conducting beyond t_3.

1-Wire Power Down (PDN)

The PDN bit is used to remove power from the 1-Wire port, e.g., to force a 1-Wire slave to perform a power-on reset. PDN can as well be used in conjunction with the sleep mode (see Table 2 for details). While PDN is 1, no 1-Wire communication is possible. To end the 1-Wire power-down state, the PDN bit must be changed to 0.

Note: When writing to the device configuration register with PDN = 1 to activate the 1-Wire power-down mode, make sure that the SPU bit is 0.

Table 2. Effects of PDN and SLPZ

PDN =	SLPZ IS LOGIC 0	SLPZ IS LOGIC 1
0	• R_{WPU} is connected. • IO is at V_{CC}, keeping the slaves powered. • The DS2483 is powered down (sleep mode).	• R_{WPU} is connected. • IO is at V_{CC}, keeping the slaves powered. • The DS2483 is powered up (normal operation).
1	• R_{WPU} is disconnected. • IO is at 0V, causing the slaves to lose power. • The DS2483 is powered down (sleep mode).	• R_{WPU} is disconnected. • IO is at 0V, causing the slaves to lose power. • The DS2483 is powered up.

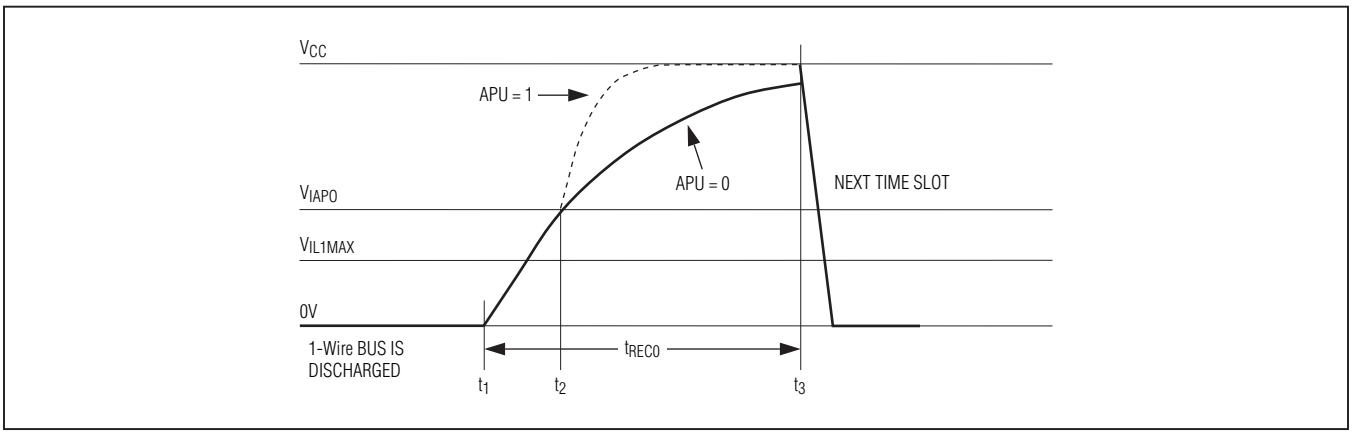


Figure 2. Rising Edge Pullup as Seen at the End of a Write-Zero Time Slot

Strong Pullup (SPU)

The SPU bit is used to activate the strong pullup function prior to a 1-Wire Write Byte or 1-Wire Single Bit command. Strong pullup is commonly used with 1-Wire EEPROM devices when copying scratchpad data to the main memory or when performing a SHA computation and with parasitically powered temperature sensors or A/D converters. The respective Maxim 1-Wire IC data sheets specify the location in the communications protocol after which the strong pullup should be applied. The SPU bit must be set immediately prior to issuing the command that puts the 1-Wire device into the state where it needs the extra power. The strong pullup uses the same internal pullup transistor as the active pullup feature. See the R_{APU} parameter in the *Electrical Characteristics* to determine whether the voltage drop is low enough to maintain the required 1-Wire voltage at a given load current and 1-Wire supply voltage.

If SPU is 1 and APU is 0, the DS2483 treats the rising edge of the time slot as if the active pullup was activated, but uses V_{IH1} as the threshold to enable the strong pullup. If SPU is 1 and APU is 1, the threshold voltage to enable the strong pullup is V_{IAPO}. Once enabled, in contrast to the active pullup, the internal pullup transistor remains conducting, as shown in Figure 3, until one of three events occurs: the DS2483 receives a command that generates 1-Wire communication (the typical case), the SPU bit in the Device Configuration register is written to 0, or the DS2483 receives the Device Reset command. When the strong pullup ends, the SPU bit is automatically reset to 0. Using the strong pullup feature does not change the state of the APU bit in the Device Configuration register.

1-Wire Speed (1WS)

The 1WS bit determines the timing of any 1-Wire communication generated by the DS2483. All 1-Wire slave devices support standard speed (1WS = 0). Many 1-Wire devices can also communicate at a higher data rate, called overdrive speed. To change from standard to overdrive speed, a 1-Wire device needs to receive an Overdrive-Skip ROM or Overdrive-Match ROM command, as explained in the Maxim 1-Wire IC data sheets. The change in speed occurs immediately after the 1-Wire device has received the speed-changing command code. The DS2483 must take part in this speed change to stay synchronized. This is accomplished by writing to the Device Configuration register with the 1WS bit as 1 immediately after the 1-Wire Byte command that changes the speed of a 1-Wire device. Writing to the Device Configuration register with the 1WS bit as 0, followed by a 1-Wire Reset command, changes the DS2483 and any 1-Wire devices on the active 1-Wire line back to standard speed.

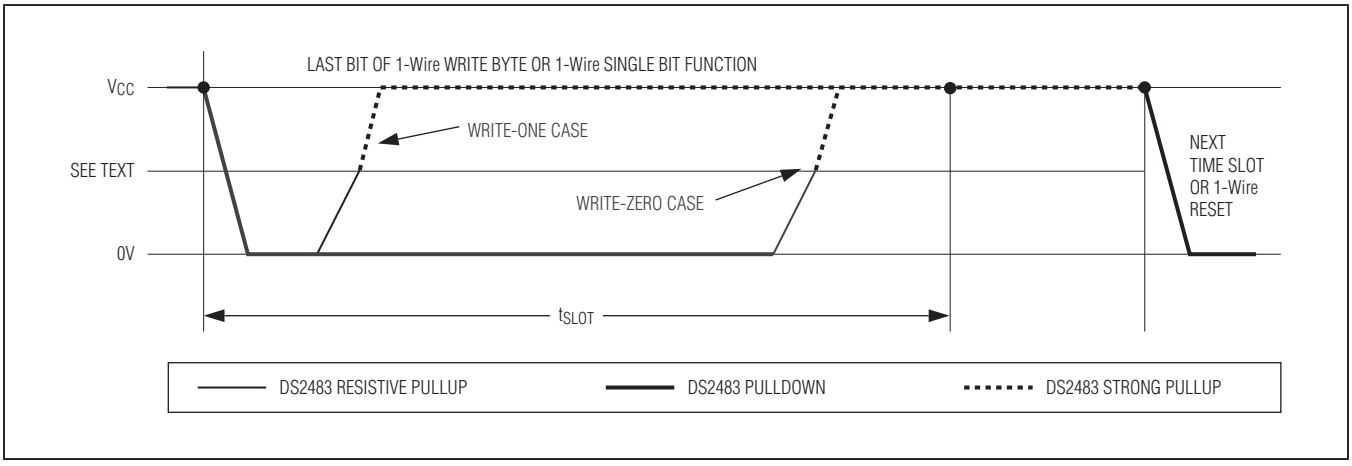


Figure 3. Low-Impedance Pullup Timing

Table 3. Status Register Bit Assignment

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DIR	TSB	SBR	RST	LL	SD	PPD	1WB

Status Register

The read-only Status register is the general means for the DS2483 to report bit-type data from the 1-Wire side, 1-Wire busy status, and its own reset status to the host processor (Table 3). All 1-Wire communication commands and the Device Reset command position the read pointer at the Status register for the host processor to read with minimal protocol overhead. Status information is updated during the execution of certain commands only. Bit details are given in the following descriptions.

1-Wire Busy (1WB)

The 1WB bit reports to the host processor whether the 1-Wire line is busy. During 1-Wire communication 1WB is 1; once the command is completed, 1WB returns to its default 0. Details on when 1WB changes state and for how long it remains at 1 are found in the *Function Commands* section.

Presence-Pulse Detect (PPD)

The PPD bit is updated with every 1-Wire Reset command. If the DS2483 detects a presence pulse from a 1-Wire device at t_{MSP} during the presence-detect cycle, the PPD bit is set to 1. This bit returns to its default 0 if there is no presence pulse or if the 1-Wire line is shorted during a subsequent 1-Wire Reset command.

Short Detected (SD)

The SD bit is updated with every 1-Wire Reset command. If the DS2483 detects a logic 0 on the 1-Wire line at t_{SI} during the presence-detect cycle, the SD bit is set to 1. This bit returns to its default 0 with a subsequent 1-Wire Reset command, provided that the short has been removed. If SD is 1, PPD is 0. The DS2483 cannot distinguish between a short and a DS1994 or DS2404 signaling a 1-Wire interrupt. For this reason, if a DS2404 or DS1994 is used in the application, the interrupt function must be disabled. The interrupt signaling is explained in the respective Maxim 1-Wire IC data sheets.

Logic Level (LL)

The LL bit reports the logic state of the active 1-Wire line without initiating any 1-Wire communication. The 1-Wire line is sampled for this purpose every time the Status register is read. The sampling and updating of the LL bit takes place when the host processor has addressed the DS2483 in read mode (during the acknowledge cycle), provided that the read pointer is positioned at the Status register.

Device Reset (RST)

If the RST bit is 1, the DS2483 has performed an internal reset cycle, either caused by a power-on reset or from executing the Device Reset command. The RST bit is cleared automatically when the DS2483 executes a Write Device Configuration command to restore the selection of the desired 1-Wire features.

Single Bit Result (SBR)

The SBR bit reports the logic state of the active 1-Wire line sampled at t_{MSR} of a 1-Wire Single Bit command or the first bit of a 1-Wire Triplet command. The power-on default of SBR is 0. If the 1-Wire Single Bit command sends a 0 bit, SBR should be 0. With a 1-Wire Triplet command, SBR could be 0 as well as 1, depending on the response of the 1-Wire devices connected. The same result applies to a 1-Wire Single Bit command that sends a 1 bit.

Triplet Second Bit (TSB)

The TSB bit reports the logic state of the active 1-Wire line sampled at t_{MSR} of the second bit of a 1-Wire Triplet command. The power-on default of TSB is 0. This bit is updated only with a 1-Wire Triplet command and has no function with other commands.

Branch Direction Taken (DIR)

Whenever a 1-Wire Triplet command is executed, this bit reports to the host processor the search direction that was chosen by the third bit of the triplet. The power-on default of DIR is 0. This bit is updated only with a 1-Wire Triplet command and has no function with other commands. For additional information, see the description of the 1-Wire Triplet command and Application Note 187: *1-Wire Search Algorithm*.

Table 4. Port Configuration Register Bit Assignment

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0	0	0	0	VAL3	VAL2	VAL1	VAL0

BITS 3:0	**VAL[3:0]**: Parameter Value Code See Table 7 for the conversion between binary code and parameter value.

Port Configuration Register

The Port Configuration register allows verifying the settings for the 1-Wire port (Table 4). The Adjust 1-Wire Port command positions the read pointer to the Port Configuration register for the host processor to read with minimal protocol overhead. When reading the Port Configuration register, the parameter values are reported in this sequence:

Parameter 000 (t_{RSTL}) standard speed, overdrive speed

Parameter 001 (t_{MSP}) standard speed, overdrive speed

Parameter 010 (t_{W0L}) standard speed, overdrive speed

Parameter 011 (t_{REC0})

Parameter 100 (R_{WPU})

If one continues reading, the parameter number rolls over to 000 and one receives the same data again.

Note that the upper 4 bits read from the port configuration register are always 0. See Table 7 for the conversion between parameter value code and actual parameter value.

Function Commands

The DS2483 understands nine function commands that fall into four categories: device control, I²C communication, 1-Wire setup, and 1-Wire communication. The feedback path to the host is controlled by a read pointer, which is set automatically by each function command for the host to efficiently access relevant information. The host processor sends these commands and applicable parameters as strings of 1 or 2 bytes using the I²C interface. The I²C protocol requires that each byte be acknowledged by the receiving party to confirm acceptance or not be acknowledged to indicate an error condition (invalid code or parameter) or to end the communication. See the *I²C Interface* section for details of the I²C protocol including acknowledge.

The function commands are as follows:

1) Device Reset
2) Set Read Pointer
3) Write Device Configuration
4) Adjust 1-Wire Port
5) 1-Wire Reset
6) 1-Wire Single Bit
7) 1-Wire Write Byte
8) 1-Wire Read Byte
9) 1-Wire Triplet

Device Reset

Command Code	F0h
Command Parameter	None
Description	Performs a global reset of device state machine logic. Terminates any ongoing 1-Wire communication.
Typical Use	Device initialization after power-up; reinitialization (reset) as desired.
Restriction	None (can be executed at any time)
Error Response	None
Command Duration	Maximum 525ns. Counted from falling SCL edge of the command code acknowledge bit.
1-Wire Activity	Ends maximum 262.5ns after the falling SCL edge of the command code acknowledge bit.
Read Pointer Position	Status register (for busy polling).
Status Bits Affected	RST set to 1; 1WB, PPD, SD, SBR, TSB, DIR set to 0.
Device Configurations Affected	1WS, APU, PDN, SPU set to 0.
Port Configurations Affected	t_{RSTL}, t_{MSP}, t_{W0L}, t_{REC0}, and R_{WPU} default values apply.

Set Read Pointer

Command Code	E1h
Command Parameter	Pointer Code (see Table 5)
Description	Sets the read pointer to the specified register. Overwrites the read pointer position of any 1-Wire communication command in progress.
Typical Use	To prepare reading the result from a 1-Wire Read Byte command; random read access of registers.
Restriction	None (can be executed at any time).
Error Response	If the pointer code is not valid, the pointer code is not acknowledged and the command is ignored.
Command Duration	None. The read pointer is updated on the rising SCL edge of the pointer code acknowledge bit.
1-Wire Activity	Not affected.
Read Pointer Position	As specified by the pointer code.
Status Bits Affected	None
Device Configurations Affected	None
Port Configurations Affected	None

Table 5. Valid Read Pointer Codes

REGISTER	CODE
Device Configuration Register	C3h
Status Register	F0h
Read Data Register	E1h
Port Configuration Register	B4h

Write Device Configuration

Command Code	D2h
Command Parameter	Configuration Byte
Description	Writes a new device configuration byte. The new settings take effect immediately. **Note:** When writing to the Device Configuration register, the new data is accepted only if the upper nibble (bits 7 to 4) is the one's complement of the lower nibble (bits 3 to 0). When read, the upper nibble is always 0h.
Typical Use	Defining the features for subsequent 1-Wire communication.
Restriction	1-Wire activity must have ended before the DS2483 can process this command.
Error Response	Command code and parameter are not acknowledged if 1WB = 1 at the time the command code is received and the command is ignored.
Command Duration	None. The Device Configuration register is updated on the rising SCL edge of the configuration-byte acknowledge bit.
1-Wire Activity	None
Read Pointer Position	Device Configuration register (to verify write).
Status Bits Affected	RST set to 0.
Device Configurations Affected	1WS, SPU, PDN, APU updated.
Port Configurations Affected	None

Adjust 1-Wire Port

Command Code	C3h
Command Parameter	Control Byte
Description	Updates the selected 1-Wire port parameter, which affects the 1-Wire timing or pullup resistor selection. See Table 6 for the control byte format. **Note: Upon a power-on reset or after a Device Reset command, the parameter default values apply.**
Typical Use	To adapt the 1-Wire port to the needs of the application. This can be necessary to accommodate the slave timing requirements, which are different at lower pullup voltage.
Restriction	1-Wire activity must have ended before this command can be processed.
Error Response	Command code and data byte are not acknowledged if 1WB = 1 at the time the command code is received and the command is ignored.
Command Duration	None. The selected port parameter is updated on the rising SCL edge of the control-byte acknowledge bit.
1-Wire Activity	None
Read Pointer Position	Port Configuration register (for verification).
Status Bits Affected	None
Device Configurations Affected	None
Port Configurations Affected	As specified by the control byte.

Table 6. Bit Allocation in the Control Byte

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
P2	P1	P0	OD	VAL3	VAL2	VAL1	VAL0

BITS 7:5	**P[2:0]:** Parameter Selection 000: selects t_{RSTL} 001: selects t_{MSP} 010: selects t_{W0L} 011: selects t_{REC0}; the OD flag does not apply (don't care) 100: selects R_{WPU}; the OD flag does not apply (don't care)
BIT 4	**OD:** Overdrive Control 0: the value provided applies to the standard speed setting 1: the value provided applies to the overdrive speed setting
BITS 3:0	**VAL[3:0]**: Parameter Value Code See Table 7 for the conversion between binary code and parameter value.

Table 7. Conversion Between Parameter Code and Typical Parameter Value

PARAMETER VALUE CODE	PARAMETER 000 t_{RSTL} (µs)		PARAMETER 001 t_{MSP} (µs)		PARAMETER 010 t_{W0L} (µs)		PARAMETER 011 t_{REC0} (µs)	PARAMETER 100 R_{WPU} (Ω)
	OD = 0	OD = 1	OD = 0	OD = 1	OD = 0	OD = 1	OD = N/A	OD = N/A
0000	440	44	58	5.5	52	5.0	2.75	500
0001	460	46	58	5.5	54	5.5	2.75	500
0010	480	48	60	6.0	56	6.0	2.75	500
0011	500	50	62	6.5	58	6.5	2.75	500
0100	520	52	64	7.0	60	7.0	2.75	500
0101	540	54	66	7.5	62	7.5	2.75	500
0110	**560**	**56**	**68**	**8.0**	**64**	**8.0**	**5.25**	**1000**
0111	580	58	70	8.5	66	8.5	7.75	1000
1000	600	60	72	9.0	68	9.0	10.25	1000
1001	620	62	74	9.5	70	9.5	12.75	1000
1010	640	64	76	10.0	70	10	15.25	1000
1011	660	66	76	10.5	70	10	17.75	1000
1100	680	68	76	11.0	70	10	20.25	1000
1101	700	70	76	11.0	70	10	22.75	1000
1110	720	72	76	11.0	70	10	25.25	1000
1111	740	74	76	11.0	70	10	25.25	1000

Note: *The power-on default values are* ***bold****.*

1-Wire Reset

Command Code	B4h
Command Parameter	None
Description	Generates a 1-Wire reset/presence-detect cycle at the 1-Wire line (Figure 4). The state of the 1-Wire line is sampled at t_{SI} and t_{MSP} and the result is reported to the host processor through the Status register bits PPD and SD.
Typical Use	To initiate or end any 1-Wire communication sequence.
Restriction	1-Wire activity must have ended before the DS2483 can process this command.
Error Response	Command code is not acknowledged if 1WB = 1 at the time the command code is received and the command is ignored.
Command Duration	2 x t_{RSTL} + maximum 262.5ns, counted from the falling SCL edge of the command code acknowledge bit.
1-Wire Activity	Begins maximum 262.5ns after the falling SCL edge of the command code acknowledge bit.
Read Pointer Position	Status register (for busy polling).
Status Bits Affected	1WB (set to 1 for 2 x t_{RSTL}), PPD is updated at t_{RSTL} + t_{MSP}, SD is updated at t_{RSTL} + t_{SI}.
Device Configurations Affected	1WS and APU apply.
Port Configurations Affected	t_{RSTL}, t_{MSP}, t_{W0L}, t_{REC0}, and R_{WPU} current values apply.

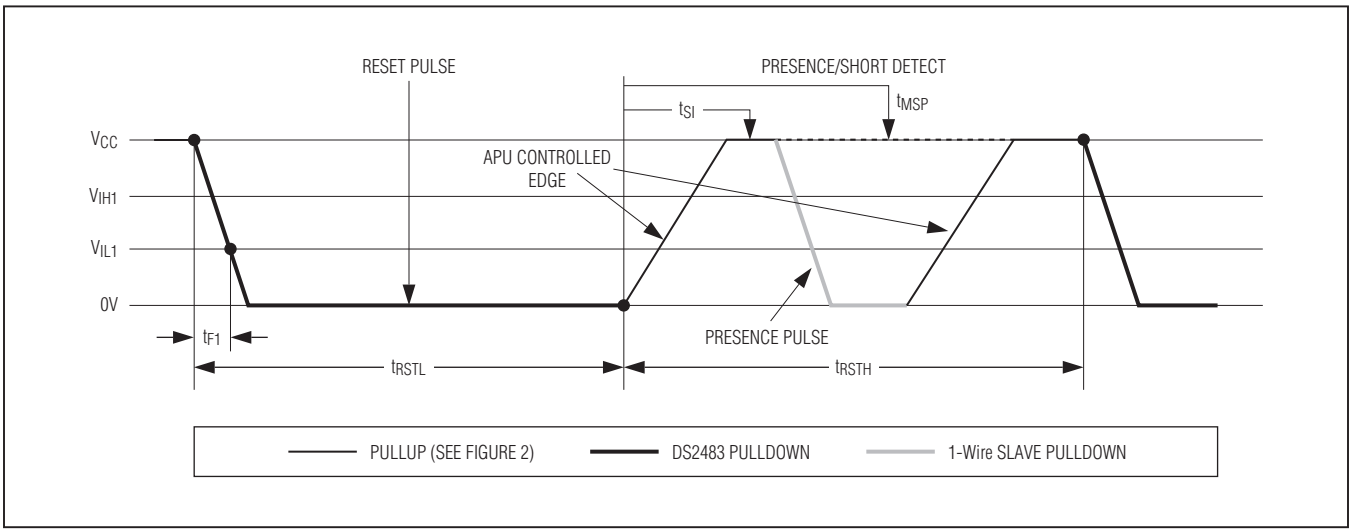


Figure 4. 1-Wire Reset/Presence-Detect Cycle

1-Wire Single Bit

Command Code	87h
Command Parameter	Bit Byte
Description	Generates a single 1-Wire time slot with a bit value “V” as specified by the bit byte at the 1-Wire line (Table 8). A V value of 0b generates a write-zero time slot (Figure 5); a V value of 1b generates a write-one time slot, which also functions as a read-data time slot (Figure 6). In either case, the logic level at the 1-Wire line is tested at t_{MSR} and SBR is updated.
Typical Use	To perform single-bit writes or reads at the 1-Wire line when single bit communication is necessary (the exception).
Restriction	1-Wire activity must have ended before the DS2483 can process this command.
Error Response	Command code and bit byte are not acknowledged if 1WB = 1 at the time the command code is received and the command is ignored.
Command Duration	t_{SLOT} + maximum 262.5ns, counted from the falling SCL edge of the first bit (MSB) of the bit byte.
1-Wire Activity	Begins maximum 262.5ns after the falling SCL edge of the MSB of the bit byte.
Read Pointer Position	Status register (for busy polling and data reading).
Status Bits Affected	1WB (set to 1 for t_{SLOT}), SBR is updated at t_{MSR}, DIR (may change its state).
Device Configurations Affected	1WS, APU, SPU apply.
Port Configurations Affected	t_{RSTL}, t_{MSP}, t_{W0L}, t_{REC0}, and R_{WPU} current values apply.

Table 8. Bit Allocation in the Bit Byte

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
V	X	X	X	X	X	X	X

X = Don’t care

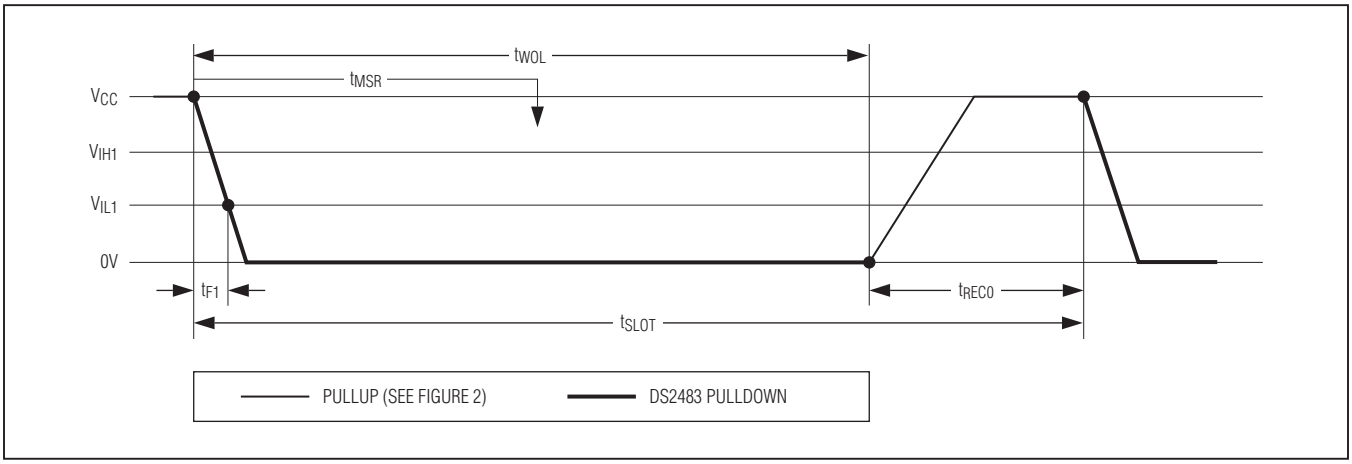
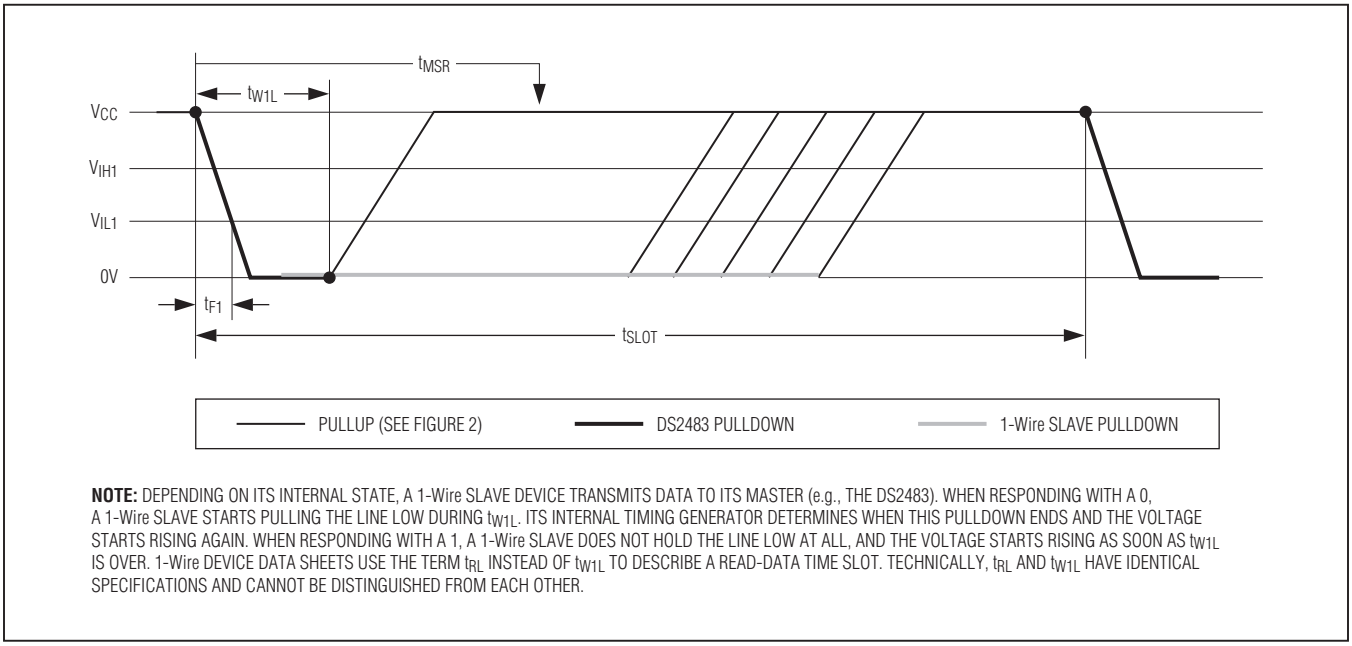


Figure 5. Write-Zero Time Slot



NOTE: DEPENDING ON ITS INTERNAL STATE, A 1-Wire SLAVE DEVICE TRANSMITS DATA TO ITS MASTER (e.g., THE DS2483). WHEN RESPONDING WITH A 0, A 1-Wire SLAVE STARTS PULLING THE LINE LOW DURING t_{W1L}. ITS INTERNAL TIMING GENERATOR DETERMINES WHEN THIS PULLDOWN ENDS AND THE VOLTAGE STARTS RISING AGAIN. WHEN RESPONDING WITH A 1, A 1-Wire SLAVE DOES NOT HOLD THE LINE LOW AT ALL, AND THE VOLTAGE STARTS RISING AS SOON AS t_{W1L} IS OVER. 1-Wire DEVICE DATA SHEETS USE THE TERM t_{RL} INSTEAD OF t_{W1L} TO DESCRIBE A READ-DATA TIME SLOT. TECHNICALLY, t_{RL} AND t_{W1L} HAVE IDENTICAL SPECIFICATIONS AND CANNOT BE DISTINGUISHED FROM EACH OTHER.

Figure 6. Write-One and Read-Data Time Slot

1-Wire Write Byte

Command Code	A5h
Command Parameter	Data Byte
Description	Writes a single data byte to the 1-Wire line.
Typical Use	To write commands or data to the 1-Wire line. Equivalent to executing eight 1-Wire Single Bit commands, but faster due to less I^2C traffic.
Restriction	1-Wire activity must have ended before the DS2483 can process this command.
Error Response	Command code and data byte are not acknowledged if 1WB = 1 at the time the command code is received and the command is ignored.
Command Duration	8 x t_{SLOT} + maximum 262.5ns, counted from falling edge of the last bit (LSB) of the data byte.
1-Wire Activity	Begins maximum 262.5ns after falling SCL edge of the LSB of the data byte (i.e., before the data-byte acknowledge). **Note:** The bit order on the I^2C bus and the 1-Wire line is different (1-Wire: LSB first; I^2C: MSB first). Therefore, 1-Wire activity cannot begin before the DS2483 has received the full data byte.
Read Pointer Position	Status register (for busy polling).
Status Bits Affected	1WB (set to 1 for 8 x t_{SLOT}).
Device Configurations Affected	1WS, SPU, APU apply.
Port Configurations Affected	t_{RSTL}, t_{MSP}, t_{W0L}, t_{REC0}, and R_{WPU} current values apply.

1-Wire Read Byte

Command Code	96h
Command Parameter	None
Description	Generates eight read-data time slots on the 1-Wire line and stores result in the Read Data register.
Typical Use	To read data from the 1-Wire line. Equivalent to executing eight 1-Wire Single Bit commands with V = 1 (write-one time slot), but faster due to less I^2C traffic.
Restriction	1-Wire activity must have ended before the DS2483 can process this command.
Error Response	Command code is not acknowledged if 1WB = 1 at the time the command code is received and the command is ignored.
Command Duration	8 x t_{SLOT} + maximum 262.5ns, counted from the falling SCL edge of the command code acknowledge bit.
1-Wire Activity	Begins maximum 262.5ns after the falling SCL edge of the command code acknowledge bit.
Read Pointer Position	Status register (for busy polling). **Note:** To read the data byte received from the 1-Wire line, issue the Set Read Pointer command and select the Read Data register. Then access the DS2483 in read mode.
Status Bits Affected	1WB (set to 1 for 8 x t_{SLOT}).
Device Configurations Affected	1WS, APU apply.
Port Configurations Affected	t_{RSTL}, t_{MSP}, t_{W0L}, t_{REC0}, and R_{WPU} current values apply.

Command Code	78h
Command Parameter	Direction Byte
Description	Generates three time slots: two read time slots and one write time slot at the 1-Wire line. The type of write time slot depends on the result of the read time slots and the direction byte. The direction byte determines the type of write time slot if both read time slots are 0 (a typical case). In this case, the DS2483 generates a write-one time slot if V = 1 and a write-zero time slot if V = 0. See Table 9. If the read time slots are 0 and 1, they are followed by a write-zero time slot. If the read time slots are 1 and 0, they are followed by a write-one time slot. If the read time slots are both 1 (error case), the subsequent write time slot is a write-one.
Typical Use	To perform a 1-Wire Search ROM sequence; a full sequence requires this command to be executed 64 times to identify and address one device.
Restriction	1-Wire activity must have ended before the DS2483 can process this command.
Error Response	Command code and direction byte is not acknowledged if 1WB = 1 at the time the command code is received and the command is ignored.
Command Duration	3 x t_{SLOT} + maximum 262.5ns, counted from the falling SCL edge of the first bit (MSB) of the direction byte.
1-Wire Activity	Begins maximum 262.5ns after the falling SCL edge of the MSB of the direction byte.
Read Pointer Position	Status Register (for busy polling).
Status Bits Affected	1WB (set to 1 for 3 x t_{SLOT}), SBR is updated at the first t_{MSR}, TSB and DIR are updated at the second t_{MSR} (i.e., at t_{SLOT} + t_{MSR}).
Device Configurations Affected	1WS, APU apply.
Port Configurations Affected	t_{RSTL}, t_{MSP}, t_{W0L}, t_{REC0}, and R_{WPU} current values apply.

Table 9. Bit Allocation in the Direction Byte

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
V	X	X	X	X	X	X	X

X = Don't care

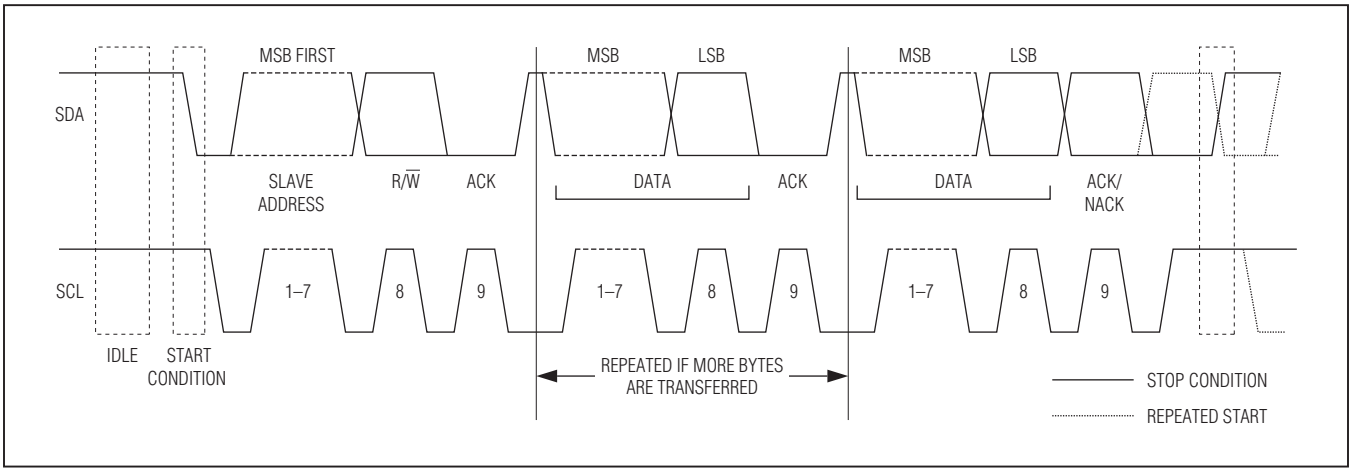


Figure 7. I²C Protocol Overview

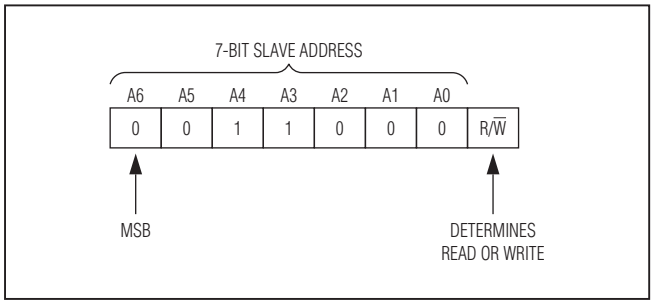


Figure 8. DS2483 Slave Address

I²C Interface

General Characteristics

The I²C bus uses a data line (SDA) and a clock signal (SCL) for communication. Both SDA and SCL are bidirectional lines connected to a positive supply voltage through a pullup resistor. When there is no communication, both lines are high. The output stages of devices connected to the bus must have an open drain or open collector to perform the wired-AND function. Data on the I²C bus can be transferred at rates of up to 100kbps in standard mode and up to 400kbps in fast mode. The DS2483 works in both modes.

A device that sends data on the bus is defined as a transmitter, and a device receiving data is defined as a receiver. The device that controls the communication is called a master. The devices that are controlled by the master are slaves. To be individually accessed, each device must have a slave address that does not conflict with other devices on the bus.

Data transfers can be initiated only when the bus is not busy. The master generates the serial clock (SCL), controls the bus access, generates the START and STOP conditions, and determines the number of data bytes transferred between START and STOP (Figure 7). Data is transferred in bytes with the most significant bit being transmitted first. After each byte follows an acknowledge bit to allow synchronization between master and slave.

Slave Address

Figure 8 shows the slave address to which the DS2483 responds. The upper 7 bits are programmed at the factory. Contact the factory for a customized version with a different address. The slave address is part of the slave address/control byte. The last bit of the slave address/control byte (R/$\overline{W}$) defines the data direction. When set to 0, subsequent data flows from master to slave (write access mode); when set to 1, data flows from slave to master (read access mode).

I²C Definitions

The following terminology is commonly used to describe I²C data transfers. See Figure 9 for a timing diagram.

Bus Idle or Not Busy: Both SDA and SCL are inactive and in their logic-high states.

START Condition: To initiate communication with a slave, the master must generate a START condition. A START condition is defined as a change in state of SDA from high to low while SCL remains high.

STOP Condition: To end communication with a slave, the master must generate a STOP condition. A STOP condition is defined as a change in state of SDA from low to high while SCL remains high.

Repeated START Condition: Repeated STARTs are commonly used for read accesses to select a specific data source or address from which to read. The master can use a repeated START condition at the end of a data transfer to immediately initiate a new data transfer following the current one. A repeated START condition is generated the same way as a normal START condition, but without leaving the bus idle after a STOP condition.

Data Valid: With the exception of the START and STOP condition, transitions of SDA can occur only during the low state of SCL. The data on SDA must remain valid and unchanged during the entire high pulse of SCL plus the required setup and hold time ($t_{HD:DAT}$ after the falling edge of SCL and $t_{SU:DAT}$ before the rising edge of SCL; see Figure 9). There is one clock pulse per bit of data. Data is shifted into the receiving device during the rising edge of SCL pulse.

When finished with writing, the master must release the SDA line for a sufficient amount of setup time (minimum $t_{SU:DAT} + t_R$ in Figure 9) before the next rising edge of SCL to start reading. The slave shifts out each data bit on SDA at the falling edge of the previous SCL pulse and the data bit is valid at the rising edge of the current SCL pulse. The master generates all SCL clock pulses, including those needed to read from a slave.

Acknowledge: Typically a receiving device, when addressed, is obliged to generate an acknowledge after the receipt of each byte. The master must generate a clock pulse that is associated with this acknowledge bit. A device that acknowledges must pull SDA low during the acknowledge clock pulse in such a way that SDA is stable low during the high period of the acknowledge-related clock pulse plus the required setup and hold time ($t_{HD:DAT}$ after the falling edge of SCL and $t_{SU:DAT}$ before the rising edge of SCL).

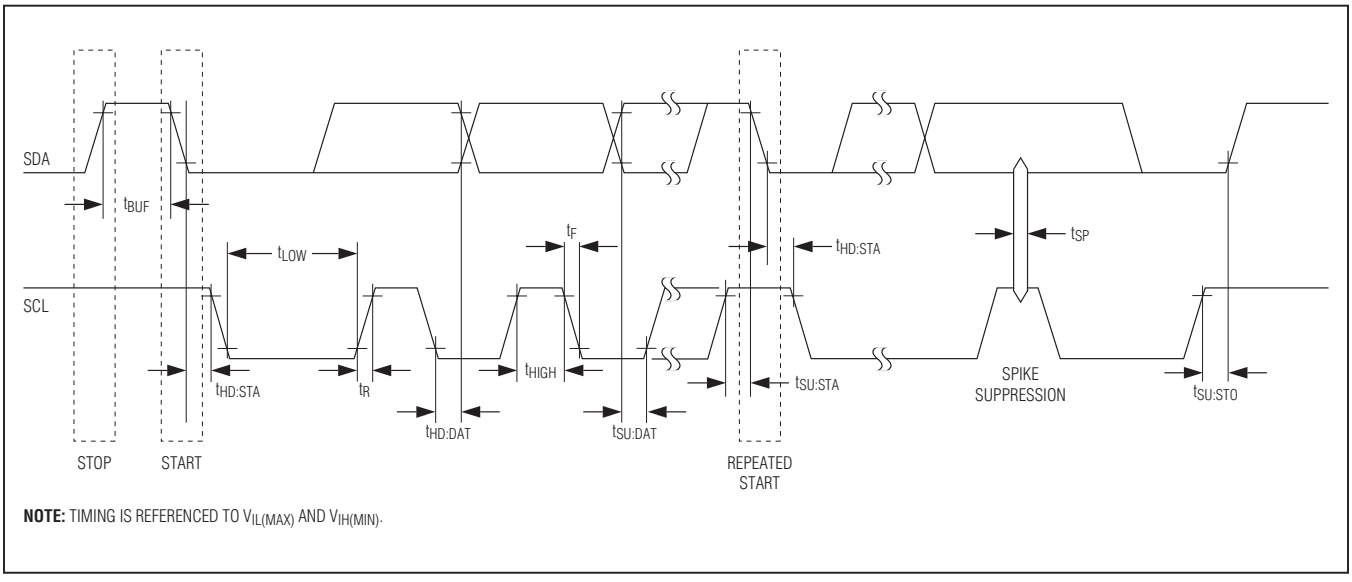


Figure 9. I²C Timing Diagram

Not Acknowledged by Slave: A slave device could be unable to receive or transmit data, e.g., because it is busy performing a real-time function or is in sleep mode. In this case, the slave device does not acknowledge its slave address and leaves the SDA line high. A slave device that is ready to communicate acknowledges at least its slave address. However, some time later the slave can refuse to accept data, e.g., because of an invalid command or parameter. In this case, the slave device does not acknowledge any of the bytes that it refuses and leaves SDA high. In either case, after a slave has failed to acknowledge, the master first should generate a repeated START condition or a STOP condition followed by a START condition to begin a new data transfer.

Not Acknowledged by Master: At some time when receiving data, the master must signal an end of data to the slave device. To achieve this, the master does not acknowledge the last byte that it has received from the slave. In response, the slave releases SDA, allowing the master to generate the STOP condition.

Writing to the DS2483

To write to the DS2483, the master must access the device in write mode, i.e., the slave address must be sent with the direction bit set to 0. The next byte to be sent is a command code, which, depending on the command, may be followed by a command parameter. The DS2483 acknowledges valid command codes and expected/valid command parameters. Additional bytes or invalid command parameters are never acknowledged.

Reading from the DS2483

To read from the DS2483, the master must access the device in read mode, i.e., the slave address must be sent with the direction bit set to 1. The read pointer determines the register that the master reads from. The master can continue reading the same register over and over again, without having to readdress the device, e.g., to watch the 1WB changing from 1 to 0. To read from a different register, the master must issue the Set Read Pointer command and then access the DS2483 again in read mode.

I²C Communication Examples

See Table 10 and Table 11 for the I²C communication legend and data direction codes.

Table 10. I²C Communication—Legend

SYMBOL	DESCRIPTION
S	START Condition
AD, 0	Select DS2483 for Write Access
AD, 1	Select DS2483 for Read Access
Sr	Repeated START Condition
P	STOP Condition
A	Acknowledged
A\	Not Acknowledged
(Idle)	Bus Not Busy
<byte>	Transfer of One Byte
DRST	Command “Device Reset” (F0h)
SRP	Command “Set Read Pointer” (E1h)
WCFG	Command “Write Device Configuration” (D2h)
ADJP	Command “Adjust 1-Wire Port” C3h)
1WRS	Command “1-Wire Reset” (B4h)
1WSB	Command “1-Wire Single Bit” (87h)
1WWB	Command “1-Wire Write Byte” (A5h)
1WRB	Command “1-Wire Read Byte” (96h)
1WT	Command “1-Wire Triplet” (78h)

Table 11. Data Direction Codes

Master-to-Slave	Slave-to-Master

I²C Communication Examples (continued)

Device Reset (After Power-Up)

S	AD,0	A	DRST	A	Sr	AD,1	A	<byte>	A\	P

Activities that are underlined denote an optional read access to verify the success of the command.

Set Read Pointer (To Read from Another Register)

Case A: Valid Read Pointer Code

S	AD,0	A	SRP	A	C3h	A	P

C3h is the read pointer code for the Device Configuration register.

Case B: Invalid Read Pointer Code

S	AD,0	A	SRP	A	E5h	A\	P

E5h is an invalid read pointer code.

Write Device Configuration (Before Starting 1-Wire Activity)

Case A: 1-Wire Idle (1WB = 0)

S	AD,0	A	WCFG	A	<byte>	A	Sr	AD,1	A	<byte>	A\	P

Activities that are underlined denote an optional read access to verify the success of the command.

Case B: 1-Wire Busy (1WB = 1)

S	AD,0	A	WCFG	A\	P

The master should stop and restart as soon as the DS2483 does not acknowledge the command code.

Adjust 1-Wire Port (after power-up, e.g., to select a 1-Wire timing other than the default)

Case A: 1-Wire Idle (1WB = 0)

S	AD,0	A	ADJP	A	<byte>	A	<byte>	A	P

Repeat to set additional port parameters

The control byte is always acknowledged, regardless of its value. See the Adjust 1-Wire Port command description for the format of the control byte.

Case B: 1-Wire Busy (1WB = 1)

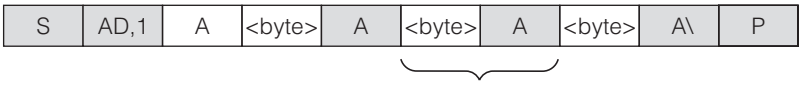
S	AD,0	A	ADJP	A\	P

The master should stop and restart as soon as the DS2483 does not acknowledge the command code.

Verifying the 1-Wire port configuration

The Adjust 1-Wire Port command sets the read pointer to the Port Configuration register. If other commands were issued to the DS2483 since then, use the Set Read Pointer command first to position the read pointer to the Port Configuration register.

Condition: 1-Wire Idle (1WB = 0), Read Pointer at Port Configuration Register



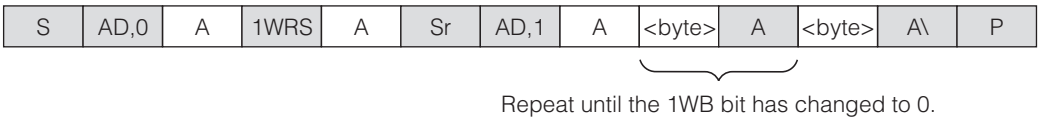
1-Wire Reset (To Begin or End 1-Wire Communication)

Case A: 1-Wire Idle (1WB = 0), No Busy Polling to Read the Result

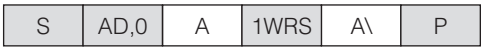


In the first cycle, the master sends the command. Then the master waits (Idle) for the 1-Wire reset to complete. In the second cycle, the DS2483 is accessed to read the result of the 1-Wire reset from the Status register.

Case B: 1-Wire Idle (1WB = 0), Busy Polling Until the 1-Wire Command is Completed, then Read the Result



Case C: 1-Wire Busy (1WB = 1)

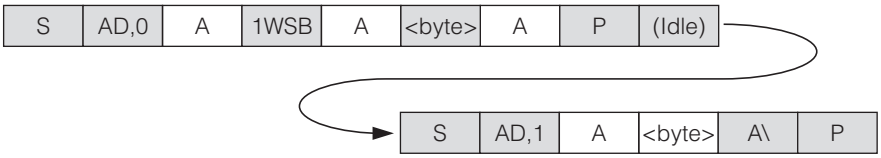


The master should stop and restart as soon as the DS2483 does not acknowledge the command code.

I²C Communication Examples (continued)

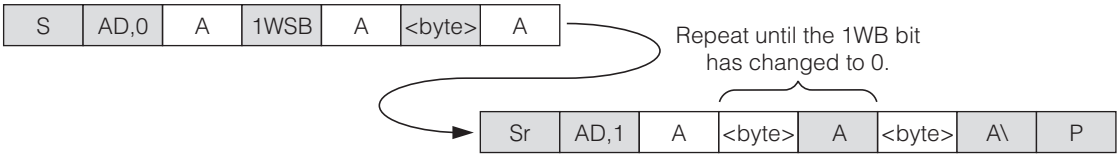
1-Wire Single Bit (To Generate a Single Time Slot on the 1-Wire Line)

Case A: 1-Wire Idle (1WB = 0), No Busy Polling



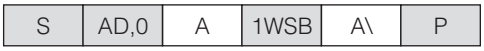
The idle time is needed for the 1-Wire function to complete. Then access the device in read mode to get the result from the 1-Wire Single Bit command.

Case B: 1-Wire Idle (1WB = 0), Busy Polling Until the 1-Wire Command is Completed



When 1WB has changed from 1 to 0, the Status register holds the valid result of the 1-Wire Single Bit command.

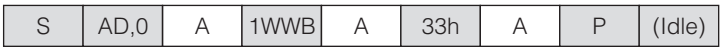
Case C: 1-Wire Busy (1WB = 1)



The master should stop and restart as soon as the DS2483 does not acknowledge the command code.

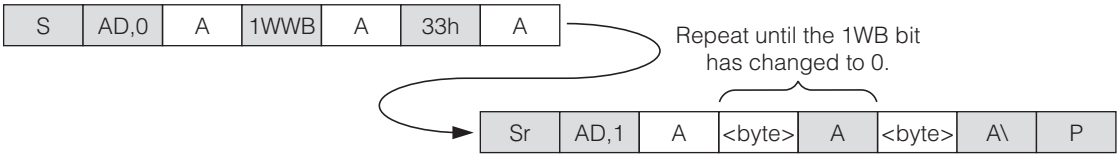
1-Wire Write Byte (To Send a Command Code or Data Byte to the 1-Wire Line)

Case A: 1-Wire Idle (1WB = 0), No Busy Polling



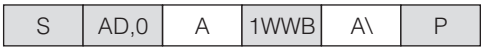
33h is the valid 1-Wire ROM function command for Read ROM. The idle time is needed for the 1-Wire function to complete. There is no data read back from the 1-Wire line with this command.

Case B: 1-Wire Idle (1WB = 0), Busy Polling Until the 1-Wire Command is Completed.



When 1WB has changed from 1 to 0, the 1-Wire Write Byte command is completed.

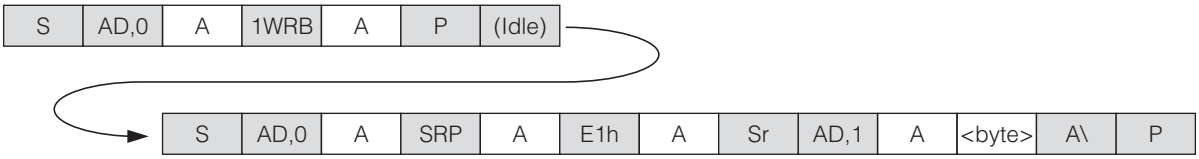
Case C: 1-Wire Busy (1WB = 1)



The master should stop and restart as soon as the DS2483 does not acknowledge the command code.

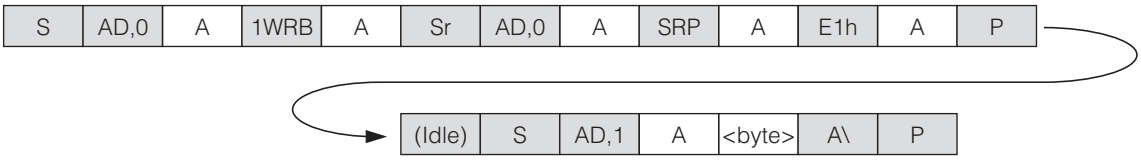
1-Wire Read Byte (To Read a Byte from the 1-Wire Line)

Case A: 1-Wire Idle (1WB = 0), No Busy Polling, Set Read Pointer **After** Idle Time



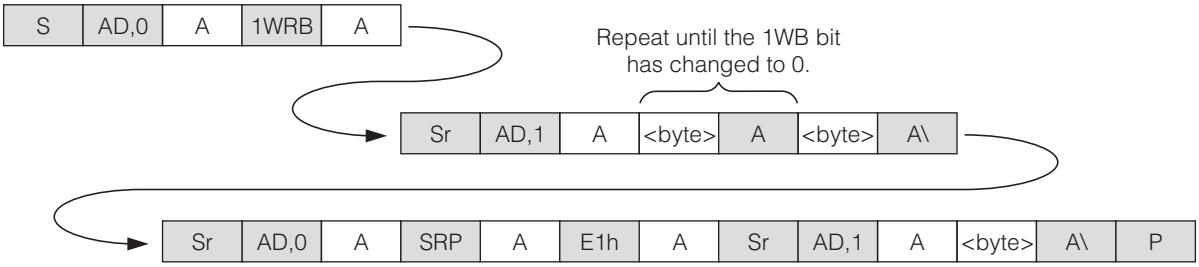
The idle time is needed for the 1-Wire function to complete. Then set the read pointer to the Read Data register (code E1h) and access the device again to read the data byte that was obtained from the 1-Wire line.

Case B: 1-Wire Idle (1WB = 0), No Busy Polling, Set Read Pointer **Before** Idle Time



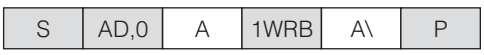
The read pointer is set to the Read Data register (code E1h) while the 1-Wire Read Byte command is still in progress. Then, after the 1-Wire function is completed, the device is accessed to read the data byte that was obtained from the 1-Wire line.

Case C: 1-Wire Idle (1WB = 0), Busy Polling Until the 1-Wire Command is Completed



Poll the Status segister until the 1WB bit has changed from 1 to 0. Then set the read pointer to the Read Data register (code E1h) and access the device again to read the data byte that was obtained from the 1-Wire line.

Case D: 1-Wire Busy (1WB = 1)

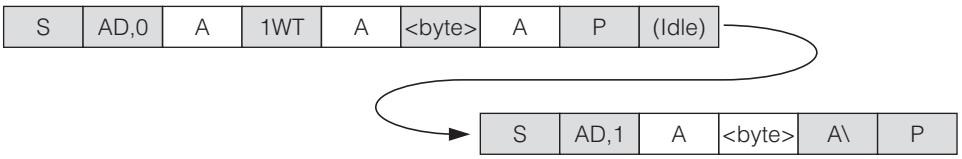


The master should stop and restart as soon as the DS2483 does not acknowledge the command code.

I²C Communication Examples (continued)

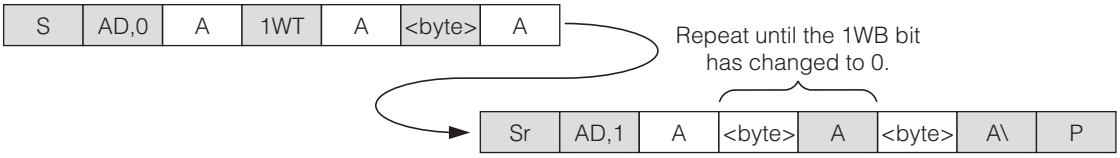
1-Wire Triplet (To Perform a Search ROM Function on 1-Wire Line)

Case A: 1-Wire Idle (1WB = 0), No Busy Polling



The idle time is needed for the 1-Wire function to complete. Then access the device in read mode to get the result from the 1-Wire Triplet command.

Case B: 1-Wire Idle (1WB = 0), Busy Polling Until the 1-Wire Command is Completed



When 1WB has changed from 1 to 0, the Status register holds the valid result of the 1-Wire Triplet command.

Case C: 1-Wire Busy (1WB = 1)



The master should stop and restart as soon as the DS2483 does not acknowledge the command code.

Applications Information

SDA and SCL Pullup Resistors

SDA is an open-drain output on the DS2483 that requires a pullup resistor to realize high-logic levels. Because the DS2483 uses SCL only as input (no clock stretching), the master can drive SCL either through an open-drain/collector output with a pullup resistor or a push-pull output.

Pullup Resistor R_P Sizing

According to the I²C specification, a slave device must be able to sink at least 3mA at a V_{OL} of 0.4V. This DC condition determines the minimum value of the pullup resistor: $\mathbf{R_{P(MIN)} = (V_{CI2C} - 0.4V)/3mA}$. With an I²C pullup voltage V_{CI2C} of 5.5V, the minimum value for the pullup resistor is 1.7kΩ. The "Minimum R_P" line in Figure 10 shows how the minimum pullup resistor changes with the operating (pullup) voltage.

For I²C systems, the rise time and fall time are measured from 30% to 70% of the pullup voltage. The maximum bus capacitance, C_B, is 400pF. The maximum rise time must not exceed 300ns. Assuming maximum rise time, the maximum resistor value at any given capacitance C_B is calculated as: $\mathbf{R_{P(MAX)} = 300ns/(C_B \times \ln(7/3))}$. For a bus capacitance of 400pF, the maximum pullup resistor would be 885Ω.

Because an 885Ω pullup resistor, as would be required to meet the rise time specification at 400pF bus capacitance, is lower than $R_{P(MIN)}$ at 5.5V, a different approach is necessary. The "Maximum Load at Minimum R_P Fast Mode" line in Figure 10 is generated by first calculating the minimum pullup resistor at any given operating voltage ("Minimum R_P" line) and then calculating the respective bus capacitance that yields a 300ns rise time.

Only for pullup voltages of 3V and lower can the maximum permissible 400pF bus capacitance be maintained. A reduced 300pF bus capacitance is acceptable for 4V and lower pullup voltages. For fast mode operation at any pullup voltage, the bus capacitance must not exceed 200pF. The corresponding pullup resistor value at the voltage is indicated by the "Minimum R_P" line.

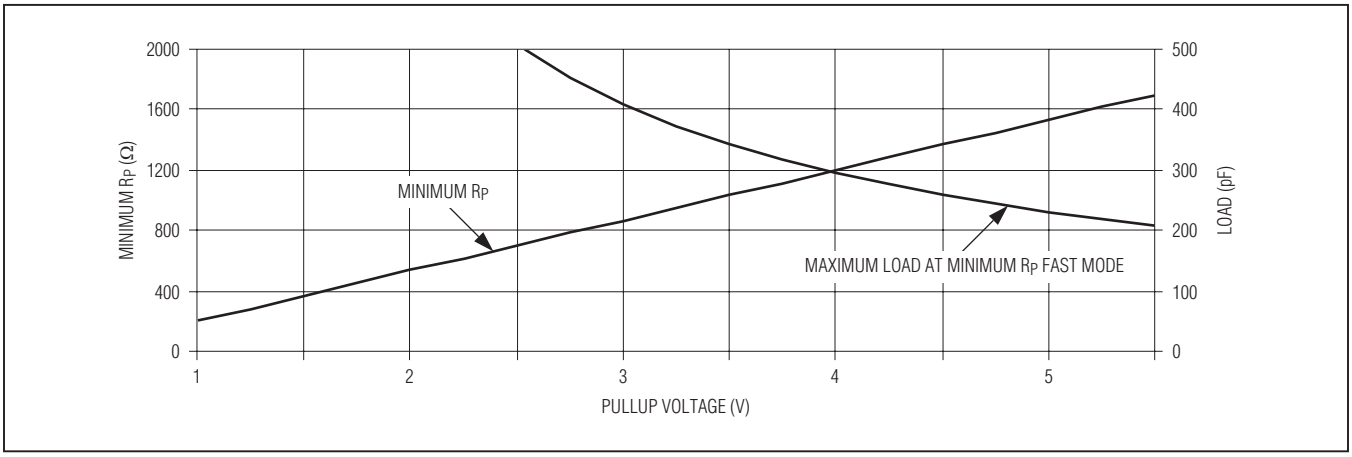


Figure 10. I²C Fast Mode Pullup Resistor Selection Chart

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS2483R+T	-40°C to +85°C	6 SOT23 (3k pieces)
DS2483Q+T	-40°C to +85°C	8 TDFN-EP* (2.5k pieces)

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.
**EP = Exposed pad.*

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
6 SOT23	U6SN+1	21-0058	90-0175
8 TDFN-EP	T823+1	21-0174	90-0091

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/11	Initial release	—

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time. The parametric values (min and max limits) shown in the Electrical Characteristics table are guaranteed. Other parametric values quoted in this data sheet are provided for guidance.

© 2011 Maxim Integrated Products Maxim is a registered trademark of Maxim Integrated Products, Inc.