Data Sheet | September 18, 2007 | FN6556.0

MP3/USB 2.0 High Speed Switch with Negative Signal Handling

The Intersil ISL54212 dual SPDT (Single Pole/Double Throw) switches combine low distortion audio and accurate USB 2.0 high speed data (480Mbps) signal switching in the same low voltage device. When operated with a 2.5V to 5.5V single supply these analog switches allow audio signal swings below-ground, allowing the use of a common USB and audio headphone connector in Personal Media Players and other portable battery powered devices.

The ISL54212 logic control pins are 1.8V compatible which allows for control via a standard µcontroller. The part has an audio enable control pin to open all the switches and put the part in a low power state.

The ISL54212 is available in a small 10 Ld 2.1mmx1.6mm ultra-thin µTQFN package and a 10 Ld 3mmx3mm TDFN package. It operates over a temperature range of -40 to +85°C.

Related Literature

- Technical Brief TB363 “Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)”
- Application Note AN557 “Recommended Test Procedures for Analog Switches”

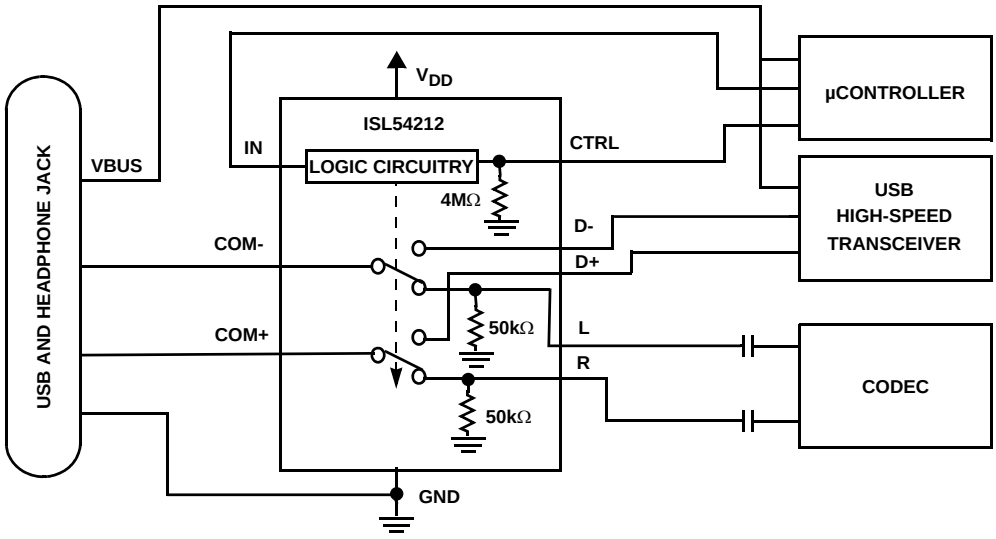
Features

- High Speed (480Mbps) and Full Speed (12Mbps) Signaling Capability per USB 2.0
- Low Distortion Negative Signal Capability
- Control Pin to Open all Switches and Enter Low Power State
- Low Distortion Headphone Audio Signals
  - THD+N at 15mW into 32Ω Load . . . . . <0.06%
- Cross-talk Audio Channels (20Hz to 20kHz) . . . . . -110dB
- Single Supply Operation (V_{DD}) . . . . . 2.5V to 5.5V
- -3dB Bandwidth USB Switches 630MHz
- Available in µTQFN and TDFN Packages
- Pb-Free (RoHS Compliant)
- Compliant with USB 2.0 Short Circuit Requirements Without Additional External Components

Applications

- MP3 and Other Personal Media Players
- Cellular/Mobile Phones
- PDA’s
- Audio/USB Switching

Application Block Diagram

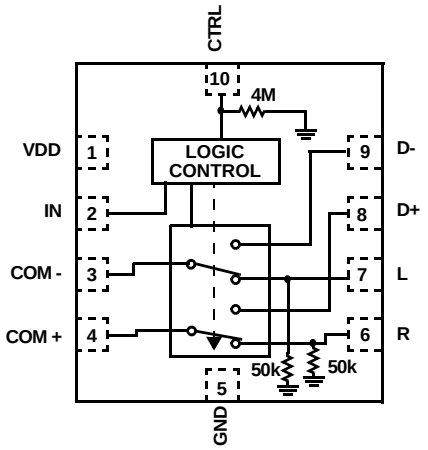


CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
1-888-INTERSIL or 1-888-468-3774 | Intersil (and design) is a registered trademark of Intersil Americas Inc.
Copyright Intersil Americas Inc. 2007. All Rights Reserved
All other trademarks mentioned are the property of their respective owners.

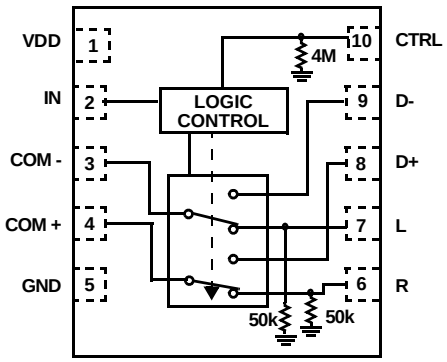
‘

Pinouts (Note 1)

ISL54212
(10 LD µTQFN)
TOP VIEW



ISL54212
(10 LD TDFN)
TOP VIEW



NOTE:

1. ISL54212 Switches shown for IN = Logic “1” and CTRL = Logic “1”.

Truth Table

ISL54212			
IN	**CTRL**	**L, R**	**D+, D-**
0	X	OFF	ON
1	0	OFF	OFF
1	1	ON	OFF

IN: Logic “0” when ≤0.5V, Logic “1” when ≥1.4V with 2.7V to 3.6V supply.
CTRL: Logic “0” when ≤0.5V or Floating, Logic “1” when ≥1.4V with 2.7V to 3.6V supply.

Pin Descriptions

ISL54212		
PIN NO.	**NAME**	**FUNCTION**
1	VDD	Power Supply
2	IN	Digital Control Input
3	COM-	Voice and Data Common Pin
4	COM+	Voice and Data Common Pin
5	GND	Ground Connection
6	R	Audio Right Input
7	L	Audio Left Input
8	D+	USB Differential Input
9	D-	USB Differential Input
10	CTRL	Digital Control Input (Audio Enable)

Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL54212IRTZ	12Z	-40 to +85	10 Ld 3mmx3mm TDFN	L10.3x3A
ISL54212IRTZ-T*	12Z	-40 to +85	10 Ld 3mmx3mm TDFN Tape and Reel	L10.3x3A
ISL54212IRUZ-T*	FX	-40 to +85	10 Ld µTQFN	L10.2.1X1.6A

*Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Absolute Maximum Ratings

VDD to GND . . . . . -0.3V to 6.0V
Input Voltages
D+, D-, L, R (Note 2) . . . . . - 2V to ((V_{DD}) + 0.3V)
IN (Note 2) . . . . . -2V to 5.5V
CTRL (Note 2) . . . . . -0.3 to ((V_{DD}) + 0.3V)
Output Voltages
COM-, COM+ (Note 2) . . . . . -2V to ((V_{DD}) + 0.3V)
Continuous Current (Audio Switches) . . . . . ±150mA
Peak Current (Audio Switches)
(Pulsed 1ms, 10% Duty Cycle, Max) . . . . . ±300mA
Continuous Current (USB Switches) . . . . . ±40mA
Peak Current (USB Switches)
(Pulsed 1ms, 10% Duty Cycle, Max) . . . . . ±100mA
ESD Rating:
HBM . . . . . >7kV
MM . . . . . >400V
CDM . . . . . >1.4kV

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} (°C/W)
10 Ld μTQFN Package	130
10 Ld 3x3 TDFN Package	110

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-free reflow profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Temperature Range . . . . . -40°C to +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

2. Signals on D+, D-, L, R, COM-, COM+, CTRL, IN exceeding V_{DD} or GND by specified amount are clamped. Limit current to maximum current ratings.
3. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications - 2.7V to 3.6V Supply

Test Conditions: V_{DD} = +3.3V, GND = 0V, V_{INH} = 1.4V, V_{INL} = 0.5V, V_{CTRLH} = 1.4V, V_{CTRLL} = 0.5V, (Note 4), unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 5, 8)	TYP	MAX (Notes 5, 8)	UNITS
ANALOG SWITCH CHARACTERISTICS						
Audio Switches (L, R)						
Analog Signal Range, V_{ANALOG}	V_{DD} = 3.0V, IN = 1.4V, CTRL = 1.4V	Full	-1.5	-	1.5	V
ON Resistance, R_{ON}	V_{DD} = 5.0V, IN = CTRL = V_{DD}, I_{COMx} = 40mA, V_L or V_R = -0.85V to 0.85V, (See Figure 3)	25	-	2.47	-	Ω
ON Resistance, R_{ON}	V_{DD} = 4.2V, IN = CTRL = V_{DD}, I_{COMx} = 40mA, V_L or V_R = -0.85V to 0.85V, (See Figure 3)	25	-	2.50	-	Ω
ON Resistance, R_{ON}	V_{DD} = 2.85V, IN = CTRL = V_{DD}, I_{COMx} = 40mA, V_L or V_R = -0.85V to 0.85V, (See Figure 3)	25	-	2.87	-	Ω
ON Resistance, R_{ON}	V_{DD} = 3.0V, IN = 1.4V, CTRL = 1.4V, I_{COMx} = 40mA, V_L or V_R = -0.85V to 0.85V, (See Figure 3)	25	-	2.65	4.0	Ω
		Full	-	-	5.5	Ω
R_{ON} Matching Between Channels, ΔR_{ON}	V_{DD} = 3.0V, IN = 1.4V, CTRL = 1.4V, I_{COMx} = 40mA, V_L or V_R = Voltage at max R_{ON} over signal range of -0.85V to 0.85V, (Note 7)	25	-	0.02	0.33	Ω
		Full	-	-	0.39	Ω
R_{ON} Flatness, $R_{FLAT(ON)}$	V_{DD} = 3.0V, IN = 1.4V, CTRL = 1.4V, I_{COMx} = 40mA, V_L or V_R = -0.85V to 0.85V, (Note 6)	25	-	0.04	0.07	Ω
		Full	-	-	0.09	Ω
Discharge Pull-Down Resistance, R_L, R_R	V_{DD} = 3.6V, IN = CTRL = 3.6V, V_{COM-} or V_{COM+} = -0.85V, 0.85V, V_L or V_R = -0.85V, 0.85V, V_{D+} and V_{D-} = floating, Measure current through the discharge pull-down resistor and calculate resistance value.	25	-	50	-	kΩ
USB Switches (D+, D-)						
Analog Signal Range, V_{ANALOG}	V_{DD} = 3.6V, IN = 0.5V, CTRL = 1.4V	Full	0	-	V_{DD}	V
ON Resistance, R_{ON}	V_{DD} = 5.0V, IN = 0V, CTRL = V_{DD}, I_{COMx} = 1mA, V_{D+} or V_{D-} = 5V (See Figure 4)	+25	-	17.7	-	Ω
ON Resistance, R_{ON}	V_{DD} = 4.2V, IN = 0V, CTRL = V_{DD}, I_{COMx} = 1mA, V_{D+} or V_{D-} = 4.2V (See Figure 4)	+25	-	19.5	-	Ω

Electrical Specifications - 2.7V to 3.6V Supply Test Conditions: V_{DD} = +3.3V, GND = 0V, V_{INH} = 1.4V, V_{INL} = 0.5V, V_{CTRLH} = 1.4V, V_{CTRLL} = 0.5V, (Note 4), unless otherwise specified. **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 5, 8)	TYP	MAX (Notes 5, 8)	UNITS
ON Resistance, R_{ON}	V_{DD} = 2.85V, IN = 0V, CTRL = V_{DD}, I_{COMx} = 1mA, V_{D+} or V_{D-} = 2.85V (See Figure 4)	+25	-	26	-	Ω
ON Resistance, R_{ON}	V_{DD} = 3.3V, IN = 0.5V, CTRL = 1.4V, I_{COMx} = 1mA, V_{D+} or V_{D-} = 3.3V (See Figure 4)	+25	-	23.5	38	Ω
		Full	-	-	43	Ω
ON Resistance, R_{ON}	V_{DD} = 3.6V, IN = 0.5V, CTRL = 1.4V, I_{COMx} = 40mA, V_{D+} or V_{D-} = 0V to 400mV (See Figure 4)	25	-	4.6	5	Ω
		Full	-	-	6.5	Ω
R_{ON} Matching Between Channels, ΔR_{ON}	V_{DD} = 3.6V, IN = 0.5V, CTRL = 1.4V, I_{COMx} = 40mA, V_{D+} or V_{D-} = Voltage at max R_{ON}over signal range of 0V to 400mV, (Note 7)	25	-	0.06	0.5	Ω
		Full	-	-	0.55	Ω
R_{ON} Flatness, $R_{FLAT(ON)}$	V_{DD} = 3.6V, IN = 0.5V, CTRL = 1.4V, I_{COMx} = 40mA, V_{D+} or V_{D-} = 0V to 400mV, (Note 6)	25	-	0.4	0.6	Ω
		Full	-	-	1.0	Ω
OFF Leakage Current, $I_{D+(OFF)}$ or $I_{D-(OFF)}$	V_{DD} = 3.6V, IN = CTRL = 3.6V, V_{COM-} or V_{COM+} = 0.5V, 0V, V_{D+} or V_{D-} = 0V, 0.5V, V_L and V_R = float	25	-10	-	10	nA
		Full	-70	-	70	nA
ON Leakage Current, I_{Dx}	V_{DD} = 3.3V, IN = 0.5V, CTRL = 0V or 3.3V, V_{D+} or V_{D-} = 2.0V, V_{COM-} ,V_{COM+} , V_L and V_R = float	25	-10	2	10	nA
		Full	-75	-	75	nA
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	V_{DD} = 2.7V, R_L = 50Ω, C_L = 10pF, (See Figure 1)	25	-	67	-	ns
Turn-OFF Time, t_{OFF}	V_{DD} = 2.7V, R_L = 50Ω, C_L = 10pF, (See Figure 1)	25	-	48	-	ns
Break-Before-Make Time Delay, t_D	V_{DD} = 2.7V, R_L = 50Ω, C_L = 10pF, (See Figure 2)	25	-	18	-	ns
Skew, t_{SKEW}	V_{DD} = 3.3V, IN = 0V, CTRL = 3.3V, R_L = 45Ω, C_L = 10pF, t_R = t_F = 750ps at 480Mbps, (Duty Cycle = 50%) (See Figure 7)	25	-	50	-	ps
Total Jitter, t_J	V_{DD} = 3.3V, IN = 0V, CTRL = 3.3V, R_L = 45Ω, C_L = 10pF, t_R = t_F = 750ps at 480Mbps	25	-	210	-	ps
Propagation Delay, t_{PD}	V_{DD} = 3.3V, IN = 0V, CTRL = 3.3V, R_L = 45Ω, C_L = 10pF, (See Figure 7)	25	-	250	-	ps
Crosstalk (Channel-to-Channel), R to COM-, L to COM+	V_{DD} = 3.3V, IN = CTRL = 3.3V, R_L = 32Ω, f = 20Hz to 20kHz, V_R or V_L = 0.707V_{RMS} ($2V_{P-P}$), (See Figure 6)	25	-	-110	-	dB
Total Harmonic Distortion	f = 20Hz to 20kHz, V_{DD} = 3.0V, IN = CTRL = 3.0V, V_L or V_R = 0.707V_{RMS} ($2V_{P-P}$), R_L = 32Ω	25	-	0.06	-	%
USB Switch -3dB Bandwidth	Signal = 0dBm, 0.2V_{DC} offset, R_L = 50Ω, C_L = 5pF	25	-	630	-	MHz
D+/D- OFF Capacitance, $C_{D+(OFF)}$, $C_{D-(OFF)}$	f = 1MHz, V_{DD} = 3.3V, IN = CTRL = 3.3V, V_{D-} or V_{D+} = V_{COMx} = 0V, (See Figure 5)	25	-	6	-	pF
L/R OFF Capacitance, C_{LOFF}, C_{ROFF}	f = 1MHz, V_{DD} = 3.3V, IN = 0V, CTRL = 3.3V, V_L or V_R = V_{COMx} = 0V, (See Figure 5)	25	-	9	-	pF
COM ON Capacitance, $C_{COM-(ON)}$, $C_{COM+(ON)}$	f = 1MHz, V_{DD} = 3.3V, IN = 0V, CTRL = 3.3V, V_{D-} or V_{D+} = V_{COMx} = 0V, (See Figure 5)	25	-	10	-	pF
POWER SUPPLY CHARACTERISTICS						
Power Supply Range, V_{DD}		Full	2.5	-	5.5	V
Positive Supply Current, I_{DD}	V_{DD} = 3.6V, IN = 0V or 3.6V, CTRL = 3.6V	25	-	6	8	µA
		Full	-	-	10	µA
Positive Supply Current, I_{DD}	V_{DD} = 4.2V, IN = 0V or 4.2V, CTRL = 4.2V	25	-	6	-	µA
Positive Supply Current, I_{DD}	V_{DD} = 5.0V, IN = 0V or 5.0V, CTRL = 5.0V	25	-	8	-	µA
Positive Supply Current, I_{DD} (Low Power State)	V_{DD} = 3.6V, IN = 3.6V, CTRL = 0V or float	25	-	1	7	nA
		Full	-	-	140	nA

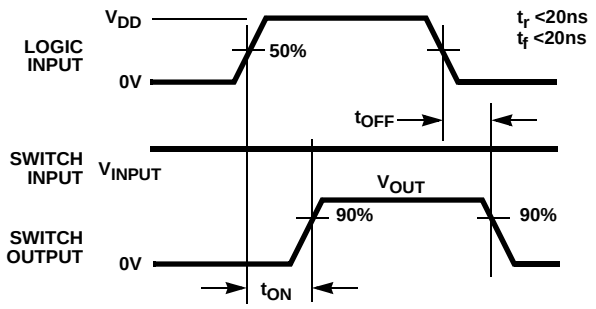
Electrical Specifications - 2.7V to 3.6V Supply Test Conditions: V_{DD} = +3.3V, GND = 0V, V_{INH} = 1.4V, V_{INL} = 0.5V, V_{CTRLH} = 1.4V, V_{CTRLL} = 0.5V, (Note 4), unless otherwise specified. **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Notes 5, 8)	TYP	MAX (Notes 5, 8)	UNITS
DIGITAL INPUT CHARACTERISTICS						
Voltage Low, V_{INL} , V_{CTRLL}	V_{DD} = 2.7V to 3.6V	Full	-	-	0.5	V
Voltage High, V_{INH}, V_{CTRLH}	V_{DD} = 2.7V to 3.6V	Full	1.4	-	-	V
Input Current, I_{INL}, I_{INH}	V_{DD} = 3.6V, IN = 0V or 3.6V, CTRL = 0V	25	-10	2.5	10	nA
		Full	-50	-	50	nA
Input Current, I_{CTRLL}	V_{DD} = 3.6V, IN = 0V, CTRL = 0V	25	-15	10	15	nA
		Full	-50	-	50	nA
Input Current, I_{CTRLH}	V_{DD} = 3.6V, IN = 0V, CTRL = 3.6V	25	-1.1	1.0	1.1	µA
		Full	-2	-	2	µA
CTRL Pull-Down Resistor, R_{CTRL}	V_{DD} = 3.6V, IN = 0V, CTRL = 3.6V	25	-	4	-	MΩ

NOTES:

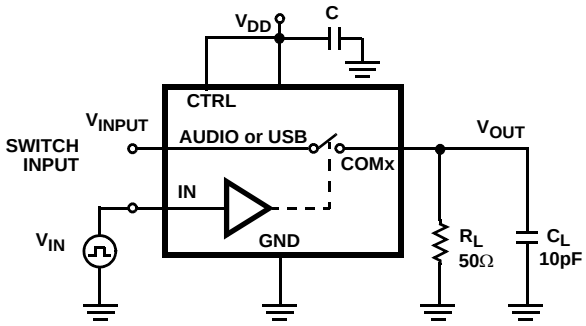
4. V_{LOGIC} = Input voltage to perform proper function.
5. The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
6. Flatness is defined as the difference between maximum and minimum value of on-resistance over the specified analog signal range.
7. R_{ON} matching between channels is calculated by subtracting the channel with the highest max R_{ON} value from the channel with lowest max R_{ON} value, between L and R or between D+ and D-.
8. Parts are 100% tested at +25°C. Over temperature limits established by characterization and are not production tested.

Test Circuits and Waveforms



Logic input waveform is inverted for switches that have the opposite logic sense.

FIGURE 1A. MEASUREMENT POINTS



Repeat test for all switches. C_L includes fixture and stray capacitance.

$$V_{OUT} = V_{(INPUT)} \frac{R_L}{R_L + R_{(ON)}}$$

FIGURE 1B. TEST CIRCUIT

FIGURE 1. SWITCHING TIMES

Test Circuits and Waveforms (Continued)

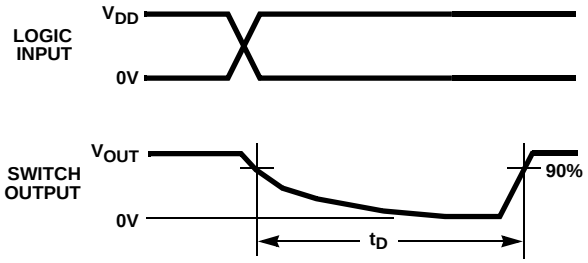
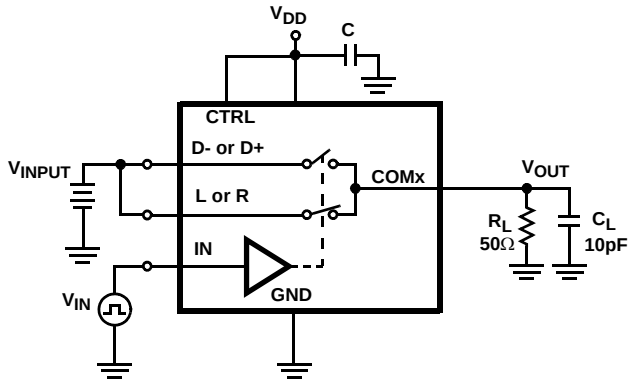


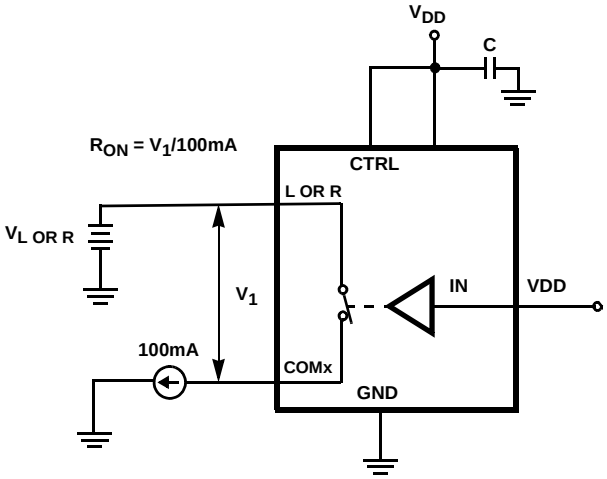
FIGURE 2A. MEASUREMENT POINTS



Repeat test for all switches. C_L includes fixture and stray capacitance.

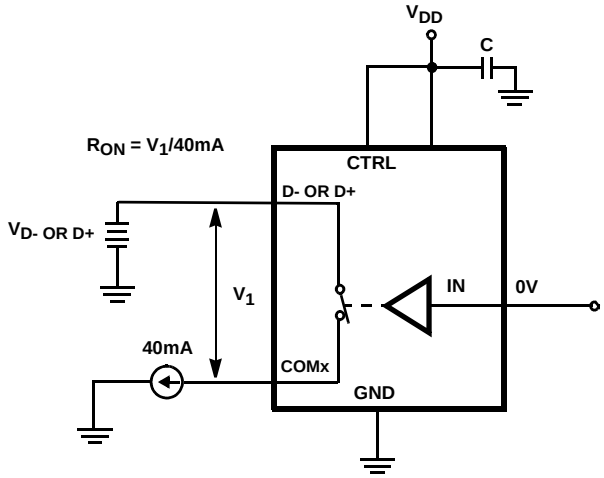
FIGURE 2B. TEST CIRCUIT

FIGURE 2. BREAK-BEFORE-MAKE TIME



Repeat test for all switches.

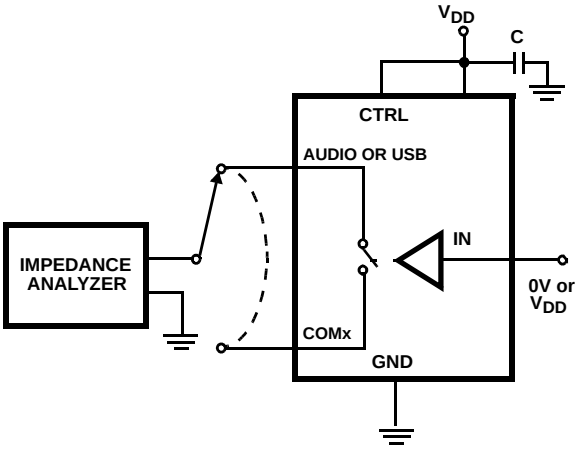
FIGURE 3. AUDIO R_{ON} TEST CIRCUIT



Repeat test for all switches.

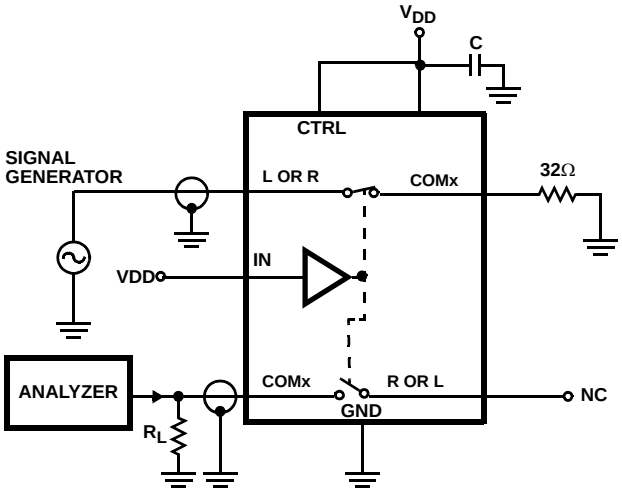
FIGURE 4. USB R_{ON} TEST CIRCUIT

Test Circuits and Waveforms (Continued)



Repeat test for all switches.

FIGURE 5. CAPACITANCE TEST CIRCUIT



Signal direction through switch is reversed, worst case values are recorded. Repeat test for all switches.

FIGURE 6. AUDIO CROSSTALK TEST CIRCUIT

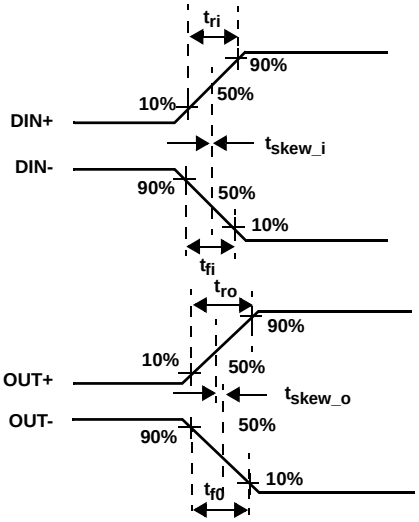
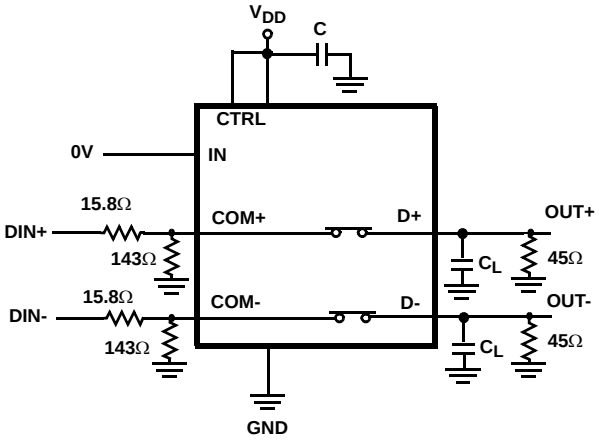


FIGURE 7A. MEASUREMENT POINTS

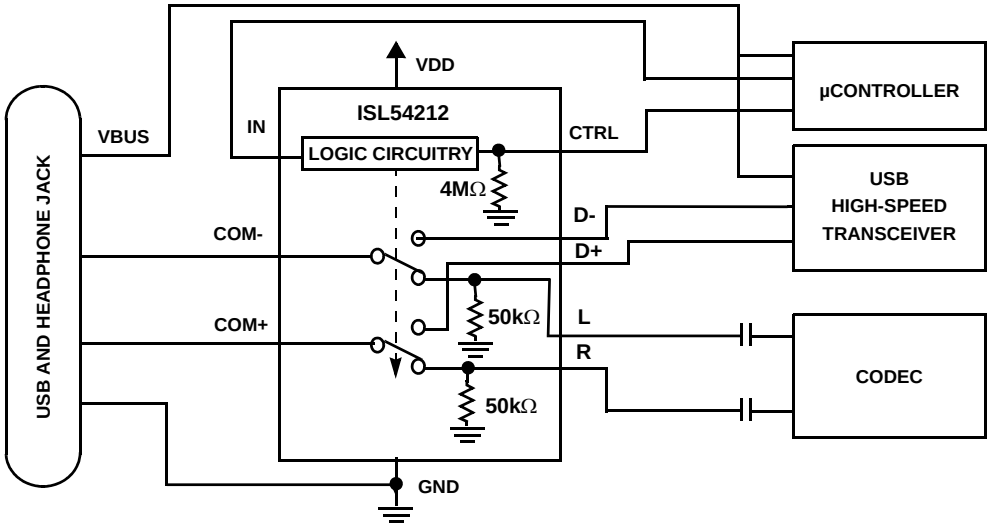


|tro - tri| Delay Due to Switch for Rising Input and Rising Output Signals.
|tfo - tfi| Delay Due to Switch for Falling Input and Falling Output Signals.
|tskew_0| Change in Skew through the Switch for Output Signals.
|tskew_i| Change in Skew through the Switch for Input Signals.

FIGURE 7B. TEST CIRCUIT

FIGURE 7. SKEW TEST

Application Block Diagram



LOGIC CONTROL VIA MICRO-PROCESSOR

Detailed Description

The ISL54212 device is a dual single pole/double throw (SPDT) analog switch device that can operate from a single DC power supply in the range of 2.5V to 5.5V. It was designed to function as a dual 2 to 1 multiplexer to select between USB differential data signals and audio L and R stereo signals. It comes in tiny µTQFN and TDFN packages for use in MP3 players, PDAs, cell phones, and other personal media players.

The part consists of two 3Ω audio switches and two 5Ω USB switches. The audio switches can accept signals that swing below ground. They were designed to pass audio left and right stereo signals, that are ground referenced, with minimal distortion. The USB switches were designed to pass high-speed USB differential data signals with minimal edge and phase distortion.

The ISL54212 was specifically designed for MP3 players, cell phones and other personal media player applications that need to combine the audio headphone jack and the USB data connector into a single shared connector, thereby saving space and component cost. Typical application block diagram of this functionality is shown above.

The ISL54212 has a single logic control pin (IN) that selects between the audio switches and the USB switches. This pin can be driven Low or High to switch between the audio CODEC drivers and USB transceiver of the MP3 player or cellphone. The ISL54212 also contains a logic control pin (CTRL) that when driven Low while IN is High, opens all switches and puts the part into a low power state, drawing typically 1nA of I_{DD} current.

A detailed description of the two types of switches is provided in the sections following. The USB transmission and audio playback are intended to be mutually exclusive operations.

Audio Switches

The two audio switches (L, R) are 3Ω switches that can pass signals that swing below ground by as much as 1.5V. They were designed to pass ground reference stereo signals with minimal insertion loss and very low distortion. Crosstalk between the audio switches over the audio band is < -110dB.

Over a signal range of ±1V (0.707Vrms) with V_{DD} >2.7V, these switches have an extremely low r_{ON} resistance variation. They can pass ground referenced audio signals with very low distortion (<0.06% THD+N) when delivering 15.6mW into a 32Ω headphone speaker load. See Figures 8, 9, 10 and 11 THD+N performance curves.

These switches are uni-directional switches. The audio drivers should be connected at the L and R side of the switch (pin 7 and pin 8) and the speaker loads should be connected at the COM side of the switch (pin 3 and pin 4).

The audio switches are active (turned ON) whenever the IN voltage is ≥1.4V and the CTRL voltage to ≥1.4V.

Note: Whenever the audio switches are ON the USB transceivers need to be in the high impedance.

USB Switches

The two USB switches (D+, D-) are bidirectional switches that can pass rail-to-rail signals. When powered with a 3.6V supply these switches have a nominal $r_{(ON)}$ of 4.6Ω over the

signal range of 0V to 400mV with a $r_{(ON)}$ flatness of 0.4Ω. The $r_{(ON)}$ matching between the D+ and D- switches over this signal range is only 0.06Ω ensuring minimal impact by the switches to USB high speed signal transitions. As the signal level increases the $r_{(ON)}$ resistance increases. At signal level of 3.3V the switch resistance is nominally 23Ω.

The USB switches were specifically designed to pass USB 2.0 high-speed (480Mbps) differential signals typically in the range of 0V to 400mV. They have low capacitance and high bandwidth to pass the USB high-speed signals with minimum edge and phase distortion to meet USB 2.0 high speed signal quality specifications. See the high-speed eye diagram in Figure 15.

The USB switches can also pass USB full-speed signals (12Mbps) with minimal distortion and meet all the USB requirements for USB 2.0 full-speed signaling. See the full-speed eye diagrams in Figures 12, 13 and 14.

The maximum signal range for the USB switches is from -1.5V to V_{DD}. The signal voltage at D- and D+ should not be allow to exceed the V_{DD} voltage rail or go below ground by more than -1.5V.

The USB switches are active (turned ON) whenever the IN voltage is ≤0.5V.

Note: Whenever the USB switches are ON the audio drivers of the CODEC need to be at AC or DC ground or floating to keep from interfering with the data transmission.

ISL54212 Operation

The sections that follow will discuss using the ISL54212 in the typical application shown in the block diagram on page 8.

VDD SUPPLY

The DC power supply connected at VDD (pin 1) provides the required bias voltage for proper switch operation. The part can operate with a supply voltage in the range of 2.5V to 5.5V.

In a typical USB/Audio application for portable battery powered devices the V_{DD} voltage will come from a battery or an LDO and be in the range of 2.7V to 3.6V. For best possible USB full-speed operation (12Mbps) it is recommended that the V_{DD} voltage be ≥2.5V in order to get a USB data signal level above 2.5V.

LOGIC CONTROL

The state of the ISL54212 device is determined by the voltage at the IN pin (pin 2) and the CTRL pin (pin 10). Refer to truth-table on page 2 of the data sheet. These logic pins are 1.8V logic compatible when V_{DD} is in the range of 2.7V to 3.6V and can be controlled by a standard µprocessor.

The CTRL pin is internally pulled low through a 4MΩ resistor to ground and can be tri-stated by the µprocessor. The CTRL control pin is only active when IN is logic “1”.

The IN pin does not have an internal pull-down resistor and must not be allowed to float. It must be driven High or Low.

Logic control voltage levels:

IN = Logic “0” (Low) when IN ≤0.5V
IN = Logic “1” (High) when IN ≥1.4V
CTRL = Logic “0” (Low) when ≤0.5V or floating
CTRL = Logic “1” (High) when ≥1.4V

Audio Mode

If the IN pin = Logic “1” and CTRL pin = Logic “1,” the part will be in the Audio mode. In Audio mode the L (left) and R (right) 3Ω audio switches are ON and the D- and D+ 5Ω USB switches are OFF.

When nothing is plugged into the common connector or a headphone is plugged into the common connector, the µprocessor will sense that there is no voltage at the VBUS pin of the connector and will drive and hold the IN control pin of the ISL54212 high. As long as the CTRL = Logic “1,” the ISL54212 part will be in the audio mode and the audio drivers of the media player can drive the headphones and play music.

USB Mode

If the IN pin = Logic “0” and CTRL pin = Logic “0” or Logic “1” the part will go into USB mode. In USB mode, the D- and D+ 5Ω switches are ON and the L and R 3Ω audio switches are OFF.

When a USB cable from a computer or USB hub is connected at the common connector, the µprocessor will sense the presence of the 5V V_{BUS} and drive the IN pin voltage low. The ISL54212 part will go into the USB mode. In USB mode, the computer or USB hub transceiver and the MP3 player or cell phone USB transceiver are connected and digital data will be able to be transmitted back and forth.

When the USB cable is disconnected, the µprocessor will sense that the 5V V_{BUS} voltage is no longer connected and will drive the IN pin high and put the part back into the Audio or Low Power mode.

Low Power Mode

If the IN pin = Logic “1” and CTRL pin = Logic “0,” the part will be in the Low Power mode. In the Low Power mode, the audio switches and the USB switches are OFF. In this state, the device draws typically 1nA of current.

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified

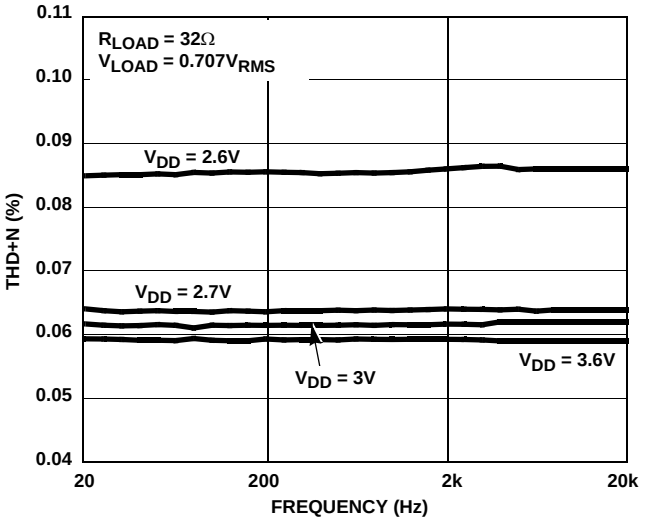


FIGURE 8. THD+N vs SUPPLY VOLTAGE vs FREQUENCY

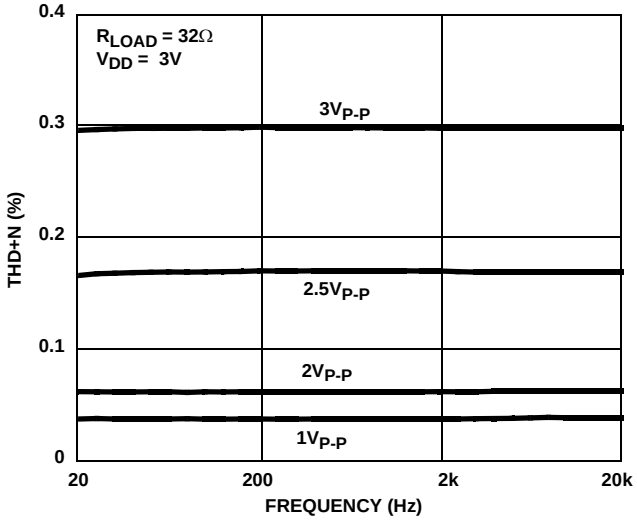


FIGURE 9. THD+N vs SIGNAL LEVELS vs FREQUENCY

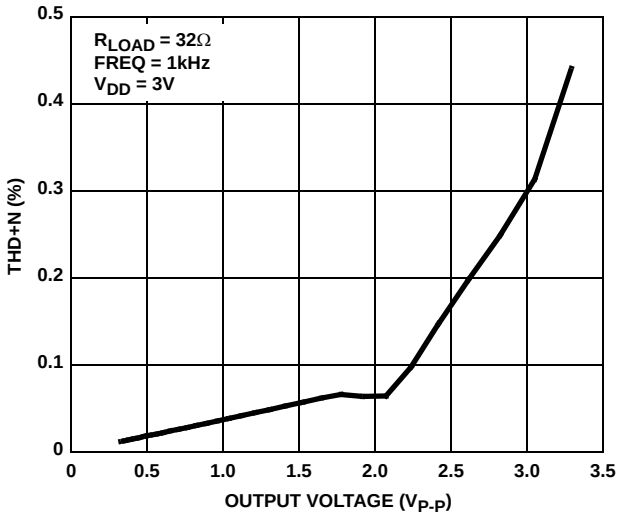


FIGURE 10. THD+N vs OUTPUT VOLTAGE

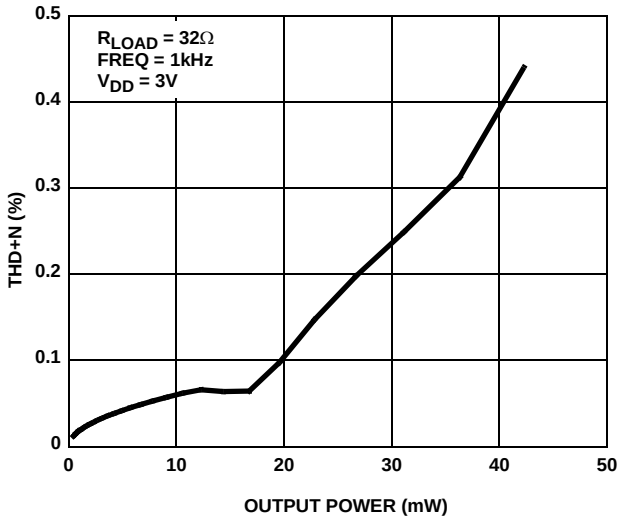


FIGURE 11. THD+N vs OUTPUT POWER

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified **(Continued)**

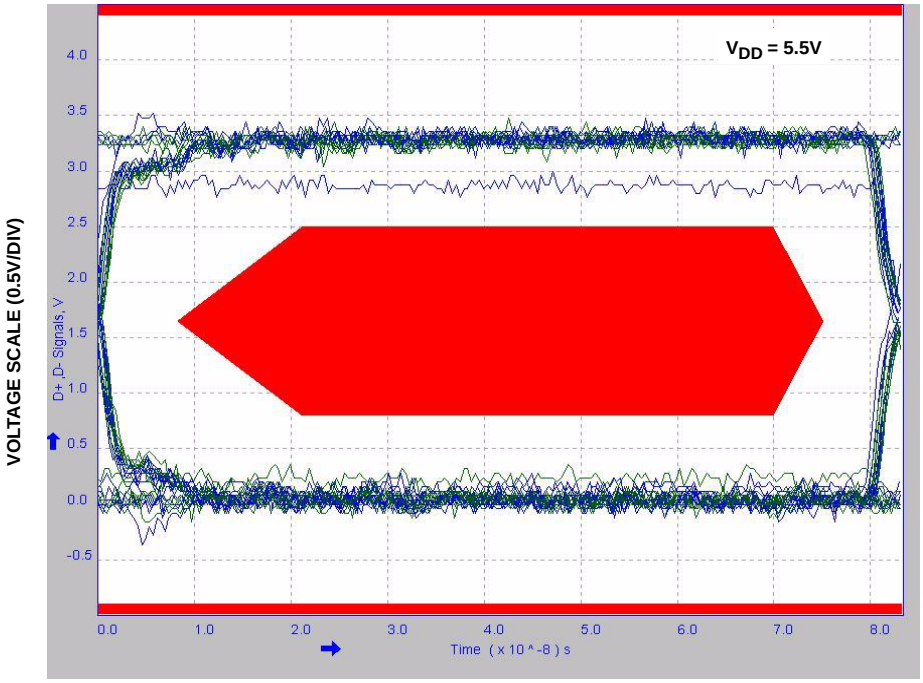


FIGURE 12. EYE PATTERN: 12MBps WITH SWITCHES IN THE SIGNAL PATH

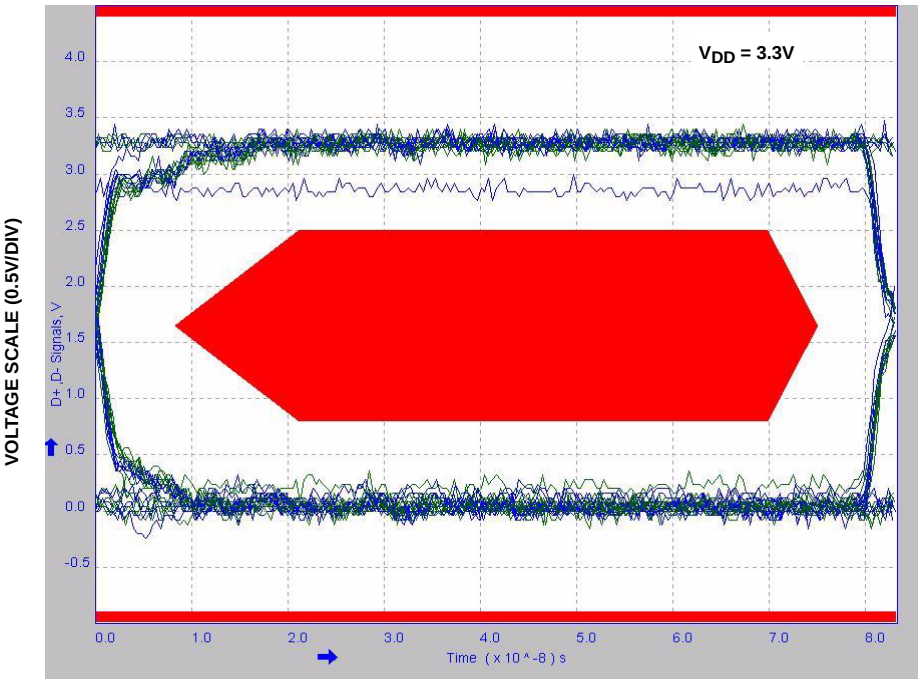


FIGURE 13. EYE PATTERN: 12MBps WITH SWITCHES IN THE SIGNAL PATH

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified **(Continued)**

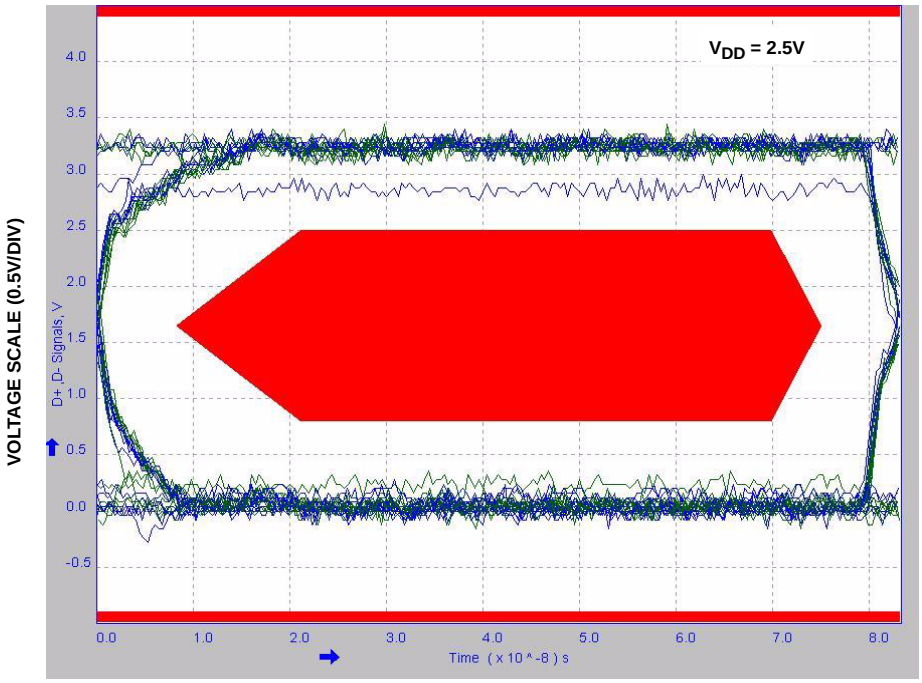


FIGURE 14. EYE PATTERN: 12MBps WITH SWITCHES IN THE SIGNAL PATH

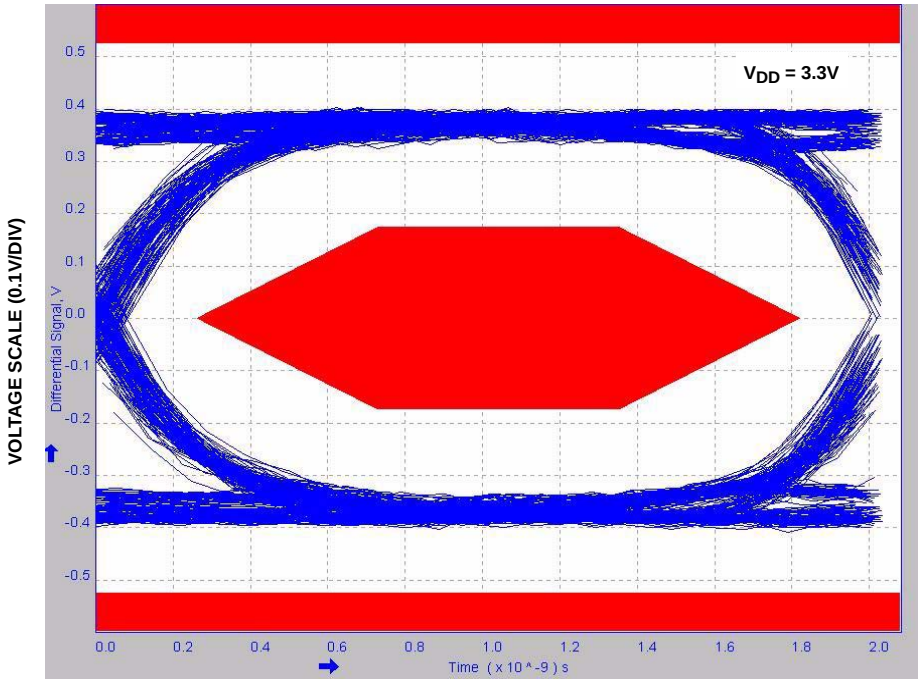


FIGURE 15. EYE PATTERN: 480MBps USB SIGNAL WITH SWITCHES IN THE SIGNAL PATH

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified **(Continued)**

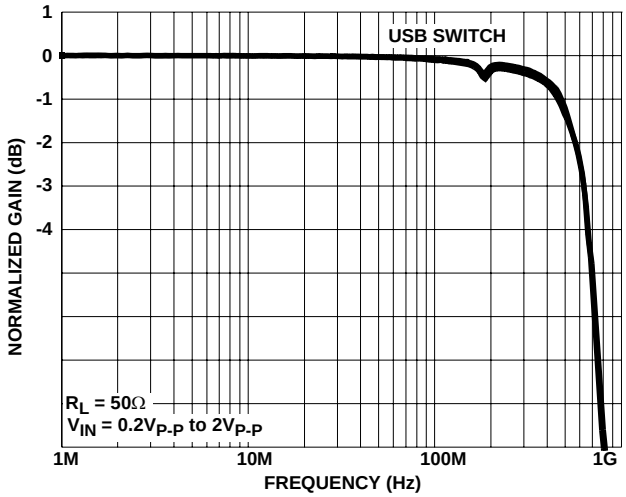


FIGURE 16. FREQUENCY RESPONSE

Die Characteristics

SUBSTRATE POTENTIAL (POWERED UP):

GND (TDFN Paddle Connection: Tie to GND or Float)

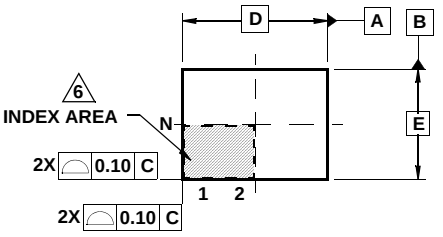
TRANSISTOR COUNT:

98

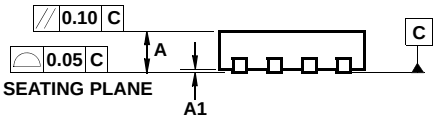
PROCESS:

Submicron CMOS

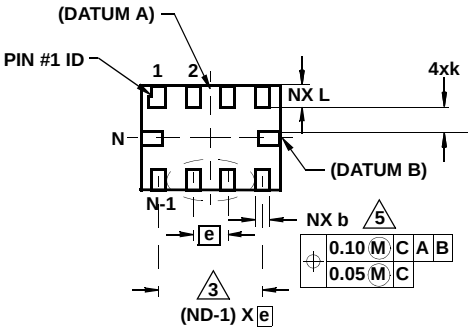
Ultra Thin Quad Flat No-Lead Plastic Package (UTQFN)



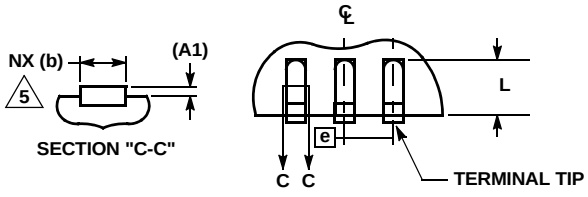
TOP VIEW



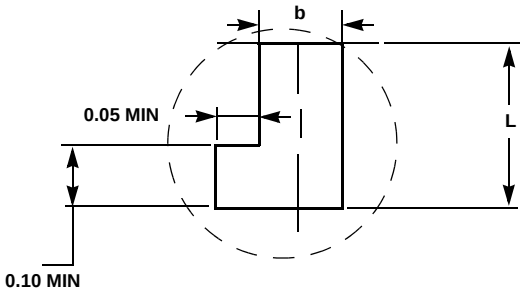
SIDE VIEW



BOTTOM VIEW



FOR ODD TERMINAL/SIDE



DETAIL "A" PIN 1 ID

L10.2.1x1.6A

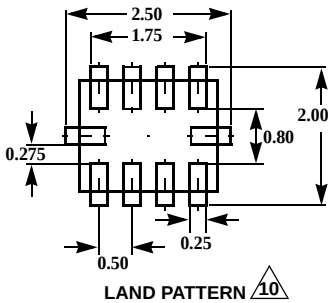
10 LEAD ULTRA THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.45	0.50	0.55	-
A1	-	-	0.05	-
A3		0.127 REF		-
b	0.15	0.20	0.25	5
D	2.05	2.10	2.15	-
E	1.55	1.60	1.65	-
e		0.50 BSC		-
k	0.20	-	-	-
L	0.35	0.40	0.45	-
N		10		2
Nd		4		3
Ne		1		3
θ	0	-	12	4

Rev. 3 6/06

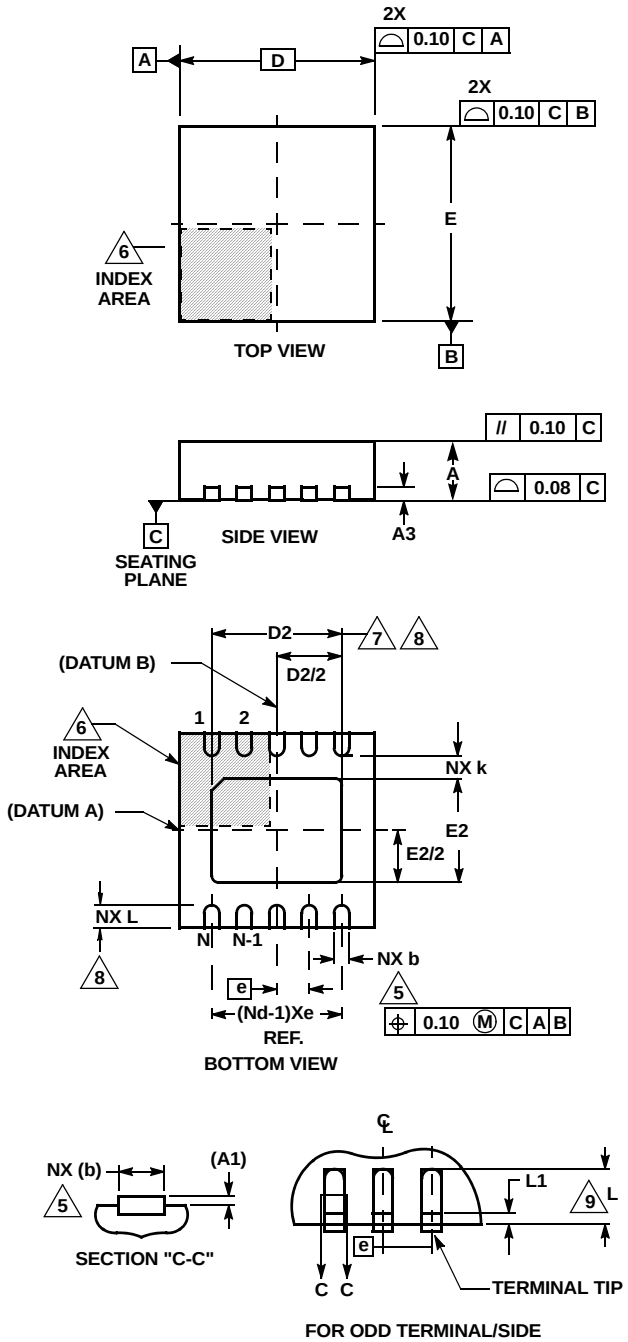
NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on D and E side, respectively.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Maximum package warpage is 0.05mm.
8. Maximum allowable burrs is 0.076mm in all directions.
9. Same as JEDEC MO-255UABD except:
   No lead-pull-back, "A" MIN dimension = 0.45 not 0.50mm
   "L" MAX dimension = 0.45 not 0.42mm.
10. For additional information, to assist with the PCB Land Pattern Design effort, see Intersil Technical Brief TB389.



LAND PATTERN 10

Thin Dual Flat No-Lead Plastic Package (TDFN)



L10.3x3A

10 LEAD THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.70	0.75	0.80	-
A1	-	-	0.05	-
A3		0.20 REF		-
b	0.20	0.25	0.30	5, 8
D	2.95	3.0	3.05	-
D2	2.25	2.30	2.35	7, 8
E	2.95	3.0	3.05	-
E2	1.45	1.50	1.55	7, 8
e		0.50 BSC		-
k	0.25	-	-	-
L	0.25	0.30	0.35	8
N		10		2
Nd		5		3

Rev. 3 3/06

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd refers to the number of terminals on D.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Compliant to JEDEC MO-229-WEED-3 except for D2 dimensions.

All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems.
Intersil Corporation's quality certifications can be viewed at www.intersil.com/design/quality

Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see www.intersil.com